Using the Serial Peripheral Interface (SPI) with AT91SAMxx Devices

1. Introduction

This application note describes the use of the Serial Peripheral Interface (SPI) implemented in AT91SAMxx ARM® Thumb®-based devices.

In this application note:

- SPI main features are summarized,
- SPI initialization is described,
- Characteristics that may be difficult to use are detailed.

Additionally, a software example of an interconnection between two SPIs is described.

AT91 ARM Thumb Microcontrollers

Application Note

6229B–ATARM–06-Aug-06

2. SPI Features

- Supports Communication with Serial External Devices
  - Four Chip Selects with External Decoder Support Allow Communication with Up to 15 Peripherals
  - Serial Memories, such as DataFlash and 3-wire EEPROMs
  - Serial Peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External Co-processors
- Master or Slave Serial Peripheral Bus Interface
  - 8- to 16-bit Programmable Data Length Per Chip Select
  - Programmable Phase and Polarity Per Chip Select
  - Programmable Transfer Delays Between Consecutive Transfers and Between Clock and Data Per Chip Select
  - Programmable Delay Between Consecutive Transfers
  - Selectable Mode Fault Detection
- Connection to PDC Channel Optimizes Data Transfers

3. Description of the SPI

The Serial Peripheral Interface (SPI) circuit is a synchronous serial data link that provides communication with external devices in Master or Slave Mode. It also enables communication between processors if an external processor is connected to the system.

The Serial Peripheral Interface is essentially a shift register that serially transmits data bits to other SPIs. During a data transfer, one SPI system acts as the “master”' which controls the data flow, while the other devices act as “slaves'' which have data shifted into and out by the master. Different CPUs can take turn being masters (Multiple Master Protocol opposite to Single Master Protocol where one CPU is always the master while all of the others are always slaves) and one master may simultaneously shift data into multiple slaves. However, only one slave may drive its output to write data back to the master at any given time.

A slave device is selected when the master asserts its NSS signal. If multiple slave devices exist, the master generates a separate slave select signal for each slave (NPCS).

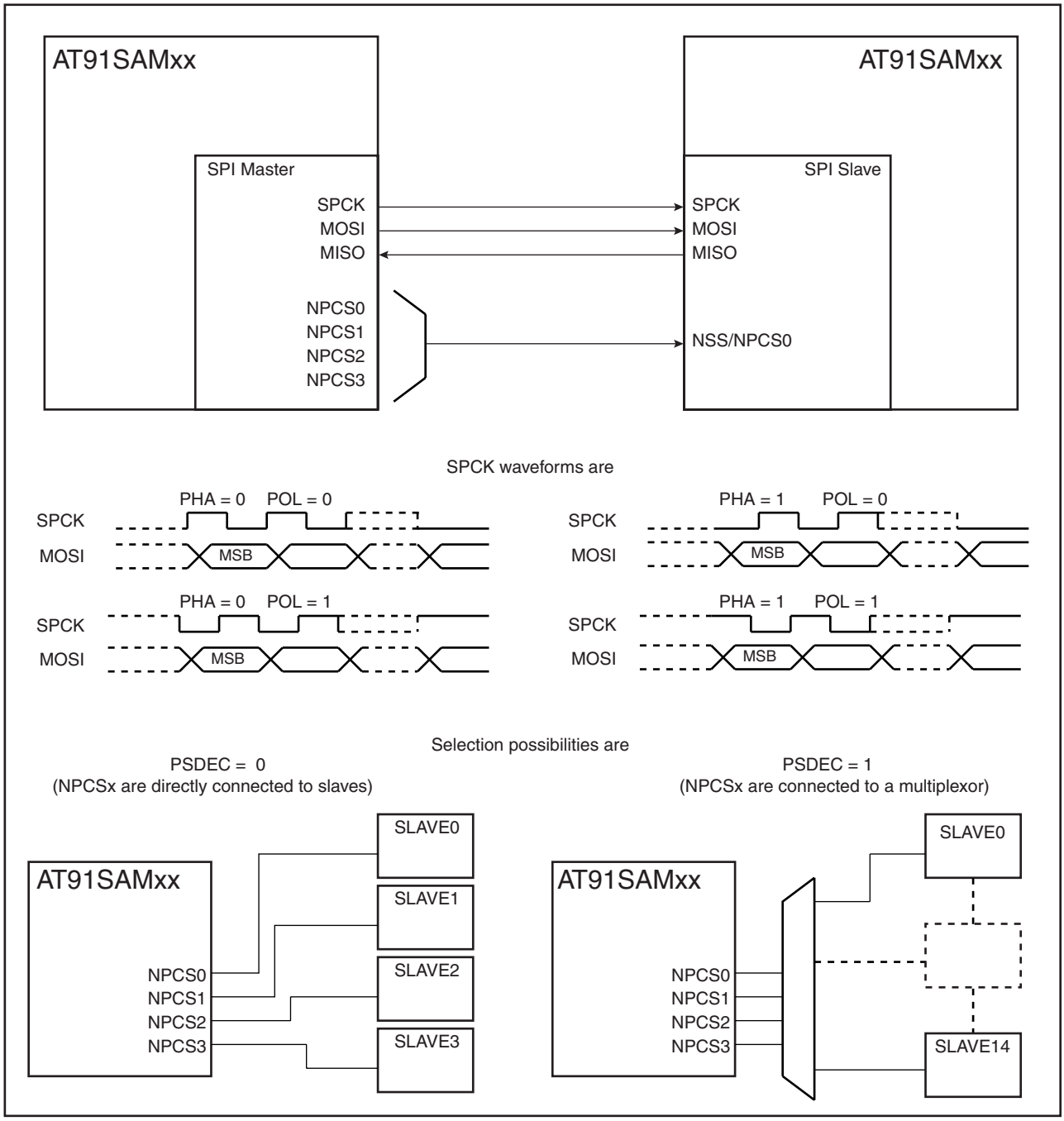
The SPI system consists of two data lines and two control lines:

- Master Out Slave In (MOSI): This data line supplies the output data from the master shifted into the input(s) of the slave(s).
- Master In Slave Out (MISO): This data line supplies the output data from a slave to the input of the master. There may be no more than one slave transmitting data during any particular transfer.
- Serial Clock (SPCK): This control line is driven by the master and regulates the flow of the data bits. The master may transmit data at a variety of baud rates; the SPCK line cycles once for each bit that is transmitted.
- Slave Select (NSS): This control line allows slaves to be turned on and off by hardware.

4. Interfacing the SPI

The following figure shows two AT91SAMxx devices exchanging data through the SPI bus.

Figure 4-1. Interfacing the SPI



Clock (SPCK) and selection signals (NPCS) are provided by the Master.

- The clock has to be compatible with the Slave in terms of waveform (phase and polarity) and speed.

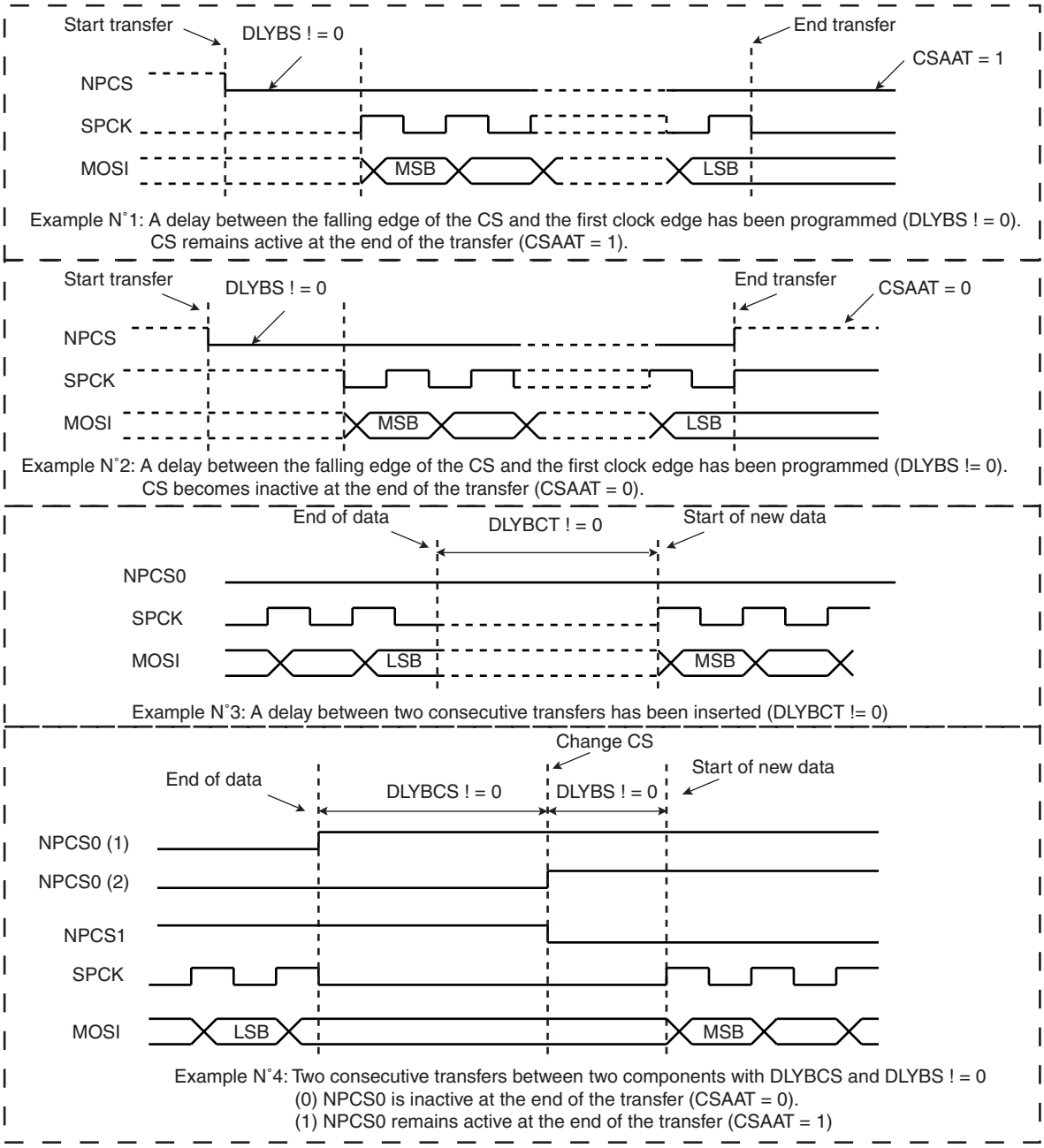
In the case where the master addresses an AT91SAMxx device the waveform has no restriction and the maximum operating baud rate is (Slave Master Clock) / 2. (Depending on I/O speeds and setup constraints.)

- The selection signal can be either one of the four NPCS lines or a decoding of those lines with an external logic.
  - in the first instance, the SPI can address up to four Slaves without external logic.
  - in the second instance, the SPI can address up to fifteen Slaves with the addition of an external decoder.

Furthermore, in order to be compliant with most SPI devices it is possible to configure the delay before the SPCK (DLYBS), the delay between consecutive transfers (DLYBCT), the state of the CS line at the end of the transfer, and to avoid bus contention, the delay between two chip selects (DLYBCS).

Figure 4-2 illustrates the use of DLYBS, BLYBCT and DLYBCS.

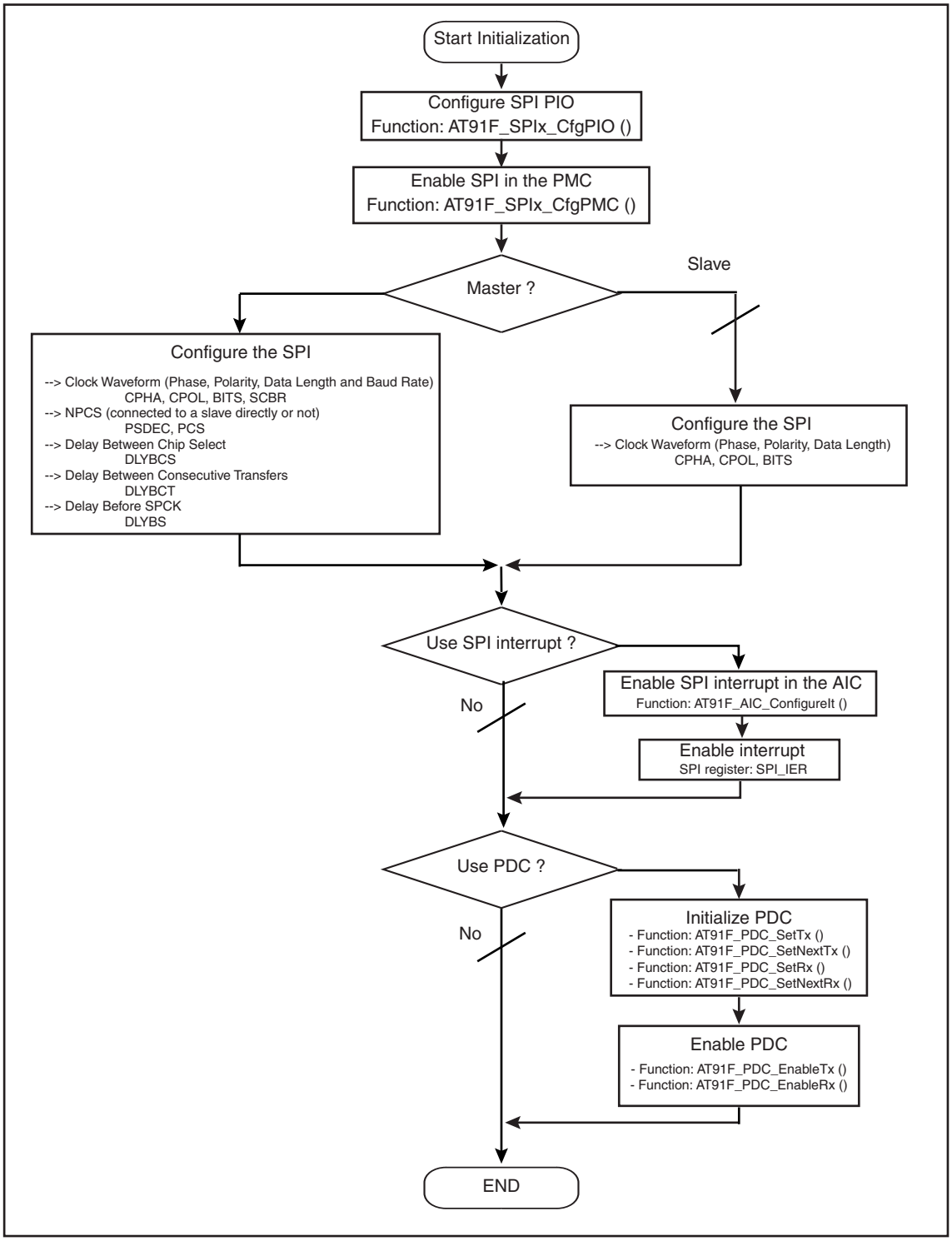
Figure 4-2. DLYBS, BLYBCT and DLYBCS



5. Initialization

The flowchart in Figure 5-1 depicts initialization of the SPI in either Master or Salve mode.

Figure 5-1. SPI Initialization



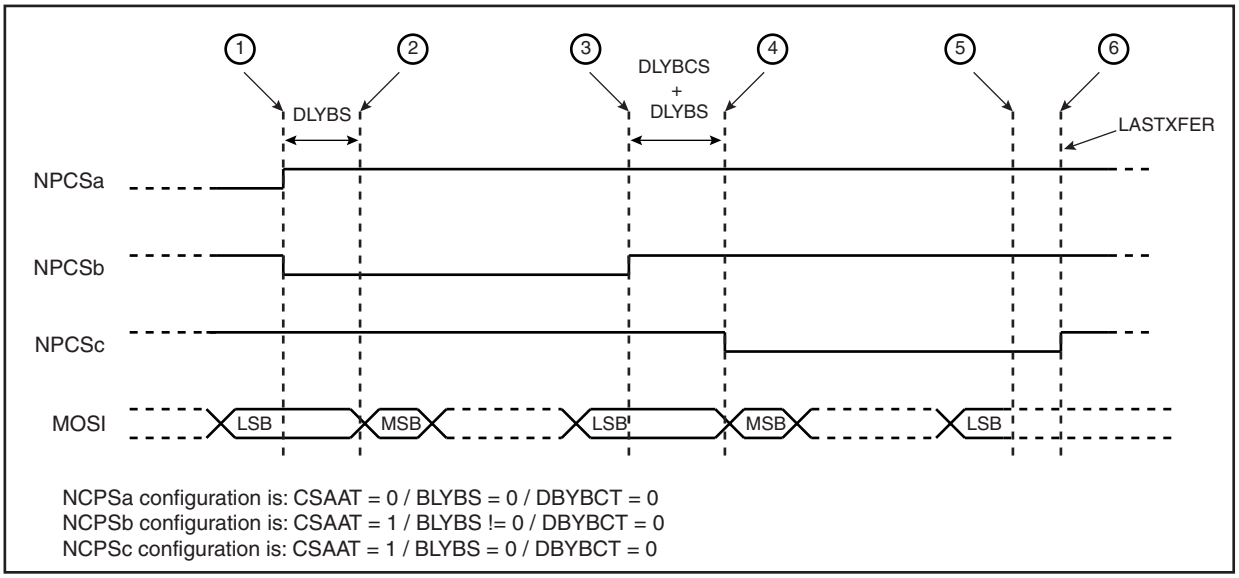
6. Use of Last Transfer

Last Transfer is used to make the current Chip Select rise under the conditions listed below.

- The data transfer is finished:
  - the shift register is empty, no new data has been written in the transmit register and DLYBCT is finished.
- The current Chip Select is programmed to remain active at the end of the transfer (CSAAT = 1).
- LASTXFER bits located in the SPI_CR register must be used when CS lines are directly connected to slaves (PSDEC = 0).
- LASTXFER bits located in the SPI_CSRx registers must be used when CS lines are connected to an external decoder (PSDEC = 1).

Figure 6-1 gives an example of using LASTXFER.

Figure 6-1. LASTXFER



1. NPCSa rises at the end of the transfer, immediately NPCSb falls,
2. The data to transmit on NPCSb starts after DLYBS,
3. NPCSb rises at the end of the transfer because it's CSAAT = 0 and the data transfer is finished,
4. NPCSc falls as soon as data is written in it's TDR and the data is immediately transmitted because DLYBS = 0,
5. The transfer is finished and NPCSc remains low because it's CSAAT = 1,
6. LASTXFER is set to 1 and NPCSc rises.

7. Software Example

The software example associated with this document describes how to use an SPI in Master or Slave mode.

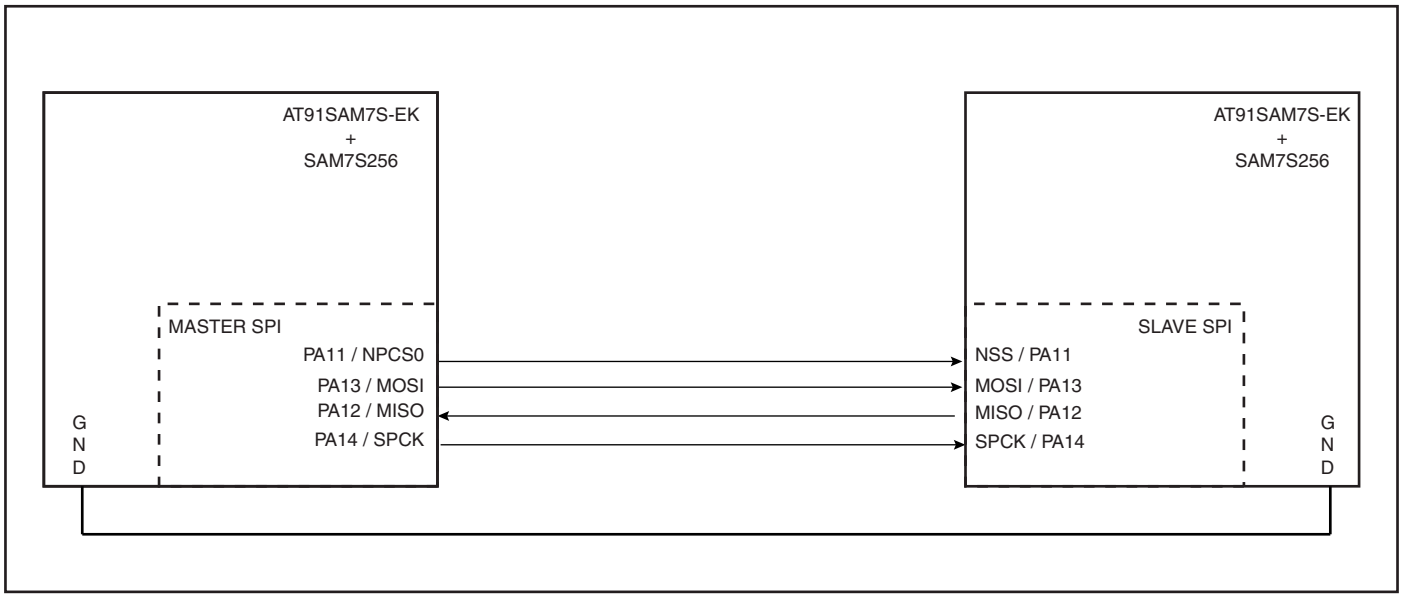
7.1 Hardware Settings

It is important to note that the hardware support used to develop this software was an AT91SAM7S-EK board that includes an AT91SAM7S256.

Atmel.com has more information on the AT91SAM7S-EK.

Figure 7-1 shows the connection between the Master and the Slave.

Figure 7-1. Master and Slave Connection



7.2 Software Considerations

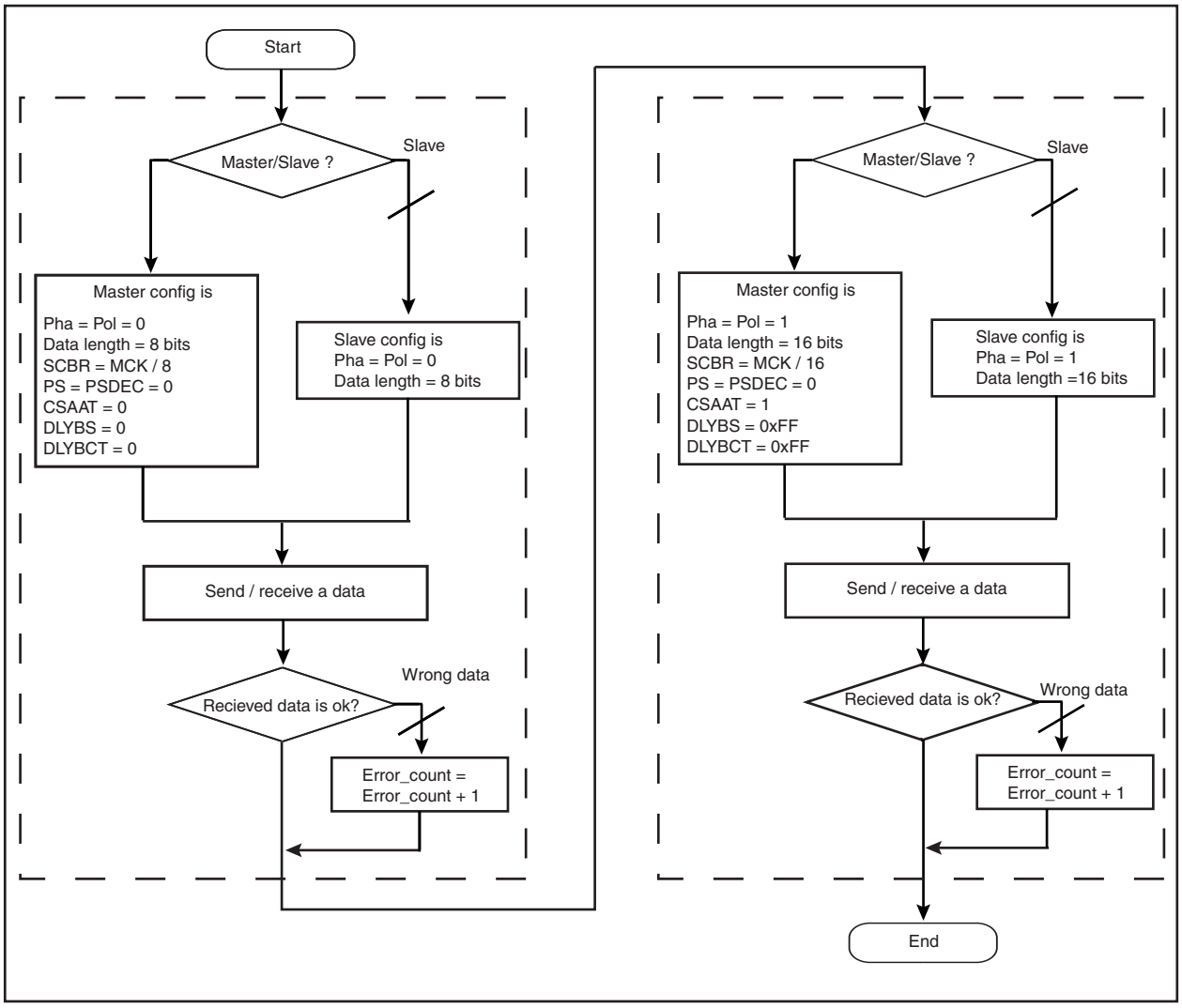
- SPI is working under interrupt.
- Software files are organized as follows:

Initialization	Cstartup.s79 Cstartup_SAM7.c main.c / main.h
Interrupt treatment	handler.c / handler.h
SPI main features	spi_main.c / spi_main.h
SPI master	spi_master.c / spi_master.h
SPI slave:	spi_slave.c / spi_slave.h

7.3 Software Flowchart

The flowchart shown in Figure 7-2 illustrates the software example.

Figure 7-2. Software Example



Revision History

Doc. Rev	Comments	Change Request Ref.
6229A	First issue	
6229B	Remove references to internal documents	3017

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