AVR181: Automotive Grade0 - PCB and Assembly Recommendations

1. Foreword

Modern cars still involve control loops between a set of captors and different actuators elements responsible for the transportation, but also the comfort and the safety of the occupants. To satisfy the constant growth of these elements, car makers and their suppliers have adopted distributed architectures with global communication networks, circulating throughout the vehicle, providing information to equipment.

However, in some circumstances, it is important that the control loop remains local, for better real-time control for instance, but more often because the price to pay for a sophisticated communication protocol is too high.

Therefore, engineers see benefits at having close connection between their sensors and the element which will be responsible for the signal conditioning and the control of the actuator. If the distributed architectures allow for placing the Electronic Control Units in safe areas, local control loops require the electronics to be located close to the sensors, sometimes in areas where the constraints go beyond the standard temperature and environmental conditions.

This paper is a collection of technical advice aiming at providing automotive electronic designers elements to manage high temperature constraints when addressing the PCB development.





Application Note







2. Automotive governing standards

2.1 AECQ100

Automotive quality is governed by a set of various standards. The most frequent and recognized one is the series of documents published by the Automotive Electronic Committee (AEC). One of these is the AEC-Q100 which describes the tests and conditions electronic components have to satisfy before the automotive qualification can be pronounced. Different grades are defined depending mainly on the operational temperature conditions.

As listed in the Table 1: Grade 0 and Grade1 environmental an endurance tests as per AECQ1001, the AECQ100 provides a list of environmental and endurance tests the components must successfully satisfy before qualification is pronounced. They vary depending on the grade level.

Table 2-1. Grade 0 and Grade1 environmental an endurance tests as per AECQ100

Part Operating Temperature Grade				-40°c to +150°c	-40 °c to +125 °c
Test Name	Conditions	Rules	Unit	Grade 0	Grade 1
A4: TC Thermal Cycles	-50°c to +150°c	Mil Std 883 method1010 JEDEC JESD22 A104	cycles	2000	1000
	-65°c to +150°c				500
	-50°c to +175°c			1000	
	-65°c to +175°c			500	
A2: THB Humidity	85 ℃ / 85%RH	JESD22-A101	hours	1000	1000
JESD22-A101					
A3: AC HAST	130℃ / 85%RH	JESD-22-A118	hours	96	96
A6: HTSL High Tem-	175℃	JESD-22-A103	hours	1000	500
perature Storage Life	150℃			2000	1000
B1: HTOL High Tem-	175℃	JESD-22-A108	hours	408	408
perature Operating Life	150℃			1000	1000
A5: PTC Power Temp	–40 to 150 ℃	JA 105	cycles	1000	
Cycle	–40 to 125℃				1000

2.2 AECQ100: comparison between Grade 0 and Grade 1

The difference between grade0 (150 °C) and grade1 (125 °C) is expressed via the duration and the operating temperature of several tests.

- Thermal cycles are more sever at grade 0: more cycles and extended temperature extremes.
- High temperature storage duration is doubled, at identical temperature.
- Power temperature cycles are executed at operational temperature (150 °C for grade0, 125 °C for grade1).

2.3 AECQ100 grade 0 limitations

Although reliability test are performed to qualify the components for applications at 150 °C, the qualification 'functional at operational conditions of 150 °C' is limited to 1000 hours.

3. High-Temp reliability issues

Operational temperature conditions in excess of the usual 125°C are known to affect the physical and mechanical characteristics of the components of most electronics. Some concerns have already been identified. Particularly of interest for the automotive equipment are:

- Inter-metallic growth between the bonding wire and the pad post
- · Mold Compound Stability.
- · Die Attach epoxy stability,
- · Thermal dissipation and different dilatation coefficients

3.1 Inter-metallic growth

The inter-metallic growth degradation is mainly related to 2 causes:

- Aluminum metal corrosion: When Mold Compound absorbs moisture, ionic impurities, such as CI or Br, can reach the internal chip surface. Therefore, positive or negative ions can reach the AI metal die Pads, resulting in AI electrochemical reaction.
- · Green Materials used for QFN contain neither CI nor Br.
- QFN packages are MSL3 and customers are requested to comply with JEDEC JSTD 20 related baking process after Moisture Barrier Bag opening. New developments are under progress for MSL1 qualifications.

3.2 Kirkendall voids

When Wire Bonding of Au wire to Al Pad is subjected to high temperature, purple alloy formation, such as AuAl2 is observed. This alloy is known as "purple plague."

Then Au2Al occurs when the proportion of Au is high. It has higher electrical resistance and is mechanically weaker than AuAl2. This is the "white plague."

When submitted to High Temperatures, as Au and Al have different diffusion constants, it generates voids (so called Kirkendall voids) due to the volume modification of the generated intermetallic.

It results in bonding degradation, and electrical opens can appear when the component is subjected to vibrations or to thermal expansion differences between mold compound and die at high temperatures.

- QFN 32 5x5 mm (with Au wire) has been subjected to:
 - High Temperature Storage test @ 175 °c (JESD-22-A103) without any reject
 - Thermal cycles, -65 °c / + 175 °c (JEDEC JESD22 A104) without any reject
- QFN 32 5x5 mm is also qualified with AuPd wire (1% Pd). After aging, cross sections reveal
 that void concentration with AuPd wire is lower than with the pure gold Wire. Palladium
 creates a natural barrier to Gold diffusion in Aluminum and thus Kirkendall voids process is
 slower. Doped wires are recommended for high temperature applications.





3.3 Mold Compound Stability & D/Attach epoxy stability

At 150°c, the stability of the compound and the die attach epoxy used for green materials is not affected. Neither porosity nor cracks appear at this temperature.

3.4 Thermal dissipation

In high temperature application, thermal dissipation is the key to allow devices to operate correctly. Therefore, selected packages must have outstanding thermal characteristics, otherwise junction temperature could be too high.

- QFN package is a good candidate when thermal dissipation is required since its thermal performance Theta Ja (°C/W) is twice better than one TQFP equivalent body. Also note that for same body dimension, QFN package allows bigger die's than TQFP.
- External pad (thermal drain) also helps to thermal dissipation when soldered to the PCB (this is not possible with ordinary TQFP).
- Pad dimension keeps a limited free space between Pad and Leads which has a positive impact on thermal dissipation through peripheral leads.

3.5 Different Dilation Coefficients

3.6 Other advantages of QFN packages

These packages have good Electrical characteristics, due to short leads. Thus they are also recommended for RF applications.

4. Recommendation and Advice for PCB

Apart from the usual task of component selection for high temperature operating systems, it is also important that the designer pays attention to the technology and the characteristics of the PCB. Also, the soldering process of the components to the PCB may affect the reliability of the application and reduce dramatically the lifetime of the system.

Therefore, different constraints must be considered by the engineer, covering:

- The PCB material and technology
- The components soldering technology and its process

4.1 Materials

4.1.1 PCB

Different alternatives exist on the market.

Standard FR4 (up to 85 °C), Cost: 1
 Standard FR4 HTG (up to 175 °C), Cost: 1.15¹
 Polyimide or Cyanate Ester (to 250 °C) Cost: 1.9¹

Aluminum Oxide (> 500 °C)

Aluminum Nitride (to 600 °C)

Note: 1. With reference to the standard FR4.

The temperature cycling resistance of FR4 <u>HTG</u> materials is sufficient for most lead-free alloys. At high reflow temperatures for Pb free solders, If FR4 is still used, increased twisting and warping is to be expected. Furthermore, out gassing and delamination can occur. In this case there are alternative board materials such as FR5, glass/BT-epoxy, glass/polyimide

© We **recommend** the FR4 HTG as the best compromise in cost and reliability.

4.1.2 Lead-free alloys

SnAgCu: The most important alternative solders of such metal alloys contain between 0.5 to 2 % Cu and 3.8 to 4.7 % Ag. With this combination the melting point is between 216° and 219 °C, which are suitable for high temperature applications up to 175 °C.

Adding only small amounts of Cu to the solder alloy decreases the tendency of the solder to disolve copper from the metallization.

© We **recommend** Solder Alloy 95.5Sn3.8Ag0.7Cu for good reliability prognosis and the Solder Alloy thickness is 150 μ m maximum.

No clean Type 3 or similar solder paste is **recommended** for assembly of the QFN to the PCB, due to its low standoff and small pad openings.

4.2 Processes and 150 °C

4.2.1 Plated solderable metallization

Cu with organic passivation:

The first metallization consists in an Organic Solderability Preservative coating (OSP) over the copper plated pad. The organic coating assists in reducing oxidation in order to preserve the copper metallization for soldering. Nitrogen atmosphere is preferred.

• Ni-Au: The second recommended solderable metallization consists in plated electroless nickel over the copper pad, followed by immersion gold. Au gives good protection against oxidation provided the application is not too thin or too porous. Rise in soldering temperature





for Pb free solders increases the risk of Ni diffusion. It must, therefore, be ascertained whether the solderability of the 2nd side of the assembly is still sufficient.

- Chemical Sn: Chemical Sn is deposited in layers of about 1µm. As the temperature increased for Pb free solders there is the danger of Cu diffusion.
- Thin silver coatings: Chemical Ag is deposited in a layer up to 0,2µm with an organic protection. At increased soldering temperatures there is a risk of destroying the protective organic coating.
- © We recommend NiAu for better process ability and is more wide spread among suppliers

4.2.2 PCB pad configurations

There are two different types of PCB pad configurations commonly used for surface mount leadless QFN style packages. These different I/O configurations are:

- Non Solder masked Defined (NSMD)
- Solder Masked Defined (SMD)
- © Typically, the NSMD pads are preferred on perimeter lead and the PCB thermal pad should be SMD.

4.2.3 Perimeter Pad

When dimensionally possible, the solder mask should be located at least a 0.076 mm (0.003 in) away from the edge of the solderable pad. The dimensions of the PCB's solderable pads should match those of the pads on the package,

The PCB terminal pad should be approximately 0.05mm longer than the length of the package lead.

The PCB pad width can be designed <u>larger</u> than the maximum possible package pad width dimension to allow for greater assembly process window. More common in the industry, would be to use a 1:1 ratio between the nominal package pad width and the PCB pad width.

4.2.4 Thermal Pad

The QFN package exposed die pad should be soldered to the PCB, due to a good thermal path to the board.

In general, the size of the thermal pad should be as close to the exposed pad of the package as possible, provided that there is no bridging between the thermal pad and the perimeter lead pads.

For assembly, the PCB exposed pad should be smaller than the nominal package QFN, The stencil opening for the exposed pad region should be segmented in several smaller regions. The PCB exposed pad region itself can also be segmented, matching the stencil pattern. If this is the case, the spacing between segments should be 0.15mm or more.

4.2.5 Plated Through Hole (PTH) Vias

Due to high temperature, applications via holes are required. Via holes, Increase the thermal conduction through dielectric layers, a greater density of vias and larger vias on the same pattern provide good solderability.

4.2.6 Stencil Design

Stainless steel stencils are recommended for solder paste application.

The sidewalls of the stencil openings should be tapered approximately 5 degrees. The stencil opening should be approximately 50% - 80% of the total PCB thermal pad area. A large opening in the thermal region allows "scooping" to occur during screen printing. An array design is recommended in the stencil opening for the thermal pad region

4.2.7 Aspect Ratios

Aspect ratio is defined as the ratio of aperture width to stencil thickness, For a good solder paste printing process, keep the aspect ratio larger than 1.5. Too small of a ratio will cause the solder paste to stick on the side wall of the stencil aperture instead of the land (area) of the PCB.

4.2.8 Reflow Profile

The QFN packages are attached to the PCB by infrared or convection mass reflow techniques as part of standard SMT processing. Thermal profiling of the convection / IR reflow machine is required for each product design. Deviation from the recommended profile should be first evaluated using a copper (Cu) coupon test.

For lead-free solder, the reflow temperature shall not exceed 260 °C with time above <u>liquids</u> temperature (217 °C) of 45 seconds minimum.

The airflow may need to be reduced in some cases to prevent lightweight parts from shifting or being blown off and the temperature adjusted accordingly to maintain their flow profile.

A nitrogen environment during reflow stops further oxidation but may cause flux bridging between pads.

Typically, extending the time in the soak zone should reduce the risk of voiding within the solder.

5. Conclusions

Backed by long history at providing solutions for extreme temperature equipments, this document is addressing the reliability questions associated to the automotive grade 0 PCB manufacturing. Know issues are addressed and possible material and techniques advices are combined to reduce engineering tasks. Correct association of excellent silicon, new packaging, together with appropriate PCB material and adapted soldering techniques are demonstrated to reach acceptable long term life time even in harsh environments while costs are kept compatible with the automotive requirements.





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