SY58020U

6 GHz, 1:4 CML Fanout Buffer/Translator with Internal I/O Termination

Features

- Precision 1:4, 400 mV CML Fanout Buffer
- Guaranteed AC Performance Over Temperature/Voltage:
- > 6 GHz f_{MAX} Clock
- < 60 ps t_r / t_f Times
- < 250 ps t_{pd}
- < 15 ps Max. Skew
- Low-jitter Performance:
- 27 fs_{RMS} Typical Additive Phase Jitter
- Accepts an Input Signal as low as 100 mV
- Unique Patented Input Termination and VT Pin Accepts DC-coupled and AC-coupled Differential Inputs: LVPECL, LVDS, and CML
- 50Ω Source Terminated CML Outputs
- Power Supply 2.5V ±5% and 3.3V ±10%
- Industrial Temperature Range: –40°C to +85°C
- Available in 3 mm × 3 mm 16-lead VQFN Package

Applications

- All SONET and All GigE Clock Distribution
- Fibre Channel Clock and Data Distribution
- Backplane Distribution
- Data Distribution: OC-48, OC-48+FEC, XAUI
- High-end, Low Skew, Multiprocessor Synchronous Clock Distribution

General Description

The SY58020U is a 2.5V/3.3V precision, high-speed, fully differential 1:4 CML fanout buffer. Optimized to provide four identical output copies with less than 15 ps of skew and 27 fs_{RMS} of typical additive phase jitter, the SY58020U can process clock signals as fast as 6 GHz.

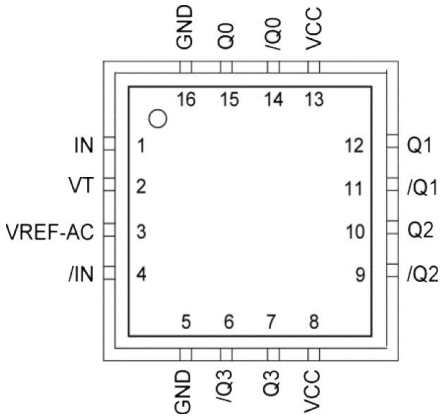
The differential input includes Microchip's unique, 3-pin input termination architecture that interfaces to differential LVPECL, LVDS, and CML signals (AC- or DC-coupled) as small as 100 mV without any level-shifting or termination resistor networks in the signal path.

For AC-coupled input interface applications, an on-board output reference voltage (V_{REF-AC}) is provided to bias the VT pin. The outputs are optimized to drive 400 mV typical swing into 50Ω loads, with extremely fast rise/fall times guaranteed to be less than 60 ps.

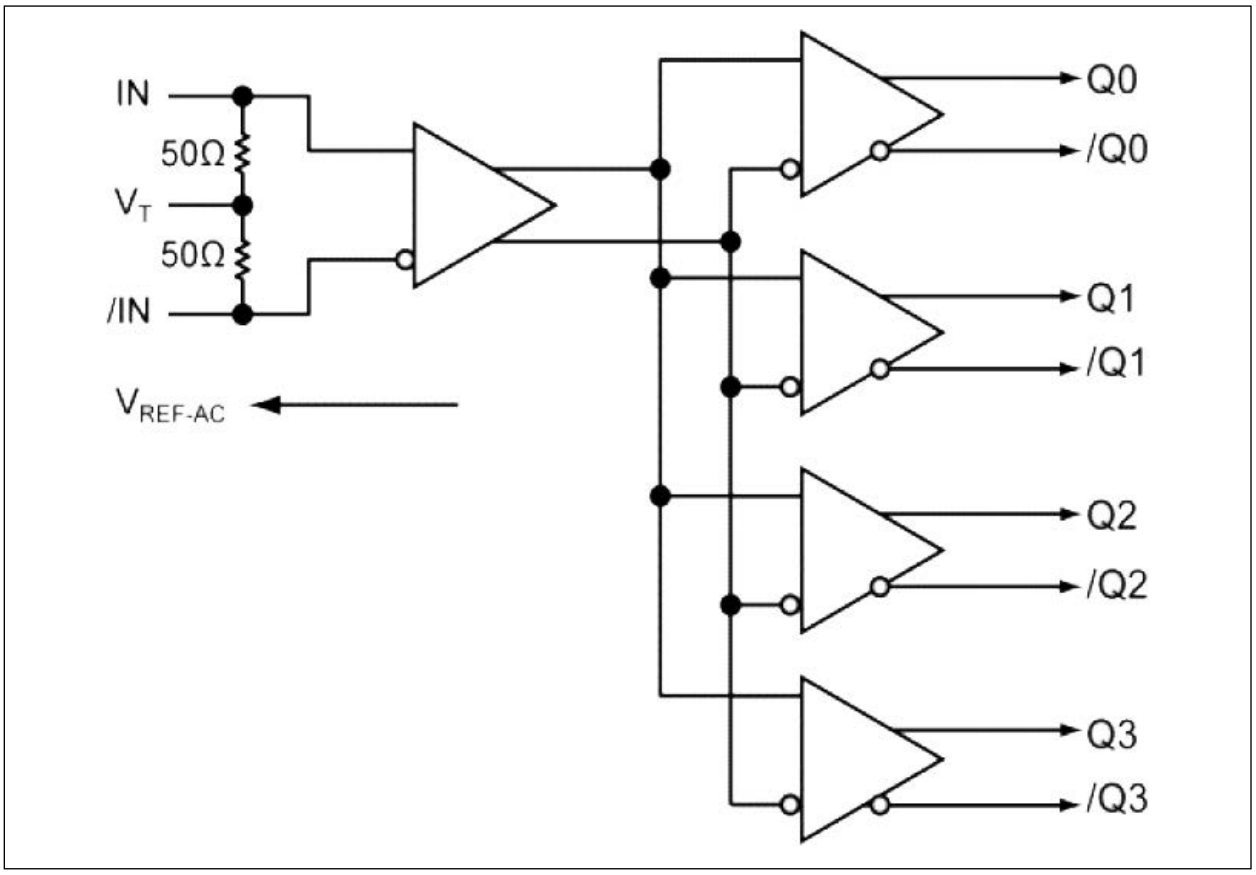
The SY58020U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). For applications that require LVPECL outputs, consider the SY58021U or SY58022U 1:4 fanout buffer with 800 mV and 400 mV output swing, respectively. The SY58020U is part of Microchip's high-speed, Precision Edge® product line.

Package Type

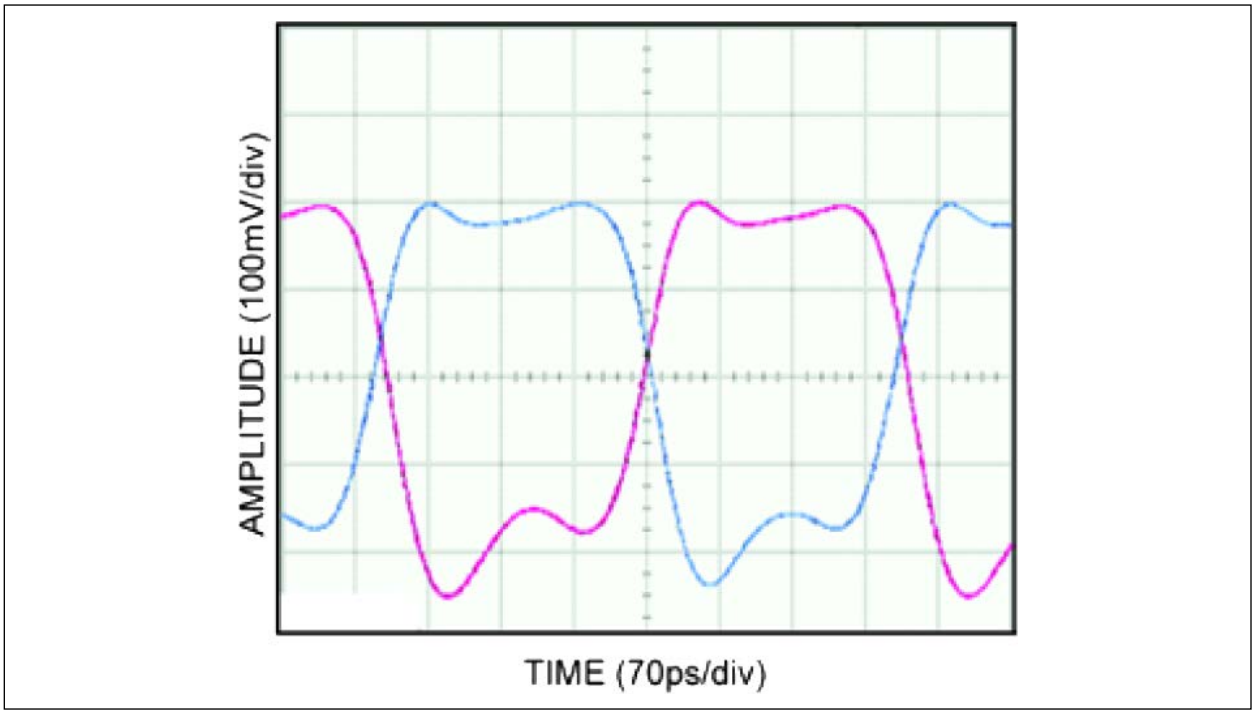
SY58020U
16-Lead VQFN



Functional Block Diagram



Typical Application (2 GHz)



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Power Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
CML Output Voltage (V_{OUT}) ..... V_{CC} – 1.0V to V_{CC} + 0.5V
Current (V_T), Source or sink current on V_T pin ..... ±100 mA
Input Current (I_{IN}), Source or sink current on IN, /IN ..... ±50 mA
Current (V_{REF}), Source or sink current on V_{REF-AC} (Note 1) ..... ±1.5 mA

Operating Ratings††

Supply Voltage (V_{CC}) ..... +2.375V to +3.60V

† **Notice:** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

†† **Notice:** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 1: Due to the limited drive capability, use for input of the same package only.

TABLE 1-1: DC ELECTRICAL CHARACTERISTICS

All values applicable for when T_A = –40°C to +85°C unless otherwise noted. (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power Supply Voltage	V_{CC}	2.375	2.500	2.625	V	V_{CC} = 2.5V
		3.000	3.300	3.600	V	V_{CC} = 3.3V
Power Supply Current	I_{CC}	—	150	180	mA	No load, VCC = max. (include internal 50Ω pull-up)
Input HIGH Voltage	V_{IH}	V_{CC} – 1.600	—	V_{CC}	V	Note 2
Input LOW Voltage	V_{IL}	0	—	V_{IH} – 0.100	V	—
Input Voltage Swing	V_{IN}	0.100	—	1.700	V	See Figure 7-1
Differential Input Voltage Swing	V_{DIFF_IN}	0.200	—	3.400	V	See Figure 7-2
IN-to-V_T Resistance	R_{IN}	40	50	60	Ω	—
Output Reference Voltage	V_{REF-AC}	V_{CC} – 1.300	V_{CC} – 1.200	V_{CC} – 1.100	V	—
IN-to-V_T Voltage	V_{T_IN}	—	—	1.280		—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

2: V_{IH} (min.) not lower than 1.2V.

TABLE 1-2: CML DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V ±10% or 2.5V ±5%; R_L = 100Ω; and T_A = –40°C to +85°C, unless otherwise noted. (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Output High Voltage	V_{OH}	V_{CC} – 0.020	V_{CC} – 0.020	V_{CC}	V	—
Output Voltage Swing	V_{OUT}	325	400	500	mV	—
Differential Output Voltage Swing	V_{DIFF_OUT}	650	800	1000	mV	—
Output Source Impedance	R_{OUT}	40	50	60	Ω	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

TABLE 1-3: AC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.5V ±5% and T_A = –40°C to + 85°C, unless otherwise noted.						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Maximum Operating Frequency	f_{MAX}	6	—	—	GHz	V_{OUT} ≥ 200 mV (Clock)
		—	10	—	Gbps	NRZ Data
Propagation Delay	t_{pd}	110	180	260	ps	—
Output-to-Output Skew	t_{SKEW}	—	4	15	ps	Note 1
Part-to-Part Skew		—	—	50	ps	Note 2
Output Rise/Fall Time 20% to 80%	t_r, t_f	20	40	60	ps	At full swing
Additive Phase Jitter	t_{JITTER}	—	27	—	fsRMS	Carrier = 622 MHz, Integration Range: 12 kHz–20 MHz
		—	128	—	fsRMS	Carrier = 156.25 MHz, Integration Range: 12 kHz–20 MHz

Note 1: Skew is measured between outputs under identical transitions.

2: Skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

TABLE 1-4: TEMPERATURE SPECIFICATIONS

Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Range						
Operating Ambient Temperature	T_A	–40	—	+85	°C	—
Lead Temperature	T_{LEAD}	—	+260	—	°C	Soldering, 20 sec.
Storage Temperature	T_S	–65	—	+150	°C	—
Package Thermal Resistance						
VQFN, Still Air	θ_{JA}	—	+60	—	°C/W	—
VQFN, 500 lfpm		—	+54	—	°C/W	—
VQFN, Junction-to-Board (Note 1)	Ψ_{JB}	—	+33	—	°C/W	—

Note 1: Thermal performance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1, 4	IN, /IN	**Differential Input:** This input pair receives the signal to be buffered. Each pin of this pair internally terminates with 50Ω to the VT pin. Note that this input will default to an indeterminate state if left open. See “Input Interface Applications” section.
2	VT	**Input Termination Center-Tap:** Each input terminates to this pin. The VT pin provides a center-tap for each input (IN, /IN) to the termination network for maximum interface flexibility. See “Input Interface Applications” section.
3	VREF-AC	**Reference Output Voltage:** This output biases to V_{CC} – 1.2V. It is used when AC-coupling to differential inputs. Connect VREF-AC directly to the VT pin. Bypass with 0.01 µF low ESR capacitor to VCC. See “Input Interface Applications” section.
8, 13	VCC	**Positive Power Supply:** Bypass with 0.1 µF || 0.01 µF low ESR capacitors as close to the pins as possible.
5, 16	GND, Exposed Pad	**Ground.** Exposed pad must be connected to a ground plane that is the same potential as the ground pin.
14, 15 11, 12 9, 10 6, 7	/Q0, Q0 /Q1. Q1 /Q2. Q2 /Q3. Q3	**CML Differential Output Pairs:** Differential buffered output copy of the input signal. The output swing is typically 400 mV into 50Ω load. Normally terminate CML output pairs with 100Ω across Q and /Q outputs at the receiving end. Unused output pairs may be left floating with no impact on jitter or skew. See “CML Output Termination” section.

3.0 TYPICAL CHARACTERISTICS

V_{CC} = 2.5V; GND = 0; V_{IN} = 100 mV; and T_A = 25°C, unless otherwise noted.

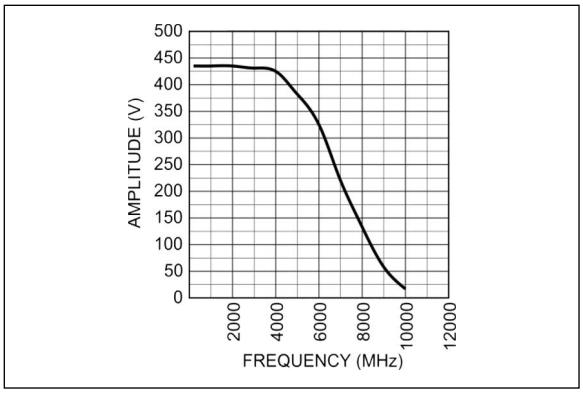


FIGURE 3-1: AMPLITUDE VS. FREQUENCY.

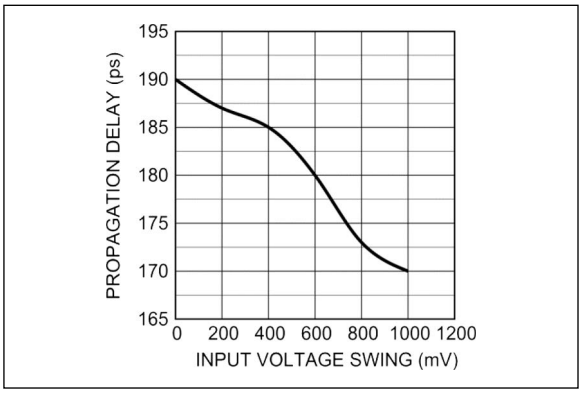


FIGURE 3-3: PROPAGATION DELAY VS. INPUT VOLTAGE SWING.

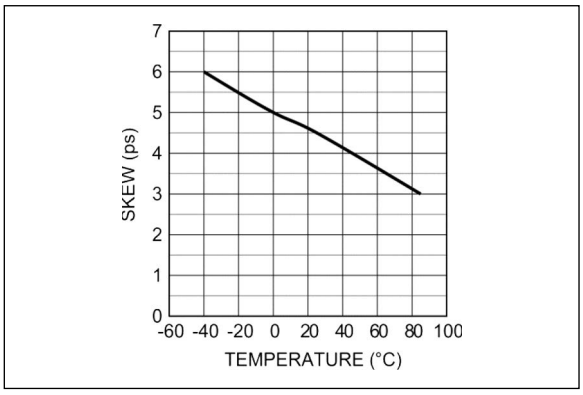


FIGURE 3-2: SKEW VS. TEMPERATURE.

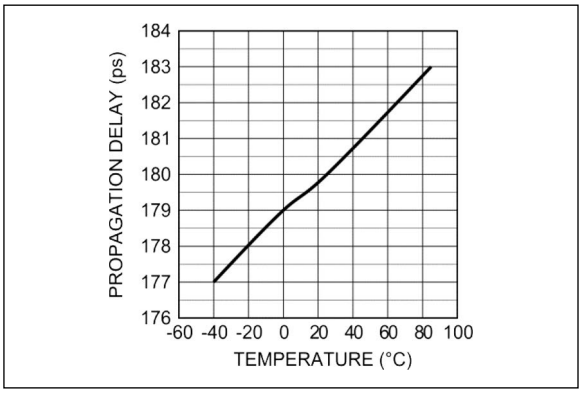


FIGURE 3-4: PROPAGATION DELAY VS. TEMPERATURE.

4.0 TYPICAL OUTPUT WAVEFORMS

V_{CC} = 2.5V; GND = 0; V_{IN} = 100 mV; and T_A = 25°C, unless otherwise noted.

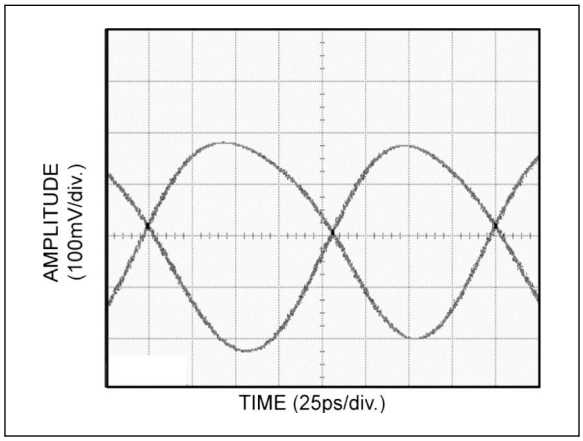


FIGURE 4-1: 5 GHZ OUTPUT.

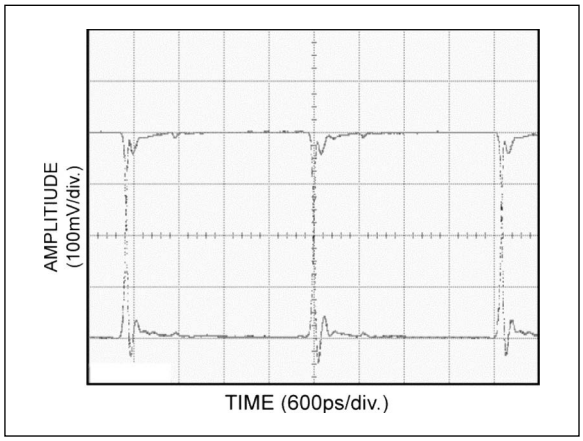


FIGURE 4-2: 200 MHZ OUTPUT.

5.0 ADDITIVE PHASE NOISE PLOTS

V_{CC} = 3.3V; GND = 0; and T_A = 25°C, unless otherwise noted.

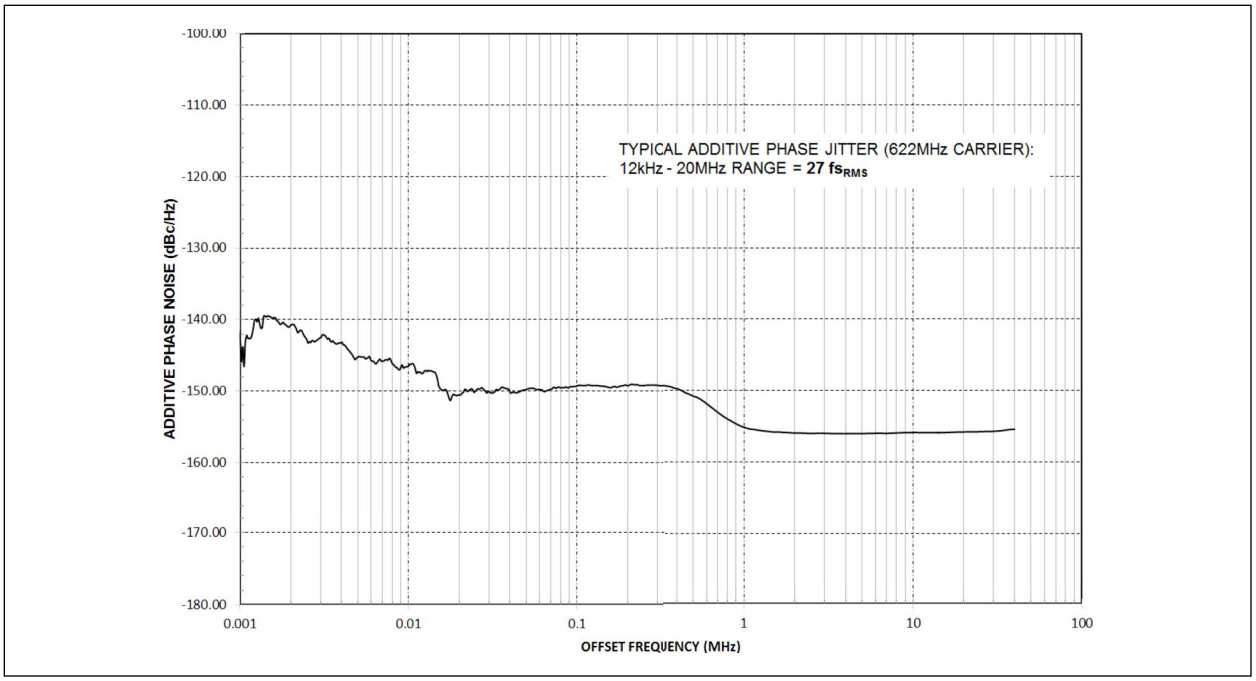


FIGURE 5-1: TYPICAL ADDITIVE PHASE JITTER (622 MHZ CARRIER), 12 KHZ–20 MHZ RANGE = 27 FS_{RMS}.

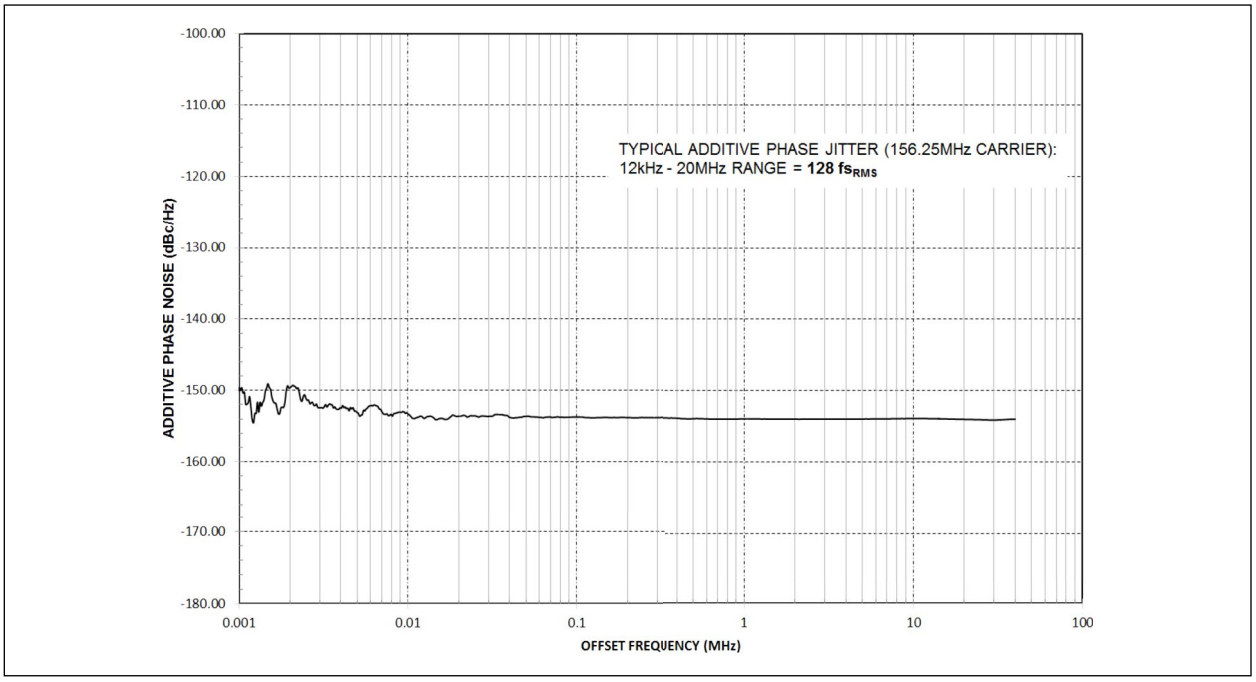


FIGURE 5-2: TYPICAL ADDITIVE PHASE JITTER (156.25 MHZ CARRIER), 12 KHZ–20 MHZ RANGE = 128 FS_{RMS}.

6.0 CML OUTPUT TERMINATION

Figure 6-1 and Figure 6-2 illustrate a CML output using both the AC-coupled and DC-coupled configuration. All outputs of the SY58020U are 50Ω with a 16 mA current source.

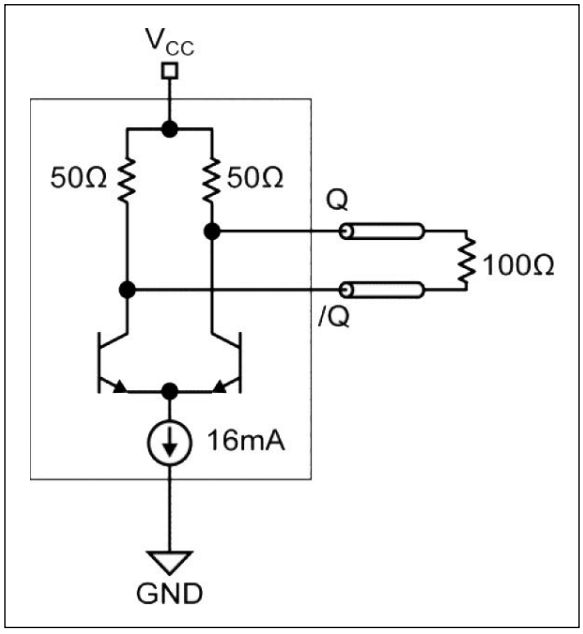


FIGURE 6-1: CML DC-COUPLED OUTPUT.

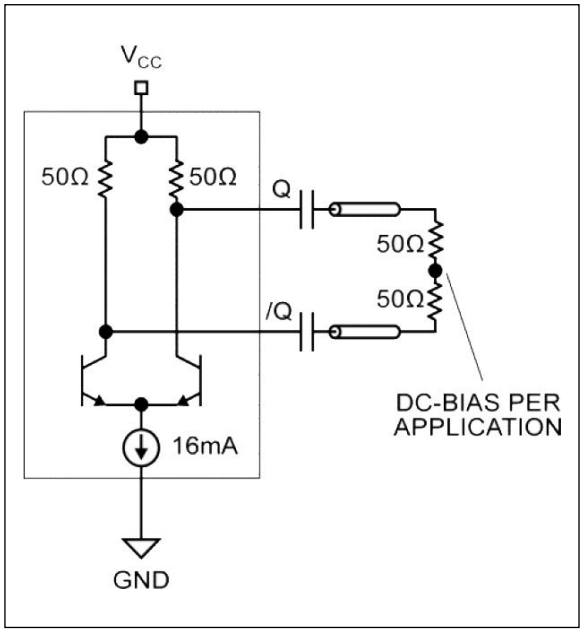


FIGURE 6-2: CML AC-COUPLED TERMINATION.

7.0 SINGLE-ENDED AND DIFFERENTIAL SWINGS

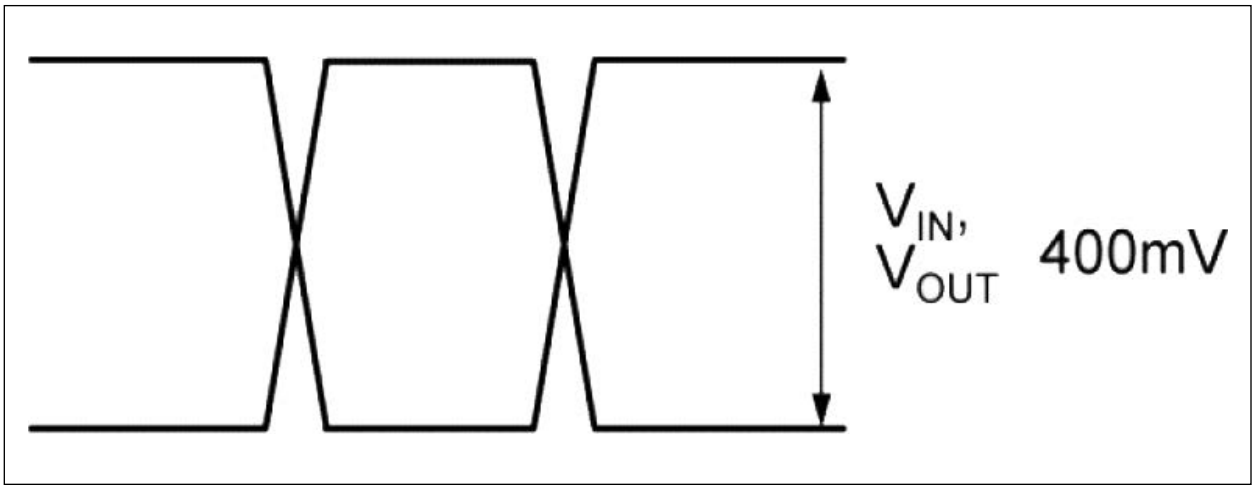


FIGURE 7-1: SINGLE-ENDED VOLTAGE SWING.

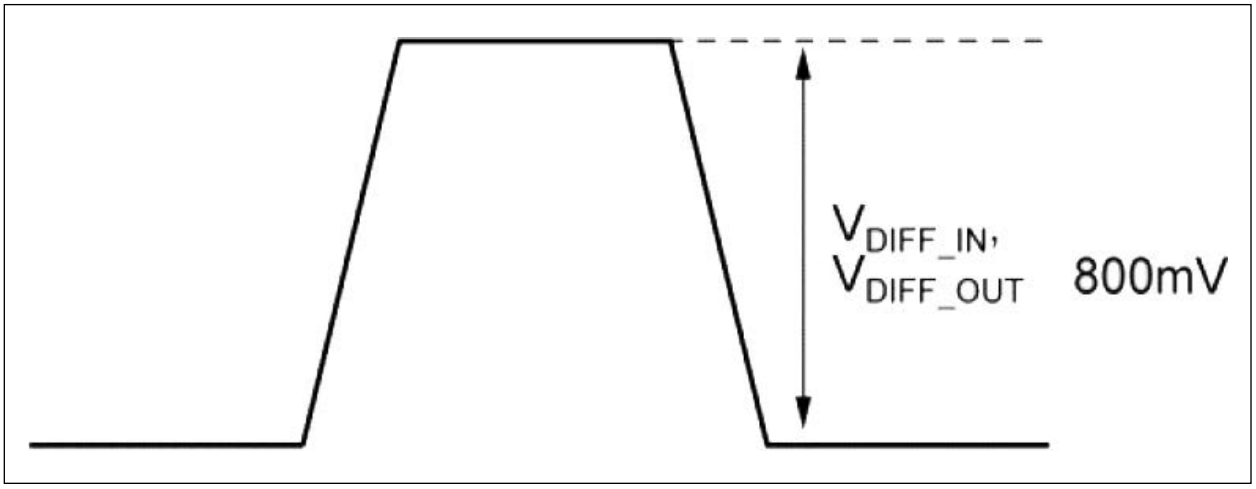


FIGURE 7-2: DIFFERENTIAL VOLTAGE SWING.

8.0 TIMING DIAGRAM

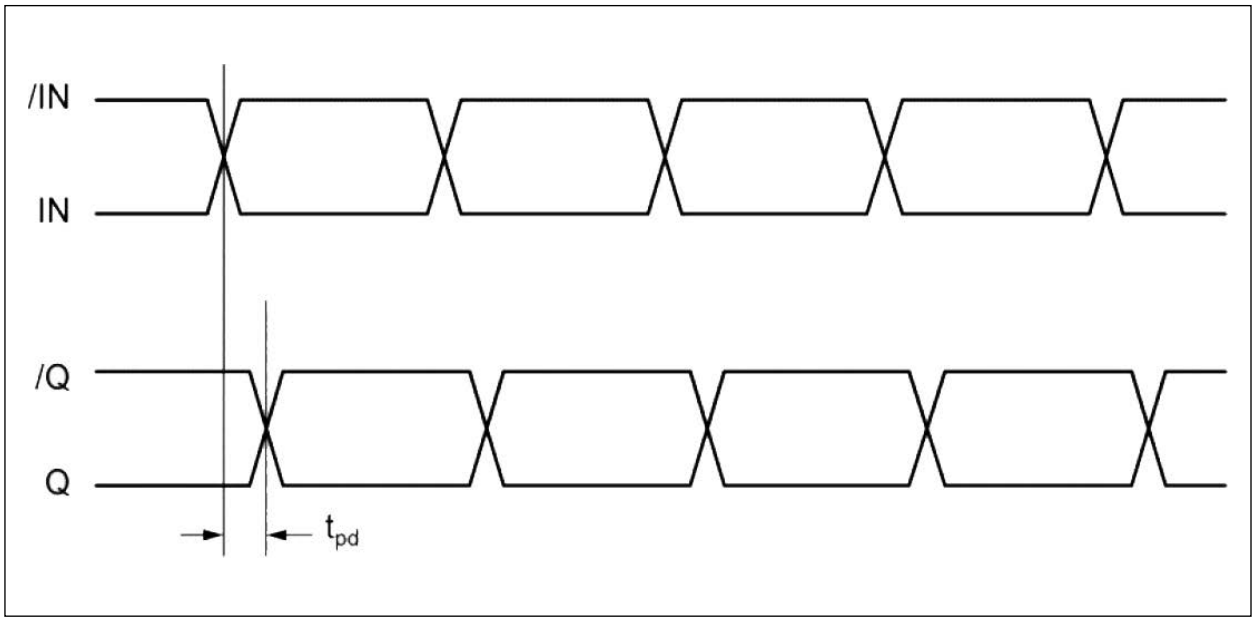


FIGURE 8-1: TIMING DIAGRAM.

9.0 INPUT STAGE

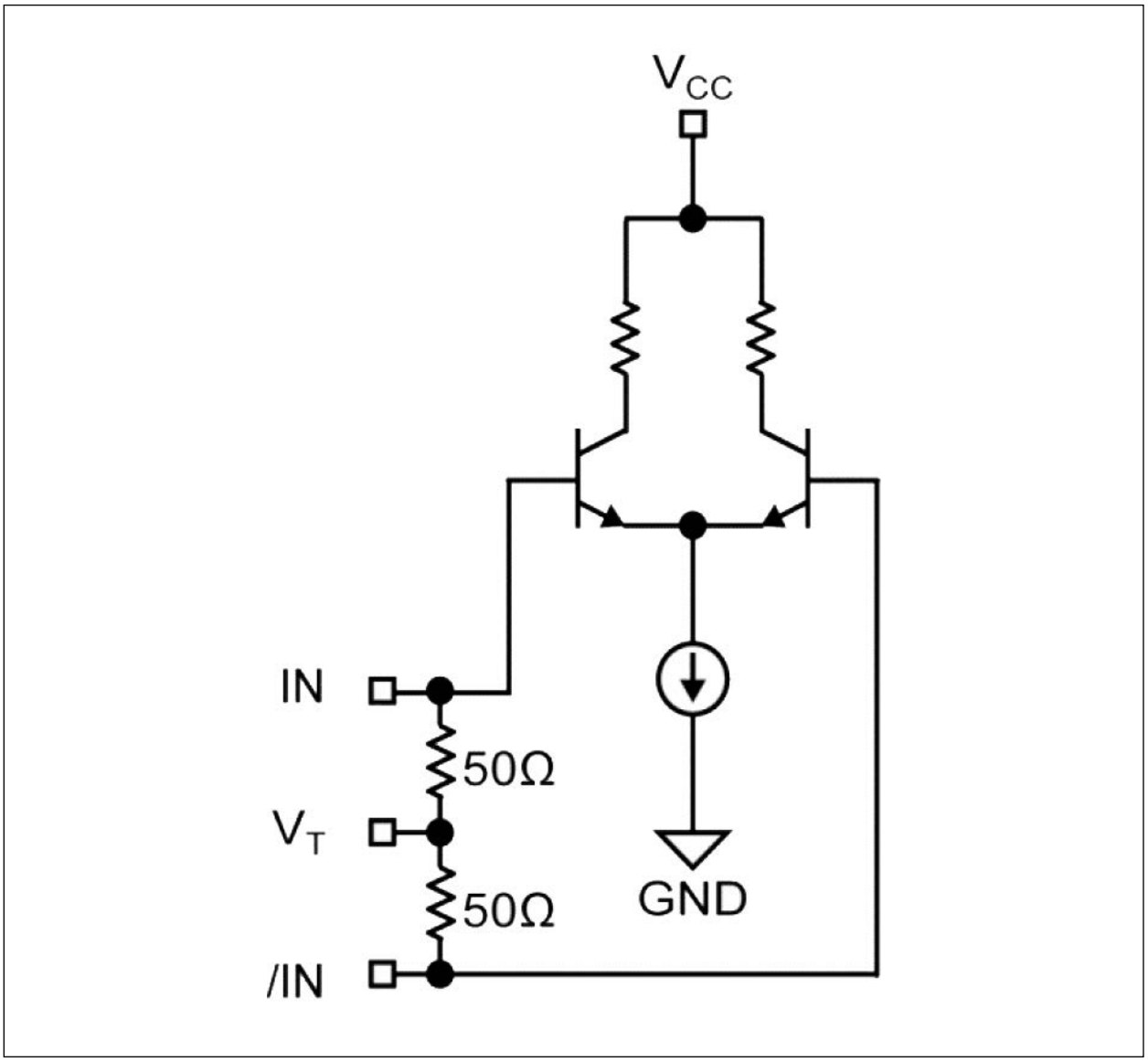


FIGURE 9-1: SIMPLIFIED DIFFERENTIAL INPUT BUFFER.

10.0 INPUT INTERFACE APPLICATIONS

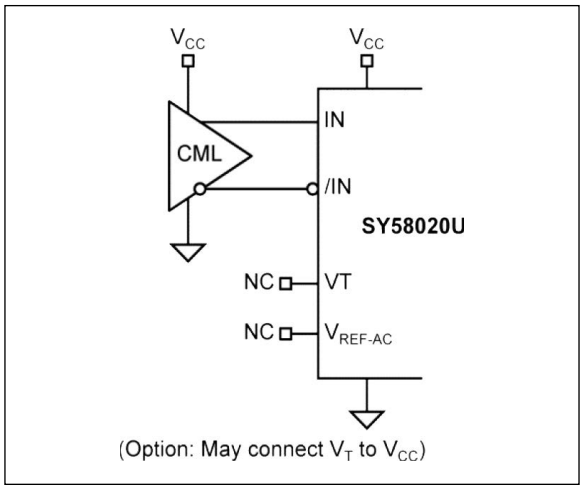


FIGURE 10-1: DC-COUPLED CML INPUT INTERFACE.

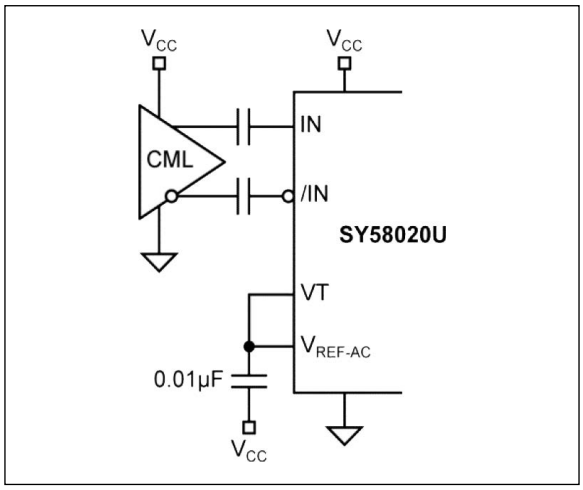


FIGURE 10-2: AC-COUPLED CML INPUT INTERFACE.

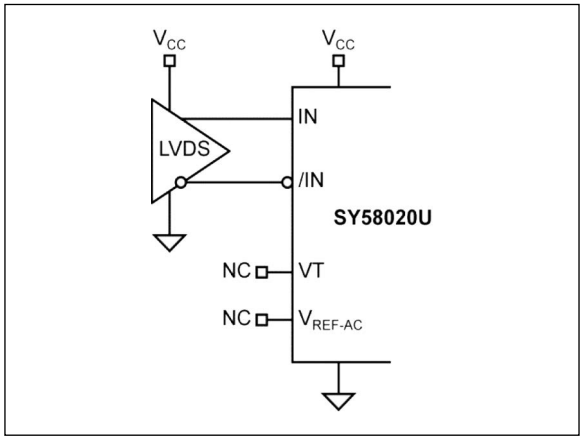


FIGURE 10-3: DC-COUPLED LVDS INPUT INTERFACE.

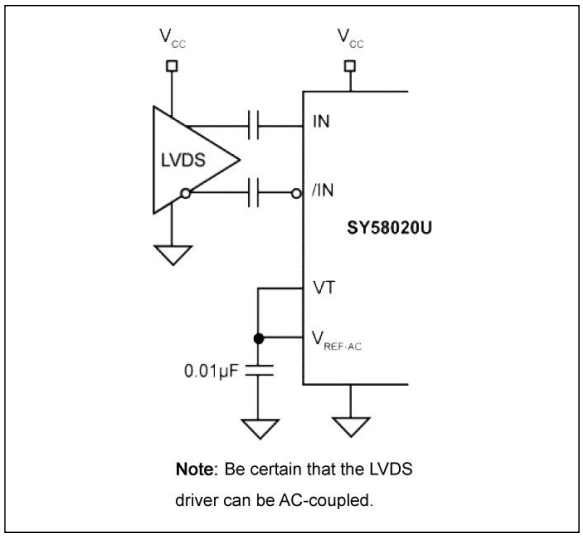


FIGURE 10-4: AC-COUPLED LVDS INPUT INTERFACE.

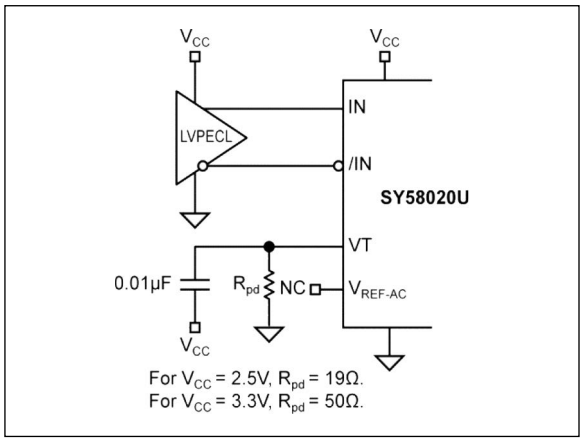


FIGURE 10-5: DC-COUPLED LVPECL INPUT INTERFACE.

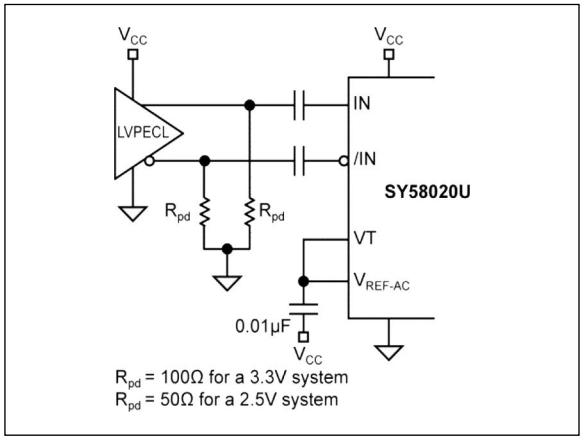
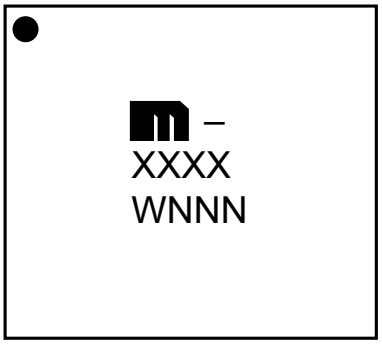


FIGURE 10-6: AC-COUPLED LVPECL INPUT INTERFACE.

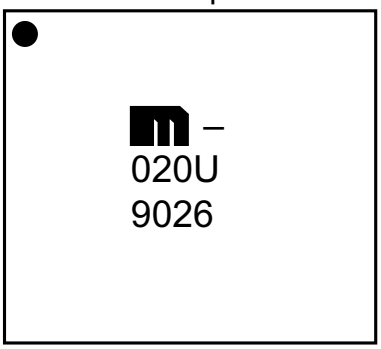
11.0 PACKAGING INFORMATION

11.1 Package Marking Information

16-Lead VQFN*



Example*



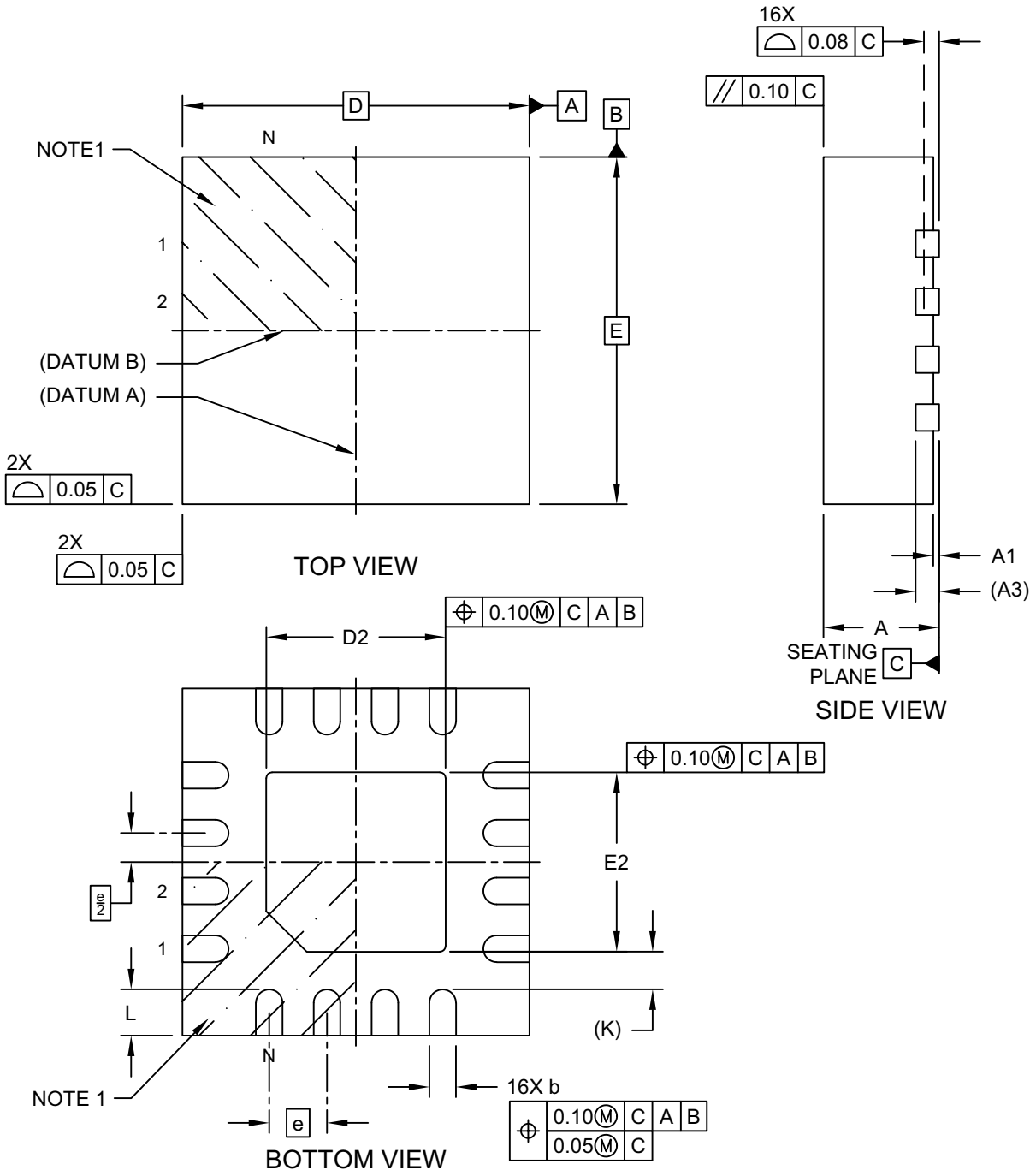
Legend:	XX...X	Product code or customer-specific information
	W	Week code
	NNN	Alphanumeric traceability code (week)
	*	This package is Pb-free. The Pb-free JEDEC designator can be found on the outer packaging for this package.
	●	Pin one index is identified by a dot

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

16-Lead 3 mm × 3 mm VQFN [NCA] Package Outline and Recommended Land Pattern

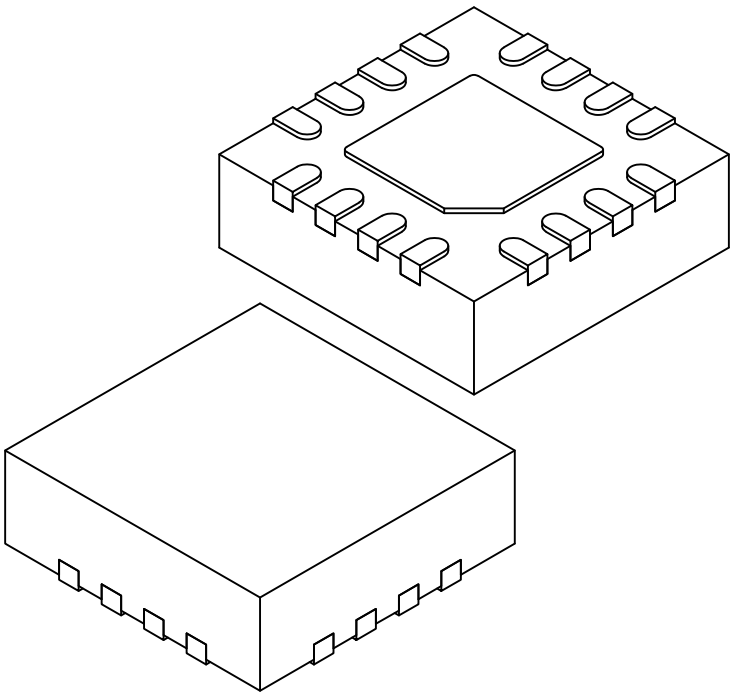
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1103-NCA Rev C Sheet 1 of 2

16-Lead 3 mm × 3 mm VQFN [NCA] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		16	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	1.50	1.55	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.55	1.60
Terminal Width	b	0.18	0.23	0.28
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.33 REF	

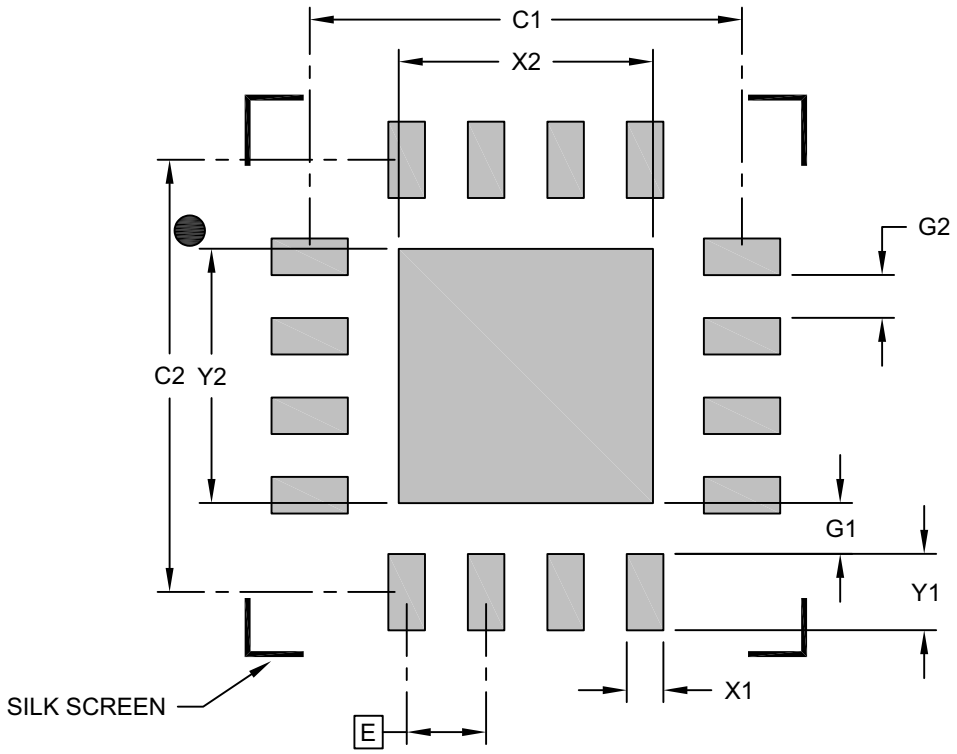
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1103-NCA Rev C Sheet 2 of 2

16-Lead 3 mm × 3 mm VQFN [NCA] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			1.60
Center Pad Length	Y2			1.60
Contact Pad Spacing	C1		2.72	
Contact Pad Spacing	C2		2.72	
Contact Pad Width (Xnn)	X1			0.23
Contact Pad Length (Xnn)	Y1			0.48
Contact Pad to Center Pad (Xnn)	G1	0.32		
Contact Pad to Contact Pad (Xnn)	G2	0.27		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3103-NCA Rev C

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (February 2024)

- Converted Micrel data sheet for SY58020U to Microchip format as DS20006872A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	-XX
Device	Supply Voltage Range	Package	Temperature Range	Special Processing

Device:	SY58020	=	6 GHz, 1:4 CML Fanout Buffer/ Translator with Internal I/O Termination
Voltage Option:	U	=	2.5V/3.3V
Package:	M	=	16-Lead VQFN
Temperature Range:	G	=	–40°C to 85°C
Special Processing:	<blank>	=	100/Tube
	TR	=	1,000/Reel

Examples:

a) **SY58020UMG**

2.5V/3.3V, 16-Lead VQFN, –40°C to 85°C, 100/Tube

b) **SY58020UMG-TR**

2.5V/3.3V, 16-Lead VQFN, –40°C to 85°C, 1,000/Reel

NOTES:

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
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