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AN4686

Watchdog Timer (WDT) on ATSAM E70/S70/V70/V71 Devices Using MPLAB Harmony v3

Introduction

The Watchdog Timer (WDT) is used to ensure that a system can recover from unforeseen failures in firmware or hardware. The WDT can detect abnormalities in the program execution and respond by resetting the microcontroller (MCU). This brings the MCU to a well-defined and known state where normal operation can be resumed.

Based on the source clock, clock prescaler, and internal counter size (number of bits) of the WDT, the timeout period can be configured up to a specified time period mostly up to an order of tens of seconds.

This document discusses the WDT theory of operations, modes, and clock sources. It also covers configuration and code generation using MPLAB® Harmony v3.

Table of Contents

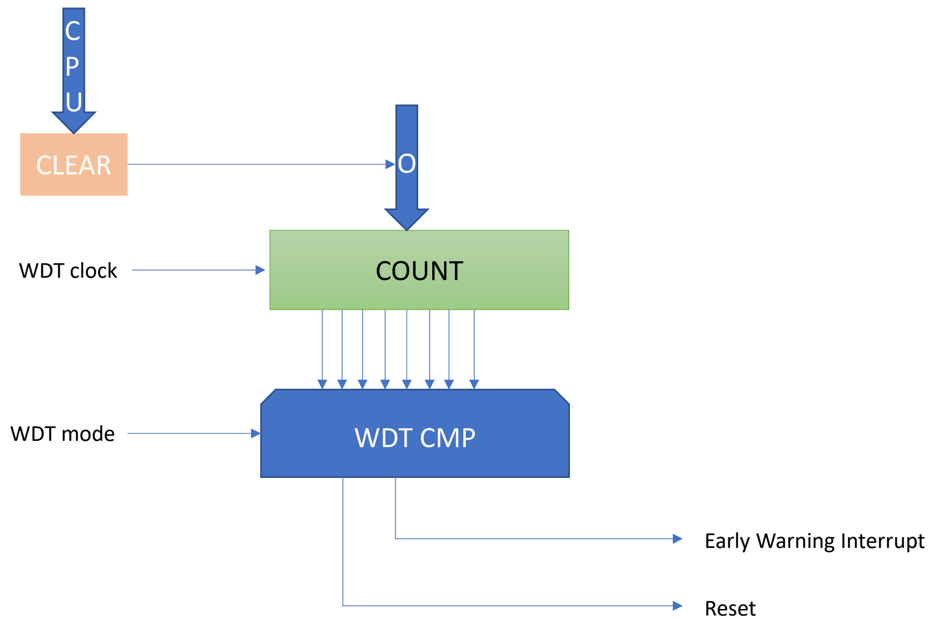
1. Acronyms

Term	Details
WDT	Watchdog Timer
CLK	Clock Source
INT	Interrupt
ISR	Interrupt Service Routine
MCU	Microcontroller
WDD	Watchdog Delta Value
WDV	Watchdog Counter Value

2. Theory of Operation

Once enabled, the WDT requires the application software to write a bit pattern to a WDT register within an allocated time period. If the WDT clear register is not updated by the application within the allotted time, a system reset signal is generated and an interrupt handler is activated.

Figure 2-1. Basic Principle of a WDT

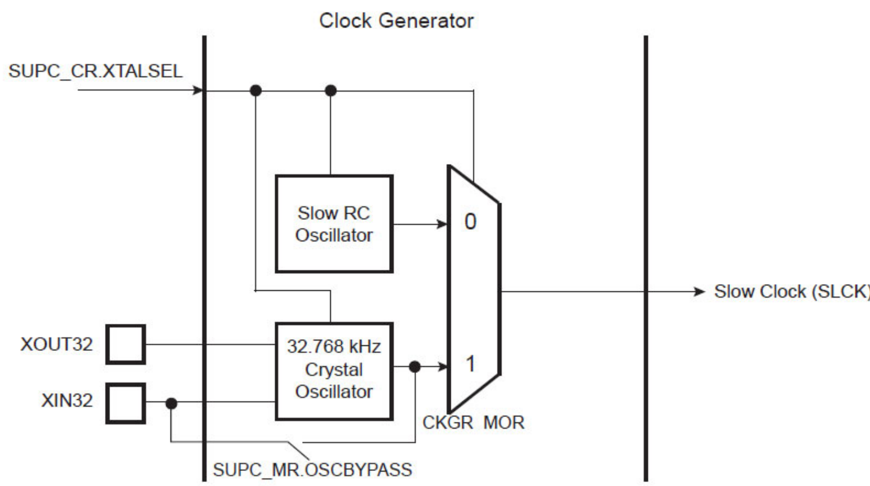


3. WDT Clock Source for ATSAM E70/S70/V70/V71 Devices

The WDT is built around a 12-bit down counter, which is loaded with the value defined in the field WDV of the Mode Register (WDT_MR). The WDT uses the slow clock divided by 128 to establish the maximum watchdog period to be 16 seconds.

The maximum value for the WDT counter is 0xFFF (or 4095). Using a clock source of 32 kHz (or a period of 31.25 μs) and a prescaler value set to a maximum value of 128, will result in a clock period of 4 ms that it will further result in a WDT timeout period of 16.38 seconds (4095 x 4 ms).

Figure 3-1. Clock Source for WDT on SAM E70/S70/V70/V71 Devices



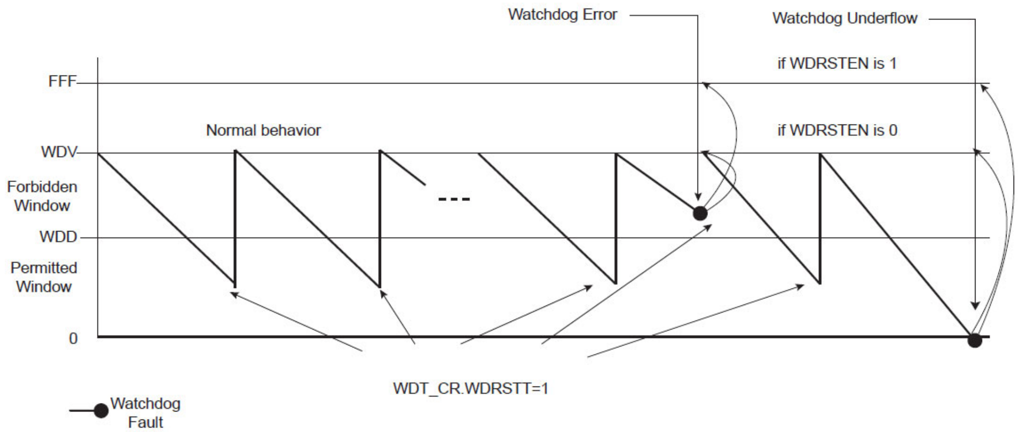
The clock source is fully configurable and must be used based on the system requirements and constraints. The internal RC oscillator has a faster startup time compared with the external crystal oscillator, but at the same time is characterized by a high tolerance that may vary with voltage supply, temperature, and the manufacturer process.

By default, the WDT starts by using the Slow RC Oscillator as a source. After startup the External Crystal Oscillator can be enabled, this operation is characterized as a glitch-free transition. The reverse transition for a clock source is only possible by shutting down the VDDIO power supply.

3.1 Modes of Operation

When enabled, the WDT is a timer which runs constantly, that is configured to a predefined time-out period. Before the end of the time-out period, the WDT must be set back or else a system Reset is issued. The WDT has two modes of operation, Normal mode and Window mode, both of these modes offer the option of Early Warning Interrupt generation.

Figure 3-2. WDT Behavior



3.1.1 Normal Mode

The WDT can be used in Normal mode, which is when a single timeout period is set for the WDT. If the WDT is not reset before the timeout occurs, the WDT will cause a system reset, or it will trigger an interrupt.

For the WDT available on the SAM E70/S70/V70/V71 devices, this mode can be activated by programming a WDT_MR.WDD value greater than or equal to the WDT_MR.WDV value. In such a configuration, restarting the Watchdog Timer is permitted in the whole range [0; WDT_MR.WDV] and does not generate an error. This is the default configuration on reset, the WDT_MR.WDD and WDT_MR.WDV values are equal.

3.1.2 Window Mode

For Window mode, the user must consider these two thresholds, and both parameters can be set within the WDR_MR register.

- WDD: Watchdog Delta Value.
- WDV: Watchdog Counter Value.

To use this Watchdog mode and to avoid errors, the reload must occur while the watchdog counter is between ‘0’ and WDD. Trying to restart the watchdog while the internal counter is above the WDD and below the WDV will result in a fault event.

4. WDT Configuration for SAM E70/S70/V70/V71 Devices

The WDT configuration permits the activation of different reactions based on the needs of the system. The control and configuration are mostly done using the Timer Control Register (WDR_CR) and Timer Mode Register (WDT_MR). The Watchdog feedback can be read from the Status Register, WDT_SR.

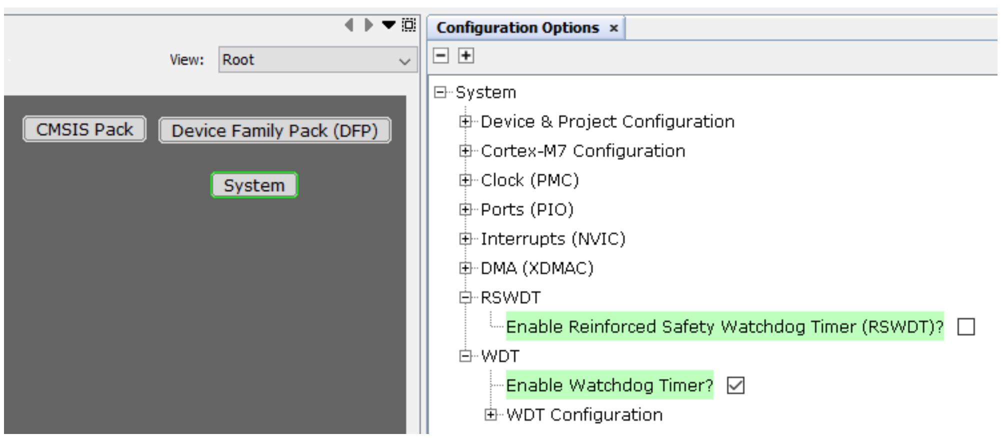
4.1 WDT Global Enabling/Disabling

After reset, the WDT is enabled by default. The user can either disable the WDT by setting the WDT_MR.WDDIS bit or reprogram the WDT to meet the maximum Watchdog period the application requires.

While the processor is in a debug state or in Sleep mode, the counter may be stopped depending on the value programmed for the WDT_MR.WDIDLEHLT and WDT_MR.WDDBGHLT bits. These bits will affect the WDT behavior only if the global WDT disable bit (WDR_MR.WDDIS) is not set.

The following figure shows the WDT global enable or disable configuration settings in the MCC project graph.

Figure 4-1. WDT Global Enable/Disable

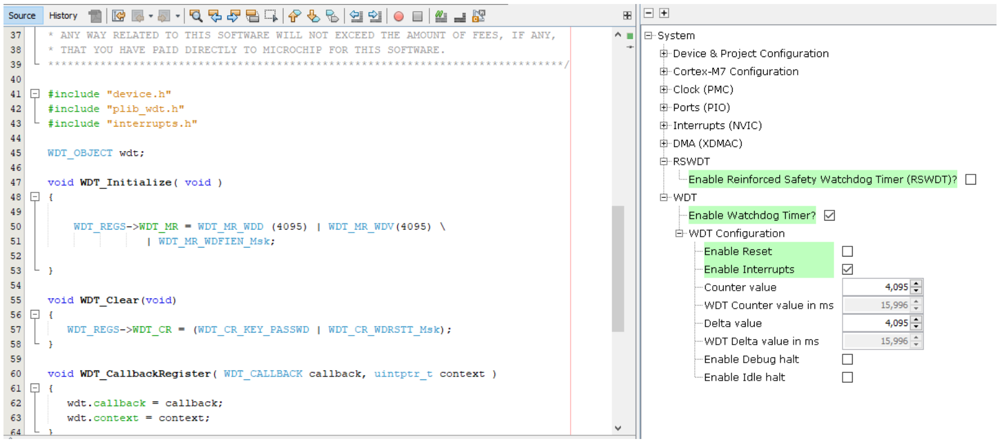


4.2 WDT Configuration for Normal Mode

After reset, the normal mode is the default configuration on reset, the WDT_MR.WDD and WDT_MR.WDV values are equal. To avoid fault events, the Watchdog counter must be reset before reaching a zero value.

The following figure shows the WDT normal mode configuration settings in the MCC project graph and the corresponding generated code.

Figure 4-2. WDT Normal Mode

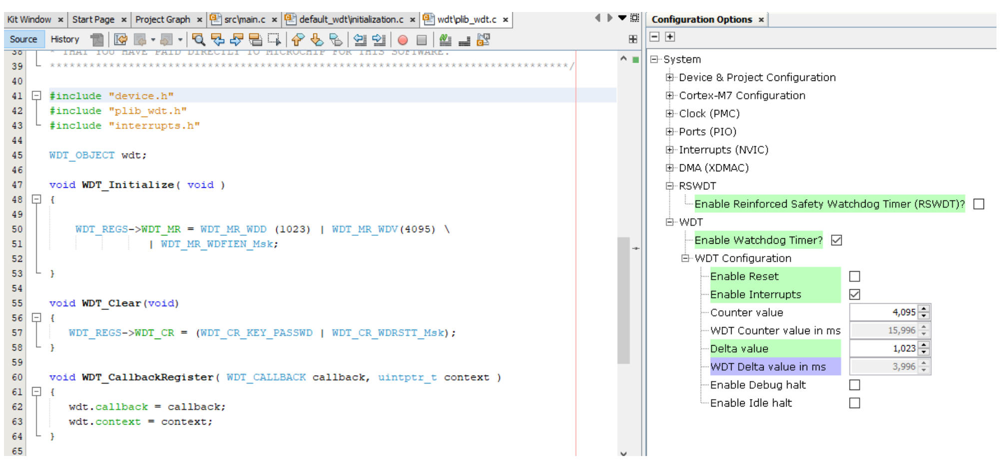


4.3 WDT Configuration for Window Mode

Reloading of the Watchdog must occur while the Watchdog counter is within a window between zero and WDT_MR.WDD. Any attempt to restart the Watchdog while the Watchdog counter is between WDT_MR.WDV and WDT_MR.WDD results in a Watchdog error, even if the Watchdog is disabled.

The following figure shows the WDT window mode configuration settings in the MCC project graph and the corresponding generated code.

Figure 4-3. WDT Window Mode



4.4 WDT Restart Counter

The user reloads the Watchdog at regular intervals before the timer underflow occurs, by setting the WDT_CR.WDRSTT bit. The Watchdog counter is then immediately reloaded from WDT_MR and restarted.

The WDT_CR register is write-protected. As a result, writing to the WDT_CR without the correct hard-coded key has no effect.

The following figure shows the MPLAB Harmony v3 API that can be called by the user application to reload the WDT counter.

Figure 4-4. WDT Clear API from MPLAB Harmony v3

```
void WDT_Clear(void)
{
    WDT_REGS->WDT_CR = (WDT_CR_KEY_PASSWD | WDT_CR_WDRSTT_Msk);
}
```

4.5 Reading the WDT Status Bits

If an underflow occur, the `wdt_fault` signal to the Reset Controller is asserted if the WDT_MR.WDRSTEN bit is set. In addition, the WDUNF bit is set in the Status register (WDT_SR).

Any attempt to restart the Watchdog while the Watchdog counter is between WDV and WDD results in a Watchdog error, even if the Watchdog is disabled. The WDT_SR.WDERR bit is updated and the `wdt_fault` signal to the Reset Controller is asserted.

Both status bits, WDT_SR.WDERR (Watchdog Error), and WDT_SR.WDUNF (Watchdog Underflow), are cleared on read.

5. WDT Timeout Calculation

The WDT is based on a source clock according to the configuration of the registers. For this clock a prescaler value can also be applied to extend the period. With this new derived clock and with the WDT counter configured internally, the user can calculate the final WDT timeout period.

The following table provides a basic SLCK value of 32 kHz and the resulting WDT timeout period by using various SLCK prescaler and WDT counter values.

Table 5-1. Basic SLCK Value as Related to WDT Timeout Periods

SLCK (32 KHz) SLCK Prescaler	SLCK Period (us)	Watchdog Counter Value WDT_MR[WDV]	WDT Timeout Period (seconds)
1	31.25	511	0.016
		2047	0.064
		4095	0.128
2	62.5	511	0.032
		2047	0.128
		4095	0.256
4	125	511	0.064
		2047	0.256
		4095	0.512
8	250	511	0.128
		2047	0.512
		4095	1.024
16	500	511	0.256
		2047	1.024
		4095	2.048
32	1000	511	0.511
		2047	2.047
		4095	4.095
64	2000	511	1.022
		2047	4.094
		4095	8.190
128	4000	511	2.044
		2047	8.188
		4095	16.380
Note: WDT Timeout Period = (1/SLCK) * PRESCALER * WDT_COUNTER.			

6. Intended Use of the Watchdog

In general, it is recommended to issue a WDT reset from somewhere in the main loop of the firmware. Do not reset the WDT in interrupt service routines, unless the interrupt routine checks a series of flags that confirms the correct execution of various parts of the firmware. If these simple rules are followed, the WDT is hard to misuse.

The WDT window mode is a bit more challenging to use than the normal mode, as it involves more strict control of the WDT Reset timing. In window mode the WDT must be reset from somewhere within the main loop, never in interrupt service routines, as this will impair the closed window protection. Because the closed window defines the minimum expected duration of the main loop (or subsections of the main loop), it can be used to catch cases where parts of the main loop code is not executed, or cases where early exit from function calls occurs.

The internal clock for the WDT is not very accurate. The oscillator is designed to draw very little power to be able to use the WDT even in long-life battery powered applications. The downside of low-power oscillators is low accuracy. The internal clock source may vary over temperature and supply voltage, though this variation is significantly less than the ±30% device-to-device variations. Refer to the device data sheet for additional information.

The WDT interrupt can only be used if WDT_MR.WDRSTEN is cleared. If the reset exception has begun processing, then the WDT interrupt will not occur. To prevent the WDT from being useless when WDT_MR.WDRSTEN is disabled, the WDT_MR.WDFIEN bit is used. This allows an interrupt to be triggered on a fault or underflow. But setting this is useless as well unless the WDT IRQ is enabled using the NVIC.

7. Application Example

The following source code example demonstrates the usage of the Watchdog Timer for the SAM E70/S70/V70/V71 family of devices.

This example describes how to configure the WDT to initiate a reset after the timeout expires. To stop the application and feed the WDT there is a switch configuration that will jump the execution into an infinite loop.

https://github.com/Microchip-MPLAB-Harmony/csp_apps_sam_e70_s70_v70_v71/tree/master/apps/wdt/wdt_timeout

To clone or download this application from Github, go to the repository csp_apps_sam_e70_s70_v70_v7, and then click the Clone button to clone this repository or download as zip file.

Alternatively, the GitHub repository can be downloaded using the MCC content manager.

The application within the repository is in the following path *apps/wdt/wdt_timeout/firmware*. The full instructions set to build, program, and run the application is detailed in the `readme.md` file.

8. References

For additional information regarding Microchip products and services, visit the Microchip Website, or contact a local Microchip sales representative.

- The MPLAB Harmony v3 Quick Docs repository provides standalone help pages for users to get started developing applications on Microchip's 32-bit SAM and PIC32 MCUs. Start from the `index.html` present in the docs folder. The online version is available for download at microchip-mplab-harmony.github.io/quick_docs/
- Harmony Landing page: www.microchip.com/harmony
- How to Build an Application by Adding a New PLIB, Driver, or Middleware to an Existing MPLAB Harmony v3 Project: www.microchip.com/DS90003253
- MPLAB Harmony v3 Developer Help page: microchipdeveloper.com/harmony3:start
- Various Timers in SAM Devices: http://ww1.microchip.com/downloads/en/DeviceDoc/Various_Timers_%20on_SAM%20Device_DS90003230A.pdf

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