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Interfacing the SGMII Port on KSZ9xx7S and KSZ8567S Switches

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INTRODUCTION

A newly added feature on some Microchip Gigabit Ethernet switches is a serial Gigabit media independent interface (SGMII) for one of the ports. This is a low pin count interface for connecting the switch to a Gigabit Ethernet PHY, to a fiber optic transceiver, or to another switch. The following sections describe these applications, the compatible devices, how to connect them, and how to configure and manage this interface.

Applicable products are:

- KSZ8567S
- KSZ9477S
- KSZ9567S
- KSZ9897S

APPLICATION CONFIGURATION

The SGMII port interface operates at a baud rate of 1.25 Gbps to support 1000BASE-T (copper), 1000BASE-X (fiber), and lower speed Ethernet applications.

TABLE 1: SUPPORTED AND UNSUPPORTED APPLICATIONS

Supported applications	Unsupported application
10/100/1000BASE-T copper PHY or module	1000BASE-KX
100BASE-FX SFP module	10 Gbps and higher speed fiber transceivers
Non-SGMII 1000BASE-T PHY or module	Half duplex for 1000BASE-X
1000BASE-X fiber transceiver (-LX, -SX, and so on)	100BASE-FX using non-SFP transceiver
Switch to switch	

The port has two modes of operation:

- **SerDes mode** is used for connecting the switch to a 1000BASE-X (-SX, -LX, or similar) fiber optic transceiver. Additionally, some 1000BASE-T small form-factor pluggable (SFP) modules have a SerDes interface that can interface to the switch in SerDes mode.
- **SGMII mode** is used for connecting the media access control (MAC) in the switch to a multi-speed 10/100/1000BASE-T PHY or any other PHY supporting SGMII. For example, there are some 100BASE-FX (100 Mbps fiber) SFP modules that support SGMII.

These modes use the same electrical interface, but SGMII supports data rates of 10 and 100 Mbps in addition to 1 Gbps, whereas the SerDes mode is strictly 1 Gbps and full duplex. This means that the two modes exchange data differently during "auto-negotiation." In SGMII mode, the MAC receives information from the PHY about the speed, duplex, and status of the link on the Cat5 media interface. In contrast, SerDes mode uses the simpler 1000BASE-X "auto-negotiation," which is symmetric.

The following sections describe these applications in detail.

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Supported Applications

10/100/1000BASE-T PHY OR MODULE

Use SGMII mode to connect to a 10/100/1000BASE-T PHY as shown in Figure 1. The PHY may be housed in a 10/100/1000BASE-T SFP module together with the magnetics and RJ45 jack, or all of these components may be placed separately on the board.

Two separate auto-negotiations may occur in this application. First, there is auto-negotiation over the Cat5 cable so that the near-end PHY and the distant PHY link at the same speed (10, 100, or 1000 Mbps) and duplex. Second is the SGMII "auto-negotiation," where the MAC and PHY confirm communication, and the PHY informs the MAC about the speed, duplex, and status of the Cat5 media link.
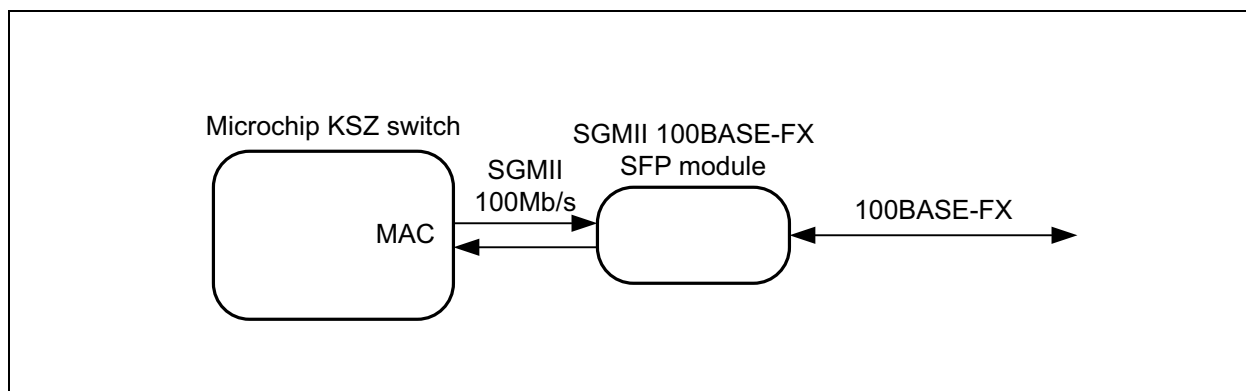
FIGURE 1:   SGMII TO CAT5 MEDIA PHY
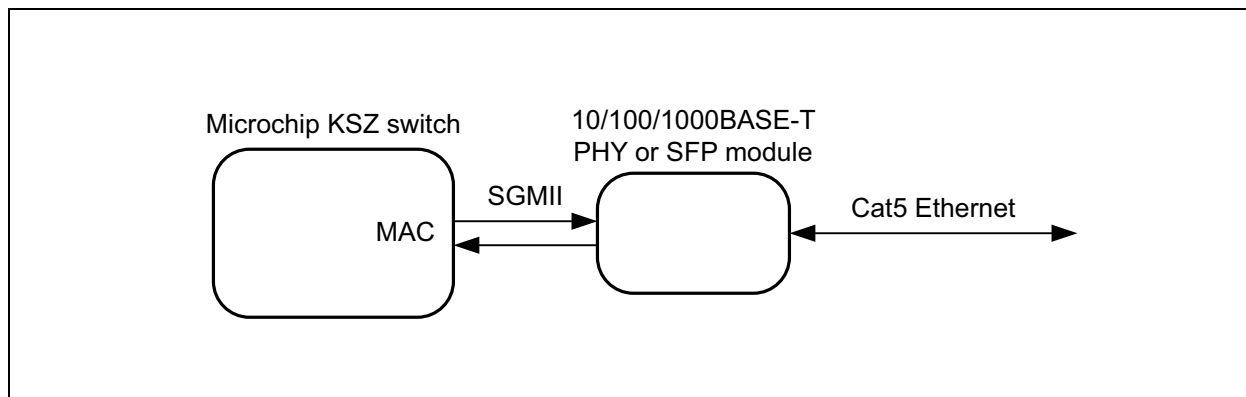
100BASE-FX SFP MODULE

There are other less commonly used SGMII devices such as the 100BASE-FX SFP module as shown in Figure 2. 100BASE-FX is always 100 Mbps and full duplex, so during SGMII auto-negotiation, the PHY (located in the SFP module) informs the MAC that the link is 100 Mbps and full duplex.

FIGURE 2:   SGMII TO 100BASE-FX SFP MODULE

NON-SGMII 1000BASE-T PHY OR MODULE

Use SerDes mode to connect to a single-speed 1000BASE-T Ethernet PHY or SFP module as shown in Figure 3. As in **Section "10/100/1000BASE-T Phy or Module"**, the PHY, magnetics, and jack may be mounted directly to the board or to an SFP module. While this configuration is similar to the 1000BASE-T configuration described earlier, the key difference is that this PHY operates only at 1000BASE-T (1 Gbps speed) and full duplex. It does not support other 10 or 100 Mbps speeds or half duplex. The only real function of this PHY is as a media converter, so SerDes mode is used instead of SGMII mode.

FIGURE 3:   SERDES MODE TO NON-SGMII 1000BASE-T PHY
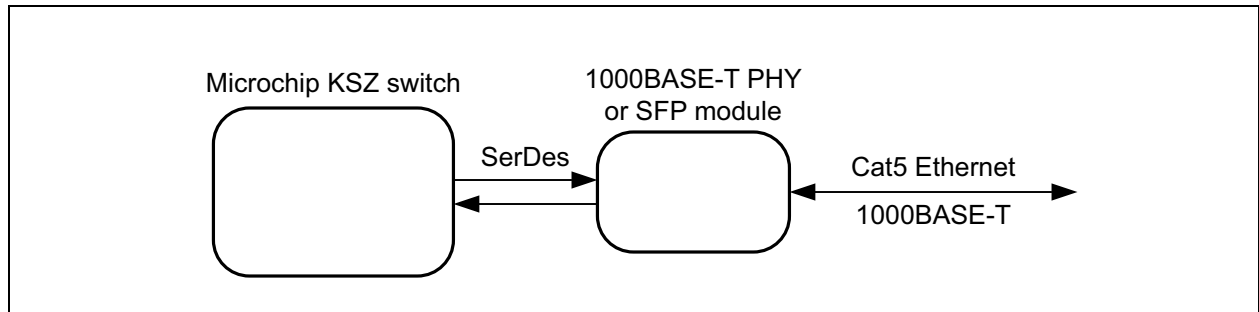
1000BASE-X FIBER TRANSCEIVER

Use SerDes mode to connect to an optical transceiver to create a 1000BASE-X (-SX, -LX, or similar) fiber Ethernet port. The switch supports only full duplex in this mode, which is standard for 1000BASE-X. The optical transceiver is not involved in auto-negotiation, so the "auto-negotiation" exchange is between the switch and the device at the far end of the optical fiber. Figure 4 illustrates this configuration.

**FIGURE 4:   1000BASE-X MODE TO OPTICAL TRANSCEIVER**
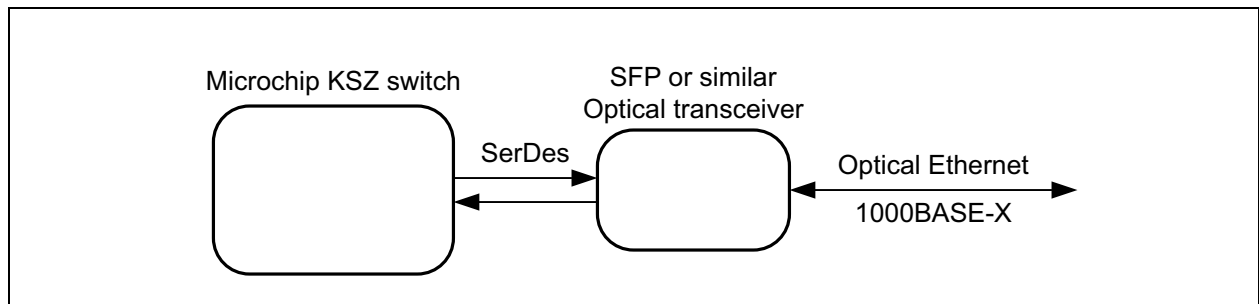
SWITCH TO SWITCH CONNECTION

Two switches can be connected together using either the SGMII mode or the SerDes mode. Neither mode has an advantage over the other, but for simplicity, this document describes only a switch-to-switch interface using SGMII mode with auto-negotiation disabled. The two switches can be on the same board, or the SGMII connection can span a backplane. This configuration is shown in Figure 5.

FIGURE 5:   SGMII SWITCH TO SGMII SWITCH
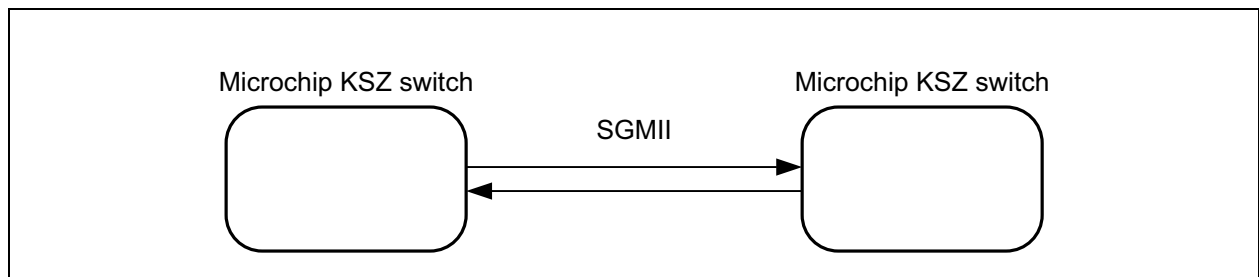
Configuration Detection

The KSZxxx7S switches cannot automatically detect the attached device, nor switch automatically between SGMII and SerDes modes. It is important to understand the limitations of each mode and which devices are compatible with each mode. For systems that can accept interchangeable interface modules such as SFP, users must be instructed about which specific SFP modules may be used for that system. If both SGMII and SerDes modes must be supported, then it is possible for the software to manage the interface and switch modes to match the installed module, as described in **Section "Supporting Multiple Types of SFP Modules"**.

SELECTING A FIBER MODULE

The IEEE 1000BASE-X standard refers to a family of interfaces such as 1000BASE-SX and 1000BASE-LX, which use different optics to span different distances. In practice, a wide range of optical transceivers is available, which supports a variety of fiber types, optical wavelengths, cable length, and data rates. In addition to the traditional two-fiber interface (one for transmit and one for receive), transceivers that transmit and receive at different wavelengths over a single fiber are available. However, the specifics of the fiber-side interface are irrelevant to the SGMII port of the switch.

To be compatible with the switch SGMII port operating in SerDes mode, an optical transceiver only needs to support 1.25 Gbps data rate. The transceiver may be SFP or any other form factor.

SELECTING A CAT5 PHY OR MODULE

Gigabit Ethernet over copper can be implemented on the SGMII port of the switch using separate PHY chip, magnetics, and RJ45 jack, or all of these components can be purchased as an integrated module, typically in SFP.

Cat5 Gigabit Ethernet SFP modules come in two types. One type supports only SGMII mode, while the other type supports only SerDes mode, so understanding the differences is important in order to design for the desired type and then install the correct module.

The 10/100/1000BASE-T SFP modules support all three speeds of Ethernet over twisted pair cable. They connect to the MAC using SGMII mode, which can operate at 10, 100, or 1000 Mbps data rates to match the link speed on the twisted pair cable interface. This type of SFP module is described as "SGMII" and supports all three Cat5 speeds: 10, 100, and 1000 Mbps. This type of module is not compatible with SerDes mode in the switch.

Another type of Cat5 media SFP module operates at fixed 1000BASE-X speed and full duplex, and connects to the MAC via SerDes mode rather than SGMII mode. From the standpoint of the switch, this fixed speed 1000BASE-T module behaves the same as a 1000BASE-X fiber module. In the documentation for this type of module, there is no mention of SGMII or 10/100BASE-T. It may or may not be referred to as having a "SerDes" interface.

If both types of modules must be supported, it is possible through software to monitor certain registers to determine the installed module type and then set the interface mode for that module. This is explained in detail in **Section "Supporting Multiple Types of SFP Modules"**.

SCHEMATIC AND LAYOUT RECOMMENDATIONS

The SGMII or SerDes interface operates at 1.25 Gbps and consists of one TX differential pair and one RX differential pair using low-voltage differential signals (LVDS). The receiver recovers the clock from the data, eliminating the need for separate clock signals.

AC coupling is required on each signal. Note that SFP modules include AC coupling capacitors on both the TX and RX pairs, so external coupling capacitors are not needed. In other applications such as switch-to-switch or switch-to-PHY, use 0.1-µF ceramic chip capacitors. Figure 6, Figure 7, and Figure 8 show the connections for each application type.

FIGURE 6: **CONNECTION DIAGRAM FOR SWITCH-TO-SWITCH**
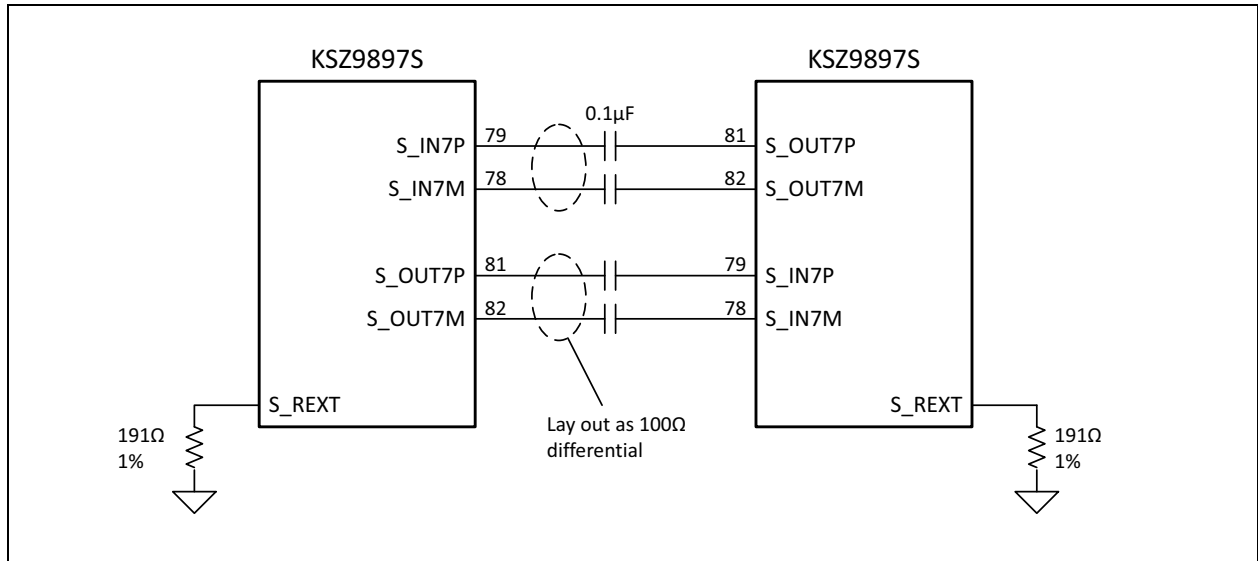

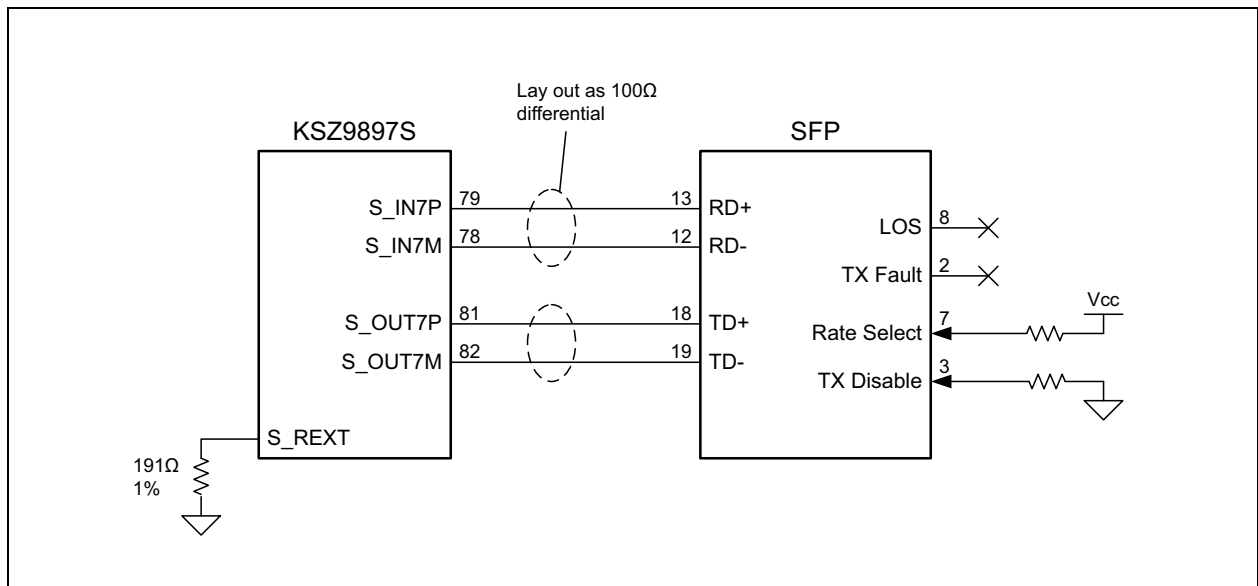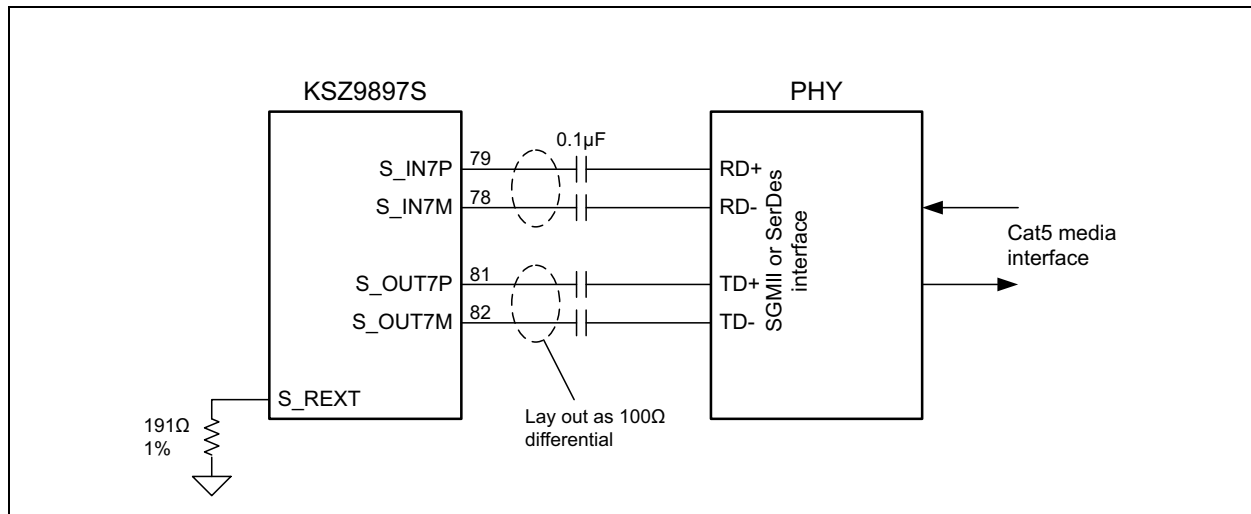**FIGURE 7:** **CONNECTION DIAGRAM FOR SWITCH TO SFP MODULE**

FIGURE 8: **CONNECTION DIAGRAM FOR SWITCH TO PHY**

The signal type is LVDS, which requires 100-ohm termination across each pair at the destination end. Microchip's switches and all SFP devices contain the termination resistors internally, so no external resistors are needed. When connecting any other device to the switch, it is important to check the documentation of that device to determine if it requires an external termination resistor at its input.

Standard best practices should be applied when routing the differential signals with appropriate clearances to other signals. The differential impedance requirement is 100 ohms. Work with PCB vendors to optimize trace widths and spacing for your particular stack-up to achieve 100 ohms. The length of each signal pair should match to within 50 mils (1.2 mm). The maximum trace length is 20 inches (50 cm). In backplane applications, use high-speed connectors rated for multi-GHz frequencies.

The main 25-MHz crystal (or oscillator) used for the switch is also used for the SGMII interface. No additional reference clock is needed. As with non-SGMII Ethernet devices, the clock tolerance should be ±50 ppm.

REGISTER CONFIGURATION

Regardless of the operating mode and the type of device connected, it is necessary to write at least one register in the switch to set up the interface. This can be done via the SPI or I^{2}C interface, or by the in-band access (IBA) method. In addition to initial register configuration, true SGMII multi-speed support requires ongoing management of the SGMII port by a management processor as in **Section "10/100/1000 Cat5 PHY or Module (SGMII Mode)"**.

The SGMII port is configured through the SGMII registers as described in each data sheet. These are indirect registers that are accessed via registers 0x7200-0x7203 and 0x7206-0x7207. (These registers are documented in the data sheet as 0xN200-0xN203 and 0xN206-0xN207.) The SGMII registers have 21-bit addresses in the ranges 0x1F0000 – 0x1F0006 and 0x1F8000 – 0x1F8002.

Example Write: How to Write Data 0x1234 to SGMII Register 0x1F0004

Reg 0x7200 = 0x001F0004

Reg 0x7206 = 0x1234

Example Read: How to Read SGMII Register 0x1F0001

Reg 0x7200 = 0x001F0001

Read register 0x7206

SGMII Errata

There are currently two known operational SGMII errata for these switches, and the workarounds are incorporated into the register details provided in **Section "Register Settings for Each Configuration"**. Please read the device errata document, as found on the Microchip web site for each device, and verify that no additional SGMII errata have been added since the publication of this document. These operational errata are described in the following subsections.

SGMII AUTO-NEGOTIATION DOES NOT SET BIT 0 IN AUTO-NEGOTIATION CODE WORD

The workaround requires writing to SGMII register 0x1F0004. This is incorporated into the details in **Section "Register Settings for Each Configuration"**.

SGMII PORT LINK DETAILS FROM THE CONNECTED SGMII PHY ARE NOT PASSED PROPERLY TO PORT 7 GMAC

For full SGMII multi-speed support, the management processor must read the status information from SGMII register 0x1F8002, and then write the appropriate data to register 0x1F0000. Details are given in **Section "Register Settings for Each Configuration"**.

Register Settings for Each Configuration

SWITCH-TO-SWITCH (SGMII MODE)

When connecting two of these switches together, two configuration alternatives are available. Implement only one alternative but not both: (a) set both switches identically to disable auto-negotiation, or (b) leave one switch in default mode (MAC-side mode) and set the other switch to PHY-side mode.

Alternative A

> Disable auto-negotiation (same configuration for both switches).
>
> SGMII reg 0x1F0000 = 0x0140 // 1000 Mbps, full duplex, disable auto-negotiation

Alternative B

> PHY-side auto negotiation (Only configure one of the two switches this way. Leave the other switch with default register settings. The errata workaround of writing to SGMII register 0x1F0004 is not necessary for the second switch.)
>
> SGMII reg 0x1F8001 = 0x001C // set SGMII PHY-side mode
>
> SGMII reg 0x1F0004 = 0x0020 // errata workaround; other values will also work
>
> SGMII reg 0x1F0000 = 0x1340 // restart auto-negotiation

10/100/1000 CAT5 PHY OR MODULE (SGMII MODE)

One time setting:

> SGMII reg 0x1F8001 = 0x0005 // (optional) enable Auto-negotiation Complete interrupt
>
> SGMII reg 0x1F0004 = 0x0020 // errata workaround; other values will also work

Erratum workaround:

The Cat5 link details are received at the switch via SGMII, but because of an erratum, one logic block does not receive these details. The switch port defaults to 1000 Mbps and full duplex, so if it is known that the Cat5 link is 1000BASE-T and full duplex, then the following erratum workaround is not required. But if it is possible to have 10BASE-T or 100BASE-TX link, or the link can be half duplex, then it is necessary to implement this workaround.

The software must read the auto-negotiation (AN) results in register 0x1F8002 and convey the link speed and duplex information by writing to register 0x1F0000. The management processor is required to do this every time an auto-negotiation exchange occurs across the SGMII interface. (An auto-negotiation exchange occurs whenever the Cat5 link goes up or down.) The processor can detect an auto-negotiation exchange by monitoring the Auto-negotiation Complete Interrupt bit (bit 0) in register 0x1F8002 (and clearing it once it is set), or by setting up Auto-negotiation Complete to drive the INTRP_N pin as described in **Section "Auto-negotiation Complete Interrupt"**.

> If 0x1F8002 = 0x001B, then write 0x1F0000 = 0x1140 // 1000 Mbps, full duplex
>
> If 0x1F8002 = 0x0017, then write 0x1F0000 = 0x3100 // 100 Mbps, full duplex
>
> If 0x1F8002 = 0x0013, then write 0x1F0000 = 0x1100 // 10 Mbps, full duplex

If 0x1F8002 = 0x0015, then write 0x1F0000 = 0x3000 // 100 Mbps, half duplex

If 0x1F8002 = 0x0011, then write 0x1F0000 = 0x1000 // 10 Mbps, half duplex

100BASE-FX MODULE (SGMII MODE)

Follow the steps in **Section "10/100/1000 Cat5 PHY or Module (SGMII Mode)"**, or follow this shortcut:

One time setting:

SGMII reg 0x1F0004 = 0x0020 // errata workaround; other values will also work

SGMII reg 0x1F0000 = 0x3100 // 100 Mbps, full duplex

(NON-SGMII) 1000BASE-T CAT5 PHY OR MODULE (SERDES MODE)

One time setting:

SGMII reg 0x1F8001 = 0x0019 // set SerDes mode

SGMII reg 0x1F0004 = 0x01A0 // errata workaround; other values will also work

SGMII reg 0x1F0000 = 0x1340 // restart auto-negotiation

1000BASE-X FIBER (SERDES MODE)

One time setting:

SGMII reg 0x1F8001 = 0x0019 // set SerDes mode

SGMII reg 0x1F0004 = 0x01A0 // auto-negotiation parameters; value may be modified

SGMII reg 0x1F0000 = 0x1340 // restart auto-negotiation

SUPPORTING MULTIPLE TYPES OF SFP MODULES

Section "Register Configuration" gives details for interfacing a specific PHY or module type. The switch does not have an auto-detect feature to detect what type of SFP module is connected. Users should be instructed about which specific module types will work in a given system design. If it is not possible to restrict the type of SFP module installed, or if maximum flexibility is desired, it is possible through software to make the switch adaptable to any of the SFP module types by following these steps:

1. Implement the errata workaround: write data 0x01A0 to register 0x1F0004.
2. Poll register 0x1F0006 until the Auto-negotiation Word Received bit (bit 0) is set. (If desired, use the Auto-negotiation Complete interrupt.) Note that SGMII applications will complete auto-negotiation when the local SGMII device (PHY or module) is present, but SerDes mode applications (fiber and Cat5) will not complete auto-negotiation until there is a link by cable to the far-end device.
3. Read reg 0x1F0005 and check bits 5-8.

   a. If any of these bits is set, the connected module is a SerDes mode device. Continue with the setup for SerDes mode as shown in **Section "1000BASE-X Fiber (SerDes Mode)"**.

   b. If none of these bits is set, the connected module is an SGMII mode device. Follow the instructions in **Section "10/100/1000 Cat5 PHY or Module (SGMII Mode)"**.

REGISTER SUMMARY

The following registers summarize the key status and control registers and bits, relating to setting up and managing data flow across this port. Control bits for functions such as reset, powerdown, and loopback modes are not included here.

TABLE 2:   STATUS BITS AND REGISTERS

Register and bit	Type	Description
0x1F0001 bit 5	RO	Auto-negotiation Complete. Indicates that an auto-negotiation word is received with the ACK bit set. The status is the same as 0x1F8002 bit 0 except that it remains set until the serial link is broken.
0x1F0001 bit 4	RO	Remote Fault indication received. Applicable only to SGMII mode, indicating that remote fault indication is received from the link partner. It is set if 0x1F0004 bit 12 or bit 13 is set.
0x1F0001 bit 2	RO, LL	Device/Link Detect. This is the most basic receiver status bit. For SGMII mode, it indicates a valid signal from the attached PHY/module. For SerDes mode, it indicates a valid signal from the far-end link partner.
0x1F0005 bits [8:5]	RO	(SerDes mode) Link partner ability received: ACK, remote fault, Pause, duplex.
0x1F0006 bit 1	RO, LH	Auto-negotiation word received. Stays set until the register is read. When this bit is set, the received auto-negotiation word information is available in register 0x1F0005 (for SerDes mode) or in 0x1F8002 (for SGMII mode).
0x1F8002 bits [4:1]	RO	(SGMII mode) Cat5 link status received: Cat5 link up/down, speed, duplex.
0x1F8002 bit 0	SS, WC	Auto-negotiation Complete. This bit functions as an interrupt; once set, it remains set until 0 is written to it. The status is the same as 0x1F0001 bit 5. It indicates that an auto-negotiation word has been received with the ACK bit set.

Legend:

    RO = Read only
    LL = Latch Low, read a second time to get the current status
    LH = Latch High
    WC = Write 0 to clear
    SS = Self setting
    R/W = Read or write

TABLE 3:   CONTROL BITS AND REGISTERS

Register and bit	Description
0x1F0000 bit 12	Auto-negotiation enable
0x1F0000 bit 9	Restart auto-negotiation. Set this bit after changing any auto-negotiation parameters in register 0x1F0004 or 0x1F8001. It is self-clearing.
0x1F0000 bits 6, 13, 8	Speed and duplex. These bits determine the speed and duplex settings from the perspective of the switch. They must be set to match the speed and duplex of the connected device. The default is 1 Gbps and full duplex. When in SGMII mode, copy the auto-negotiation results from register 0x1F8002 to these bits. For SerDes mode, do not change these bits.
0x1F0004	For both SerDes and SGMII modes, these are the link parameter advertisement values. Except for Pause ability, there is rarely a need to change these values. Note that the Pause and Remote Fault bits are used only for 1000BASE-X (SerDes mode).
0x1F8001	After making any changes to this register, write to register 0x1F0004 in order for the changes to take effect.
0x1F8001 bit 4	SGMII Link Status control. Set to 1 when in SGMII PHY-side mode. For SerDes mode, always set this bit.
0x1F8001 bit 3	SGMII PHY-side mode or MAC-side mode. When connecting two switches together and enabling auto-negotiation, set one of the switches to PHY-side mode and set the SGMII Link control bit in bit 4. Otherwise, leave in default MAC-side mode. For SerDes mode, always set this bit.
0x1F8001 bits 2, 1	SGMII or SerDes mode select. Set to 10 (default) for SGMII mode. Set to 00 for SerDes mode. For SerDes mode, also set bits 3 and 4.
0x1F8001 bit 0	Enable for Auto-negotiation Complete interrupt. Set this bit as one step in enabling Auto-negotiation Complete to drive the INTRP_N pin of the chip. If only using the Auto-negotiation Complete interrupt bit in register 0x1F8002, it is not necessary to set this bit.

AUTO-NEGOTIATION COMPLETE INTERRUPT

The switch can generate an interrupt on the INTRP_N pin in response to Auto-negotiation Complete on the SGMII or SerDes interface. This pin can be connected to a management processor to notify it that a new auto-negotiation has taken place. This feature must be enabled both in the SGMII registers and in the main register space. This feature is not needed when the SGMII or SerDes port of the switch is connected to a fixed PHY or to a specific type of interface module, but it can be useful for applications implementing an auto-detect feature in the software for different types of interface modules. The alternative to using the interrupt is to poll the auto-negotiation complete bit in register 0x1F0001.

Follow these steps to enable the interrupt:

1. Set bit 0 in SGMII register 0x1F8001.
2. Set bit 3 in main register 0x701F.
3. Set bit 6 in main register 0x001C-001F.

   Note: The Auto-negotiation Complete Interrupt bit in register 0x1F8002 is always functional and is not affected by the enable bit in register 0x1F8001.

AUTO-NEGOTIATION EXPLAINED

The term "auto-negotiation" has different meanings depending on the context. In copper Ethernet applications (10BASE-T, 100BASE-TX, and 1000BASE-T), each link partner uses fast link pulses (FLP) to transmit ("advertise") its link capabilities (speed and duplex), and then each one sets its modes to match the best mode supported by both devices. Flow control (Pause) and other parameters can also be included.

1000BASE-X (SerDes mode) uses special in-band codes to do auto-negotiation. Auto-negotiation variables include duplex and Pause, but not speed which is fixed at 1 Gbps. Since fiber links almost always use full duplex and Pause is often neglected, the default settings are almost always used. In this event, the main purpose of "auto-negotiation" is to confirm that the link is up. This is done by each device automatically setting the ACK bit in the transmitted auto-negotiation word in response to receiving a valid auto-negotiation word.

SGMII is based on 1000BASE-X, but it uses different bits in the auto-negotiation word and re-assigns two bits to different functions. With 1000BASE-X, the two link partners are equal peers, so the auto-negotiation process is completely symmetric. In comparison, SGMII is the interface between a MAC and a PHY, so it is inherently asymmetric. Specifically, the SGMII PHY uses the auto-negotiation word to inform the MAC about the details of the Cat5 link: link up/down, speed, and duplex. This is a one-way communication of information. The auto-negotiation word that is sent by the MAC does not contain any "auto-negotiation" information; its only purpose is to verify that the MAC and PHY are communicating. It is essential that one SGMII auto-negotiation partner be a PHY (or in PHY-side mode) while the other partner is a MAC (or in MAC-side mode).

In a 1000BASE-X application, the fiber transceiver is not involved in the auto-negotiation. The auto-negotiation is between the two silicon devices (for example, the KSZ9897S switch) at either end of the fiber cable. There is no separate communication between the switch and the fiber transceiver, and the switch cannot detect the fiber transceiver. Only when the complete end-to-end fiber link is established can the switch complete auto-negotiation to verify that a link partner is present. The SerDes/1000BASE-X auto-negotiation results can be found in SGMII register 0x1F0005. 1000BASE-X auto-negotiation is defined in IEEE802.3 clause 37.

With an SGMII 10/100/1000BASE-T PHY or module, the SGMII auto-negotiation occurs only locally between the PHY and MAC devices. The auto-negotiation across the Cat5 copper cable between the two PHYs is separate from the SGMII auto-negotiation. Even when the Cat5 link is down, the PHY and MAC can still complete auto-negotiation, although the MAC device may block egress traffic until it has learned from the PHY that the Cat5 link is up. Any time there is a Cat5 link up or link down event, the PHY will restart auto-negotiation to inform the MAC about the updated link information. The SGMII auto-negotiation results can be found in SGMII register 0x1F8002. The SGMII auto-negotiation bits are defined in the SGMII specification.

Initially, each device repeatedly transmits an auto-negotiation word with the ACK bit cleared. Once it receives an auto-negotiation word, it transmits with the ACK bit set. At this point, auto-negotiation is complete and it stops sending auto-negotiation words and can start normal operation sending and receiving data traffic. Auto-negotiation is restarted if the link goes down.

There are three status bits in the SGMII registers for determining auto-negotiation status:

• Register 0x1F0006 bit 1 indicates when an auto-negotiation word has been received, with or without the ACK bit set. Once this bit is set, registers 0x1F0005 and 0x1F8002 can be read to determine which bits were set in the received word. This bit is "latch high," so it does not clear until it is read.

• Register 0x1F0001 bit 5 indicates when auto-negotiation is complete, which means that an auto-negotiation word is received with the ACK bit set.

• Register 0x1F8002 bit 0 is the "interrupt" version of the auto-negotiation complete status bit, meaning that when set, it stays high until 0 is written to it.

Auto-negotiation can be disabled. If it is enabled on one device, it must also be disabled on the other device, and the two devices must be set to the same speed and duplex settings.

APPENDIX A: DEFINITION OF COMMON TERMS

TABLE A-1: COMMON TERMS

Term	Definition
1000BASE-X	Includes 1000BASE-SX, 1000BASE-LX
1000BASE-T	Gigabit Ethernet on unshielded twisted pair cable. Auto-negotiation (802.3 clause 28 and 40) with 100BASE-TX and 10BASE-T is possible.
100BASE-TX	100 Mbps Ethernet on unshielded twisted pair cable. Auto-negotiation (802.3 clause 28 and 40) with 1000BASE-T and 10BASE-T is possible.
10BASE-T	10 Mbps Ethernet on unshielded twisted pair cable. Auto-negotiation (802.3 clause 28 & 40) with 1000BASE-T and 100BASE-TX is possible.
10/100/1000BASE-T PHY Also 10/100/1000BASE-TX Also 10/100/1000	A triple-mode Cat5 media Ethernet PHY that can auto-negotiate to operate at any of 10BASE-T, 100BASE-TX, and 1000BASE-T.
802.3z	1000BASE-X specification. Now 802.3 clauses 36, 37, and 38
Auto-negotiation	An information exchange between two nodes. At a minimum, it is used to mutually verify the communication channel. It can also be used for negotiating the channel's speed, duplex, and so on.
Clause 28 auto-negotiation	Auto-negotiation for Cat5 media 10/100/1000BASE-T
Clause 37 auto-negotiation	Auto-negotiation for 1000BASE-X (excluding 1000BASE-KX). SGMII is often said to use Clause 37 auto-negotiation although there are differences in the details of how it is used in SGMII.
MAC	Media access control. This block connects on one side to the PHY and on the other side to the switching block of the switch. If the PHY and MAC are in separate chips, they connect via SGMII, GMII, RGMII, RMII, MII, and so on. This is ISO layer 2.
MSA	Multi-source agreement (defines SFP)
PHY	The physical interface block. It connects on one side to the physical media, and on the other side to the MAC. If the PHY and MAC are in separate chips, they connect via SGMII, GMII, RGMII, RMII, MII, and so on. This is ISO layer 1.
SerDes	Serializer-deserializer. Although this is often a generic term, it is commonly used here to refer to the serial PHY-to-MAC interface that does not support the SGMII protocol.
Serial interface	Serializer-deserializer. A generic term for the physical interface without referring specifically to 1000BASE-X or SGMII.
SFP	Small form-factor pluggable. A standardized footprint for interface modules. Modules can be optical or copper, at various speeds. Mechanical, pinout, and basic pin functionality are defined, but not cable side interface or data rate.
SGMII	Serial Gigabit media independent interface. On an Ethernet port, SGMII interfaces between the MAC and the PHY, takes GMII signals and serializes them, then deserializes them at the receive side. Reference the SGMII specification.
Switch	Refers to the Microchip KSZ9897S, KSZ9567S, KSZ9477S, KSZ8567S

APPENDIX B: REVISION HISTORY

TABLE B-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00002647B (08-22-18)	Register Settings for Each Configuration on page 7	Changed the instances of "0x1F80002" to "0x1F8002" under the Erratum workaround section.
DS00002647A (02-12-18)	Initial release	

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