IEEE 802.11 b/g/n Link Controller Module

ATWILC1000-MR110xB

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Introduction

The ATWILC1000-MR110xB module is a low-power consumption IEEE 802.11 b/g/n IoT (Internet of Things) module, which is specifically optimized for low-power IoT applications. The ATWILC1000-MR110xB modules feature small form factor (21.7 mm x 14.7 mm x 2.1 mm) while fully integrating Power Amplifier (PA), Low Noise Amplifier (LNA), Transmit/Receive (T/R), switch and power management. The ATWILC1000-MR110PB includes a PCB antenna, whereas the ATWILC1000-MR110UB module includes a U.FL connector to use with an external antenna. With advanced security, it is interoperable with various vendors using IEEE 802.11b/g/n Access Points in wireless LAN. The module provides Serial Peripheral Interface (SPI) and Secure Digital Input Output (SDIO) to interface with the host controller.

Notes: All references to the ATWILC1000-MR110xB module include all the modules listed below unless otherwise noted:

- ATWILC1000-MR110PB
- ATWILC1000-MR110UB

Features

- IEEE 802.11 b/g/n, Single Stream (1x1) 20 MHz Bandwidth WLAN Link
  - Compatible with Wi-Fi® 6/7 2.4 GHz band
- Supports Single Spatial Stream in 2.4 GHz ISM Band
- Integrated Power Amplifier (PA) and Transmit/Receive (T/R) Switch
- Superior Sensitivity and Range through Advanced PHY Signal Processing
- Advanced Equalization and Channel Estimation
- Advanced Carrier and Timing Synchronization
- Supports Soft-AP
- Supports IEEE 802.11 WEP, WPA, WPA2 and WPA2-Enterprise Security
- Superior Medium Access Control (MAC) Throughput Through Hardware Accelerated Aggregate A-MPDUs/A-MDSU Frame Reception and Block Acknowledgment
- On-Chip Memory Management Engine to Reduce the Host Load
- SPI and SDIO Host Interfaces
- Operating Temperature Ranges from -40°C to +85°C
- Input/Output Operating Voltage (VDDIO) of 1.62V to 3.6V
- Power supply for DC/DC Convertor (VBAT) has a Range of 3.0V to 4.2V
- Built-In 26 MHz Crystal
- Power-Save Modes:
  - <1 µA Power-down mode typical at 3.3V I/O
  - 380 µA Doze mode with chip settings preserved (used for beacon monitoring)

  - On-chip low-power sleep oscillator
  - Fast host wake-up from Doze mode by a pin or the host I/O transaction
- Wi-Fi Alliance® Certified for Connectivity and Optimizations
  - ID: WFA65340

Table of Contents

1. Ordering Information and Module Marking

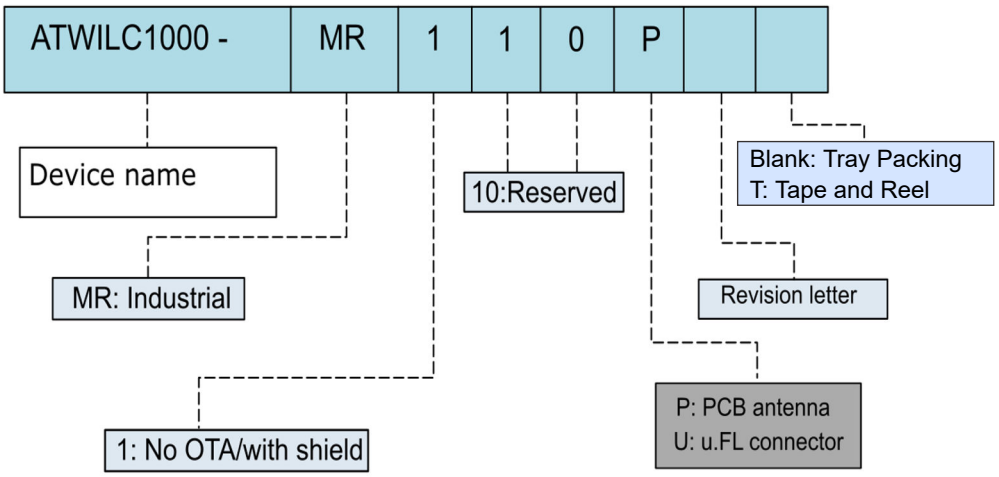
The following table provides the ordering information of the ATWILC1000-MR110xB module.

Table 1-1. Ordering Information

Model Number	Ordering Code	Package	No. of Pins	Description	Regulatory Certification
ATWILC1000-MR110PB	ATWILC1000-MR110PB	21.7x14.7x2.1 mm	28	Certified module with ATWILC1000B-MU chip and PCB antenna	FCC, ISED, CE, MIC, KCC, NCC, SRRC
ATWILC1000-MR110UB	ATWILC1000-MR110UB	21.7x14.7x2.1 mm	28	Certified module with ATWILC1000B-MU chip and uFL connector	FCC, ISED, CE

The following figure provides the marking information of the ATWILC1000-MR110xB module.

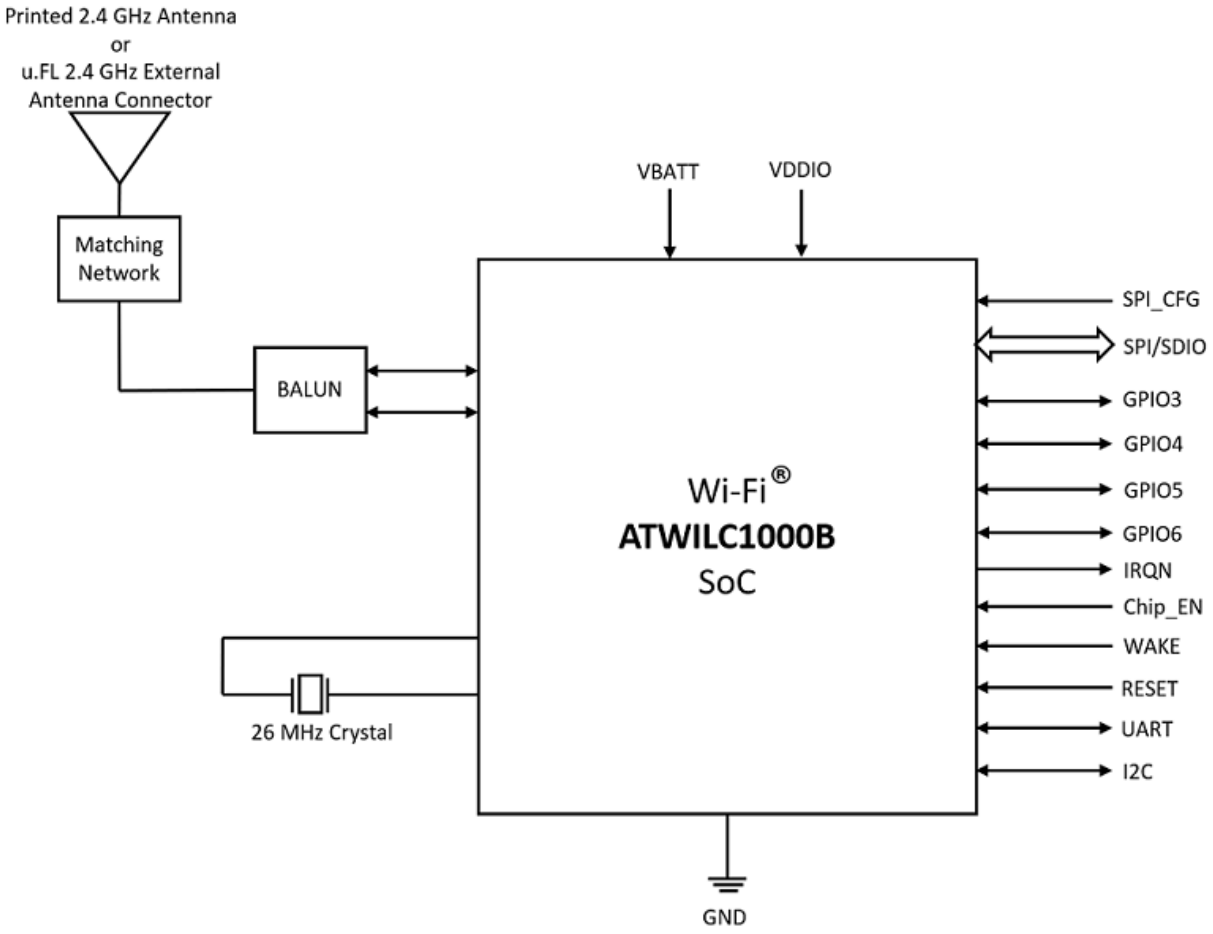
Figure 1-1. Marking Information



2. Functional Overview

The ATWILC1000-MR110xB module block diagram is shown in the following figure.

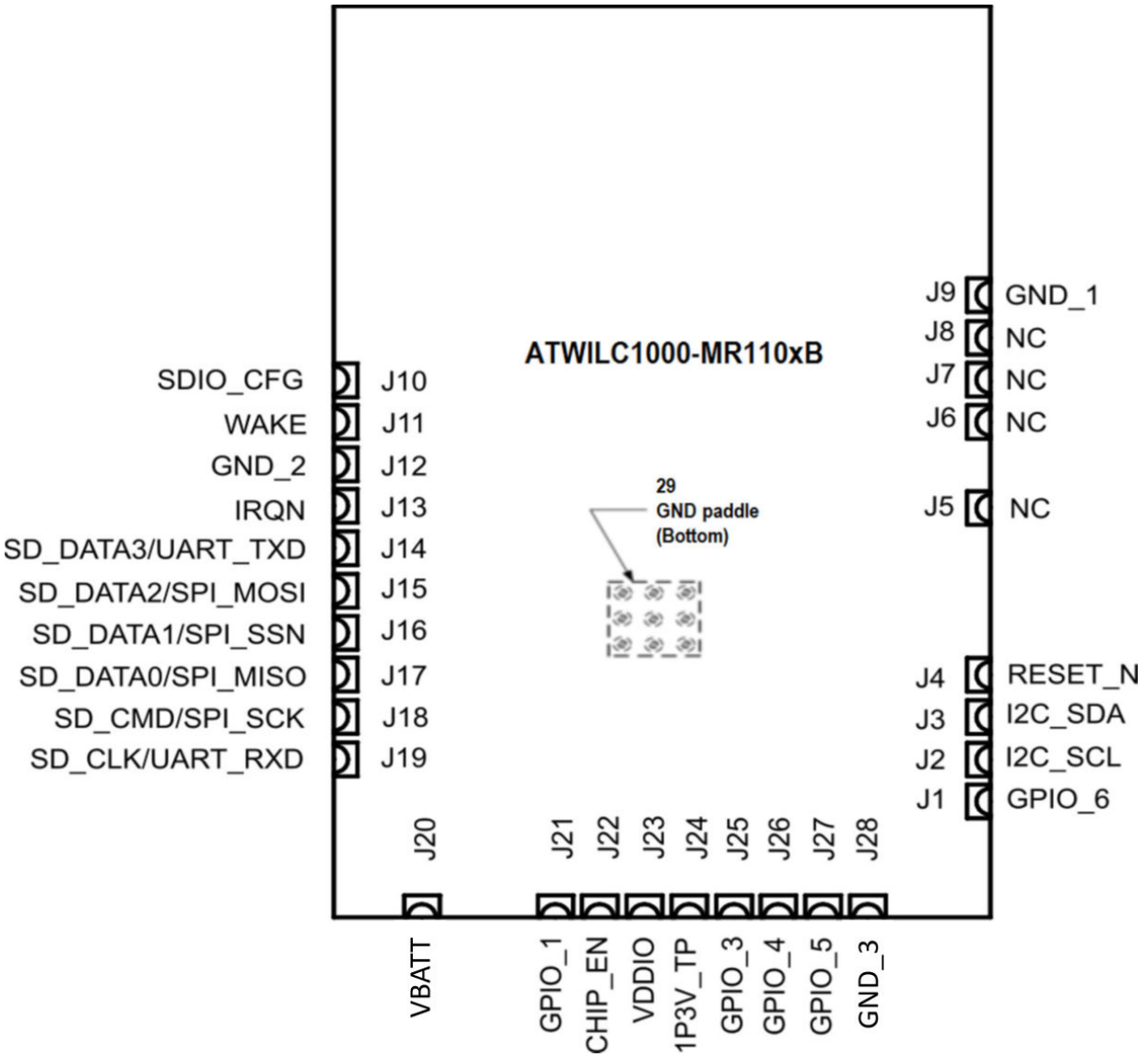
Figure 2-1. ATWILC1000-MR110xB Module Block Diagram



3. Pinout and Package Information

The ATWILC1000-MR110xB package has an exposed paddle that must be connected to the system board ground. The module pin assignment is shown in the following figure.

Figure 3-1. Pin Assignment



Note: This pin assignment is applicable for both the ATWILC1000-MR110PB and ATWILC1000-MR110UB modules.

The following table shows the pin description of this module.

Table 3-1. Pin Details

Pin No.	Name	Type	Description	Programmable Pull-Up Resistor
1	GPIO_6[1]	I/O	General purpose I/O.	—

Table 3-1. Pin Details (continued)

Pin No.	Name	Type	Description	Programmable Pull-Up Resistor
2	I^2C_SCL	I/O	I^2C client clock. Used only for development debugging purposes. It is recommended to add a test point for this pin.	—
3	I^2C_SDA	I/O	I^2C client data. Used only for development debugging purposes. It is recommended to add a test point for this pin.	Yes
4	RESET_N	I	Active-low hard reset. When this pin is asserted low, the module is placed in the Reset state. When this pin is asserted high, the module is out of reset and functions normally. Connect to a host output that defaults low at power-up. If the host output is tri-stated, add a 1 MΩ pull-down resistor to ensure a low level at power-up.	Yes
5	NC	—	No connection.	—
6	NC	—	No connection.	—
7	NC	—	No connection.	—
8	NC	—	No connection.	—
9	GND_1	Ground	Ground.	—
10	SDIO_SPI_CFG	I	Connect to VDDIO through a 1 MΩ resistor to enable the SPI interface. Connect to the ground to enable the SDIO interface.	No
11	WAKE	I	Host wake control. Can be used to wake up the module from Doze mode. Current FW implementation makes use of the IRQ/SDIO interface to wake up the host.	Yes
12	GND_2	Ground	—	—
13	IRQN	O	The ATWILC1000-MR110xB device interrupt output. Connect to a host interrupt pin.	Yes
14	SD_DAT3	SDIO = I/O UART = O	SDIO Data Line 3 from the ATWILC1000-MR110xB when the module is configured for SDIO.	Yes
15	SD_DAT2/SPI_RXD	SDIO = I/O SPI = I	SDIO Data Line 2 signal from ATWILC1000-MR110xB when the module is configured for SDIO. SPI MOSI (Host Out Client In) pin when the module is configured for SPI.	Yes
16	SD_DAT1/SPI_SSN	SDIO = I/O SPI = I	SDIO Data Line 1 from ATWILC1000-MR110xB when the module is configured for SDIO. Active low SPI client select from the ATWILC1000 when the module is configured for SPI.	Yes
17	SD_DAT0/SPI_TXD	SDIO = I/O SPI = O	SDIO Data Line 0 from the ATWILC1000-MR110xB when the module is configured for SDIO. SPI MISO (Host In Client Out) pin from ATWILC1000 when the module is configured for SPI.	Yes
18	SD_CMD/SPI_CLK	SDIO = I/O SPI = I	SDIO CMD line from ATWILC1000-MR110xB when the module is configured for SDIO. SPI Clock from ATWILC1000 when the module is configured for SPI.	Yes
19	SD_CLK	SDIO = I UART = I	SDIO clock line for the ATWILC1000-MR110xB when the module is configured for SDIO.	Yes
20	VBATT	Power supply	Power supply pin for the DC/DC convertor.	Yes
21	GPIO_1[1]	I/O	General purpose I/O.	Yes

Table 3-1. Pin Details (continued)

Pin No.	Name	Type	Description	Programmable Pull-Up Resistor
22	CHIP_EN	I	Module enable. High level enables the module, low level places the module in Power-Down mode. Connect to a host Output that defaults low at power-up. If the host output is tri-stated, add a 1 MΩ pull-down resistor if necessary to ensure a low level at power-up.	No
23	VDDIO	Power supply	I/O power supply. Must match host I/O voltage.	—
24	1P3V_TP	—	1.3V VDD Core Test Point. Decouple with 10 uF and 0.01 uF to the GND close to pin 24.	—
25	GPIO_3[1]	I/O	General purpose I/O. By default, UART receives input from the ATWILC1000-MR110xB. Used only for development debugging purposes. It is recommended to add a test point for this pin.	Yes
26	GPIO_4[1]	I/O	General purpose I/O.	Yes
27	GPIO_5[1]	I/O	General purpose I/O. By default, UART transmits output to the ATWILC1000-MR110xB. Used only for development debugging purposes. It is recommended to add a test point for this pin.	Yes
28	GND_3	Ground	—	—
29	Paddle	Ground	Exposed paddle GND. This pad must be soldered to the system ground.	—

Note:

1. Use of the GPIO functionality is not supported by the WILC1000 FW. The data sheet will be updated once the support for this feature is added.

The following table provides the ATWILC1000-MR110xB module package dimensions.

Table 3-2. ATWILC1000-MR110xB Module Package Information

Parameter	Value	Units
Package Size	21.7 x 14.7 x 2.1	mm
Pad Count	28	—
Total Thickness	2.11	mm
Pad Pitch	1.016	
Pad Width	0.82	
Exposed Pad size	3.7 x 3.7	

4. Electrical Specifications

4.1 Absolute Ratings

The absolute maximum ratings for this module are listed in the following table.

Table 4-1. ATWILC1000-MR110xB Module Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBATT	Input supply voltage	-0.3	5.0	V
VDDIO	I/O voltage	-0.3	5.0	V

CAUTION

InfoStresses beyond those listed under "Absolute Maximum Ratings" cause permanent damage to the device. This is a stress rating only. The functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to the maximum rating conditions for extended periods affects the device's reliability.

4.2 Recommended Operating Conditions

The recommended operating conditions for this module are listed in the following table.

Table 4-2. ATWILC1000-MR110xB Module Recommended Operating Conditions

Characteristics	Symbol	Min.	Typ.	Max.	Unit
I/O Supply Voltage Low Range	$VDDIO_L$	1.62	1.80	2.00	V
I/O Supply Voltage Mid Range	$VDDIO_M$	2.00	2.50	3.00	V
I/O Supply Voltage High Range	$VDDIO_H$	3.00	3.30	3.60	V
Battery voltage	VBATT	3.00	3.30	4.20	V
Operating temperature	—	-40	—	+85	°C

Notes:

1. VBATT must be equal to or greater than VDDIO.
2. The voltage of VDDIO is dependent on the system I/O voltage.
3. Test Conditions: -40°C to +85°C

4.3 DC Electrical Characteristics

The following table provides the DC characteristics for the ATWILC1000-MR110xB digital pads.

Table 4-3. DC Electrical Characteristics

VDDIO Condition	Characteristic	Min.	Typ.	Max.	Unit
$VDDIO_L$	Input Low Voltage (V_{IL})	-0.30	—	0.60	V
	Input High Voltage (V_{IH})	VDDIO-0.60	—	VDDIO + 0.30	
	Output Low Voltage (V_{OL})	—	—	0.45	
	Output High Voltage (OV_{OH})	VDDIO-0.50	—	—	
$VDDIO_M$	Input Low Voltage (V_{IL})	-0.30	—	0.63	
	Input High Voltage (V_{IH})	VDDIO-0.60	—	VDDIO + 0.30	
	Output Low Voltage (V_{OL})	—	—	0.45	
	Output High Voltage (OV_{OH})	VDDIO-0.50	—	—	
$VDDIO_H$	Input Low Voltage (V_{IL})	-0.30	—	0.65	
	Input High Voltage (V_{IH})	VDDIO-0.60	—	VDDIO + 0.30 (up to 3.60)	
	Output Low Voltage (V_{OL})	—	—	0.45	
	Output High Voltage (OV_{OH})	VDDIO-0.50	—	—	
All	Output Loading	—	—	20	pF
All	Digital Input Load	—	—	6	
$VDDIO_L$	Pad Drive Strength (regular pads[1])	1.7	2.4	—	mA
$VDDIO_M$	Pad Drive Strength (regular pads[1])	3.4	6.5	—	
$VDDIO_H$	Pad Drive Strength (regular pads[1])	10.6	13.5	—	
$VDDIO_L$	Pad Drive Strength (high-drive pads[1])	3.4	4.8	—	
$VDDIO_M$	Pad Drive Strength (high-drive pads[1])	6.8	13	—	
$VDDIO_H$	Pad Drive Strength (high-drive pads[1])	21.2	27	—	

Note:

1. The following are high-drive pads: I2C_SCL, I2C_SDA; all other pads are regular.

4.4 Receiver Performance

The following are the typical conditions for radio receiver performance:

VBATT at 3.3V, VDDIO at 3.3V, temperature at 25°C and WLAN Channel 6 (2437 MHz).

The following table provides the receiver performance characteristics for the module.

Table 4-4. Receiver Performance

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	—	2,412	—	2,484	MHz

Table 4-4. Receiver Performance (continued)

Parameter	Description	Min.	Typ.	Max.	Unit
Sensitivity 802.11b	1 Mbps DSSS	—	-94	—	dBm
	2 Mbps DSSS	—	-91	—	
	5.5 Mbps DSSS	—	-89	—	
	11 Mbps DSSS	—	-86	—	
Sensitivity 802.11g	6 Mbps OFDM	—	-88	—	dBm
	9 Mbps OFDM	—	-87	—	
	12 Mbps OFDM	—	-86	—	
	18 Mbps OFDM	—	-84	—	
	24 Mbps OFDM	—	-82	—	
	36 Mbps OFDM	—	-78	—	
	48 Mbps OFDM	—	-74	—	
	54 Mbps OFDM	—	-73	—	
Sensitivity 802.11n (BW at 20 MHz)	MCS 0	—	-87	—	dBm
	MCS 1	—	-85	—	
	MCS 2	—	-83	—	
	MCS 3	—	-80	—	
	MCS 4	—	-76	—	
	MCS 5	—	-73	—	
	MCS 6	—	-71	—	
	MCS 7	—	-69	—	
Maximum Receive Signal Level	1-11 Mbps DSSS	—	0	—	dBm
	6-54 Mbps OFDM	—	-5	—	
	MCS 0 – 7	—	-5	—	
Adjacent Channel Rejection	1 Mbps DSSS (30 MHz offset)	—	50	—	dB
	11 Mbps DSSS (25 MHz offset)	—	43	—	
	6 Mbps OFDM (25 MHz offset)	—	40	—	
	54 Mbps OFDM (25 MHz offset)	—	25	—	
	MCS 0 – 20 MHz BW (25 MHz offset)	—	40	—	
	MCS 7 – 20 MHz BW (25 MHz offset)	—	20	—	
Cellular Blocker Immunity	776-794 MHz CDMA	—	-14	—	dBm
	824-849 MHz GSM	—	-10	—	
	880-915 MHz GSM	—	-10	—	
	1710-1785 MHz GSM	—	-15	—	
	1850-1910 MHz GSM	—	-15	—	
	1850-1910 MHz WCDMA	—	-24	—	
	1920-1980 MHz WCDMA	—	-24	—	

4.5 Transmitter Performance

The following are the typical conditions for radio transmitter performance:

VBATT at 3.3V, VDDIO at 3.3V, temperature at 25°C and WLAN Channel 6 (2437 MHz).

The following table provides the transmitter performance characteristics for the module.

Table 4-5. Transmitter Performance*(3, 5, 6, 7)*

Parameter	Description	Unit	Minimum	Typical	Maximum
Frequency	—	MHz	2,412	—	2,484

Table 4-5. Transmitter Performance[3, 5, 6, 7] (continued)

Parameter	Description	Unit	Minimum	Typical	Maximum
Output Power[1, 2], ON_Transmit	802.11b 1 Mbps	dBm	—	13.6	—
	802.11b 11 Mbps	dBm	—	15.3	—
	802.11g 6 Mbps	dBm	—	18.9	—
	802.11g 54 Mbps	dBm	—	14.3	—
	802.11n MCS 0	dBm	—	18.9	—
	802.11n MCS 7	dBm	—	12.2	—
TX Power Accuracy	—	dB	—	±1.5[2]	—
Carrier Suppression	802.11b mode	dBc	—	-19.4	—
	802.11g mode	dBc	—	-27.5	—
	802.11n mode	dBc	—	-21.1	—
Out of Band Transmit Power	76-108	dBm/Hz	—	-125	—
	776-794	dBm/Hz	—	-125	—
	869-960	dBm/Hz	—	-125	—
	925-960	dBm/Hz	—	-125	—
	1570-1580	dBm/Hz	—	-125	—
	1805-1880	dBm/Hz	—	-125	—
	1930-1990	dBm/Hz	—	-125	—
	2110-2170	dBm/Hz	—	-125	—
Harmonic Output Power[4]	2nd	dBm/MHz	—	-28	—
	3rd	dBm/MHz	—	-33	—
	4th	dBm/MHz	—	-40	—
	5th	dBm/MHz	—	-28	—

Notes:

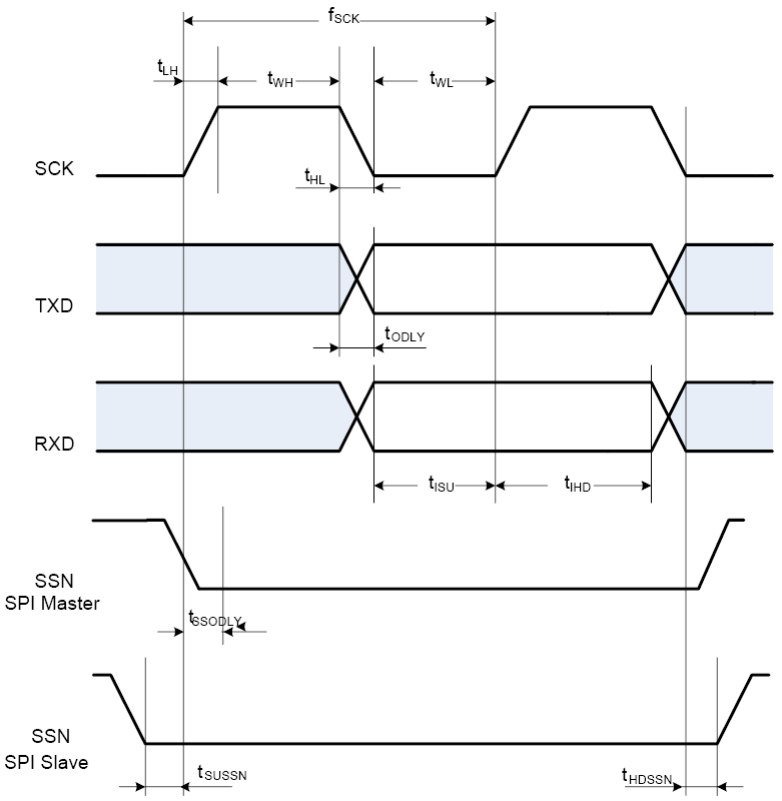
1. Measured at 802.11 spec compliant EVM/Spectral Mask.
2. Measured at RF balun output.
3. Operating temperature range is -40°C to +85°C. RF performance is assured at room temperature of 25°C with a 2-3 dB change at boundary conditions.
4. Measured at 11 Mbps, DG (Digital Gain) = -7, WLAN Channel 6 (2437 MHz).
5. With respect to TX power, different (higher/lower) RF output power settings may be used for specific antennas and/or enclosures, in which case recertification may be required.
6. The availability of some specific channels and/or operational frequency bands are country dependent and must be programmed at the host product factory to match the intended destination. Regulatory bodies prohibit exposing the settings to the end user. This requirement needs to be taken care of via host implementation.
7. The RF parameters for the ATWILC1000-MR110UB will be approximately 1 dB less than the values in the table. This insertion loss accounts for PCB trace losses and the filter network loss to the U.FL connector.

4.6 Timing Characteristics

4.6.1 SPI Timing

The SPI timing is shown in the following figure.

Figure 4-1. SPI Timing Diagram (SPI MODE CPOL = 0, CPHA = 0)



The SPI client timing parameters are provided in the following table.

Table 4-6. SPI Client Timing Parameters*(1)*

Parameter	Symbol	Min.	Max.	Units
Clock Input Frequency(2)	f_{SCK}	—	48	MHz
Clock Low Pulse Width	t_{WL}	4	—	ns
Clock High Pulse Width	t_{WH}	5	—	
Clock Rise Time	t_{LH}	0	7	
Clock Fall Time	t_{HL}	0	7	
TXD Output Delay(3)	t_{ODLY}	4	9 from SCK fall	
RXD Input Setup Time	t_{ISU}	1	—	
RXD Input Hold Time	t_{IHD}	5	—	
SSN Input Setup Time	t_{SUSSN}	3	—	
SSN Input Hold Time	t_{HDSSN}	5.5	—	

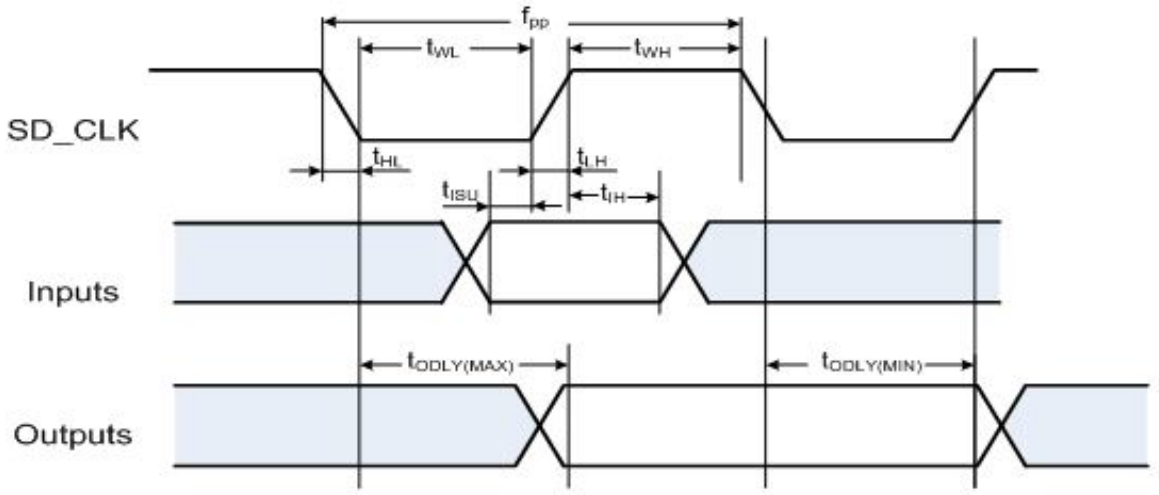
Notes:

1. Timing is applicable to all of the SPI modes.
2. Maximum clock frequency specified is limited by the SPI client interface internal design; the actual maximum clock frequency can be lower and depends on the specific PCB layout.
3. Timing is based on 15 pF output loading. Under all conditions, $t_{LH} + t_{WH} + t_{HL} + t_{WL}$ must be less than or equal to $1/ f_{SCK}$.

4.6.2 SDIO Timing

The SDIO client interface timing is shown in the following figure.

Figure 4-2. SDIO Timing Diagram



SDIO client timing parameters are provided in the following table.

Table 4-7. SDIO Timing Parameters

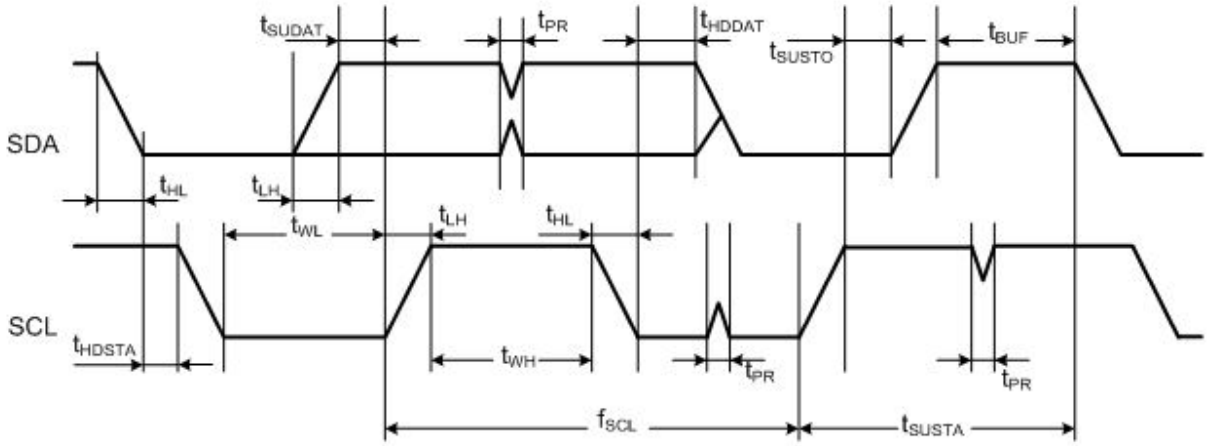
Parameter	Symbol	Min	Max	Units
Clock Input Frequency(1)	f_{PP}	0	50	MHz
Clock Low Pulse Width	t_{WL}	9	—	ns
Clock High Pulse Width	t_{WH}	4.5	—	
Clock Rise Time	t_{LH}	0	5	
Clock Fall Time	t_{HL}	0	5	
Input Setup Time	t_{ISU}	6	—	
Input Hold Time	t_{IH}	4	—	
Output Delay(2)	t_{ODLY}	3	11	

1. Maximum clock frequency specified is limited by the SDIO client interface internal design; the actual maximum clock frequency can be lower and depends on the specific PCB layout.
2. Timing is based on 15 pF output loading.

4.6.3 I^2C Timing

The following figure illustrates the I^2C client timing.

Figure 4-3. I²C Timing Diagram



The following table provides I²C client timing parameters.

Table 4-8. I²C Timing Parameters

Parameter	Symbol	Min	Max	Units	Remarks
SCL Clock Frequency	f_{SCL}	0	400	kHZ	—
SCL Low Pulse Width	t_{WL}	1.3	—	µs	—
SCL High Pulse Width	t_{WH}	0.6	—	µs	—
SCL, SDA Fall Time	t_{HL}	—	300	ns	—
SCL, SDA Rise Time	t_{LH}	—	300	ns	This is dictated by external components
START Setup Time	t_{SUSTA}	0.6	—	µs	—
START Hold Time	t_{HDSTA}	0.6	—	µs	—
SDA Setup Time	t_{SUDAT}	100	—	ns	—
SDA Hold Time	t_{HDDAT}	0	—	ns	Client and Host Default
		40	—	ns	Host Programming Option
STOP Setup Time	t_{SUSTO}	0.6	—	µs	—
Bus Free Time Between STOP and START	t_{BUF}	1.3	—	µs	—
Glitch Pulse Reject	t_{PR}	0	50	ns	—

5. Power Management

The ATWILC1000-MR110xB module has several device states:

- On states:
  - ON_Transmit – Device actively transmits an 802.11 signal. Highest output power and nominal current consumption.
  - ON_Receive – Device actively receivies an 802.11 signal. Lowest sensitivity and nominal current consumption.
  - ON_Doze – Device is powered on but it does not actively transmit or receive the data.
  - Power_Down – Device core supply is powered off.

The following pins are used to switch between the ON and Power_Down states:

- CHIP_EN – This pin (pin 22) enables or disables the DC/DC converter.
- VDDIO – I/O supply voltage from external supply.

In the ON states, VDDIO is ON and CHIP_EN is high (at VDDIO voltage level). To change from the ON states to Power_Down state, connect the RESETN and CHIP_EN pin to logic low (GND) by following the power-down sequence mentioned in **Section Power-Up/Down Sequence**. When VDDIO is off and CHIP_EN is low, the chip is powered off with no leakage (also see **Section Restrictions for Power States**).

5.1 Current Consumption in Various Device States

The following table provides this module's current consumption in various device states.

Table 5-1. Current Consumption

Device State	Code Rate	Output Power (dBm)	Current Consumption(1, 2)	
			I_{VBATT}	I_{VDDIO}
ON_Transmit	802.11b 1 Mbps	17.6	266 mA	22 mA
	802.11b 11 Mbps	18.5	239 mA	22 mA
	802.11g 6 Mbps	18.6	249 mA	22 mA
	802.11g 54 Mbps	16.9	173 mA	22 mA
	802.11n MCS 0	17.7	253 mA	22 mA
	802.11n MCS 7	14.0	164 mA	22 mA
ON_Receive	802.11b 1 Mbps	N/A	63 mA	22 mA
	802.11b 11 Mbps	N/A	63 mA	22 mA
	802.11g 6 Mbps	N/A	63 mA	22 mA
	802.11g 54 Mbps	N/A	63 mA	22 mA
	802.11n MCS 0	N/A	63 mA	22 mA
	802.11n MCS 7	N/A	63 mA	22 mA
ON_Doze	N/A	N/A	380 µA	<10 µA
Power_Down	N/A	N/A	1.25 µA(3)	

Notes:

1. The power consumption values are measured when VBAT is 3.3V and VDDIO is 3.3V at 25°C.
2. The current consumption in the Active TX state is done with a Duty cycle configuration – 5.
3. The current consumption mentioned for these states is the sum of current consumed in the VDDIO and VBATT voltage rails.

5.2 Restrictions for Power States

When no power is supplied to the device, the DC/DC converter output and VDDIO are both turned off (at ground potential). In this case, a voltage cannot be applied to the device pins because each pin contains an ESD diode from the pin to supply. This diode will turn on when voltage higher than one diode-drop is supplied to the pin.

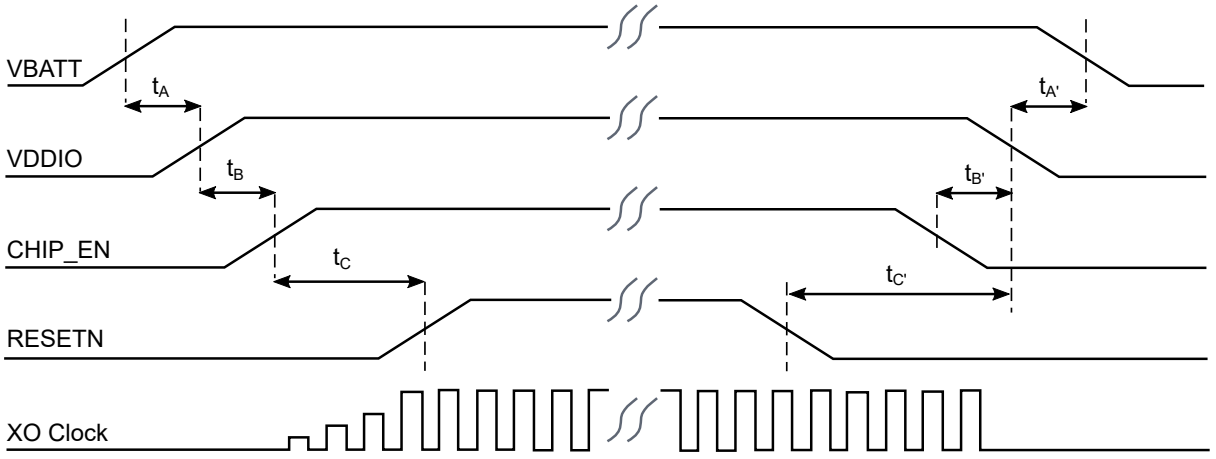
If a voltage must be applied to the signal pads while the chip is in a low power state, the VDDIO supply must be on, so the Sleep mode or power-down state must be used.

Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode-drop below ground to any pin.

5.3 Power-Up/Down Sequence

The following figure illustrates the power-up/down sequence for the ATWILC1000-MR110xB.

Figure 5-1. Power-Up/Down Sequence



The following table provides power-up/down sequence timing parameters.

Table 5-2. Power-Up/Down Sequence Timing

Parameter	Min.	Max.	Units	Description	Notes
t_A	0	—	ms	VBAT rise to VDDIO rise	VBAT and VDDIO can rise simultaneously or connected together. VDDIO must not rise before VBAT.
t_B	0	—	ms	VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low and must not be left floating.
t_C	5	—	ms	CHIP_EN rise to RESETN rise	This delay is required to stabilize the XO clock before RESETN removal. RESETN must be driven high or low and must not be left floating.
$t_{A'}$	0	—	ms	VDDIO fall to VBAT fall	VBAT and VDDIO must fall simultaneously or be connected together. VBAT must not fall before VDDIO.
$t_{B'}$	0	—	ms	CHIP_EN fall to VDDIO fall	VDDIO must not fall before CHIP_EN. CHIP_EN and RESETN must fall simultaneously.
$t_{C'}$	0	—	ms	RESETN fall to VDDIO fall	VDDIO must not fall before RESETN. RESETN and CHIP_EN fall simultaneously.

5.4 Digital I/O Pin Behavior During Power-Up Sequences

The following table represents the digital I/O pin states corresponding to the device power modes.

Table 5-3. Digital I/O Pin Behavior in Different Device States

Device State	VDDIO	CHIP_EN	RESETN	Output Driver	Input Driver	Pull-Up/Down Resistor (96 kΩ)
Power_Down: Core Supply Off	High	Low	Low	Disabled (High-Z)	Disabled	Disabled
Power-on Reset: Core Supply and Hard Reset On	High	High	Low	Disabled (High-Z)	Disabled	Enabled
Power-on Default: Core Supply On, Device Out of Reset and Not Programmed	High	High	High	Disabled (High-Z)	Enabled	Enabled
On_Doze/On_Transmit/ On_Receive: Core Supply On, Device Programmed by Firmware	High	High	High	Programmed by Firmware for Each Pin: Enabled or Disabled	Opposite of Output Driver State	Programmed by Firmware for Each Pin: Enabled or Disabled

6. CPU and Memory Subsystems

6.1 Processor

This ATWILC1000-MR110xB module has a Cortus APS3 32-bit processor. This processor performs many of the MAC functions including but not limited to association, authentication, power management, security key management and MSDU aggregation/deaggregation. In addition, the processor provides flexibility for various modes of operation, such as the STA and AP modes.

6.2 Memory Subsystem

The APS3 core uses a 128 KB instruction/boot ROM along with a 160 KB instruction RAM and a 64 KB data RAM. In addition, the device uses a 128 KB shared RAM, accessible by the processor and MAC, which allows the APS3 core to perform various data management tasks on the TX and RX data packets.

6.3 Nonvolatile Memory (eFuse)

The ATWILC1000-MR110xB modules have 768 bits of nonvolatile eFuse memory that is read by the CPU after device reset. The eFuse is partitioned into six 128-bit banks (Bank 0 – Bank 5). Each bank has the same bit map (see the following figure). The purpose of the first 108 bits in each bank is fixed and the remaining 20 bits are general-purpose, software-dependent bits or reserved for future use.

Note: If IQ Amp Used, IQ Amp Correction, IQ Pha Used and IQ Pha Correction bit fields are programmed, Bank 2 must not be programmed with any values, and only the Bank Invalid bit must be programmed.

This nonvolatile one-time-programmable (OTP) memory can be used for storing the following customer-specific parameters:

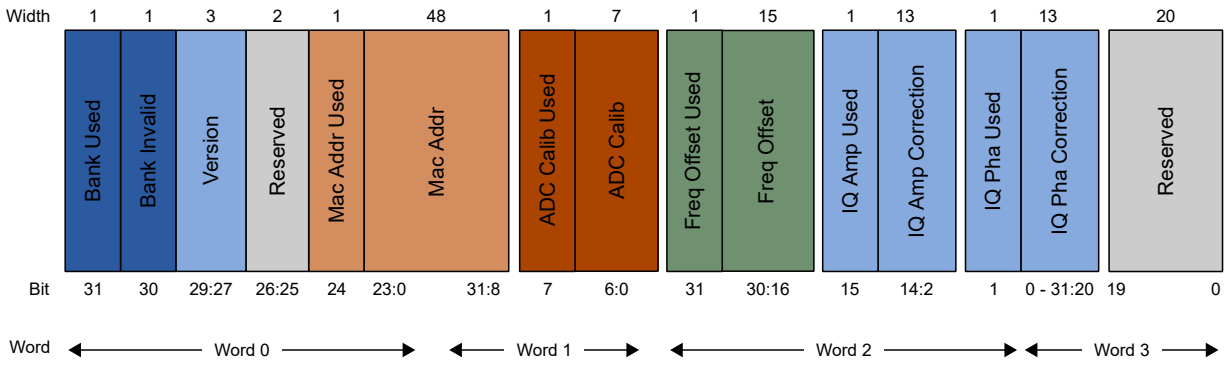
- MAC address
- Calibration information (crystal frequency offset and so on)
- Other software-specific configuration parameters

Each bank can be programmed independently, which allows for several updates of the device parameters following the initial programming. For example, if the MAC address is currently programmed in Bank 1, and to update the new MAC address, perform the following steps:

1. Invalidate the contents of Bank 1 by programming the Bank Invalid bit field of Bank 1.
2. If the IQ Amp Used, IQ Amp Correction, IQ Pha Used, and IQ Pha Correction bit fields are programmed, skip Bank 2 by programming only the Bank Invalid bit of Bank 2 (see above note).
3. Program Bank 3 with the new MAC address along with the values of ADC Calib (if used in Bank 1), Frequency Offset (from Bank 1), IQ Amp Correction (from Bank 1) and IQ Pha Correction (from Bank 1). The Used bit field for each corresponding value bit field should also be programmed.
4. Validate the contents of Bank 3 by programming the Bank Used bit field of Bank 3.

Each bit field (i.e., MAC Address, ADC Calibration, Frequency Offset, IQ Amp Correction, and IQ Pha Correction) has its corresponding Used bit field. Each Used bit field indicates the firmware that the value in the related bit field is valid. A value of '0' in the Used bit field indicates that the following bit field is invalid and a value of '1' programmed to the Used bit field indicates that the corresponding bit field is valid and can be used by firmware. By default, ATWILC1000-MR110xB modules are programmed with the MAC Address, Frequency Offset, IQ Amp, and IQ Phase fields of Bank 1.

Figure 6-1. Bit Map for ATWILC1000-MR110xB eFuse Bank



Note: The bit map has been updated with the IQ Amp Correction and IQ Pha Correction fields from firmware version 15.3 for WILC Linux, and 4.5 for WILC RTOS onwards. Earlier these bit fields were reserved for future use. For customers using a firmware older than 15.3 for WILC Linux and 4.5 for WILC RTOS, the IQ Amp Correction and IQ Pha Correction bit fields must not be used by the firmware. The matrix table below provides details on how different versions of the firmware handle the IQ Amp Used, IQ Amp Correction, IQ Pha Used, and IQ Pha Correction bit fields during Initialization.

Firmware Version	IQ Amp Used and IQ Pha Used Bit Status	
	Device with IQ Amp Used and IQ Pha Used Bit Fields with Value as '1'	Device with IQ Amp Used and IQ Pha Used Bit Fields with Value as '0'
15.3 or later for WILC Linux 4.5 or later for WILC RTOS	The firmware loads the IQ calibration values from the IQ Amp Correction and IQ Pha Correction bit fields of the corresponding eFuse bank and proceeds with Initialization.	The firmware ignores the values in the IQ Amp Correction and IQ Pha Correction bit fields and proceeds with Initialization.
Prior to 15.3 for WILC Linux Prior to 4.5 for WILC RTOS	The firmware does not check for the IQ Amp Used and IQ Pha Used bit fields and proceeds with Initialization.	

7. WLAN Subsystem

The WLAN subsystem is composed of the Media Access Controller (MAC), Physical Layer (PHY) including the radio.

7.1 MAC

7.1.1 Description

This module is designed to operate at low power while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated datapath engines, hardwired control logic and a low-power, high-efficiency microprocessor. The combination of dedicated logic with a programmable processor provides optimal power efficiency and real-time response while providing the flexibility to accommodate evolving standards and future feature enhancements.

The dedicated datapath engines are used to implement datapath functions with heavy computational requirements. For example, a Frame Check Sequence (FCS) engine checks the Cyclic Redundancy Check (CRC) of the transmitting and receiving packets, and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP, WPA2 CCMP-AES and WPA2 Enterprise security requirements.

Control functions, which have real-time requirements, are implemented using hardwired control-logic modules. These logic modules offer real-time response while maintaining configurability through the processor. Examples of hardwired control-logic modules are the channel access control module (implements EDCA, Beacon TX control, interframe spacing and so on), protocol timer module (responsible for the Network Access vector, back-off timing, timing synchronization function and slot management), MAC Protocol Data Unit (MPDU) handling module, aggregation/deaggregation module, block ACK controller (implements the protocol requirements for burst block communication) and TX/RX control Finite State Machine (FSM) (coordinate data movement between PHY and MAC interface, cipher engine and the Direct Memory Acces (DMA) interface to the TX/RX FIFOs).

The following are the characteristics of the MAC functions implemented solely in the software on the microprocessor:

- Functions with high-memory requirements or complex data structures. Examples are: association table management and power save queuing.
- Functions with low computational load or without critical real-time requirements. Examples are: authentication and association.
- Functions that require flexibility and upgradeability. Examples are: beacon frame processing and QoS scheduling.

7.1.2 Features

The ATWILC1000-MR110xB IEEE 802.11 MAC supports the following functions:

- IEEE 802.11b/g/n
- IEEE 802.11e WMM QoS EDCA Multiple Access Categories
- Advanced IEEE 802.11n Features:
  - Reception of aggregated MPDUs (A-MPDU)
  - Reception of aggregated MSDUs (A-MSDU)
  - Immediate block acknowledgment
  - Reduced Interframe Spacing (RIFS)
- IEEE 802.11i and WFA Security with Key Management

  - WEP 64/128
  - WPA-TKIP
  - 128-bit WPA2 CCMP (AES)
  - WPA2 Enterprise
- Advanced Power Management
  - Standard IEEE 802.11 Power save mode
  - Wi-Fi Alliance® WMM-PS (U-APSD)
- RTS-CTS and CTS Self Support
- Either STA or AP Mode in the Infrastructure Basic Service Set Mode
- Concurrent Mode of Operation

7.2 PHY

The ATWILC1000-MR110xB module WLAN PHY is designed to achieve the reliable and power-efficient physical layer communication specified by IEEE 802.11 b/g/n in single-stream mode with 20 MHz bandwidth. The advanced algorithms are used to achieve maximum throughput in a real-world communication environment with impairments and interference. The PHY implements all the required functions, such as Fast Fourier Transform (FFT), filtering, Forward Error Correction (FEC) that is a Viterbi decoder, frequency, timing acquisition and tracking, channel estimation and equalization, carrier sensing, clear channel assessment and automatic gain control.

7.2.1 Features

The IEEE 802.11 PHY supports the following functions:

- Single Antenna 1x1 Stream in 20 MHz Channels
- IEEE 802.11b DSSS-CCK Modulation: 1, 2, 5.5 and 11 Mbps
- IEEE 802.11g OFDM Modulation: 6, 9, 12,18, 24, 36, 48 and 54 Mbps
- IEEE 802.11n HT Modulations MCS0-7, 20 MHz, 800 and 400 ns Guard Interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0 and 72.2 Mbps(1)
- IEEE 802.11n Mixed Mode Operation
- Per Packet TX Power Control
- Advanced Channel Estimation/Equalization, Automatic Gain Control, CCA, Carrier/Symbol Recovery and Frame Detection

Note:

1. Short GI is currently not supported by Firmware. The data sheet will be updated when the feature is supported.

7.3 Radio

This section describes the properties and characteristics of the ATWILC1000- MR110xB and Wi-Fi® radio transmit and receive performance capabilities of the device. The performance measurements are taken at the RF pin assuming 50Ω impedance and the RF performance is assured at room temperature of 25°C with a derating of 2-3 dB at boundary conditions.

The measurements were taken under typical conditions: VBATT at 3.3V, VDDIO at 3.3V and temperature at 25ºC.

Table 7-1. Features and Properties

Feature	Description
Module Part Number	ATWILC1000-MR110xB
WLAN Standard	IEEE 802.11b/g/n, Wi-Fi compliant

Table 7-1. Features and Properties (continued)

Feature	Description
Host Interface	SPI, SDIO
Dimension	L x W x H: 21.7 x 14.7 x 2.1 (typical) mm
Frequency range	2.412 GHz ~ 2.484 GHz (2.4 GHz ISM band)
Number of channels	11 for North America, 13 for Europe
Modulation	802.11b: DQPSK, DBPSK, CCK 802.11g/n: OFDM/64-QAM, 16-QAM, QPSK, BPSK
Data rate	802.11b: 1, 2, 5.5, 11 Mbps 802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps
Data rate (20 MHz, short GI, 400 ns)(2)	802.11n: 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65, 72.2 Mbps
Operating temperature(1)	-40°C to 85°C
Storage temperature	-40°C to 125°C
Humidity	Operating humidity: 10% to 95% non-condensing Storage humidity: 5% to 95% non-condensing

Notes:

1. RF performance is assured at a room temperature of 25°C with a 2-3 dB change at the boundary conditions.
2. Short GI is currently not supported by Firmware. The data sheet will be updated when the feature is supported.

8. External Interfaces

This section describes the various host and debug interfaces of the ATWILC1000-MR110xB module.

The ATWILC1000-MR110xB external interfaces include:

- I^2C for debug
- SPI/SDIO for control and data transfer
- UART for debug
- General purpose Input/Output GPIO pins(1)

Note:

1. Usage of the GPIO functionality is not supported by the WILC1000 FW. The datasheet will be updated once the support for this feature is added.

8.1 Interfacing with the Host Microcontroller

This section describes how to interface the ATWILC1000-MR110xB module with the host microcontroller. The interface is comprised of a client SPI/SDIO and additional control signals, as shown in the following figure. Additional control signals are connected to the GPIO/IRQ interface of the microcontroller.

Figure 8-1. Interfacing with the Host Microcontroller

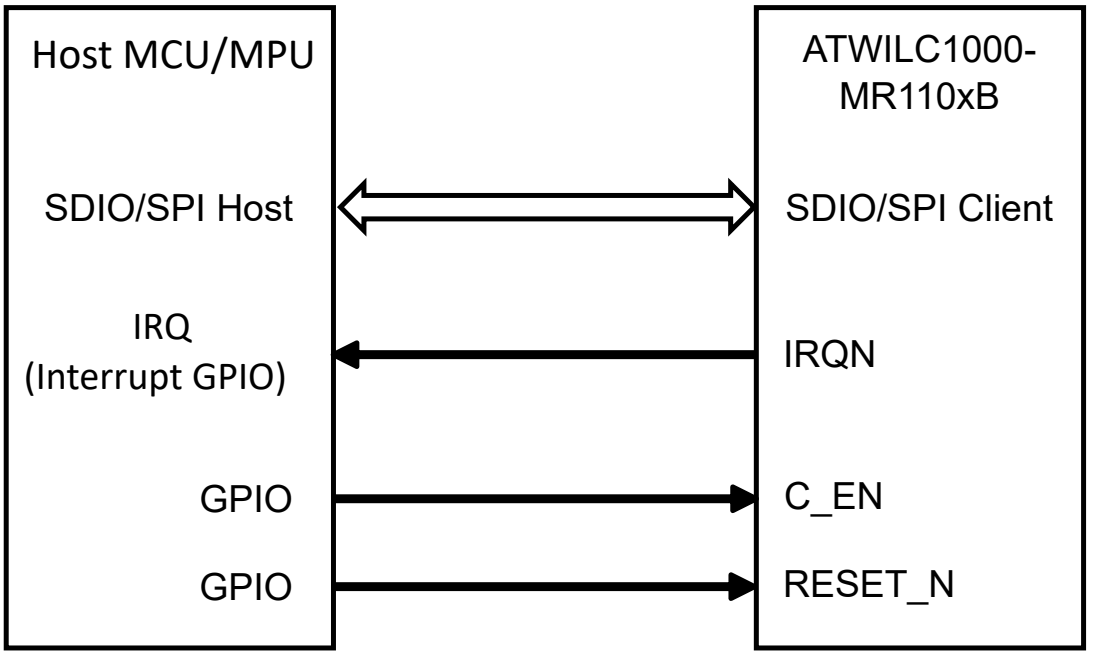


Table 8-1. Host Microcontroller Interface Pins(2)

Module Pin	Function(1)
4	RESET_N
13	IRQ_N
22	CHIP_EN
16	SPI_SSN/SD_DATA1
15	SPI_MOSI/SD_DATA2
17	SPI_MISO/SD_DATA0

Table 8-1. Host Microcontroller Interface Pins[2] (continued)

Module Pin	Function[1]
18	SPI_SCK/SD_CMD
14	SD_DATA3
19	SD_CLK

Notes:

1. Logic input for module pin SDIO_SPI_CFG(10) determines whether SDIO or SPI client interface is enabled. Connect SDIO_SPI_CFG to VDDIO through a 1 MΩ resistor to enable the SPI interface. Connect SDIO_SPI_CFG to ground to enable SDIO interface.
2. It is recommended to place test points for pins I2C_SDA(3), I2C_SCL(2), GPIO_3(25) and GPIO_5(27) in the design.

8.2 SPI Client Interface

The SPI client interface can be enabled by connecting the SDIO_SPI_CFG pin to VDDIO. This SPI interface is used to exchange the control and 802.11 data. The SPI is a full duplex client-synchronous serial interface that is available following reset when pin 10 (SDIO_SPI_CFG) is connected to VDDIO.

The SPI interface pin mapping configuration is provided in the following table.

Table 8-2. SPI Interface Pin Mapping

Pin Number	SPI Function
10	SDIO_SPI_CFG: Must be connected to VDDIO
16	SSN: Active-Low Client Select
15	MOSI: Serial Data Receive
18	SCK: Serial Clock
17	MISO: Serial Data Transmit

When the SPI is not selected, i.e., when SSN is high, the SPI interface will not interfere with data transfers between the serial host and other serial client devices. When the serial client is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the MISO line.

The SPI interface responds to a protocol that allows an external host to read or write any register in the chip and also initiate DMA transfers.

The SPI SSN, MOSI, MISO and SCK pins of this module have internal programmable pull-up resistors. These resistors are programmed to be disabled. Otherwise, if any of the SPI pins are driven to a low level while this module is in the Low-Power Sleep state, current will flow from the VDDIO supply through the pull-up resistors, increasing the current consumption of the module.

The SPI client interface supports four standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are described in the following table.

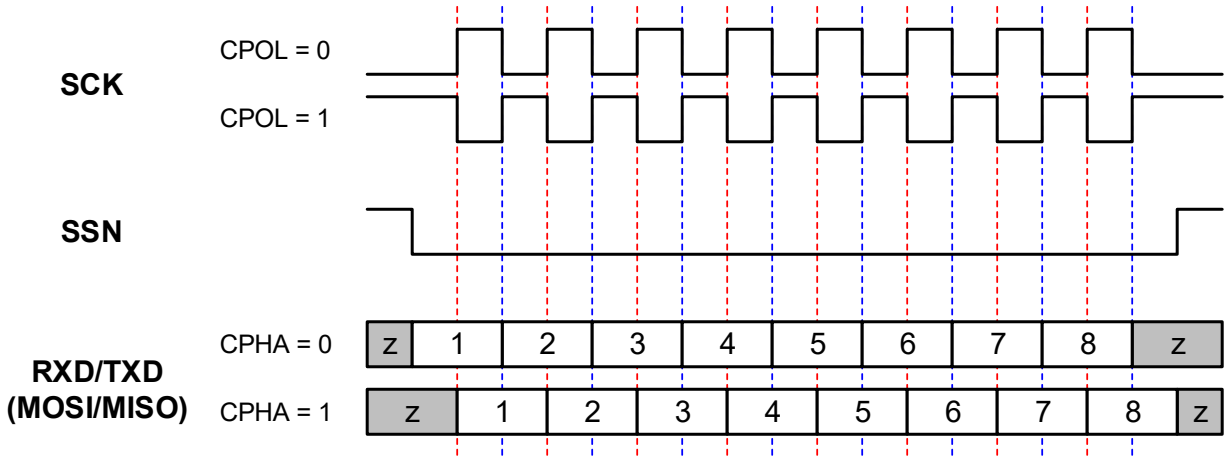
Table 8-3. SPI Client Modes

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

Note: The ATWILC1000 firmware uses "SPI Mode 0" to communicate with the host.

The red lines in the following figure correspond to clock phase at 0 and the blue lines correspond to clock phase at 1.

Figure 8-2. SPI Client Clock Polarity and Clock Phase Timing



8.3 SDIO Client Interface

The SDIO interface is enabled by connecting the SDIO_SPI_CFG pin to the ground. This SDIO interface is used to exchange the control and 802.11 data. The SDIO interface is available after reset when pin 10 (SDIO_SPI_CFG) is connected to the ground.

This SDIO is a full-speed interface. The interface supports the 1-bit/4-bit SD transfer mode at the clock range of 0-50 MHz. The host uses this interface to read and write from any register within the chip and also configures this module for DMA data transfer.

The SDIO interface pin mapping configuration is provided in the following table.

Table 8-4. ATWILC1000 SDIO Interface Pin Mapping

Pin #	SDIO Function
10	SDIO_SPI_CFG: Must be connected to the ground
14	DAT3: Data 3
15	DAT2: Data 2
16	DAT1: Data 1
17	DAT0: Data 0
18	CMD: Command
19	CLK: Clock

The SDIO card is detected when it is inserted into an SDIO host. During the normal initialization and interrogation of the card by the host, the card identifies itself as an SDIO device. The host software obtains the card information in a tuple (linked list) format and determines if that card's I/O function(s) are acceptable to activate. If the card is acceptable, it is allowed to power up fully and start the I/O function(s) built into the card.

The SD memory card communication is based on an advanced 9-pin interface (clock, command, four data and three power lines) designed to operate at a maximum operating frequency of 50 MHz.

8.3.1 Features

- Compliant with SDIO card specification version 2.0
- Host clock rate variable between 0 and 50 MHz
- Supports 1-bit/4-bit SD bus modes
- Allows card to interrupt host
- Responds to direct read/write (IO52) and extended read/write (IO53) transactions

- Supports suspend/resume operation

8.4 UART Debug Interface

This module has a Universal Asynchronous Receiver/Transmitter (UART) interface on the J25 (RXD) and J27 (TXD) pins. This interface is intended to be used only for debugging purposes. The UART is compatible with the RS-232 standard, where ATWILC1000-MR110xB operates as Data Terminal Equipment (DTE). It has a two-pin RXD/TXD interface.

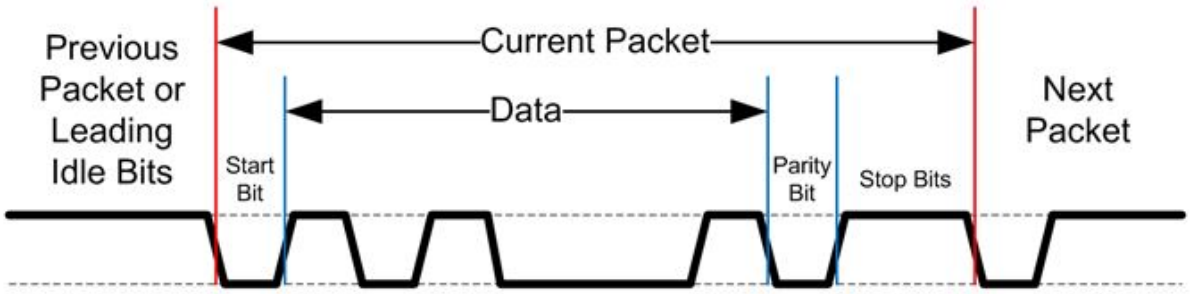
The following is the default configuration for the UART interface of ATWILC1000-MR110xB:

- Baud rate: 115200
- Data: 8 bit
- Parity: None
- Stop bit: 1 bit
- Flow control: None

It also has RX and TX FIFOs, which ensure reliable high-speed reception and low software overhead transmission. FIFO size is 4 x 8 for both RX and TX direction. The UART has status registers that show the number of received characters available in the FIFO and various error conditions; in addition, it has the ability to generate interrupts based on these status bits.

An example of UART receiving or transmitting a single packet is shown in the following figure. This example shows 7-bit data (0x45), odd parity and two stop bits.

Figure 8-3. Example of UART RX or TX Packet



8.5 I²C Client Interface

This module provides an I²C bus client that allows for easy debugging of the ATWILC1000-MR110xB devices. It supports I²C bus Version 2.1 – 2000.

The I²C interface is used only for debug. This interface is a two-wire serial interface consisting of a serial data line (SDA, Pin 17) and a serial clock (SCL, Pin 18). It responds to the seven-bit address value 0x60. This module I²C interface operates in standard mode (with data rates up to 100 Kbps) and fast mode (with data rates up to 400 Kbps).

The I²C is a synchronous serial interface. The SDA line is a bidirectional signal and changes only when the SCL line is low, except for STOP, START and RESTART conditions. The output drivers are open-drain to perform wire AND functions on the bus. The devices on the bus are limited to the 400 pF capacitance. Data is transmitted in byte packages.

For specific information, refer to the Philips Specification entitled “The I2C -Bus Specification, Version 2.1.”

9. Notes on Interfacing with the ATWILC1000-MR110xB

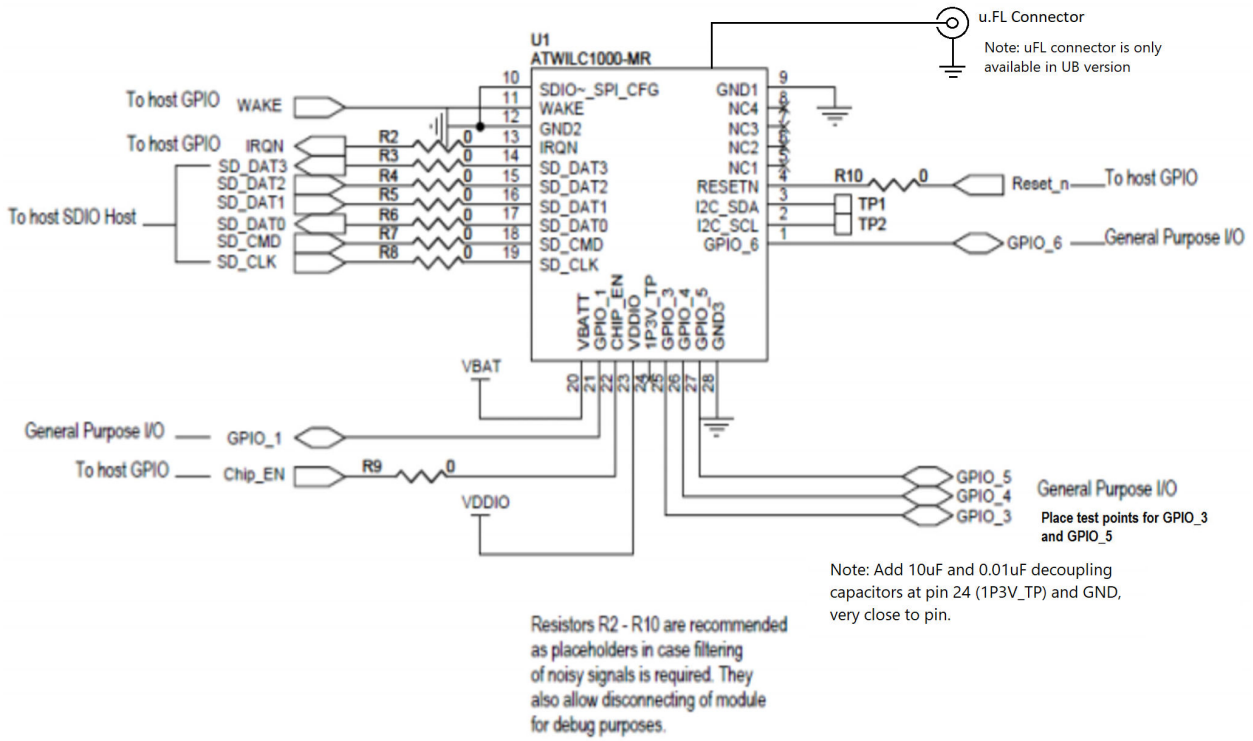
Programmable Pull-Up Resistors

The ATWILC1000-MR110xB module provides programmable pull-up resistors on various pins. The purpose of these resistors is to keep any unused input pins from floating, which causes excess current to flow through the input buffer from the VDDIO supply. Any unused pin on the device must leave these pull-up resistors enabled, so that the pin will not float. The default state at power-up is for the pull-up resistor to be enabled; however, any pin that is used must have the pull-up resistor disabled. This is so if any pins are driven to a low level while the device is in the low-power sleep state, the current flows from the VDDIO supply through the pull-up resistors, increasing the current consumption of the module. The current through any pull-up resistor that is being driven low is VDDIO/100K because the value of the pull-up resistor is approximately 100kOhm. For VDDIO = 3.3V, the current is approximately 33 µA. The pins that are used and have the pull-up resistor disabled must always be actively driven to either a high or low level and not be allowed to float.

10. Reference Design

This section provides the reference schematic for the ATWILC1000-MR110xB module with SPI and SDIO host interfaces.

Figure 10-1. Reference Schematic - SDIO Host Interface



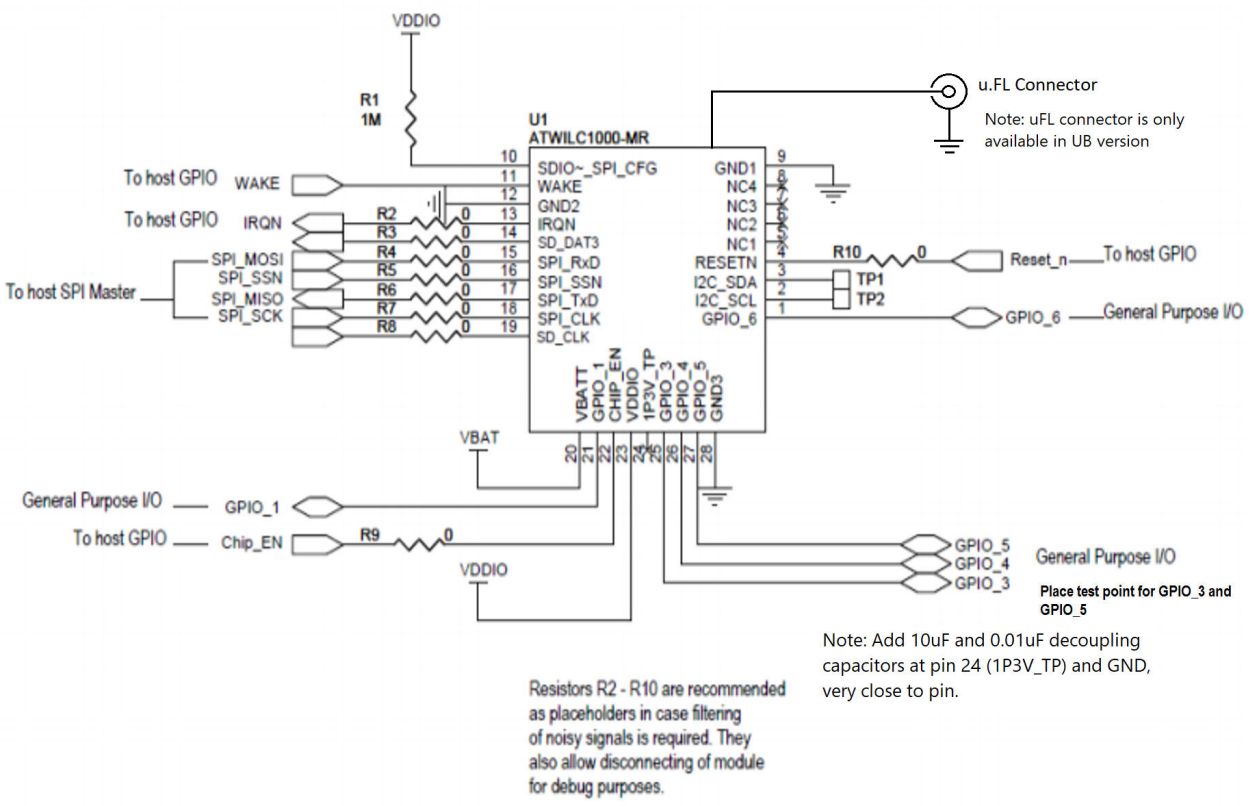
Notes:

1. Add 10 uF and 0.01 uF decoupling capacitors very close to pin 24 (1P3V_TP) and GND.
2. Add test points for pins 2, 3, 25 and 27.

Table 10-1. Bill of Materials - SDIO Host Interface Reference Schematic

Item	Qty.	Reference	Value	Description	Manufacturer	Part Number	Footprint
1	9	R2, R3, R4,R 5, R6, R7, R8, R9, R10	0R	RESISTOR,Thick Film, 0 Ohm, 0402	Yageo Corporation	RC0402JR-070RL	0402
2	1	U1	ATWILC1000-MR110xB	Wi-Fi Module	Microchip Technology Inc.	ATWILC1000-MR110xB	—

Figure 10-2. Reference Schematic - SPI Host Interface



Notes:

1. Add 10 uF and 0.01 uF decoupling capacitors very close to pin 24 (1P3V_TP) and GND.
2. Add test points for pins 2, 3 , 25 and 27.

Table 10-2. Bill of Materials - SPI Host Interface Reference Schematic

Item	Qty.	Reference	Value	Description	Manufacturer	Part Number	Footprint
1	1	R1	1M	RESISTOR,Thick Film, 1M Ohm, 0402	Yageo Corporation	RC0100FR-071ML	0402
2	9	R2, R3, R4, R5, R6, R7, R8, R9, R10	0R	RESISTOR,Thick Film, 0 Ohm, 0402	Yageo Corporation	RC0402JR-070RL	0402
3	1	U1	ATWILC1000-MR110xB	Wi-Fi Module	Microchip Technology Inc.	ATWILC1000-MR110xB	—

11. Module Outline Drawings

The ATWILC1000-MR110PB module package details are outlined in the following figure. Dimensions are in mm.

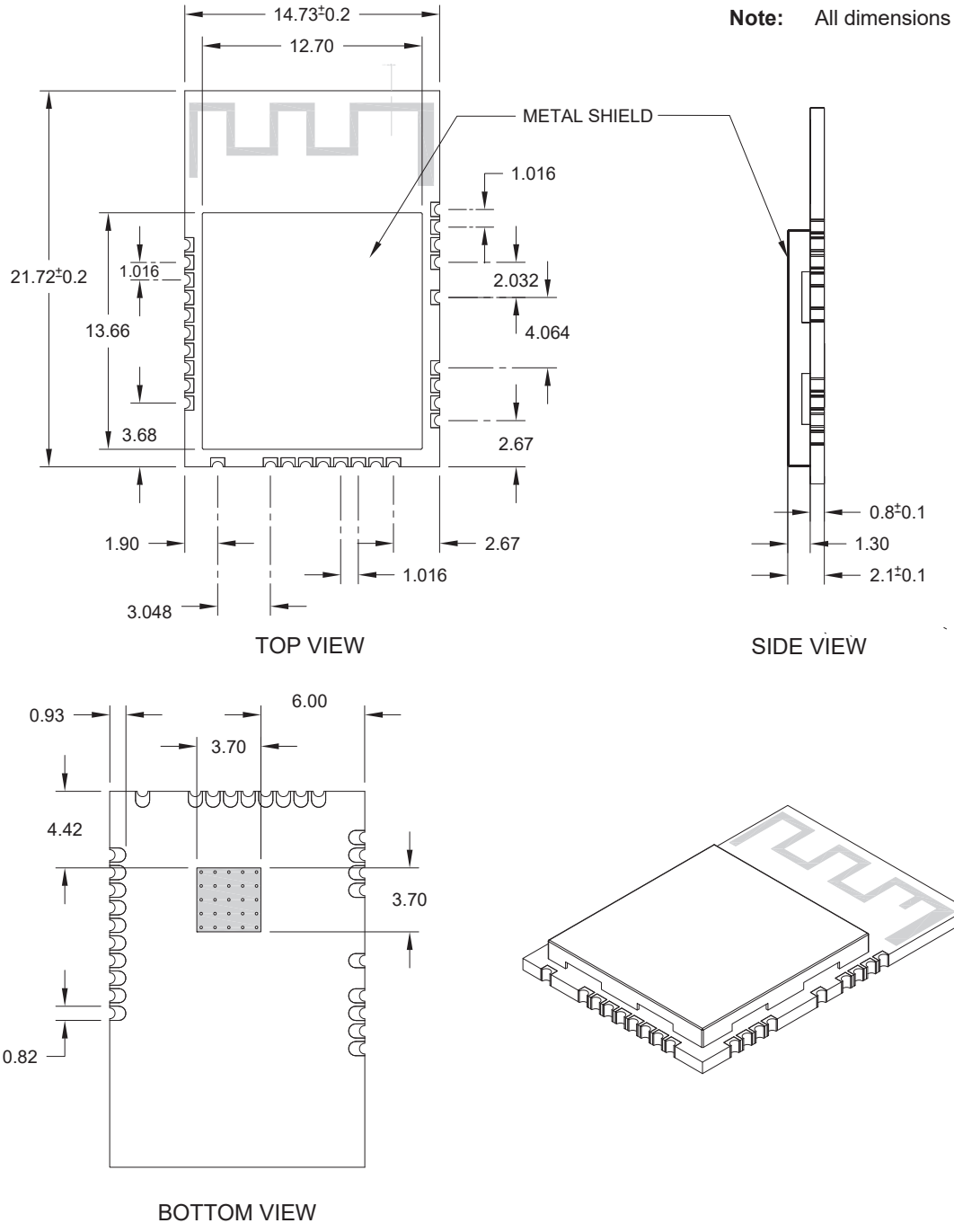
Tolerance details for the mechanical dimensions:

- L: 21.72 mm ± 0.15 mm
- W: 14.73 mm ± 0.15 mm
- H: 2.113 mm ± 0.15 mm

28-Lead PCB Module - 21.72x14.73x2.1 mm Body [Module]
ATWINC15x0-MR210PB and ATWILC1000-MR110PB (Package LCB)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Note: All dimensions are in mm.



Microchip Technology Drawing C04-21305PB Rev D

The ATWILC1000-MR110UB module package details are outlined in the following figure. Dimensions are in mm.

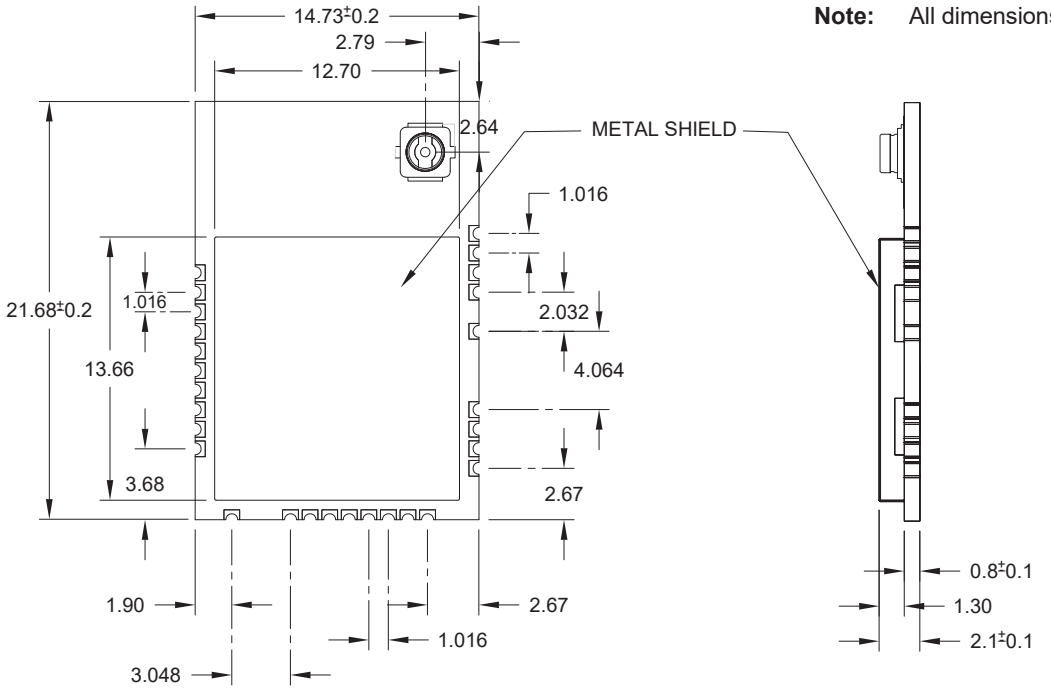
Tolerance details for the mechanical dimensions:

- L: 21.72 mm ± 0.15 mm
- W: 14.73 mm ± 0.15 mm
- H: 2.113 mm ± 0.15 mm

28-Lead PCB Module - 21.72x14.73x2.1 mm Body [Module]
ATWINC15x0-MR210UB and ATWILC1000-MR110UB (Package LFB)

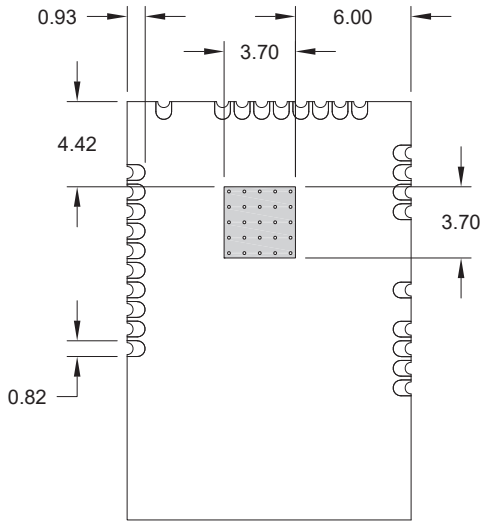
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Note: All dimensions are in mm.

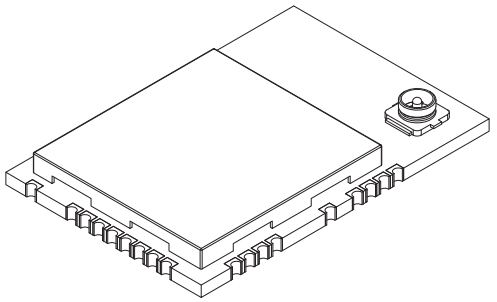


TOPVIEW

SIDE VIEW



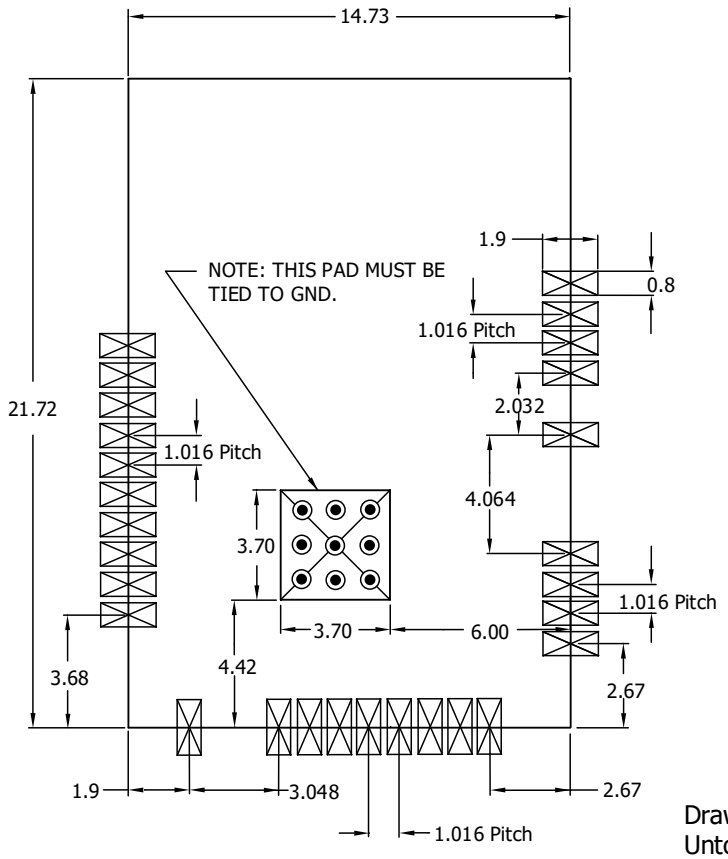
BOTTOM VIEW



Microchip Technology Drawing C04-21305UB Rev D

This section provides the outline drawing for the recommended footprint for the ATWILC1000-MR110xB module. It is imperative that the center Ground Pad is provided, with an array of GND vias to provide a good ground and act as a thermal sink for the ATWILC1000-MR110xB module.

Figure 11-1. Recommended Solder Pad Footprint



SOLDER PAD FOOTPRINT

Drawing not to scale.
Untoleranced dimensions.
Units=mm.

12. Design Consideration

This section provides the guidelines on placement and routing to achieve the best performance.

12.1 ATWILC1000-MR110PB Placement and Routing Guidelines

It is critical to follow the recommendations listed below to achieve the best RF performance:

- The module must be placed on a host board and the printed antenna area must overlap with the carrier board. The portion of the module containing the antenna must not stick out over the edge of the host board. The antenna is designed to work properly when it is sitting directly on top of a 1.5 mm thick printed circuit board. Figure 12-2 shows the best, poor and worst case module placements in a host board.
- If the module is placed at the edge of the host board, a minimum 22 mm by 5 mm area directly under the antenna must be clear of all metal on all layers of the board. “In-land” placement is acceptable; however, the depth of the keep-out area must groove to: the module edge to the host board edge plus 5 mm.
  Note: Do not place the module in the middle of the host board or far away from the host board edge.
- Follow the module placement, keepout and host PCB cutout recommendation, as shown in Figure 12-1.
  - Avoid routing any traces in the highlighted region on the top layer of the host board, which is directly below the module area.
  - Follow the electrical keep-out layer recommendation, as shown in Figure 12-1. There must not be any copper in any of the layers of the host board in this region. Avoid placing any components (like mechanical spacers, bumpon, etc.) in the recommended electrical keep-out area.
  - Place GND polygon pour below the module with the recommended boundary in the top layer of the host board, as shown in Figure 12-1. Do not have any breaks in this GND plane.
  - Place sufficient GND vias in the highlighted area below the module for better RF performance.
  - It is recommended to have a 3 x 3 grid of GND vias solidly connecting the exposed GND paddle of the module to the inner layer ground plane. This will act as a good ground and thermal conduction for the ATWILC1000-MR110PB module. The GND vias must have a minimum via hole size of 0.3 mm.
  - Follow the mechanical boundary of the host PCB, as shown in Figure 12-1.
- Keep large metal objects away from the antenna to avoid electromagnetic field blocking.
- Do not enclose the antenna within a metal shield.
- Keep any components that may radiate noise or signals within the 2.4 GHz – 2.5 GHz frequency band away from the antenna and if possible, shield those components. Any noise radiated from the host board in this frequency band will degrade the sensitivity of the module.
- Make sure the width of the traces routed to the GND, VDDIO and VBAT rails are sufficiently larger for handling the peak TX current consumption.

Figure 12-1. ATWILC1000-MR110PB Placement Reference

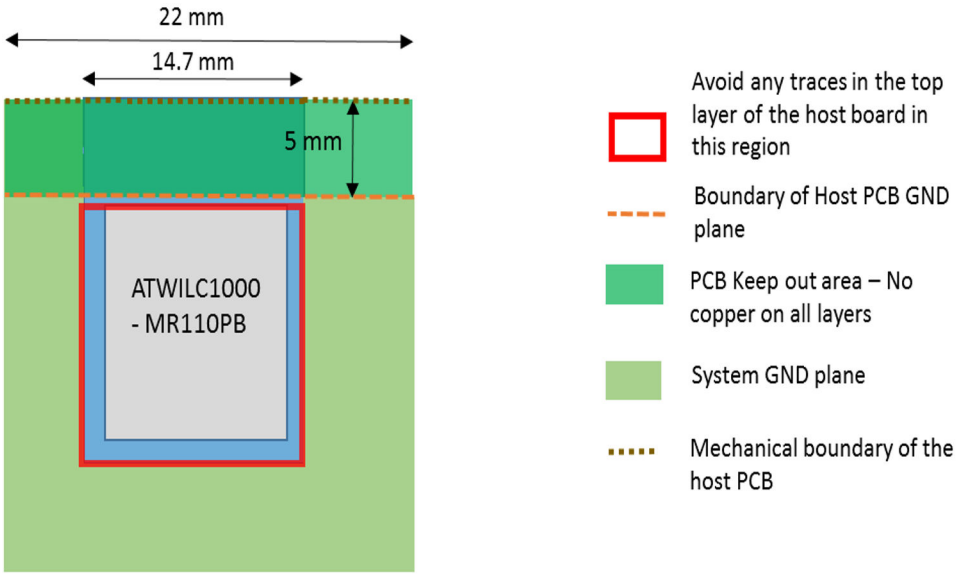
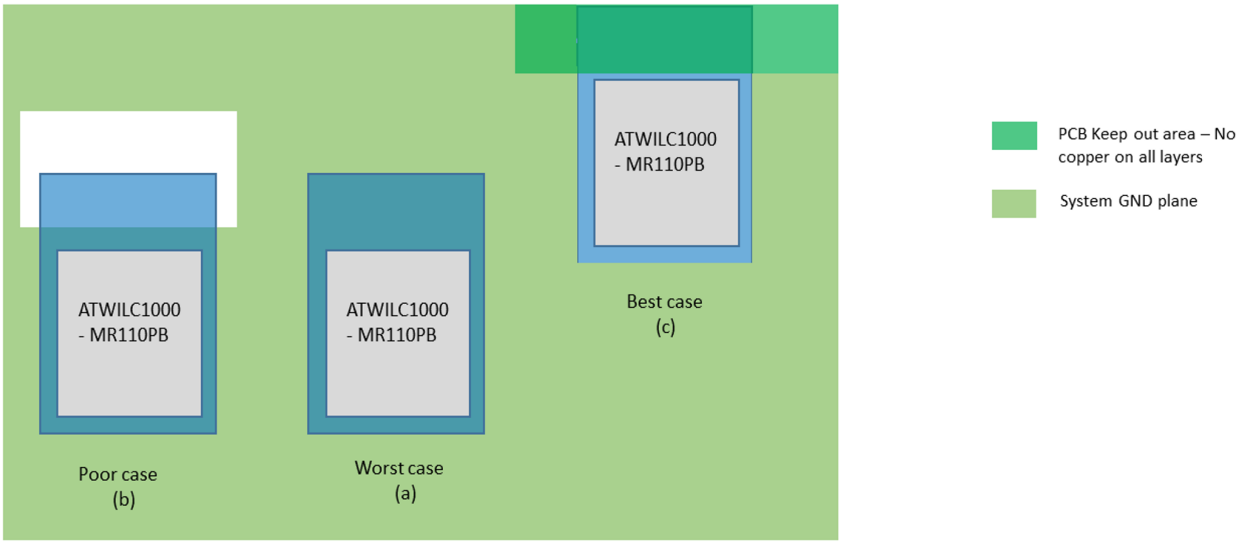


Figure 12-2. ATWILC1000-MR110PB Placement Example



12.2 Printed PCB Antenna Performance of ATWILC1000-MR110PB

The printed PCB antenna on the ATWILC1000-MR110PB is a meandered Inverted F Antenna (IFA). The antenna is fed via matching network, which is matched for the module installed on 1.5 mm thick main board. Main board thickness deviation by ±1 mm changes RX/TX performance by ±1 dB maximum referring to the RX/TX performance with the default antenna-matching network and installed on 1.5 mm thick main board (FR-4 substrate).

Measured antenna gain is -0.3 dBi.

Antenna Radiation Pattern

The following figures illustrate the antenna radiation pattern. During the measurement, the printed antenna is placed in the XZ plane with the Y axis being perpendicular to the module and pointing to the back of the module.

Figure 12-3. Antenna Radiation Pattern when Phi = 0 Degree

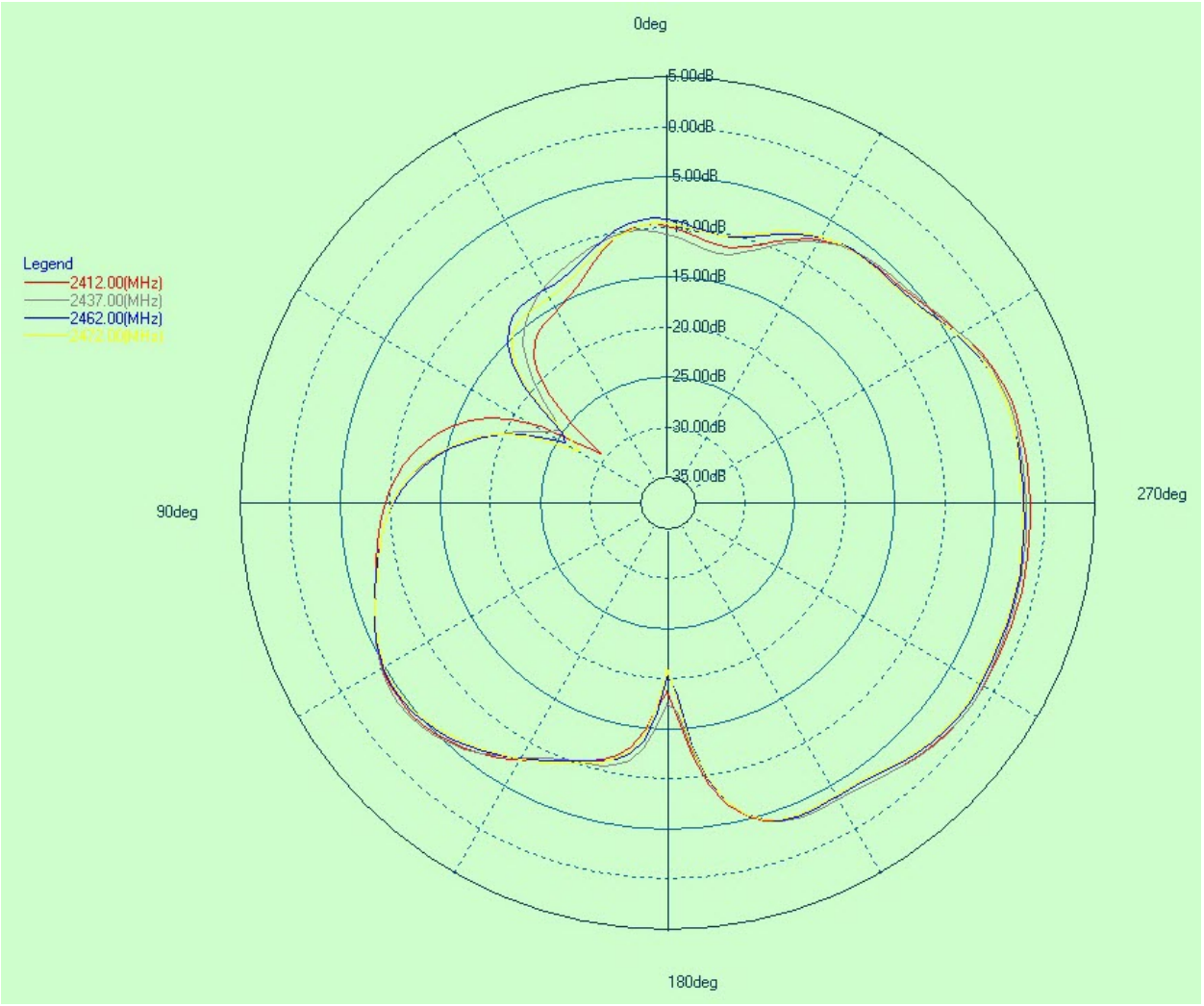


Figure 12-4. Antenna Radiation Pattern when Phi = 90 Degree

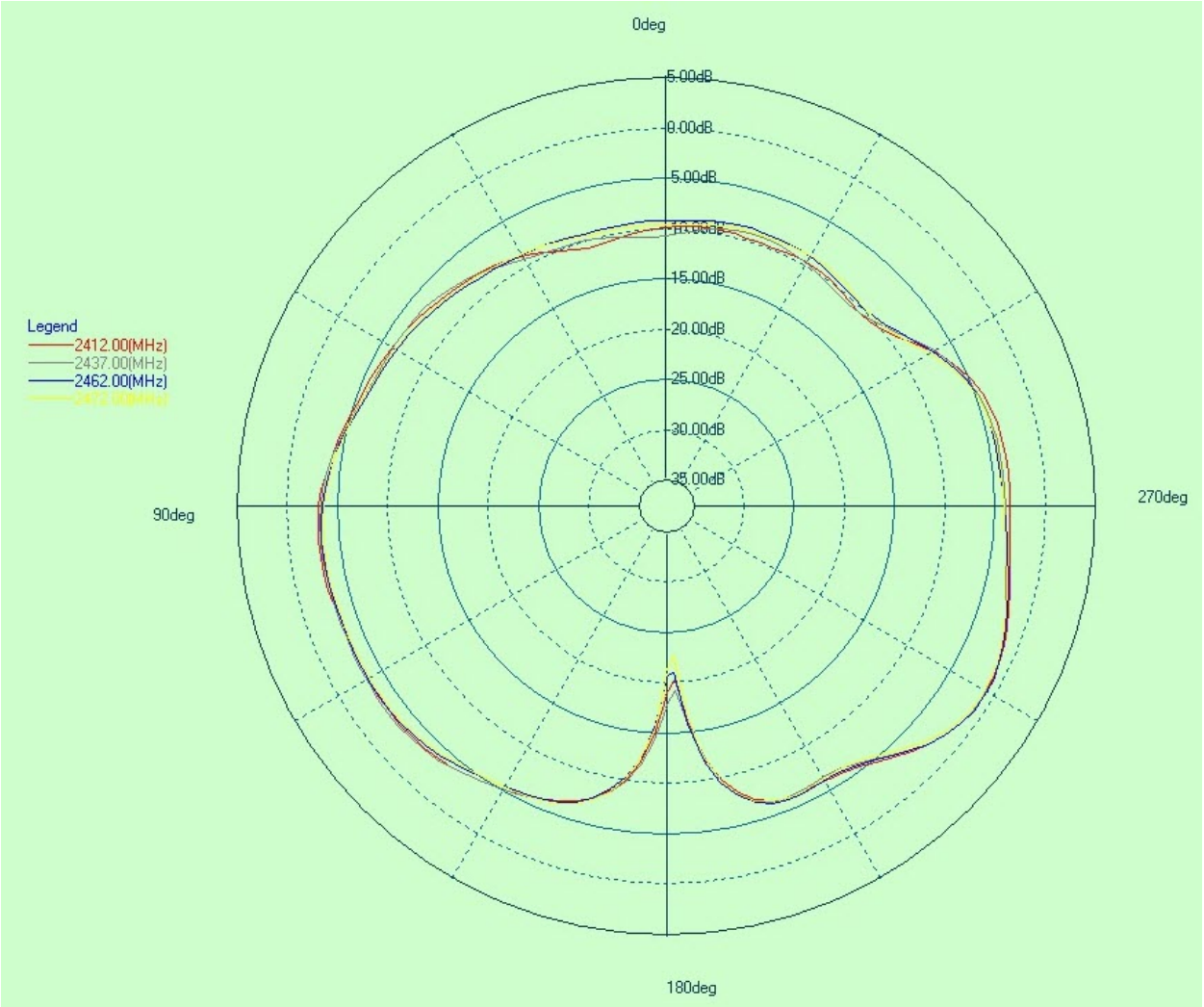
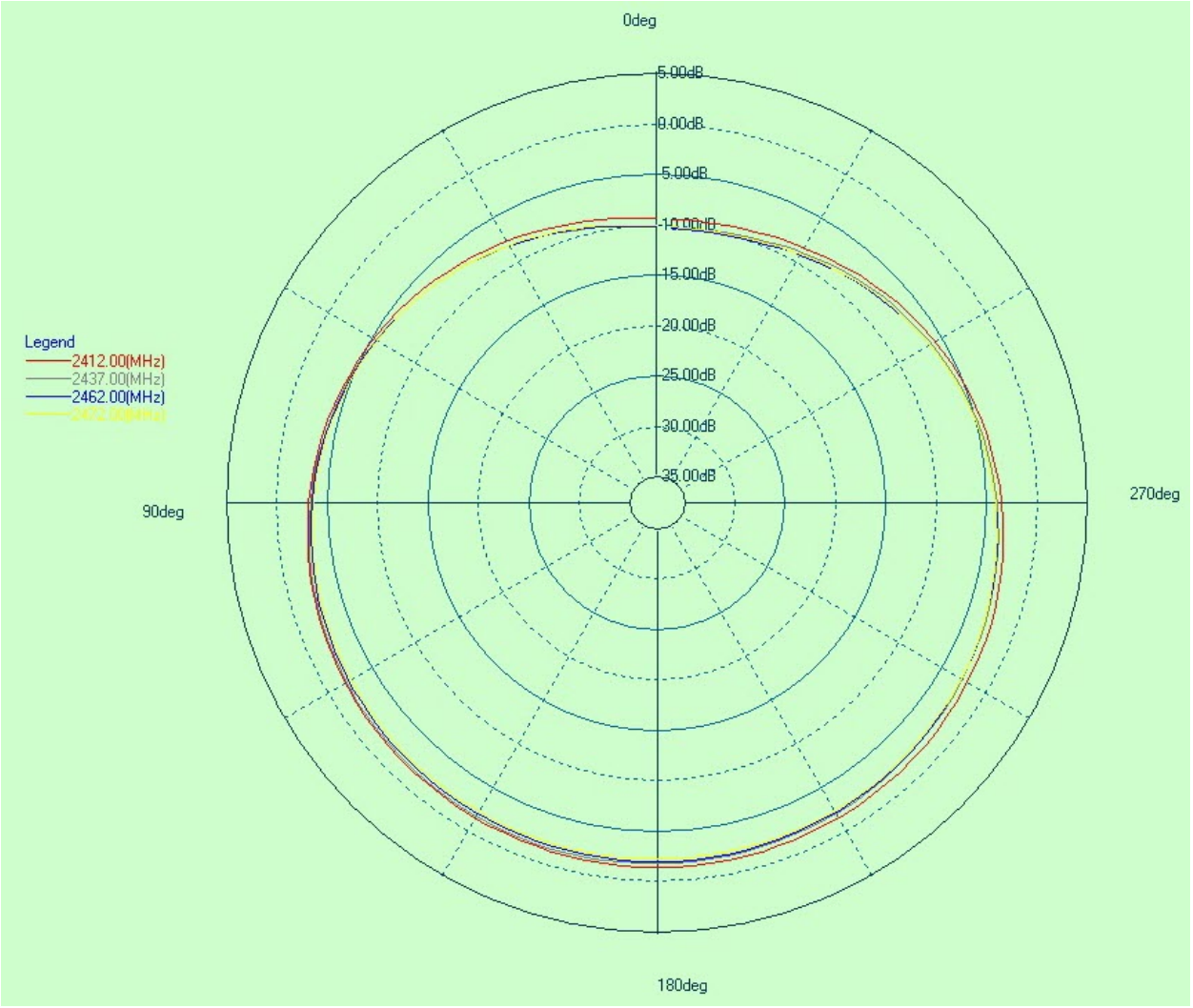


Figure 12-5. Antenna Radiation Pattern when Theta = 90 Degree



12.3 ATWILC1000-MR110UB Placement and Routing Guidelines

The ATWILC1000-MR110UB module has an Ultra Small Miniature RF Connector (U.FL) for the external antenna.

The choice of antenna is limited to the antenna types that the module was tested and approved for. For a list of tested and approved antennas that may be used with the module, refer to the respective country in the Regulatory Approval section.

An approved list of external antennas tested and certified with ATWILC1000-MR110UB module is shown in Table 12-1.

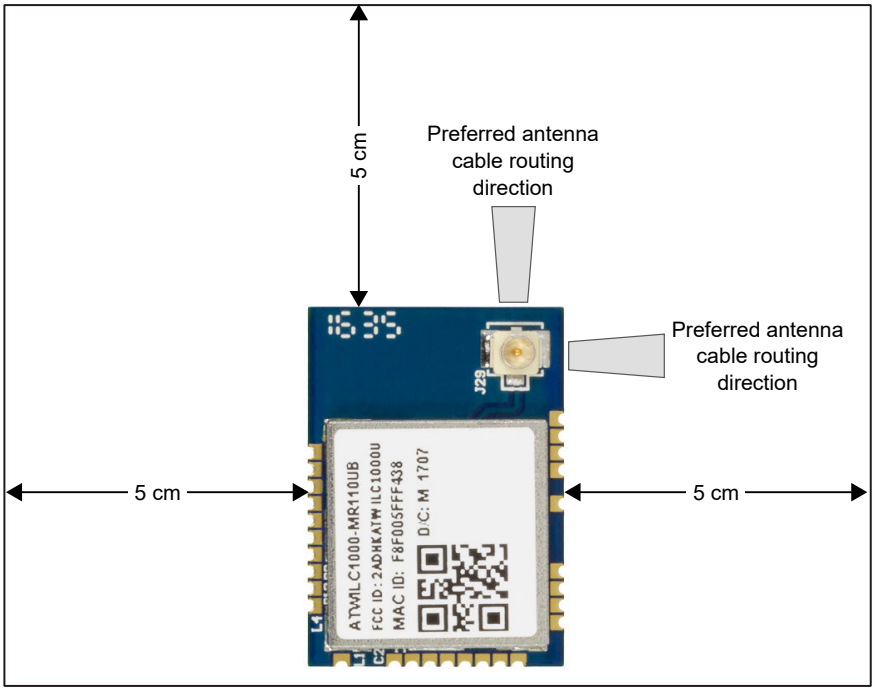
It is critical to follow the recommendations listed below to achieve the best RF performance:

1. Avoid routing any traces on the top layer of the host board, which is directly below the module area.
2. Place the GND polygon pour below the complete module area. Do not have any breaks in this GND plane.
3. Place sufficient GND vias in the GND polygon pour below the module area for better RF performance.
4. It is recommended to have a 3 x 3 grid of GND vias solidly connecting the exposed GND paddle of the module to the inner layer ground plane of the host board. This will act as a good ground

and thermal conduction path for the ATWILC1000-MR110UB module. The GND vias must have a minimum via hole size of 0.3 mm.

5. Keep large metal objects away from the external antenna to avoid electromagnetic field blocking.
6. Do not enclose the external antenna within a metal shield.
7. Keep any components that may radiate noise or signals within the 2.4 GHz – 2.5 GHz frequency band away from the external antenna and if possible, shield those components. Any noise radiated from the host board in this frequency band will degrade the sensitivity of the module.
8. Make sure the width of the traces routed to the GND, VDDIO and VBAT rails are sufficiently larger for handling the peak TX current consumption.
9. The antenna should preferably be placed at a distance greater than 5 cm away from the module. The following figure shows the antenna keep out area indication; where the antenna must not be placed in this area. This recommendation is based on an open-air measurement and does not take into account by any metal shielding of the customer end product. When a metal enclosure is used, the antenna can be located closer to the ATWILC1000-MR110UB module.
   The following figure illustrates how an antenna cable should be routed based on the antenna's location with respect to the ATWILC1000-MR110UB PCB. There are two possible options for the optimum routing of the cable.

Figure 12-6. ATWILC1000-MR110UB Antenna Placement Guidelines



12.4 Recommended External Antennas

The ATWILC1000-MR110UB module is approved to use with the antennas listed in the following table.

It is permissible to use different antenna, provided the same antenna type, antenna gain (equal or less than), and similar in-band and out-of-band characteristics are present (refer to specification sheet for cutoff frequencies).

If other antenna types are used, the OEM installer must conduct the necessary assessments and authorize the antenna with respective regulatory agencies and ensure compliance. For more details on the corresponding regulatory approval sections, refer to Appendix A: Regulatory Approval.

Table 12-1. List of External Antenna - Antenna Gain at 2.4 GHz (dBi)

List Item	Part Number	Manufacturer	Antenna Gain at 2.4 GHz Band	Antenna Type	Regulatory Authority(1)		
					FCC	ISED	CE
1	RFA-02-P33	Aristotle	2	PCB	X	X	X
2	RFA-02-D3	Aristotle	2	Dipole	X	X	X
3	RFA-02-G03	Aristotle	2	Metal Stamp	X	X	X
4	RFA-02-L2H1	Aristotle	2	Dipole	X	X	X
5	RFA-02-P05	Aristotle	2	PCB	X	X	X
6	RFA-02-C2M2(2)(3)	Aristotle	2	Dipole	X	X	X
7	86254	Delock	2	PCB	—	—	X
8	W3525B039	Pulse Electronics	2	PCB	X	X	X
9	RFDPA870920IMLB301	WALSIN	1.84	Dipole	X	X	X
10	RN-SMA-S	Microchip	0.56	Dipole	X	X	X

Notes:

1. X = Antennas covered under the certification.
2. If the end-product using the module is designed to have an antenna port that is accessible to the end user, an RP (Reverse Polarity)-SMA socket must be used.
3. If an RF coaxial cable is used between the module RF output and the enclosure, then an RP-SMA connector must be used in the enclosure wall for the interface with the antenna.
4. Contact the antenna vendor for detailed antenna specifications to review suitability to end-product operating environment and to identify alternatives.

12.5 Reflow Profile Information

For information on the reflow process guidelines, refer to the “Solder Reflow Recommendation” Application Note (www.microchip.com/DS00233).

12.6 Module Assembly Considerations

The ATWILC1000-MR110xB module is assembled with an EMI shield to ensure compliance with EMI emission and immunity rules. The EMI shield is made of a tin-plated steel (SPTE) and is not hermetically sealed. Solutions such as IPA and similar solvents can be used to clean this module. Cleaning solutions containing acid must never be used on the module.

12.7 Conformal Coating

The modules are not intended for use with a conformal coating and the customer assumes all risks (such as the module reliability, performance degradation and so on) if a conformal coating is applied to the modules.

13. Appendix A: Regulatory Approval

The ATWILC1000-MR110PB and ATWILC1000-MR110UB modules have received regulatory approval for the following countries:

- ATWILC1000-MR110PB
  - United States/FCC ID: 2ADHKATWILC1000
  - Canada/ISED:
    - IC: 20266-ATWILC1000
    - HVIN: ATWILC1000-MR110PB
    - PMN: ATWILC1000-MR110PB
  - Europe/CE
  - Japan/MIC: 005-101763
  - Korea/KCC: R-CRM-mcp-WILC1000MR110P
  - Taiwan/NCC: CCAN18LP0310T7
  - China/SRRC: CMIIT ID: 2018DJ1313
- ATWILC1000-MR110PB
  - United States/FCC ID: 2ADHKATWILC1000U
  - Canada/ISED:
    - IC: 20266-WILC1000UB
    - HVIN: ATWILC1000-MR110UB
    - PMN:
  - Europe/CE

Gain Table for Individual Regulatory Region

The ATWILC1000-MR110PB module has received regulatory approvals for many regions in the world, namely United States/FCC, Canada/ISED, Europe/CE, Japan/MIC, Korea/KCC, Taiwan/NCC, and China/SRRC. The ATWILC1000-MR110UB module has received regulatory approvals for United States/FCC, Canada/ISED and Europe/CE.

The default firmware uses a common gain table that meets IEEE 802.11 specifications, and regulatory regions as noted above.

In some cases, the output power is limited by the regulatory region with the most stringent transmit power limits. To optimize performance, and if end products' destination is known, the specific gain table for that region can be optionally embedded into the firmware.

The regulatory region certified gain table for individual regulatory region is available on ATWILC1000-MR110PB and ATWILC1000-MR110UB product page. Customers can update the gain table in firmware by following the instructions in section 6. Updating Application Gain Table into WILC1000 of *ATWILC1000 – Deriving Application Gain Table Application Note*.

13.1 United States

The ATWILC1000-MR110PB and ATWILC1000-MR110UB modules have received Federal Communications Commission (FCC) CFR47 Telecommunications, Part 15 Subpart C "Intentional Radiators" single-modular approval in accordance with Part 15.212 Modular Transmitter approval. Single-modular transmitter approval is defined as a complete RF transmission sub-assembly, designed to be incorporated into another device, that must demonstrate compliance with FCC rules and policies independent of any host. A transmitter with a modular grant can be installed in different end-use products (referred to as a host, host product or host device) by the grantee or other equipment manufacturer, then the host product may not require additional testing or

equipment authorization for the transmitter function provided by that specific module or limited module device.

The user must comply with all of the instructions provided by the Grantee, which indicate installation and/or operating conditions necessary for compliance.

A host product itself is required to comply with all other applicable FCC equipment authorization regulations, requirements, and equipment functions that are not associated with the transmitter module portion. For example, compliance must be demonstrated: to regulations for other transmitter components within a host product; to requirements for unintentional radiators (Part 15 Subpart B), such as digital devices, computer peripherals, radio receivers, etc.; and to additional authorization requirements for the non-transmitter functions on the transmitter module (i.e., Suppliers Declaration of Conformity (SDoC) or certification) as appropriate (e.g., Bluetooth and Wi-Fi transmitter modules may also contain digital logic functions).

13.1.1 Labeling and User Information Requirements

The ATWILC1000-MR110PB and ATWILC1000-MR110UB modules have been labeled with its own FCC ID number, and if the FCC ID is not visible when the module is installed inside another device, then the outside of the finished product into which the module is installed must display a label referring to the enclosed module. This exterior label must use the following wording:

• For ATWILC1000-MR110PB
Contains Transmitter Module FCC ID: 2ADHKATWILC1000 or Contains FCC ID: 2ADHKATWILC1000 **This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation**.
• For ATWILC1000-MR110UB
Contains Transmitter Module FCC ID: 2ADHKATWILC1000U or Contains FCC ID: 2ADHKATWILC1000U **This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation**.

The user's manual for the finished product must include the following statement:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures: • Reorient or relocate the receiving antenna • Increase the separation between the equipment and receiver • Connect the equipment into an outlet on a circuit different from that to which the receiver is connected • Consult the dealer or an experienced radio/TV technician for help

Additional information on labeling and user information requirements for Part 15 devices can be found in KDB Publication 784748, which is available at the FCC Office of Engineering and Technology (OET) Laboratory Division Knowledge Database (KDB) apps.fcc.gov/oetcf/kdb/index.cfm.

13.1.2 RF Exposure

All transmitters regulated by FCC must comply with RF exposure requirements. KDB 447498 General RF Exposure Guidance provides guidance in determining whether proposed or existing transmitting facilities, operations or devices comply with limits for human exposure to Radio Frequency (RF) fields adopted by the Federal Communications Commission (FCC).

From the FCC Grant: Output power listed is conducted. This transmitter is restricted for use with the specific antenna(s) tested in this application for Certification.

The antenna(s) used with this transmitter must be installed to provide a separation distance of at least 6.5 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter. Users and installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying RF exposure compliance.

13.1.3 Approved Antenna Types

To maintain modular approval in the United States, only the antenna types that have been tested shall be used. It is permissible to use a different antenna, provided the same antenna type and antenna gain (equal to or less than) is used. An antenna type comprises antennas having similar in-band and out-of-band radiation patterns.

Testing of the ATWILC1000-MR110PB module was performed with the integral PCB antenna.

Testing of the ATWILC1000-MR110UB module was performed with the antenna types mentioned in the Table 12-1.

13.1.4 Helpful Web Sites

- Federal Communications Commission (FCC): www.fcc.gov.
- FCC Office of Engineering and Technology (OET) Laboratory Division Knowledge Database (KDB) apps.fcc.gov/oetcf/kdb/index.cfm.

13.2 Canada

The ATWILC1000-MR110PB and ATWILC1000-MR110UB modules have been certified for use in Canada under Innovation, Science and Economic Development Canada (ISED, formerly Industry Canada) Radio Standards Procedure (RSP) RSP-100, Radio Standards Specification (RSS) RSS-Gen and RSS-247. Modular approval permits the installation of a module in a host device without the need to recertify the device.

13.2.1 Labeling and User Information Requirements

Labeling Requirements (from RSP-100 - Issue 12, Section 5): The host product shall be properly labeled to identify the module within the host device.

The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host device; otherwise, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number of the module, preceded by the word “Contains” or similar wording expressing the same meaning, as follows:

• For ATWILC1000-MR110PB
Contains IC: 20266-ATWILC1000
• For ATWILC1000-MR110UB
Contains IC: 20266-WILC1000UB

User Manual Notice for License-Exempt Radio Apparatus (from Section 8.4 RSS-Gen, Issue 5, March 2019): User manuals for license-exempt radio apparatus shall contain the following or equivalent notice in a conspicuous location in the user manual or alternatively on the device or both:

This device contains license-exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development Canada's license-exempt RSS(s). Operation is subject to the following two conditions:

(1) This device may not cause interference;

(2) This device must accept any interference, including interference that may cause undesired operation of the device.

L'émetteur/récepteur exempt de licence contenu dans le présent appareil est conforme aux CNR d'Innovation, Sciences et Développement économique Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

1. L'appareil ne doit pas produire de brouillage;

2. L'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Transmitter Antenna (From Section 6.8 RSS-GEN, Issue 5, March 2019): User manuals, for transmitters shall display the following notice in a conspicuous location:

This radio transmitter [IC: 20266-ATWILC1000 and IC: 20266-WILC1000UB] has been approved by Innovation, Science and Economic Development Canada to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Le présent émetteur radio [IC: 20266-ATWILC1000 and IC: 20266-WILC1000UB] a été approuvé par Innovation, Sciences et Développement économique Canada pour fonctionner avec les types d'antenne énumérés cidessous et ayant un gain admissible maximal. Les types d'antenne non inclus dans cette liste, et dont le gain est supérieur au gain maximal indiqué pour tout type figurant sur la liste, sont strictement interdits pour l'exploitation de l'émetteur.

Immediately following the above notice, the manufacturer shall provide a list of all antenna types approved for use with the transmitter, indicating the maximum permissible antenna gain (in dBi) and required impedance for each.

13.2.2 RF Exposure

All transmitters regulated by Innovation, Science and Economic Development Canada (ISED) must comply with RF exposure requirements listed in RSS-102 - Radio Frequency (RF) Exposure Compliance of Radio communication Apparatus (All Frequency Bands).

This transmitter is restricted for use with a specific antenna tested in this application for certification, and must not be co-located or operating in conjunction with any other antenna or transmitters within a host device, except in accordance with Canada multi-transmitter product procedures.

The installation of the transmitter must ensure that the antenna has a separation distance of at least 6.5 cm from all persons or compliance must be demonstrated according to the ISED SAR procedures.

13.2.3 Approved Antenna Types

Testing of the ATWILC1000-MR110PB module was performed with the integral PCB antenna.

Testing of the ATWILC1000-MR110UB module was performed with the antenna types mentioned in the Table 12-1.

13.2.4 Helpful Web Sites

Innovation, Science and Economic Development Canada (ISED): www.ic.gc.ca/.

13.3 Europe

The ATWILC1000-MR110PB and ATWILC1000-MR110UB modules is/are a Radio Equipment Directive (RED) assessed radio module that is CE marked and has been manufactured and tested with the intention of being integrated into a final product.

The ATWILC1000-MR110PB and ATWILC1000-MR110UB modules has/have been tested to RED 2014/53/EU Essential Requirements mentioned in the following European Compliance table.

Table 13-1. European Compliance

Certification	Standards	Article
Safety	EN 62368	3.1a
Health	EN 62311	
EMC	EN 301 489-1	3.1b
	EN 301 489-17	
Radio	EN 300 328	3.2

The ETSI provides guidance on modular devices in the "*Guide to the application of harmonised standards covering articles 3.1b and 3.2 of the RED 2014/53/EU (RED) to multi-radio and combined radio and non-radio equipment*" document available at http://www.etsi.org/deliver/etsi_eg/203300_203399/20 3367/01.01.01_60/eg_203367v010101p.pdf.

Note: To maintain conformance to the standards listed in the preceding European Compliance table, the module shall be installed in accordance with the installation instructions in this data sheet and shall not be modified. When integrating a radio module into a completed product, the integrator becomes the manufacturer of the final product and is therefore responsible for demonstrating compliance of the final product with the essential requirements against the RED.

13.3.1 Labeling and User Information Requirements

The label on the final product that contains the ATWILC1000-MR110PB and ATWILC1000-MR110UB modules must follow CE marking requirements.

13.3.2 Conformity Assessment

From ETSI Guidance Note EG 203367, section 6.1, when non-radio products are combined with a radio product:

If the manufacturer of the combined equipment installs the radio product in a host non-radio product in equivalent assessment conditions (i.e. host equivalent to the one used for the assessment of the radio product) and according to the installation instructions for the radio product, then no additional assessment of the combined equipment against article 3.2 of the RED is required.

13.3.2.1 Simplified EU Declaration of Conformity

Hereby, Microchip Technology Inc. declares that the radio equipment type ATWILC1000-MR110PB and ATWILC1000-MR110UB modules is/are in compliance with Directive 2014/53/EU.

The full text of the EU declaration of conformity for this product is available at http://www.microchip.com/ATWILC1000 (available under Documents > Certifications).

13.3.3 Approved Antenna Types

Testing of the ATWILC1000-MR110PB module was performed with the integral PCB antenna.

Testing of the ATWILC1000-MR110UB module was performed with the antenna types mentioned in the Table 12-1.

13.3.4 Helpful Websites

A document that can be used as a starting point in understanding the use of Short Range Devices (SRD) in Europe is the European Radio Communications Committee (ERC) Recommendation 70-03 E, which can be downloaded from the European Communications Committee (ECC) at: http://www.ecodocdb.dk/.

Additional helpful web sites are:

- Radio Equipment Directive (2014/53/EU): https://ec.europa.eu/growth/single-market/european-standards/harmonised-standards/red_en
- European Conference of Postal and Telecommunications Administrations (CEPT):

http://www.cept.org

- European Telecommunications Standards Institute (ETSI): http://www.etsi.org
- The Radio Equipment Directive Compliance Association (REDCA): http://www.redca.eu/

13.4 Japan

The ATWILC1000-MR110PB module has/have received type certification and is required to be labeled with its own technical conformity mark and certification number as required to conform to the technical standards regulated by the Ministry of Internal Affairs and Communications (MIC) of Japan pursuant to the Radio Act of Japan.

Integration of this module into a final product does not require additional radio certification provided installation instructions are followed and no modifications of the module are allowed. Additional testing may be required:

- If the host product is subject to electrical appliance safety (for example, powered from an AC mains), the host product may require Product Safety Electrical Appliance and Material (PSE) testing. The integrator should contact their conformance laboratory to determine if this testing is required
- There is an voluntary Electromagnetic Compatibility (EMC) test for the host product administered by VCCI: www.vcci.jp/vcci_e/index.html

13.4.1 Labeling and User Information Requirements

The label on the final product which contains the ATWILC1000-MR110PB module must follow Japan marking requirements. The integrator of the module should refer to the labeling requirements for Japan available at the Ministry of Internal Affairs and Communications (MIC) website.

For the ATWILC1000-MR110PB module, due to a limited module size, the technical conformity logo and ID is displayed in the data sheet and/or packaging and cannot be displayed on the module label. The final product in which this module is being used must have a label referring to the type certified module inside:

13.4.2 Helpful Web Sites

- Ministry of Internal Affairs and Communications (MIC): www.tele.soumu.go.jp/e/index.htm.
- Association of Radio Industries and Businesses (ARIB): www.arib.or.jp/english/.

13.5 Korea

The ATWILC1000-MR110PB module has/have received certification of conformity in accordance with the Radio Waves Act. Integration of this module into a final product does not require additional radio certification provided installation instructions are followed and no modifications of the module are allowed.

13.5.1 Labeling and User Information Requirements

The label on the final product which contains the ATWILC1000-MR110PB module must follow KC marking requirements. The integrator of the module should refer to the labeling requirements for Korea available on the Korea Communications Commission (KCC) website.

For ATWILC1000-MR110PB, due to a limited module size, the KC mark and ID are displayed in the data sheet and/or packaging and cannot be displayed on the module label. The final product requires the KC mark and certificate number of the module:

13.5.2 Helpful Websites

- Korea Communications Commission (KCC): www.kcc.go.kr.
- National Radio Research Agency (RRA): rra.go.kr.

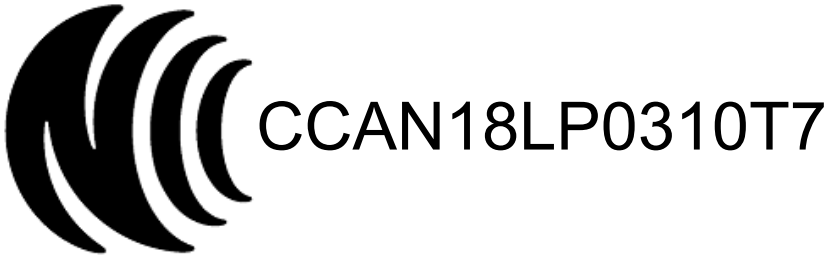
13.6 Taiwan

The ATWILC1000-MR110PB module has/have received compliance approval in accordance with the Telecommunications Act. Customers seeking to use the compliance approval in their product should contact Microchip Technology sales or distribution partners to obtain a Letter of Authority.

Integration of this module into a final product does not require additional radio certification provided installation instructions are followed and no modifications of the module are allowed.

13.6.1 Labeling and User Information Requirements

For the ATWILC1000-MR110PB module, due to the limited module size, the NCC mark and ID are displayed in the data sheet only and cannot be displayed on the module label:



The user's manual should contain following warning (for RF device) in traditional Chinese:

根據 NCC LP0002 低功率射頻器材技術規範_章節 3.8.2：

取得審驗證明之低功率射頻器材，非經核准，公司、商號或使用者均不得擅自變更頻率、加大功率或變更原設計之特性及功能。

低功率射頻器材之使用不得影響飛航安全及干擾合法通信；經發現有干擾現象時，應立即停用，並改善至無干擾時方得繼續使用。

前述合法通信，指依電信管理法規定作業之無線電通信。

低功率射頻器材須忍受合法通信或工業、科學及醫療用電波輻射性電機設備之干擾。

13.6.2 Helpful Web Sites

National Communications Commission (NCC): www.ncc.gov.tw

13.7 China

The ATWILC1000-MR110PB module has/have received certification of conformity in accordance with the China MIIT Notice 2014-01 of State Radio Regulation Committee (SRRC) certification scheme. Integration of this module into a final product does not require additional radio certification, provided installation instructions are followed and no modifications of the module are allowed. Refer to SRRC certificate available in ATWILC1000-MR110xB product page for expiry date.

13.7.1 Labeling and User Information Requirements

The ATWILC1000-MR110PB module is labeled with its own CMIIT ID as follows:

CMIIT ID: 2018DJ1313

When Host system is using an approved Full Modular Approval (FMA) radio: The host must bear a label containing the statement “This device contains SRRC approved Radio module CMIIT ID: 2018DJ2733”.

13.8 Other Regulatory Information

- For information about other countries' jurisdictions not covered here, refer to www.microchip.com/ATWILC1000 (available under Documents > Certifications).
- If the customer needs another regulatory jurisdiction certification or to recertify the module for other reasons, contact Microchip for the required utilities and documentation.

14. Reference Documentation

The following table provides the set of collateral documents to ease integration and device ramp.

Table 14-1. Reference documents

Title	Content
ATWILC1000/ATWILC3000 Wi-Fi Link Controller Linux® User Guide	This user guide describes how to run Wi-Fi on the ATWILC1000 SD card and how to run Wi-Fi/BLE on the ATWILC3000 Shield board on the SAMA5D4 Xplained Ultra running with the Linux kernel 4.9.
ATWILC1000B-MU Data sheet	Data sheet for the ATWILC1000 SmartConnect Wi-Fi component.
ATWILC1000/ATWILC3000 Devices Linux Porting Guide	This user guide describes how to port the ATWILC1000 and ATWILC3000 Linux drivers to another platform and contains all the required modifications for driver porting.
ATWILC1000/ATWILC3000 Baremetal Wi-Fi/BLE Link Controller Software Design Guide	This design guide helps the user in integrating ATWILC1000/ ATWILC3000 in the application using RTOS from Advanced Software Framework (ASF).
ATWILC1000B/ATWILC1000-MR110xB Errata	This document provides details on the anomalies identified in the ATWILC1000 family of devices.
ATWILC1000B – Deriving Application Gain Table Application Note	This application note describes the Wi-Fi gain table structure and procedure to derive the application gain table. This document provides further details on the steps to update the device with the gain table.

Note: For a complete listing of development support tools and documentation, visit http://www.microchip.com/wwwproducts/en/ATWILC1000 or refer to the customer support section for contacting the nearest Microchip field representative.

15. Document Revision History

Revision	Date	Section	Description
F	03/2025	Features	• Added compatibility for Wi-Fi® 6/7 2.4 GHz band • Removed Wi-Fi Direct Support • Updated Superior MAC throughput features
		Module Outline Drawings	Updated Package Drawings
		MAC Features	• Removed PCF and Traffic scheduling in IEEE 802.11e WMM QoS • Removed Transmission in Advanced IEEE 802.11n Features • Removed Independent Basic Service Set (IBSS) from features
		Description	Removed HCCA
		PHY Features	Editorial updates
		WLAN Subsystem	Updated content
E	06/2021	Document	Updated terminologies. For more details, see the following note.
		Ordering Information and Module Marking	Updated Figure 1-1 with packing information.
		Appendix A: Regulatory Approval	Updated Safety related standard in Europe
D	10/2020	Features	Updated this section
		Pinout and Package Information	Updated this section
		Electrical Specifications	• Updated VDDIO and VBAT specification in Recommended Operating Conditions • Added 4.3 DC Characteristics • Updated Table 4-5.
		Nonvolatile Memory (eFuse)	Updated this section with new information and Figure 6-1
		WLAN Subsystem	Added footnotes for Short GI feature
		External Interfaces	• Updated this section • Updated Figure 8-1
		Reference Design	Added Notes
		Design Consideration	• Updated ATWILC1000-MR110UB Placement and Routing Guidelines • Added Recommended External Antennas section • Updated following sections with standard text: – Reflow Profile Information – Module Assembly Considerations • Added Conformal Coating section
		Module Outline Drawings	Added tolerance details for the mechanical dimensions
		Appendix A: Regulatory Approval	• Added Gain Table for Individual Regulatory Region section • Updated United States and Canada with the details of antennas used for approval • Revamped Europe • Updated module label information in Korea • Updated expiry date information in China • Added product webpage link in Other Regulatory Information
		Reference Documentation	Updated

Document Revision History (continued)			
Revision	**Date**	**Section**	**Description**
C	05/2019	Ordering Information and Module Marking	Updated Regulatory Certification
		Appendix A: Regulatory Approval	• Updated with ATWILC1000-MR110PB information • Added European Compliance table • Added Japan Korea, Taiwan and China
B	10/2017	MAC Features	Editorial updates
A	08/2017	Document	• Updated from Atmel to Microchip template. • Assigned a new Microchip document number. Previous version is Atmel 42503 revision C. • ISBN number added. • Updated module reference to ATWILC1000-MR110xB throughout the document. • Removed reference to Bluetooth coexistence • Added WFA certification details • Updated block diagram Figure 2-1 • Updated pin description in Table 3-1 • Updated VDDIO absolute maximum voltage rating in Table 4-1 and added caution footnote • Added operating temperature to Table 4-2 • Moved Transmitter Performance, Receiver Performance and Timing Characteristics under Electrical Specifications • Updated description in Nonvolatile Memory (eFuse) • Revised the Transmitter Performance and Receiver Performance • Updated Reference Design • Added Design Consideration • Updated Reference Documentation

Note: *Microchip is aware that some terminologies used in the technical documents and existing software codes of this product are outdated and unsuitable. This document may use these new terminologies, which may or may not reflect on the source codes, software GUIs, and the documents referenced within this document. The following table shows the relevant terminology changes made in this document.*

Table 15-1. Terminology Related Changes

Old Terminology	New Terminology	Description
Master	Host	The following sections are updated with new terminology: • Pinout and Package Information • SPI Timing • SDIO Timing • I2C Timing • Interfacing with the Host Microcontroller • SPI Client Interface • SDIO Client Interface • I2C Client Interface
Slave	Client	

(Atmel) Rev C - 11/2016

Section	Changes
Document	• Updated the device pinout drawing Figure 3-1 to make it easier to read • Added section regarding PCBA coatings • Updated Marking diagram in Figure 1-1 • Revised values for Transmit Power and added notes in Table 4-5 • Added Pins and Agencies to Ordering Information in Table 1-1 • Added section ATWILC1000-MR110UB Placement and Routing Guidelines Types for ATWILC1000-MR110UB • Added Certification Notices • Added Appendix A: Regulatory Approval • Updated Description to indicate both the MR110PB and MR110UB are covered • Removed "With seamless roaming capabilities" from description • Revised features to only support SPI and SDIO hosts • Removed references to WAPI • Removed UART • Moved Solder Pad drawing to be with POD drawings as in #unique_41/unique_41_Connect_42_GUID-225A316F-B518-4A6E-98B1-B8B18BBDB52F • Minor edits

(Atmel) Rev B - 5/2016

Section	Changes
Document	• Revised POD drawings in Module Outline Drawings • Revised Footprint drawing in Module Outline Drawings • Removed Module schematics and BOM's • Added Reflow profile Reflow Profile Information • Updated SDIO timing content in SDIO Client Timing • Added footnotes to recommended operating ratings in Recommended Operating Conditions • Updated SPI timing content in SPI Client Timing

(Atmel) Rev A - 8/2015

Section	Changes
Document	Updated due to changes from ATWILC100A(42380D) to ATWILC1000B: • Updated power numbers and description, added high-power and low-power modes • Updated radio performance numbers • Fixed typos in SPI interface timing • Added hardware accelerators in feature list (security and checksum) • Increased instruction RAM size from 128KB to 160KB • Improved and corrected description of Coexistence interface • Miscellaneous minor updates and corrections

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ISBN: 979-8-3371-0703-5

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