
MCP3914 Rev. A Silicon Errata and Data Sheet Clarification

The MCP3914 parts you have received conform functionally to the Device Data Sheet (DS20005216A), except for the anomalies described in this document.

All of the issues discussed will be addressed in future revisions of the MCP3914 silicon.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.
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Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS20005216A):

None.

1. Module: ADC Conversion

The converter internal phases can be erroneously generated if there is a simultaneous occurrence of a master clock edge and a reset event (a RESETn pin rising edge, the last SCK rising edge of a write communication that generates an ADC reset and restart, as defined in [Section 6.6 Situations that Reset and Restart Active ADCs](#), or a Power-on Reset). This perturbation in the internal clock phase's generation can cause modulator instability and generate erroneous results, therefore, it is highly recommended these events are not synchronized.

Work around

A possible workaround of this issue is to freeze the master clock during all the above-detailed events (a RESETn pin rising edge, the last SCK rising edge of a write communication that generate an ADC reset and restart, as defined in [Section 6.6 Situations that Reset and Restart Active ADCs](#), or a Power-on Reset). In this case, the part will not exhibit any issues .

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (4/2015)

- Initial release of this document.

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