
Section 39. Op amp/Comparator

This section of the manual contains the following major topics:

39.1	Introduction	39-2
39.2	Op amp/Comparator Registers	39-4
39.3	Comparator Operation	39-15
39.4	Comparator operation in Power-Saving modes	39-21
39.5	Comparator Configuration.....	39-21
39.6	Comparator Interrupts.....	39-26
39.7	Op amp Operation	39-28
39.8	Op amp Configuration.....	39-29
39.9	Revision History	39-34

Note: This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all PIC32 devices.

Please consult the note at the beginning of the “Op amp/Comparator” chapter in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: <http://www.microchip.com>

39.1 INTRODUCTION

Certain PIC32 family devices implement up to eight Op amp/Comparator modules. Some modules may not implement an Op amp and such modules are referred to as stand-alone Comparator modules to distinguish from the standard type, which implements both a Comparator and an Op amp. When Op amps and Comparators are available on a device, they can be enabled independently of each other. The actual number of Op Amp/Comparator module instances vary with the device. In addition, each device implements at least one “Comparator-only” or “stand-alone” module.

The Op amps have both the inverting and non-inverting inputs available for access, as well as outputs to allow for connection of external gain/filtering feedback elements. Also, the output of the Op amps can be internally connected to the ADC module without another external pin for that purpose. In addition, the output of the Op amps can be connected to the Comparator inputs within the module or to the stand-alone Comparators. The Op amps can be disabled entirely when not used.

The Comparators also have both their inverting and non-inverting inputs accessible through device pins. The non-inverting input pins can be connected to an internally generated reference or to an external reference through a pin. The inverting inputs can be connected to up to four external pins or internally to output of the Op amps. The Comparator outputs can be entirely disabled from appearing on the output pins which relieves a pin for other uses. In addition, the outputs are re-mappable to different pins through the peripheral pin select module.

The stand-alone Comparator implements a 4 x 1 multiplexer at the inverting input to enable selection of the desired signal to compare against the non-inverting input. Up to three outputs of Op amps can be internally connected to the input of the stand-alone Comparator through the multiplexer.

Note: Refer to the “Op amp/Comparator” chapter in the specific device data sheet to determine the number of available Op amps/Comparators for your device.

The Op amp modules provide the user with the ability to amplify small signals to gains greater than eight.

The outputs of the Comparators can be further blanked/masked for programmable durations and/or digitally filtered. The digital filter has the capability to sample at different frequencies using various clock sources.

39.1.1 Features

The Comparator module includes the following features:

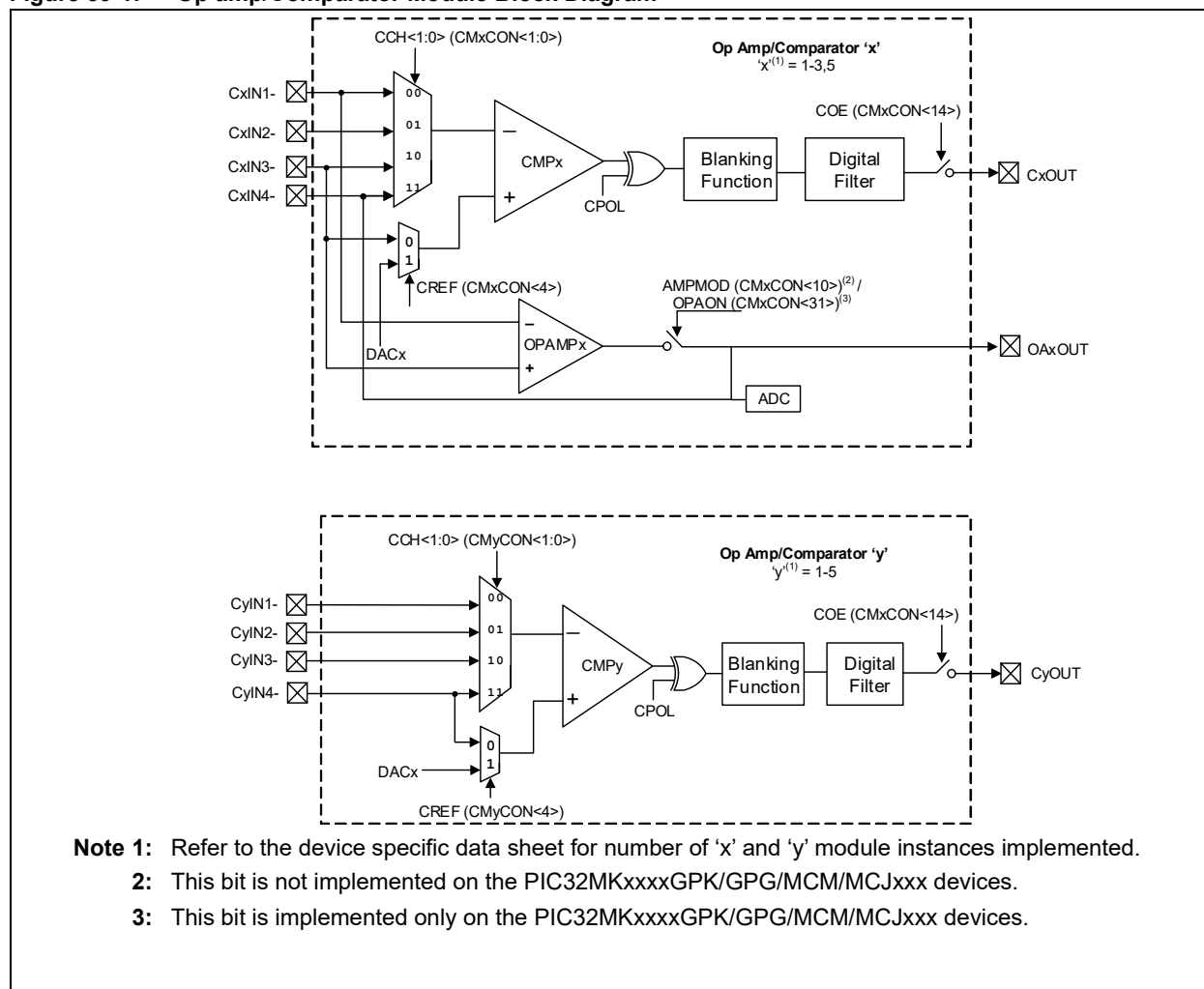
- External access to differential inputs
- Rail-to-Rail operation
- Built-in hysteresis
- Power-down mode for power savings
- Software selectable Comparator output polarity
- Software selectable edge for trigger/interrupt generation
- Outputs available on select reprogrammable pins (CxOUT)
- Blanking logic for masking undesired output state transition events
- Digital comparator output noise/debounce filters

The Op amp module includes the following features:

- Differential inputs
- Rail-to-Rail input voltage range
- Tri-stateable output

Figure 39-1 illustrates the Op amp/Comparator module options that are specified by the Special Function Register (SFR) control bits.

Figure 39-1: Op amp/Comparator Module Block Diagram



39.2 OP AMP/COMPARATOR REGISTERS

The following registers are available to the Op amp/Comparator module:

- **CMSTAT: Op amp/Comparator Status Register for PIC32MKxxxGPD/GPE/MCFxxx Devices**

The CMSTAT register provides configuration bits for control to disable or continue operation of all Op amp/Comparators in Idle mode. In normal operation mode, this register provides the individual status of all Comparator outputs and events in a single SFR, which are replicated here as read-only bits of their equivalents in the CMxCON<9:8>. In addition, it also enables selection of the Comparator reference from an external or internal reference source.

- **CMxCON: Op amp/Comparator Control Register for PIC32MKxxxGPK/MCM/GPG/MCJxxx Devices**

The CMxCON register allows the application program to enable, configure and interact with the individual Op amp/Comparators.

- **CMxMSKCON: Comparator Mask Control Register**

The CMxMSKCON register allows the application program to select sources for the input to the blanking function. It also allows the application program to specify the blank function logic.

Table 39-1 provides a brief summary of all related Op amp/Comparator module registers. Corresponding registers appear after the summary, followed by a detailed description of each register.

Table 39-1: Op amp/Comparator Special Function Register Summary for PIC32MKxxxGPD/GPE/MCFxxx devices

Register Name ⁽¹⁾	Bit Range	Bit 31/15	Bit 30/14	Bit 29/13	Bit 28/12	Bit 27/11	Bit 26/10	Bit 25/9	Bit 24/8	Bit 23/7	Bit 22/6	Bit 21/5	Bit 20/4	Bit 19/3	Bit 18/2	Bit 17/1	Bit 16/0
CMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	—	—	SIDL	—	—	—	—	—	—	—	—	C5OUT	C4OUT	C3OUT	C2OUT	C1OUT
CMxCON	31:24	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>		
	23:16	ON	COE	CPOL	—	OA0	AMPMOD	CEVT	COU	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	
CMxMSKCON	31:24	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>			
	23:16	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN

Legend: — = unimplemented, read as '0'.

Note 1: All registers have an associated Clear, Set, and Invert register at an offset of 0x4, 0x8, and 0xC bytes, respectively. These registers have the same name with CLR, SET, or INV appended to the end of the register name (for example, CMSTATCLR). Writing a '1' to any bit position in these registers will clear valid bits in the associated register. Reads from these registers should be ignored.

Table 39-2: Op amp/Comparator Special Function Register Summary for PIC32MKxxxGPK/MCM/GPG/MCJxxx Devices

Register Name ⁽¹⁾	Bit Range	Bit 31/15	Bit 30/14	Bit 29/13	Bit 28/12	Bit 27/11	Bit 26/10	Bit 25/9	Bit 24/8	Bit 23/7	Bit 22/6	Bit 21/5	Bit 20/4	Bit 19/3	Bit 18/2	Bit 17/1	Bit 16/0
CMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	—	—	SIDL	—	—	—	—	CVREFSEL	—	—	—	C5OUT	C4OUT	C3OUT	C2OUT	C1OUT
CMxCON	31:24	OPAON	ENPGA	—	HYSPOL	—	—	HYSSEL<1:0>		—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>		
	23:16	ON	COE	CPOL	OPLPWR	—	—	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	
CMxMSKCON	31:24	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>			
	23:16	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN

Legend: — = unimplemented, read as '0'.

Note 1: All registers have an associated Clear, Set, and Invert register at an offset of 0x4, 0x8, and 0xC bytes, respectively. These registers have the same name with CLR, SET, or INV appended to the end of the register name (for example, CMSTATCLR). Writing a '1' to any bit position in these registers will clear valid bits in the associated register. Reads from these registers should be ignored.

PIC32 Family Reference Manual

Register 39-1: CMSTAT: Op amp/Comparator Status Register for PIC32MKxxxxGPD/GPE/MCFxxx Devices

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	SIDL	—	—	—	—	—
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	C5OUT	C4OUT	C3OUT	C2OUT	C1OUT

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Discontinue operation of all Op amp/Comparators when device enters Idle mode

0 = Continue module operation in Idle mode

bit 12-5 **Unimplemented:** Read as '0'

bit 4-0 **C5OUT:C1OUT:** Op amp/Comparator 5 through Comparator 1 Output Status bit

When CPOL = 0:

1 = $V_{IN+} > V_{TH+}$

0 = $V_{IN+} < V_{TH-}$

When CPOL = 1:

1 = $V_{IN+} < V_{TH-}$

0 = $V_{IN+} > V_{TH+}$

Section 39. Op amp/Comparator

Register 39-2: CMSTAT: OP amp/Comparator Status Register for PIC32MKxxxxGPK/MCM/GPG/MCJxxx

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	C5EVT	C4EVT	C3EVT	C2EVT	C1EVT
15:8	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	SIDL	—	—	—	—	—
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	C5OUT	C4OUT	C3OUT	C2OUT	C1OUT

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20-16 **C5EVT:C1EVT:** Op amp/Comparator 5 through Comparator 1 Event Status bit

1 = Comparator event according to EVPOL<1:0> settings occurred. Future events/triggers and interrupts are disabled until the CEVT bit (CMxCON<9> for PIC32MKxxxxGPK/MCM/GPG/MCJxxx) is cleared by user software.

0 = Op amp/Comparator event did not occur

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop n Idle Mode bit

1 = Discontinue operation of all Op amp/Comparators when device enters Idle mode

0 = Continue module operation in Idle mode

bit 12-5 **Unimplemented:** Read as '0'

bit 4-0 **C5OUT:C1OUT:** Op amp/Comparator 5 through Comparator 1 Output Status bit

When CPOL = 0:

1 = $V_{IN+} > V_{TH+}$

0 = $V_{IN+} < V_{TH-}$

When CPOL = 1:

1 = $V_{IN+} < V_{TH-}$

0 = $V_{IN+} > V_{TH+}$

PIC32 Family Reference Manual

Register 39-3: CMxCON: Op amp/Comparator Control Register for PIC32MKxxxGPD/GPE/MCFxxx Devices

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	CFSEL<2:0> ⁽¹⁾			CFLTREN	CFDIV<2:0>		
15:8	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0
	ON	COE	CPOL	—	OA0	AMPMOD	CEVT	COOUT
7:0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-23 **Unimplemented:** Read as '0'

bit 22-20 **CFSEL<2:0>:** Comparator Output Filter Clock Source Select bits⁽¹⁾

bit 19 **CFLTREN:** Comparator Output Digital Filter Enable bit

1 = Digital Filters are enabled

0 = Digital Filters are disabled

bit 18-16 **CFDIV<2:0>:** Comparator Output Filter Clock Divide Select bits

111 = 1:128 Clock Divide

110 = 1:64 Clock Divide

101 = 1:32 Clock Divide

100 = 1:16 Clock Divide

011 = 1:8 Clock Divide

010 = 1:4 Clock Divide

001 = 1:2 Clock Divide

000 = 1:1 Clock Divide

bit 15 **ON:** Comparator Enable bit

1 = Comparator is enabled

0 = Comparator is disabled

bit 14 **COE:** Comparator Output Enable bit

1 = Comparator output is present on the CxOUT pin

0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit

1 = Comparator output is inverted

0 = Comparator output is not inverted

bit 12 **Unimplemented:** Read as '0'

bit 11 **OA0:** Op amp Output Enable bit

1 = Op amp output is present on the OAxOUT pin

0 = Op amp output is not present on the OAxOUT pin

bit 10 **AMPMOD:** Op amp Mode Enable bit

1 = Amplifier/Comparator operating in Dual mode (both Op amps and Comparators are enabled)

0 = Amplifier/Comparator operating in Comparator-only mode

- bit 9 **CEVT:** Comparator Event bit
1 = Comparator event according to the EVPOL<1:0> bit settings occurred
 Note: CEVT = 1 disables future events/triggers and interrupts until the bit is cleared by the user software.
0 = Comparator event did not occur
- bit 8 **COOUT:** Comparator Output bit
When CPOL = 0 (non-inverted polarity):
1 = $V_{IN+} > V_{TH+}$
0 = $V_{IN+} < V_{TH+}$
When
CPOL = 1 (inverted polarity):
1 = $V_{IN+} < V_{TH-}$
0 = $V_{IN+} > V_{TH-}$
- bit 7-6 **EVPOL<1:0>:** Trigger/Event Polarity Select bits
11 = Trigger/Event generated on any change of the comparator output
10 = Trigger/Event generated only on high-to-low transition of the polarity-selected comparator output
 If CPOL = 0 (non-inverted polarity):
 High-to-low transition of the comparator output
 If CPOL = 1 (inverted polarity):
 Low-to-high transition of the comparator output
01 = Trigger/Event generated only on low-to-high transition of the polarity-selected comparator output
00 = Trigger/Event generation is disabled
- bit 5 **Unimplemented:** Read as '0'
- bit 4 **CREF:** Op amp/Comparator Reference Select bit
1 = V_{IN+} input connects to internal DAC output voltage. Refer to the "Op amp/Comparator" chapter in the specific device data sheet to know the exact instance of the DAC peripheral available as a comparator reference.
0 = V_{IN+} input connects to CxIN1+ pin
- bit 3-2 **Unimplemented:** Read as '0'
- bit 1-0 **CCH<1:0>:** Comparator Channel Select bits
11 = CxIN4-
10 = CxIN3-
01 = CxIN2-
00 = CxIN1-
- Note 1:** Refer to the "Op amp/Comparator" chapter in the specific device data sheet for more information on the clock sources.

PIC32 Family Reference Manual

Register 39-4: CMxCON: Op amp/Comparator Control Register for PIC32MKxxxxGPK/MCM/GPG/MCJxxx Devices

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	OPAON	ENPGA	—	HYSPOL	—	—	HYSSEL<1:0>	
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	CFSEL<2:0> ⁽¹⁾			CFLTREN	CFDIV<2:0>		
15:8	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R-0
	ON	COE	CPOL	OPLPWR	—	—	CEVT	COUT
7:0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 31 **OPAON:** Op amp Enable bit
 1 = Op amp is enabled and connected to the pin
 0 = Op amp is disabled and the pin is released to other functions
- bit 30 **ENPGA:** Op amp Fixed Gain Enable bit
 1 = Op amp is operating in Fixed Gain 1X mode
 0 = Op amp is operating in Open Loop mode (default)
- bit 29 **Unimplemented:** Read as '0'
- bit 28 **HYSPOL:** Comparator Hysteresis Polarity Selection
 1 = Hysteresis on falling edge, rising edge is accurate
 0 = Hysteresis on rising edge, falling edge is accurate
- bit 27-26 **Unimplemented:** Read as '0'
- bit 25-24 **HYSSEL<1:0>:** Hysteresis Selection bits
 11 = Set highest hysteresis level (typical 45 mV)
 10 = Set medium hysteresis level (typical 30 mV)
 01 = Set lowest hysteresis level (typical 15 mV)
 00 = No hysteresis selected.
- Note:** These bits select the hysteresis of the analog comparator.
- bit 23 **Unimplemented:** Read as '0'
- bit 22-20 **CFSEL<2:0>:** Comparator Output Filter Clock Source Select bits⁽¹⁾
- bit 19 **CFLTREN:** Comparator Output Digital Filter Enable bit
 1 = Digital Filters are enabled
 0 = Digital Filters are disabled
- bit 18-16 **CFDIV<2:0>:** Comparator Output Filter Clock Divide Select bits
 111 = 1:128 Clock Divide
 110 = 1:64 Clock Divide
 101 = 1:32 Clock Divide
 100 = 1:16 Clock Divide
 011 = 1:8 Clock Divide
 010 = 1:4 Clock Divide
 001 = 1:2 Clock Divide
 000 = 1:1 Clock Divide

Note 1: For additional information on clock sources, refer to the chapter “Op amp/Comparator” in the device-specific data sheet.

Register 39-4: CMxCON: Op amp/Comparator Control Register for PIC32MKxxxGPK/MCM/GPG/MCJxxx Devices (Continued)

bit 15	ON: Comparator Enable bit 1 = Comparator is enabled 0 = Comparator is disabled
bit 14	COE: Comparator Output Enable bit 1 = Comparator output is present on the CxOUT pin 0 = Comparator output is internal only
bit 13	CPOL: Comparator Output Polarity Select bit 1 = Comparator output is inverted 0 = Comparator output is not inverted
bit 12	OPLPWR: Op amp/Comparator Low-Power Mode Select bit 1 = Comparator operates in low-power/low-speed mode 0 = Comparator operates in standard power mode
bit 11-10	Unimplemented: Read as '0'
bit 9	CEVT: Comparator Event bit 1 = Comparator event according to the EVPOL<1:0> bit settings occurred Note: CEVT = 1 disables future events/triggers and interrupts until the bit is cleared by the user software. 0 = Comparator event did not occur
bit 8	COUT: Comparator Output bit <u>When CPOL = 0 (non-inverted polarity):</u> 1 = $V_{IN+} > V_{TH+}$ 0 = $V_{IN+} < V_{TH-}$ <u>When CPOL = 1 (inverted polarity):</u> 1 = $V_{IN+} < V_{TH-}$ 0 = $V_{IN+} > V_{TH+}$
bit 7-6	EVPOL<1:0>: Trigger/Event Polarity Select bits 11 = Trigger/Event generated on any change of the comparator output 10 = Trigger/Event generated only on high-to-low transition of the polarity-selected comparator output <u>If CPOL = 0 (non-inverted polarity):</u> High-to-low transition of the comparator output <u>If CPOL = 1 (inverted polarity):</u> Low-to-high transition of the comparator output 01 = Trigger/Event generated only on low-to-high transition of the polarity-selected comparator output <u>If CPOL = 0 (non-inverted polarity):</u> Low-to-high transition of the comparator output <u>If CPOL = 1 (inverted polarity):</u> High-to-low transition of the comparator output 00 = Trigger/Event generation is disabled
bit 5	Unimplemented: Read as '0'
bit 4	CREF: Op amp/Comparator Reference Select bit 1 = V_{IN+} input connects to internal DAC output voltage. Refer to the chapter "Op amp/Comparator" in the specific device data sheet to know the instance of the DAC peripherals available as a comparator reference. 0 = V_{IN+} input connects to CxIN1+ pin
bit 3-2	Unimplemented: Read as '0'

Note 1: For additional information on clock sources, refer to the chapter "Op amp/Comparator" in the device-specific data sheet.

Register 39-4: CMxCON: Op amp/Comparator Control Register for PIC32MKxxxGPK/MCM/GPG/MCJxxx Devices (Continued)

bit 1-0 **CCH<1:0>**: Comparator Channel Select bits
 11 = CxIN4-
 10 = CxIN3-
 01 = CxIN2-
 00 = CxIN1-

Note 1: For additional information on clock sources, refer to the chapter “Op amp/Comparator” in the device-specific data sheet.

Section 39. Op amp/Comparator

Register 39-5: CMxMSKCON: Comparator Mask Control Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	SELSRCC<3:0> ⁽¹⁾			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SELSRCB<3:0> ⁽¹⁾				SELSRCA<3:0> ⁽¹⁾			
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27-24 **SELSRCC<3:0>:** Mask C Input Select bits⁽¹⁾

bit 23-20 **SELSRCB<3:0>:** Mask B Input Select bits⁽¹⁾

bit 19-16 **SELSRCA<3:0>:** Mask A Input Select bits⁽¹⁾

bit 15 **HLMS:** High or Low Level Masking Select bit

1 = The comparator deasserted state is 1, and the masking (blanking) function will prevent any asserted ('0') comparator signal from propagating

0 = The comparator deasserted state is 0, and the masking (blanking) function will prevent any asserted ('1') comparator signal from propagating

bit 14 **Unimplemented:** Read as '0'

bit 13 **OCEN:** OR Gate "C" Input Enable bit

1 = "C" input enabled as input to OR gate

0 = "C" input disabled as input to OR gate

bit 12 **OCNEN:** OR Gate "C" Input Inverted Enable bit

1 = "C" input (inverted) enabled as input to OR gate

0 = "C" input (inverted) disabled as input to OR gate

bit 11 **OBEN:** OR Gate "B" Input Enable bit

1 = "B" input enabled as input to OR gate

0 = "B" input disabled as input to OR gate

bit 10 **OBNEN:** OR Gate "B" Input Inverted Enable bit

1 = "B" input (inverted) enabled as input to OR gate

0 = "B" input (inverted) disabled as input to OR gate

bit 9 **OAEN:** OR Gate "A" Input Enable bit

1 = "A" input enabled as input to OR gate

0 = "A" input disabled as input to OR gate

bit 8 **OANEN:** OR Gate "A" Input Inverted Enable bit

1 = "A" input (inverted) enabled as input to OR gate

0 = "A" input (inverted) disabled as input to OR gate

bit 7 **NAGS:** Negative AND Gate Output Select bit

1 = The negative (inverted) output of the AND gate to the OR gate is enabled

0 = The negative (inverted) output of the AND gate to the OR gate is disabled

Note 1: Refer to the "Op amp/Comparator" chapter in the specific device data sheet for the mask values.

PIC32 Family Reference Manual

Register 39-5: CMxMSKCON: Comparator Mask Control Register (Continued)

bit 6	PAGS: Positive AND Gate Output Select bit 1 = The positive output of the AND gate to the OR gate is enabled 0 = The positive output of the AND gate to the OR gate is disabled
bit 5	ACEN: AND Gate “C” Input Enable bit 1 = “C” input enabled as input to AND gate 0 = “C” input disabled as input to AND gate
bit 4	ACNEN: AND Gate “C” Inverted Input Enable bit 1 = “C” input (inverted) enabled as input to AND gate 0 = “C” input (inverted) disabled as input to AND gate
bit 3	ABEN: AND Gate “B” Input Enable bit 1 = “B” input enabled as input to AND gate 0 = “B” input disabled as input to AND gate
bit 2	ABNEN: AND Gate “B” Inverted Input Enable bit 1 = “B” input (inverted) enabled as input to AND gate 0 = “B” input (inverted) disabled as input to AND gate
bit 1	AAEN: AND Gate “A” Input Enable bit 1 = “A” input enabled as input to AND gate 0 = “A” input disabled as input to AND gate
bit 0	AAEN: AND Gate “A” Inverted Input Enable bit 1 = “A” input (inverted) enabled as input to AND gate 0 = “A” input (inverted) disabled as input to AND gate

Note 1: Refer to the “Op amp/Comparator” chapter in the specific device data sheet for the mask values.

39.3 COMPARATOR OPERATION

The operation of a typical Op amp/Comparator and the relationship between the analog input levels and the digital output are illustrated in Figure 39-2. Depending on the comparator operating mode, the monitored analog signal is compared to either an external voltage reference or internal voltage reference. Each of the comparators can be configured to use the same or different reference sources. For example, one comparator can use an external reference while the others can use the internal reference. For more information on the Op amp/comparator voltage reference, refer to **Section 20. “Comparator Voltage Reference”** (DS60001109) of the “PIC32 Family Reference Manual”.

In Figure 39-2, the external reference V_{IN-} is a fixed voltage. The analog signal that exists at V_{IN+} is compared to the reference signal at V_{IN-} , and the digital output of the comparator is created by the difference between the two signals. When $V_{IN+} < V_{TH-}$, the output of the comparator is a digital low level. When V_{IN+} is greater than V_{TH+} , the output of the comparator is a digital high level. The polarity of the comparator output can be inverted such that it is a digital low level when $V_{IN+} > V_{IN-}$.

Figure 39-2: Comparator Configuration for Devices with Symmetrical Hysteresis - V_{HYST}

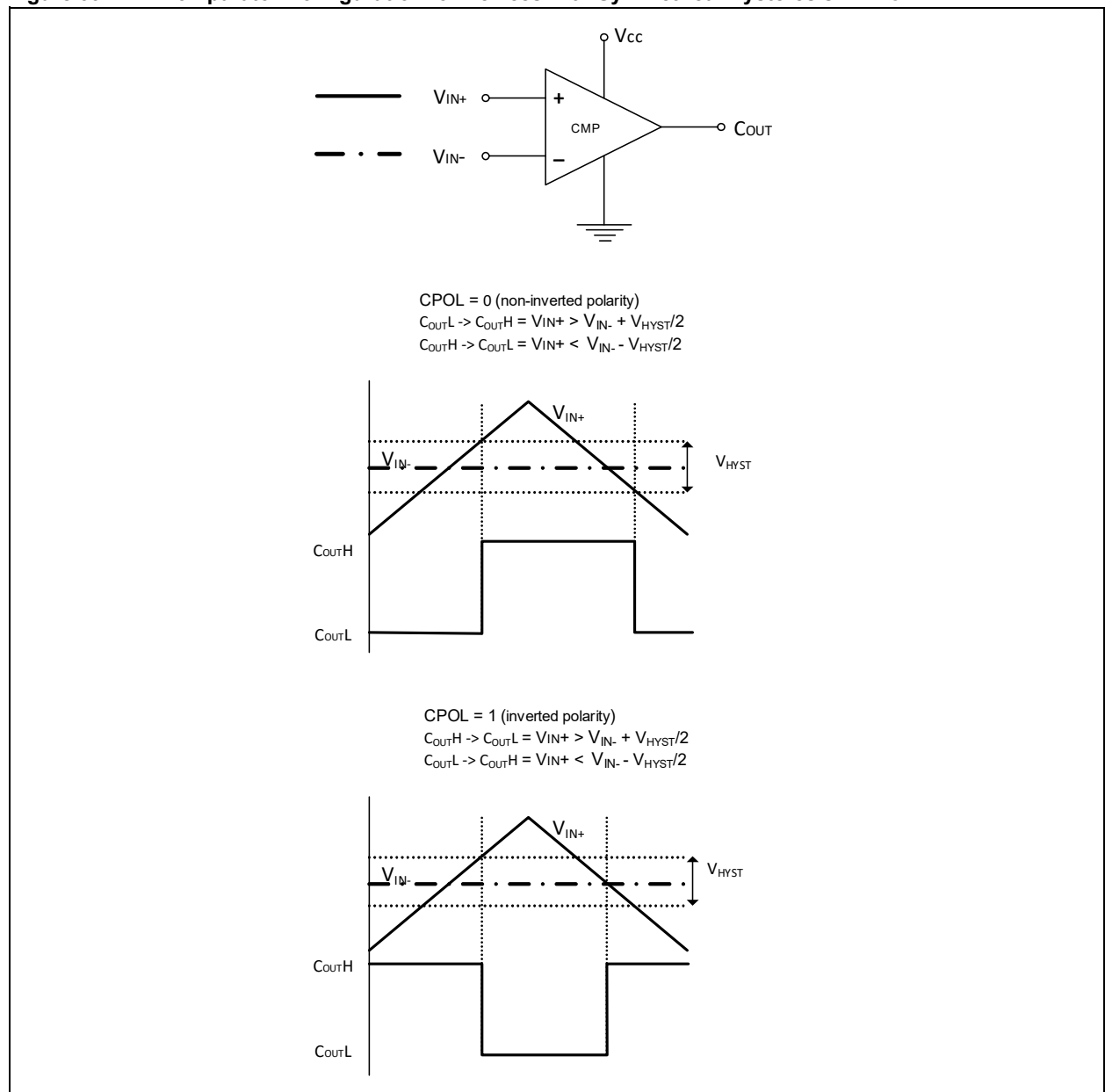
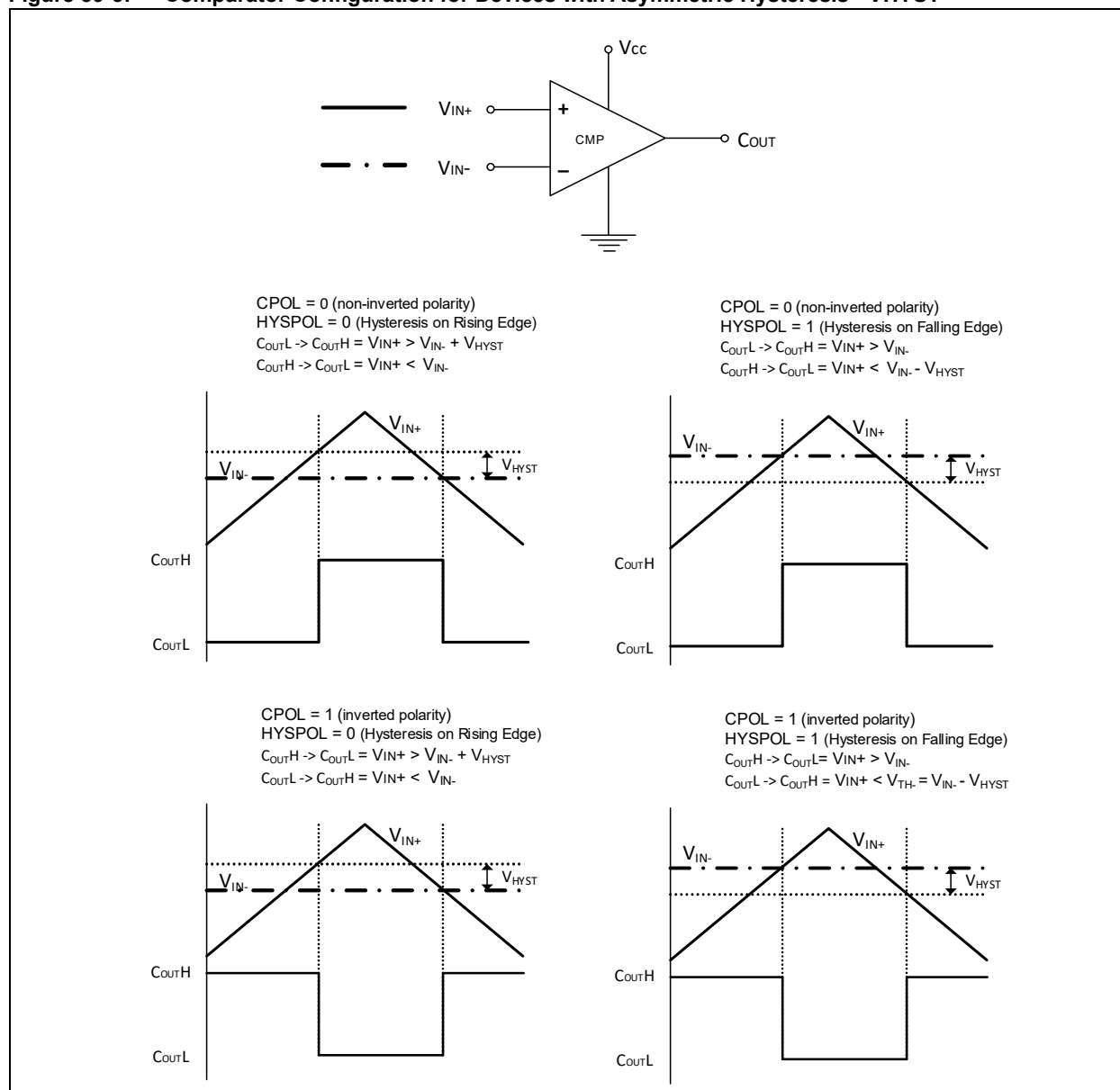


Figure 39-3: Comparator Configuration for Devices with Asymmetric Hysteresis - VHYST



Note: Figure 39-3 is applicable only to the PIC32MKxxxxGPK/GPG/MCM/MCJxxx devices.

39.3.1 Comparator Output to Device Pin

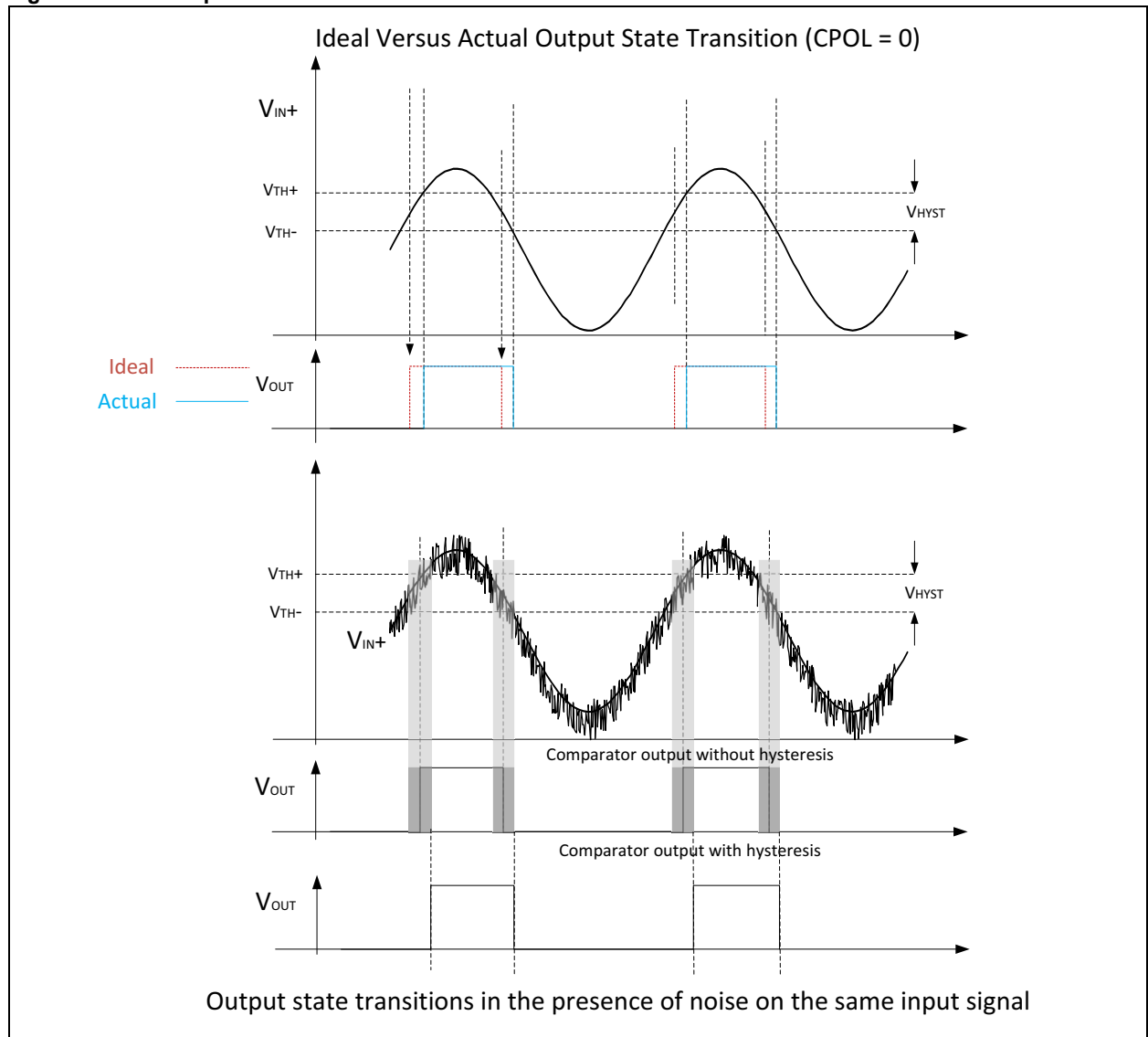
The Comparator outputs can be made available for external connections through the Peripheral Pin Select (PPS) function as a remappable output (CxOUT). The associated TRIS bit for the output pin must be configured as an output.

The comparator output can also be configured as a push-pull or open-drain/collector type output through the associated ODC bit for the output pin. When outputs are open-drain type, the output from two or more Comparators can be pulled up to VDD in a wired “OR” configuration. Care should be taken at start-up and while changing the drive configuration to prevent inadvertent mutual shorts/current spikes between the outputs when they could be momentarily in Push-Pull mode.

A certain amount of hysteresis is always desirable to prevent multiple transitions/switchings of the output when difference of V_{IN+} and V_{IN-} is small. Any noise in the system will result in unstable output in the absence of built-in hysteresis.

Refer to the AC characteristics in the “**Electrical Characteristics**” chapter of the specific device data sheet for the hysteresis value. Figure 39-4 shows the output with shifted transitions instances due to hysteresis from the ideal for a noise-free input signal. In the same figure, the Comparator output is shown for noisy input. The figure highlights the role of hysteresis in removing jitter from the Comparator output for a noisy input signal.

Figure 39-4: Output State Transitions

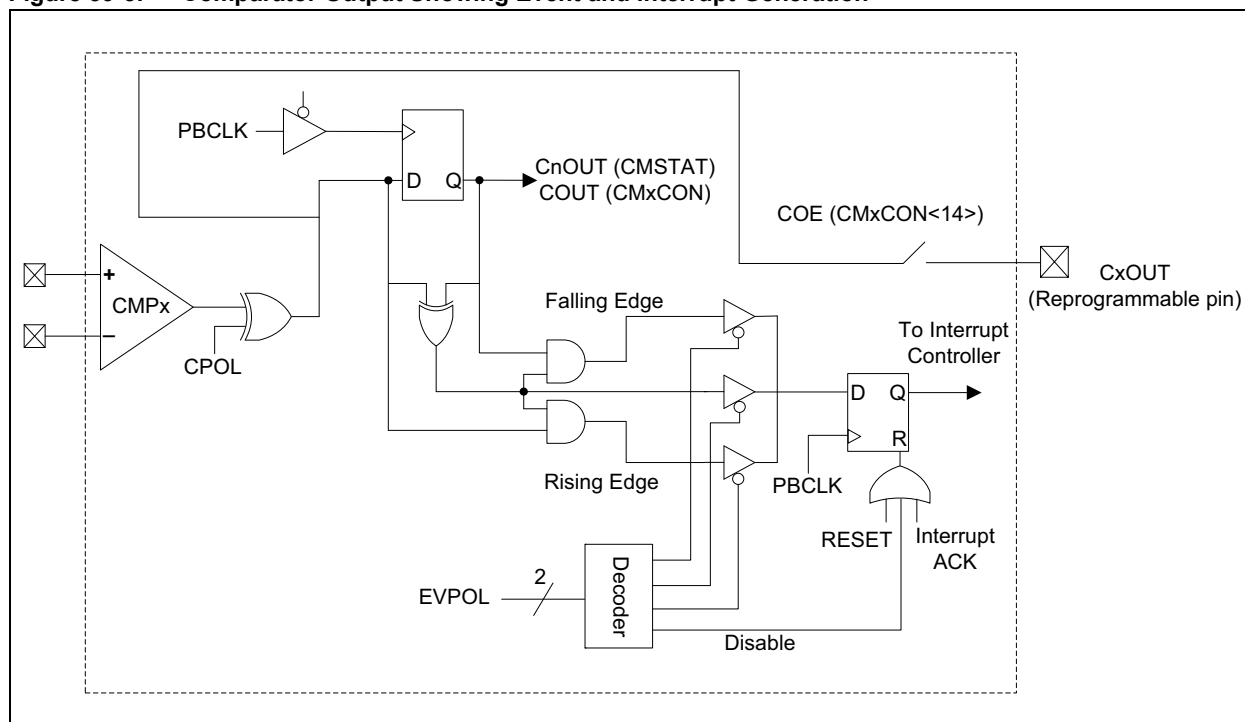


39.3.2 Comparator Internal Output

The polarity corrected Comparator output is always available internally as a read-only status by accessing the COUT bit in the CMxCON register. The CMSTAT register also reflects the COUT of each implemented comparator (maximum of eight) in the CMSTAT<7:0> bits. These bits are therefore also read-only and a convenience that facilitates access to outputs of all comparators in one access.

There are two common methods used to detect a change in the comparator output, software polling and interrupt generation.

Figure 39-5: Comparator Output Showing Event and Interrupt Generation



39.3.2.1 SOFTWARE POLLING METHOD

Software polling of COUT is performed by periodically reading the COUT bit. This allows the output to be read at desired time intervals; however, a change in the Comparator output is not detected until the next read of the COUT bit. If the input signal changes at a rate faster than the polling, a brief change in output may not be detected. Therefore, the polling rate will have a bearing on the perceived response time of the output.

39.3.2.2 INTERRUPT GENERATION METHOD

Interrupt generation is the other method for detecting a change in the Comparator output. The Comparator module can be configured to generate an interrupt when the COUT bit changes.

An interrupt will be generated when the Comparator's output changes (subject to the interrupt priorities). This method responds more rapidly to changes than the software polling method; however, rapidly changing signals will cause an equally large number of interrupts. This can cause interrupt loading and potentially undetected interrupts due to new interrupts being generated while the previous interrupt is still being serviced or even before the interrupt can be serviced. If the input signal changes rapidly, reading the COUT bit in the Interrupt Service Routine (ISR) may yield a different result than the one that generated the Interrupt. This is due to the COUT bit representing the value of the comparator output when the bit was read and not the value that caused the interrupt. Refer to [39.6 "Comparator Interrupts"](#) for more information.

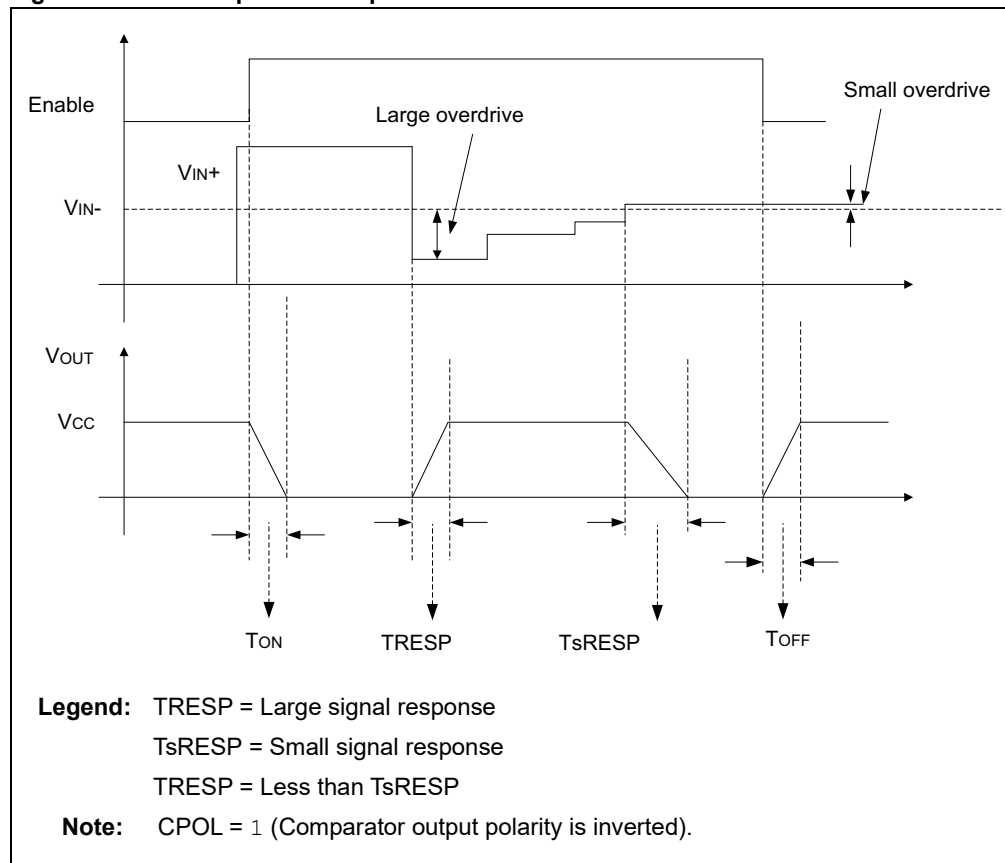
39.3.3 Comparator Response Times

Response time is the minimum amount of time that elapses from the moment a change is made in the input voltage of a Comparator to the moment the output reflects the new level. If the internal reference is changed, the maximum delay of the internal voltage reference must also be considered when using the Comparator outputs. Otherwise, the maximum delay of the Comparators should be used. For more information, refer to the DC characteristics in the “**Electrical Characteristics**” chapter of the specific device data sheet.

The Comparator response times for large and small signals is different. Small signal responses are always longer due to finite values of the amplifier gain.

Figure 39-6 shows the different response times.

Figure 39-6: Comparator Response Times



39.3.4 Comparator Hysteresis

39.3.4.1 COMPARATOR HYSTERESIS CONTROL

A hysteresis selection capability is provided on PIC32MKxxxGPK/GPG/MCM/MCJxxx devices. On these devices, the hysteresis type can be either positive or negative.

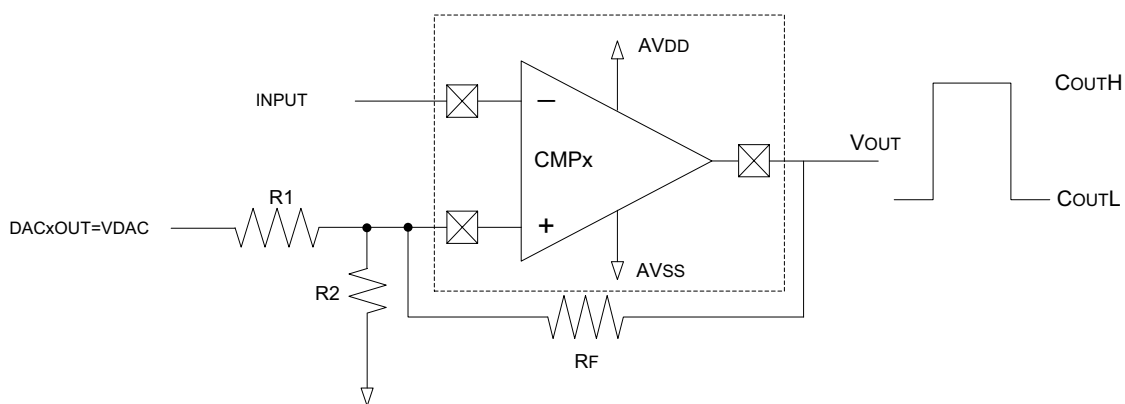
On devices with no hysteresis selection capability, the comparators have a built-in default hysteresis. Refer to the DC characteristics in the “**Electrical Characteristics**” chapter of the specific device data sheet to determine the actual default values.

39.3.4.2 EXTERNAL HYSTERESIS

The built-in hysteresis needs no external configuration. Any external hysteresis adds to the built-in default hysteresis. If applications require additional hysteresis, traditional methods of creating hysteresis with positive feedback loops using external resistors can be implemented. This requires CxOUT to be brought out to a pin as described in [39.3.1 “Comparator Output to Device Pin”](#). The output drive should be set to Push-pull mode preferably for symmetric hysteresis about the reference point. The following method can be used to add hysteresis through external configuration.

[Figure 39-7](#) shows a circuit configuration for adding external hysteresis. An on-chip DAC output is used to generate the reference voltage. The output of the Comparator may not swing from Rail-to-Rail due to loading effects, which must be considered for a precise hysteresis.

Figure 39-7: Comparator Configuration for Additional Hysteresis



$$V_{TH} * (1 / R1 + 1 / R2 + 1 / R_F) = V_{DAC} / R1 + C_{OUTH} / R_F$$

$$V_{TL} * (1 / R1 + 1 / R2 + 1 / R_F) = V_{DAC} / R1 + C_{OUTL} / R_F$$

$$\text{Total hysteresis} = (V_{TH} - V_{TL}) + 10 \text{ millivolts}$$

39.4 COMPARATOR OPERATION IN POWER-SAVING MODES

The Op amp/Comparator module supports the following modes of low-power operation:

- Sleep mode
- Idle mode

39.4.1 Sleep mode

In this mode, all clocks to the module are disabled; however, event/trigger and interrupt generation will still occur for any enabled comparator. The event/trigger and associated interrupt will be asynchronously asserted, and synchronously deasserted after exiting Sleep mode.

39.4.2 Idle mode

In this mode, the CPU clocks are disabled, but the peripheral clocks are still active. The module will continue to run normally in Idle mode as long as the SIDL bit = 0. If SIDL = 1, the module will be completely disabled in Idle mode, without any ability to generate events/triggers or interrupts.

39.5 COMPARATOR CONFIGURATION

Each of the comparators in the Op amp/Comparator module are configured independently by various control bits in the following registers:

- **Register 39-1: “CMSTAT: Op amp/Comparator Status Register for PIC32MKxxxGPD/GPE/MCFxxx Devices”**
- **Register 39-4: “CMxCON: Op amp/Comparator Control Register for PIC32MKxxxGPK/MCM/GPG/MCJxxx Devices”**
- **Register 39-5: “CMxMSKCON: Comparator Mask Control Register”**

The exact number of Op amp/Comparator modules implemented is device-specific. The stand-alone Comparator module can be internally connected to up to three Op amp outputs from other modules.

The voltage reference source to each Comparator can be either external or internal. Refer to the specific device data sheet for the availability and type of internal reference generator.

39.5.1 Comparator Enable/Disable

The comparator may be enabled or disabled using the corresponding Op amp/Comparator Enable bit, ON, in the Op amp/Comparator Control register (CMxCON<15>). When the comparator is disabled, the corresponding trigger and interrupt generation is disabled.

It is recommended to first configure the CMxCON register with all bits to the desired value, and then set the ON bit. When not used, the Comparator should be disabled expressly by writing a '0' to the ON bit.

39.5.2 Comparator Output Blanking Function

In many power control and motor control applications, there are periods of time in which the inputs to the analog comparator are known to be invalid. The blanking (masking) function enables the user to ignore the comparator output during predefined periods of time. In this document, the terms “masking” and “blanking” are used interchangeably.

Figure 39-8 illustrates a block diagram of the comparator blanking circuitry. A blanking circuit is associated with each comparator.

Each comparator's blanking function consists of the following user selectable inputs:

- Mask A Input (MAI)
- Mask B Input (MBI)
- Mask C Input (MCI)

The MAI, MBI and MCI signal sources are selected through the Mask A Input Select bits (SELSRCA<3:0>), Mask B Input Select bits (SELSRCB<3:0>), and Mask C Input Select bits (SELSRCC<3:0>) in the Comparator Masking Control registers, CMxMSKCON.

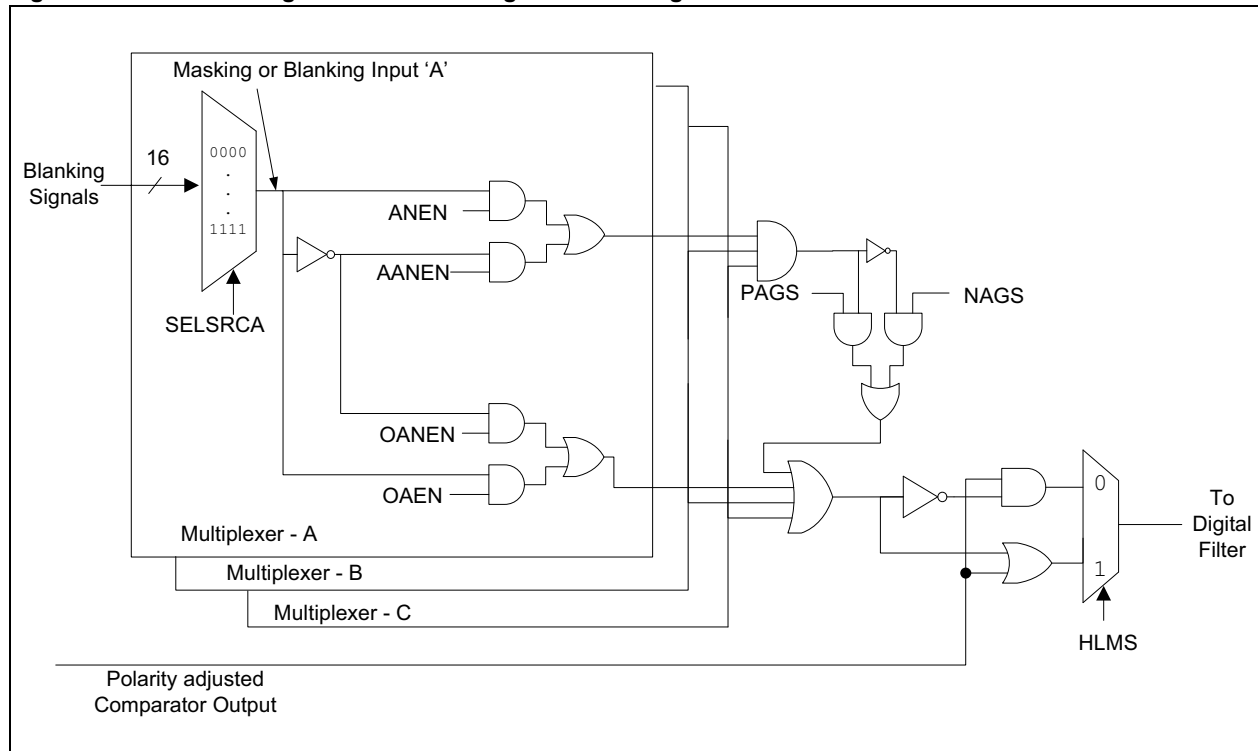
The MAI, MBI and MCI signals are passed to AND-OR function blocks, which enables the user to construct a blanking (masking) signal from these inputs. The blanking (masking) function is disabled following a system Reset.

The High or Low Level Masking Select bit, HLMS (CMxMSKCON<15>), configures the masking logic to operate, depending on the default (deasserted) state of the comparators. The HLMS selection is dependent on the polarity of the comparator output (CPOL).

If the Comparator output is configured for positive logic (i.e., to output logic '1' when +VIN is greater than -VIN), the HLMS bit should be set to '0' so that the blanking function, when active, will prevent a logic '1' of the Comparator output from propagating to the digital filter or output pin.

If the Comparator output is configured for negative logic (i.e., to output logic '0' when +VIN is greater than -VIN), the HLMS bit should be set to '1' so that the blanking function, when active, will prevent a logic '0' of the comparator output from propagating to the digital filter or output pin.

Figure 39-8: User Programmable Blanking Function Diagram



39.5.3 Digital Output Filter

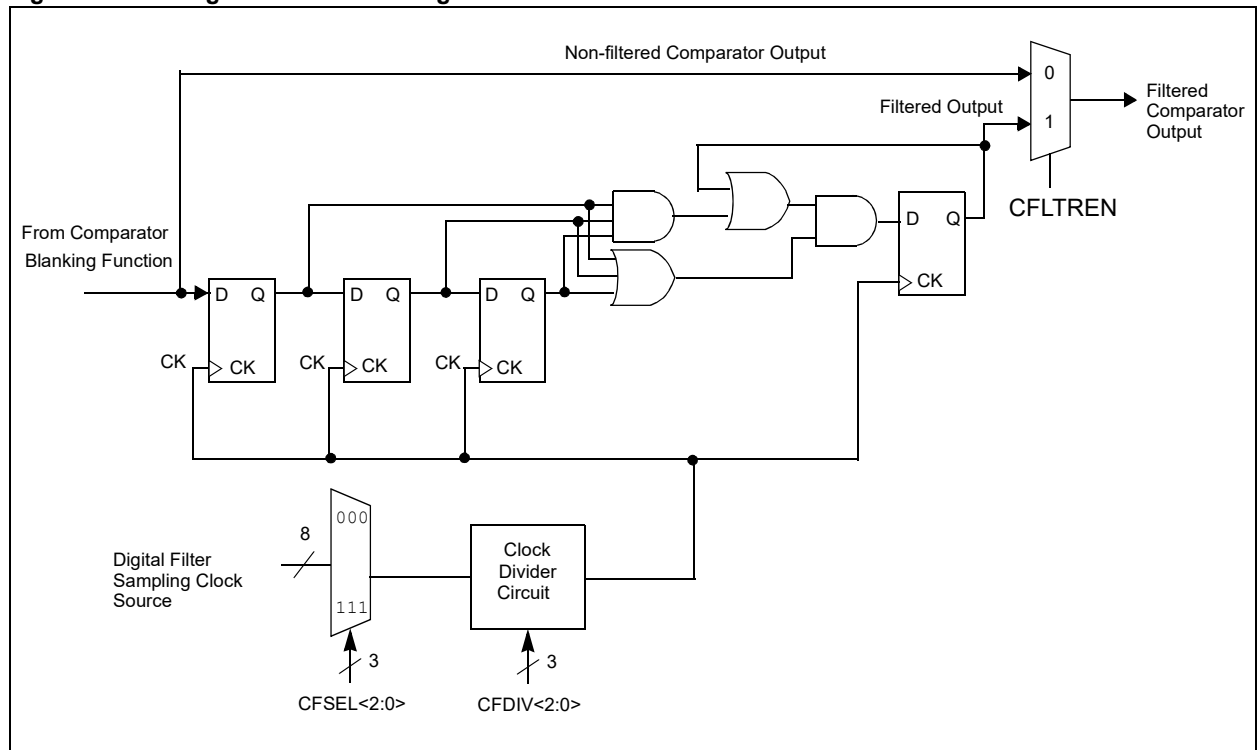
In many motor and power control applications, the comparator input signals can be corrupted by the large electromagnetic fields generated by the associated external switching power transistors. Corruption of the analog input signals to the comparator can cause unwanted comparator output transitions. The programmable digital output filter can minimize the effects of input signal corruption.

The digital filter requires three consecutive input samples to be similar before the output of the filter can change state. Assuming the current state is '0', a string of inputs such as '001010110111' will only yield an output state of '1' at the end of the example sequence after the three consecutive '1's. Similarly, a sequence of three consecutive '0's are required before the output will change to zero state.

Since it takes three samples of similar consecutive states for the filter to update the output state, the selected digital filter clock frequency must be three or more times greater than the maximum desired comparator response time. Response time requirements are application-specific and vary greatly with the magnitude of overdrive (see Figure 39-6). Refer to the Comparator output response times (TRESP) in the “**Electrical Characteristics**” chapter of the specific device data sheet for the selection of the filter clock source and clock scaler that is most appropriate for the application.

As illustrated in Figure 39-9, the digital filter is enabled by setting the Comparator Output Digital Filter Enable bit, CFLTREN (CMxCON<19>). The Comparator Output Filter Clock Divide Select bits, CFDIV<2:0> (CMxCON<18:16>), select the clock divider ratio for the clock signal input to the digital filter block. The Comparator Output Filter Clock Source Select bits, CFSEL<2:0> (CMxCON<22:20>), select the desired clock source for the digital filter. The digital filter is disabled (bypassed) following a system Reset.

Figure 39-9: Digital Filter Block Diagram



39.5.4 Comparator Polarity Selection

To provide maximum flexibility, the output of the Comparator may be inverted using the Comparator Output Polarity Select bit, CPOL (CMxCON<13>). This functionality is identical to reversing the inverting and non-inverting inputs of the comparator for a particular mode.

The CPOL bit should be changed only when the comparator is disabled by setting the Comparator Output Enable bit, ON (CMxCON<15>), to '0'. Internal logic will prevent the generation of any corresponding triggers or interrupts when ON = 0. The logic allows both the ON bit and the CPOL bit to be set with a single register write.

TABLE 39-3: PIN CONTROL ENCODING

CPOL	Inputs	COUT
0	$V_{IN+} < V_{IN-}$	0
0	$V_{IN+} > V_{IN-}$	1
1	$V_{IN+} < V_{IN-}$	1
1	$V_{IN+} > V_{IN-}$	0

39.5.5 Event Polarity Selection

In addition to a programmable comparator output polarity, the Op amp/Comparator module also allows software selection for trigger/interrupt edge polarity through the Trigger/Event/Interrupt Polarity Select bits, EVPOL<1:0>, in the corresponding CMxCON register. This feature allows independent control of the comparator output, as seen on any external pins, and the trigger/interrupt generation. Refer to [Figure 39-5](#) for the polarity and interrupt generation block diagram.

Note: The corresponding comparator must be enabled (ON = 1) for the specific trigger/interrupt generation to be enabled.

Table 39-4: Event Polarity and Generation Conditions

EVPOL<1:0>	(VIN+ – VIN-) Transition > VTH	Comparator Output Level	CxOUT		Event Generated
			CPOL = 0	CPOL = 1	
11	Positive	High	High	Low	Yes
11	Negative	Low	Low	High	Yes
10	Positive	High	High	Low	No
10	Negative	Low	Low	High	Yes
01	Positive	High	High	Low	Yes
01	Negative	Low	Low	High	No
00	Positive	High	High	Low	No
00	Negative	Low	Low	High	No

39.5.6 Comparator Input Selection

The channel selection varies for the Comparator-only sub-module and the Op amp/Comparator sub-module. Refer to [Figure 39-1](#) for the various channel and reference input options that are available for the different Comparators.

The analog channel number associated with the Comparator inputs is device-specific.

39.5.6.1 COMPARATOR REFERENCE INPUT SELECTION

The input to the non-inverting input of the Comparator, also known as the reference input, can be selected by the value of the CREF bit (CMxCON<4>). Each comparator has an input pin, CxIN1, which can be used to supply an external reference voltage. CMxCON<4> (CREF) = 0 connects the CxIN1 pin to the Comparator. When CMxCON<4> (CREF) is '1', the internal 12-bit high-speed DAC connects to the Comparator. Refer to the “[Section 45. Control Digital-to-Analog Converter](#)” (DS60001327) for more information on reference generation using on-chip DACs.

39.5.6.2 COMPARATOR CHANNEL SELECTION

The input to the inverting input of the comparator, also known as the channel input, can be selected by the Comparator Channel Selection bits, CCH<1:0> (CMxCON<1:0>). Each Comparator can connect to one of three external pins or internally connect to the output (OAxOUT) of the associated Op amp.

The Comparator-only sub-module internally accepts the outputs of the Op amps of other sub-modules as inputs for the same CCH<1:0> selections.

Refer to the module block diagram in [Figure 39-1](#) for the various channel and reference input options available for the different comparators.

39.5.7 Status Register

To provide an overview of all comparator results, the Comparator Output bit, COUT (CMxCON<8>), is replicated as a status bit in the Op amp/Comparator Voltage Reference Status register, CMSTAT.

These bits are read-only, and can be modified only by manipulating the corresponding CMxCON register or the comparator input signals.

39.6 COMPARATOR INTERRUPTS

Note: Refer to the “Interrupts” chapter in the specific device data sheet for the exact bit position and interrupt register.

Each of the available comparators has a dedicated interrupt flag bit, CMPxIF (IFSx), and a corresponding interrupt enable/mask bit, CMPxIE (IECx). These bits are used to determine the source of an interrupt and to enable or disable an individual interrupt source. The priority level of each of the channels can also be set independently of the other channels.

The CMPxIF bit is set when the CMPx channel detects a predefined match condition that is defined as an event using the EVPOL<1:0> bits (CMxCON<7:6>). The CMPxIF bit will then be set without regard to the state of the corresponding CMPxIE bit. The CMPxIF bit can be polled by software if desired.

If the interrupt is enabled (i.e., CMPxIE = 1), the CMPxIF interrupt flag must be cleared in software prior to exiting the ISR.

For devices, where the CEVT bit (CMxCON<9>) is writable, a simulated interrupt can be software initiated by writing a ‘1’ to the CEVT bit. Refer to the specific device data sheet to determine whether the CEVT bit is writable.

Note 1: The CMPxIF bit is a device-specific bit. Refer to the “Interrupts” chapter in the specific device data sheet for more information.

The CMPxIE (IECx) bit controls the interrupt generation. If the CMPxIE bit is set, the CPU will be interrupted (subject to the priority and sub-priority as outlined in the following paragraphs). It is the responsibility of the user application software routine that services a particular interrupt, to clear the CMPxIF interrupt flag bit whenever a Comparator interrupt event occurs before exiting the ISR.

The priority of each comparator channel can be set independently through the CMPxIP<2:0> bits (IPCx). This priority defines the priority group to which the interrupt source will be assigned. The priority groups range from a value of 7 (the highest priority), to a value of 0 (which does not generate an interrupt). An interrupt being serviced will be preempted by an interrupt in a higher priority group.

The sub-priority bits allow setting the priority of an interrupt source within a priority group. The values of the sub-priority bits, CMPxIS<1:0>, range from 3 (the highest priority), to 0 (the lowest priority). An interrupt within the same priority group but having a higher sub-priority value will not pre-empt a lower sub-priority interrupt that is in progress. After completion of ongoing ISR, the pending interrupts within the same priority group will be executed in the descending order of their sub-priority.

The priority group and sub-priority bits allow more than one interrupt source to share the same priority and sub-priority. If simultaneous interrupts occur in this configuration, the natural order of the interrupt sources within a priority/sub-group pair determine the interrupt generated. The natural priority is based on the vector numbers of the interrupt sources. The lower the vector number, the higher the natural priority of the interrupt. Any other pending interrupts that were overridden by natural order will then generate their respective ISR based on priority, sub-priority, and natural order after the interrupt flag for the current interrupt is cleared.

Examples of interrupt and comparator initialization and ISR are shown in [Example 39-1](#) and [Example 39-2](#).

Example 39-1: Comparator Initialization with Interrupts Enabled Code Example

```
// Configure both comparators to generate an interrupt on any output transition

CM1CON = 0x40D0; // Initialize Comparator 1
                // Comparator disabled, output enabled, interrupt on any output
                // change, inputs: DAC1OUT, C1IN1-

CM2CON = 0x20C2; // Initialize Comparator 2
                // Comparator disabled, output disabled, output polarity inverted,
                // interrupt on any output change, inputs: C2IN1+, C2IN3-

CM1CONSET = 0x8000; // Enable comparator 1 after configuration.
CM2CONSET = 0x8000; // Enable comparator 2 after configuration.

// Enable interrupts for Comparator modules and set priorities

IPC8SET = 0x0000001F; // Set CMP1 interrupt priority to 7 and interrupt sub-priority to 3
IFS1CLR = 0x00000001; // Clear the CMP1 interrupt flag
IEC1SET = 0x00000001; // Enable CMP1 interrupt

IPC8SET = 0x00001B00; // Set CMP2 interrupt priority to 6 and interrupt sub-priority to 3
IFS1CLR = 0x00000002; // Clear the CMP2 interrupt flag
IEC1SET = 0x00000002; // Enable CMP2 interrupt
```

Example 39-2: Comparator ISR Code Example

```
void __ISR(_COMPARATOR_2_VECTOR, IPL6) Cmp2_IntHandler(void)
{
    // Insert user code here
    IFS1CLR = 0x00000002; // Clear the CMP2 interrupt flag
}

void __ISR(_COMPARATOR_1_VECTOR, IPL7) Cmp1_IntHandler(void)
{
    // Insert code user here
    IFS1CLR = 0x00000001; // Clear the CMP1 interrupt flag
}
```

39.6.1 Interrupt Operation During Sleep Mode

If a comparator is enabled and the PIC32 device is placed in Sleep mode, the Comparator remains active. If the Op amp/Comparator interrupt is enabled in the Interrupt module, it remains functional. Under these conditions, an op amp/comparator interrupt event will wake the device from Sleep mode.

Each enabled Comparator consumes additional current. To minimize power consumption in Sleep mode, turn the unused comparators off before entering Sleep mode by disabling the ON bit (CMxCON<15>). When the device exits Sleep mode, the contents of the CMxCON register are not affected.

For more information on Sleep mode, refer to the **Section 9. “Watchdog Timer and Power-Saving Modes”** (DS60001114).

39.6.2 Interrupt Operation During Idle Mode

Comparator operation during Idle mode is controlled by the Stop-in-Idle Mode bit, SIDL (CMSTAT<13>). If SIDL = 0, normal operation with event/trigger and interrupt generation (when enabled) will occur for any enabled comparator. If SIDL = 1, the Comparator is completely disabled, without any ability to generate events/triggers or interrupts.

For more information on Idle mode, refer to the **Section 9. “Watchdog Timer and Power-Saving Modes”** (DS60001114).

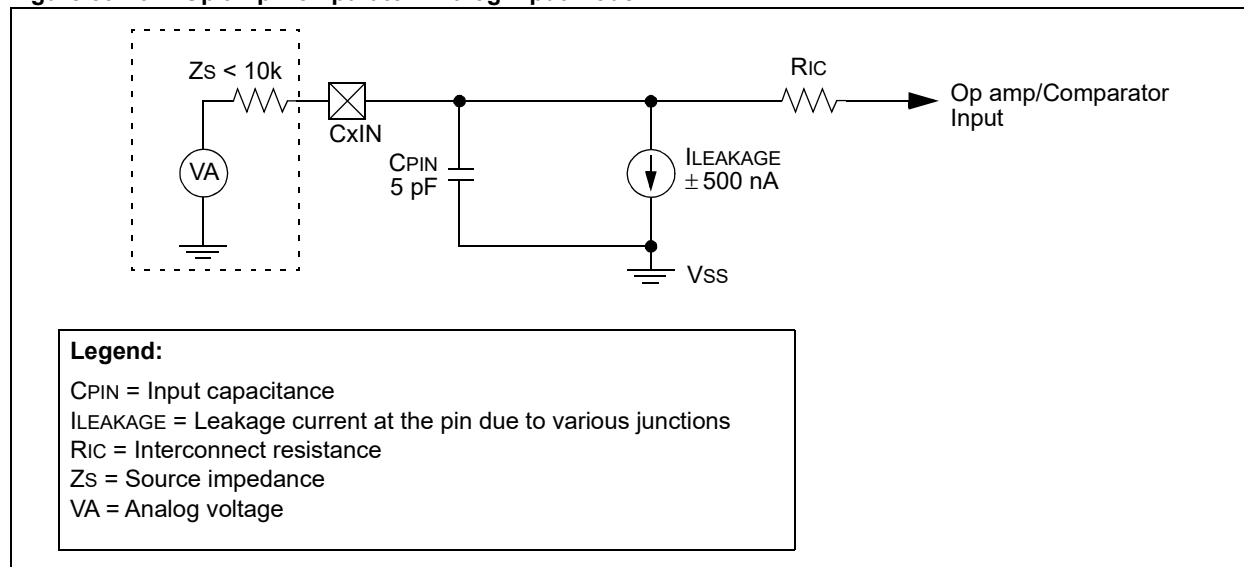
39.6.3 Effects of a Reset State

A device Reset forces the CMxCON register to its reset state, causing the op amp/comparators to be turned off (ON = 0). However, the input pins multiplexed with the analog input sources are configured as analog inputs by default on a device Reset.

39.6.4 Analog Input Connection Considerations

A simplified circuit for an analog input is illustrated in Figure 39-10. A maximum source impedance of 10 k Ω is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have little leakage current.

Figure 39-10: Op amp/Comparator Analog Input Model



39.6.4.1 COMPARATOR INPUT SELECTION ENCODING

The complete decoding for a specific comparator is shown in Table 39-6.

Table 39-5: Comparator Positive Input Selection Encoding

ON	CREF	Source
0	x	Tri-stated
1	0	CxIN1
1	1	DACx internal

Table 39-6: Comparator Negative Input Selection Encoding

ON	CCH<1:0>	Source
0	x x	Tri-stated
1	0 0	CxIN1
1	0 1	CxIN2
1	1 0	CxIN3
1	1 1	OAxOUT

39.7 OP AMP OPERATION

The non-inverting input, inverting input, and the output of all op amps are accessible to external circuits through device pins to allow connection of external gain and/or filtering components. The op amp outputs can also be connected internally to the ADC module, saving an analog input pin.

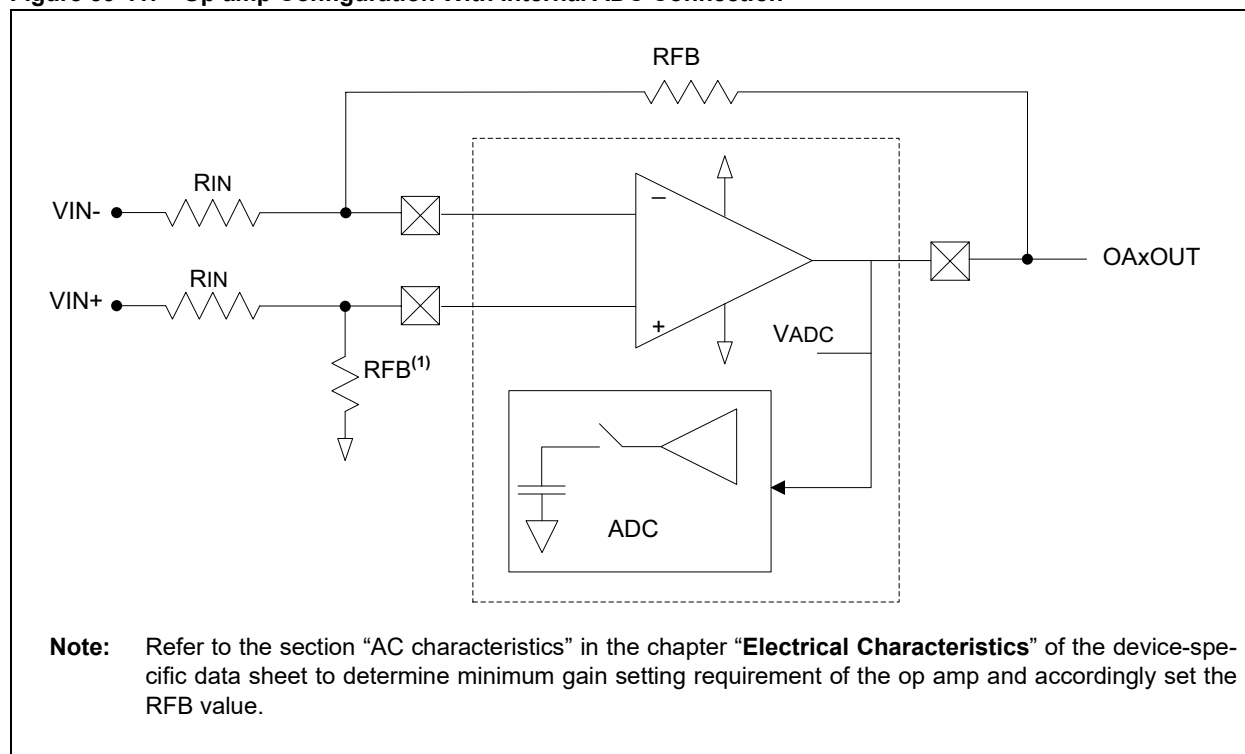
39.8 OP AMP CONFIGURATION

39.8.1 Op amp Output Configured for Internal ADC Connection

The Op amp can be enabled by setting the OPAON bit (CMxCON<31>) on the PIC32MKxxxGPK/GPG/MCM/MCJxxx devices or the AMPMOD bit (CMxCON<10>) on other devices with the Op amp/Comparator peripheral. The external gain/filtering passive components are to be added in the feedback path between the OAxOUT pin to either of the op amp inputs.

Figure 39-11 illustrates the configuration where the op amp output is internally sampled without having to route the output externally to an analog input channel pin. For more information on configuring the ADC, refer to the **Section 18. “12-bit Analog-to-Digital Converter (ADC)”** (DS60001194).

Figure 39-11: Op amp Configuration With Internal ADC Connection



39.8.2 Op amp Low-Power Mode

The Op amp module on the PIC32MKxxxGPK/GPG/MCM/MCJxxx can be configured to operate in Low-Power mode by setting the OPLPWR bit (CMxCON<12>). In Low-Power mode, the op amp current consumption, slew rate, and bandwidth is approximately 1/10th of its normal mode values. Refer to the section “AC characteristics” in the chapter “**Electrical Characteristics**” of the device-specific data sheet to determine the slew rate and gain bandwidth product in Low-Power mode.

Figure 39-12 shows the Comparators configured to compare voltages using a common reference.

Figure 39-12: Example 1: Comparator/ADC Usage Model (Common Reference Input)

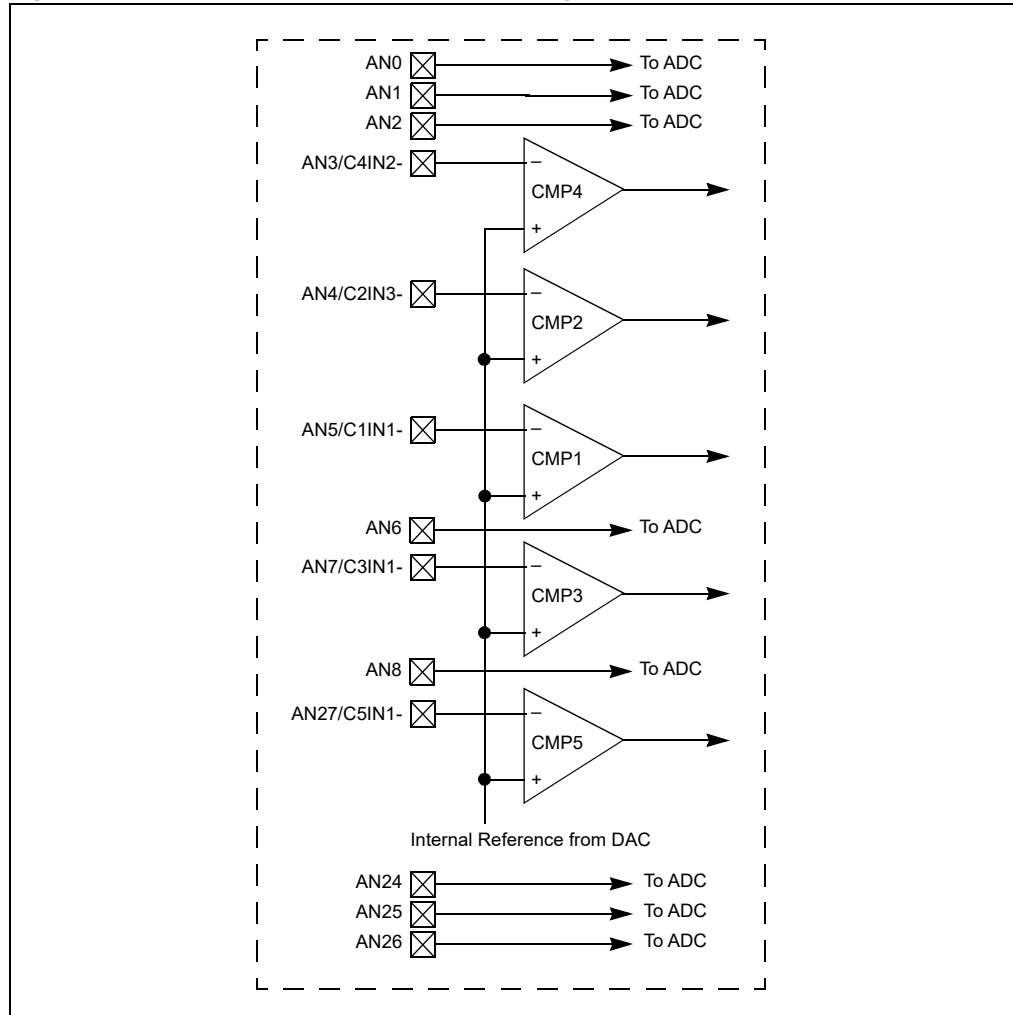


Figure 39-13 shows the comparators configured to compare voltages independent of each other.

Figure 39-13: Comparator/ADC Usage Model (Independent Reference Input)

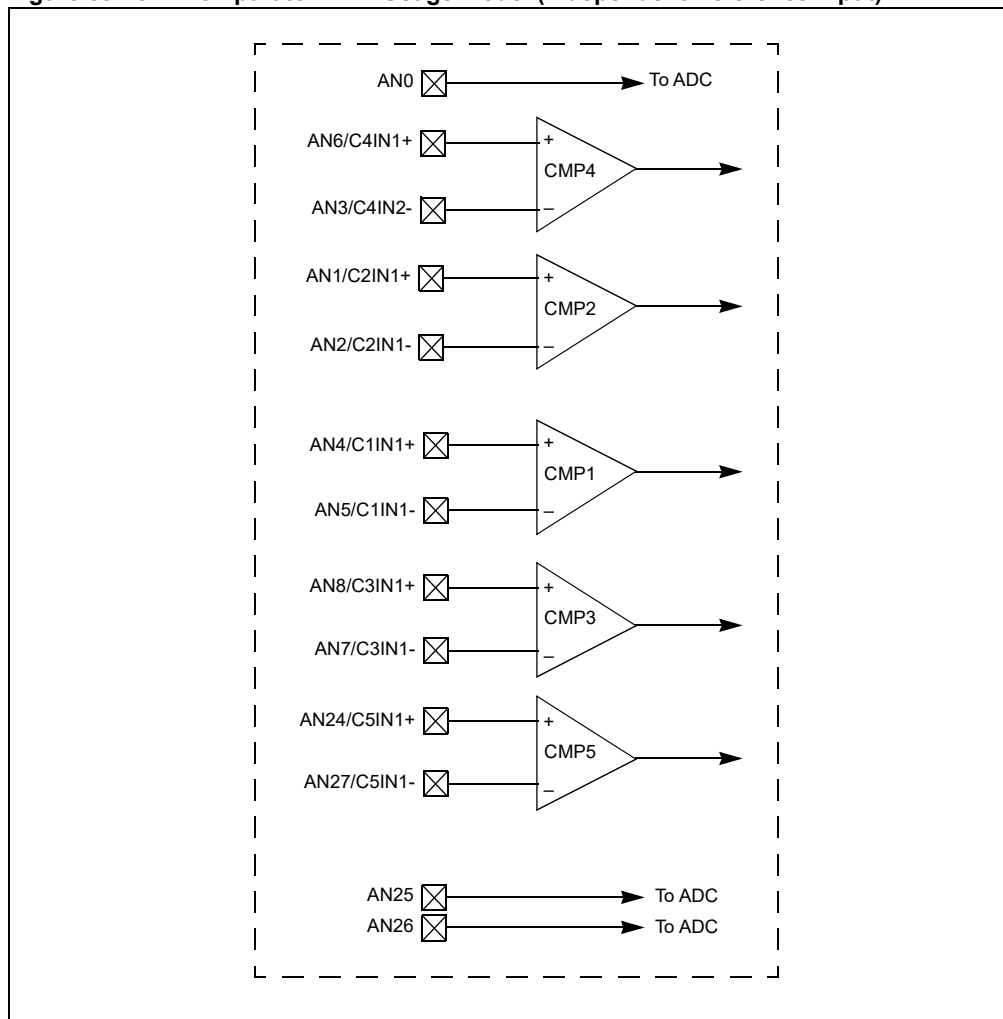


Figure 39-14 Shows the combined usage of comparators and op amps. The comparators are internally connected to the outputs of the op amps. Additionally the stand-alone comparator sub-module can be configured to internally connect to the outputs of up to three op amps.

Figure 39-14: Example 3: Op amp/Comparator/ADC Usage Model

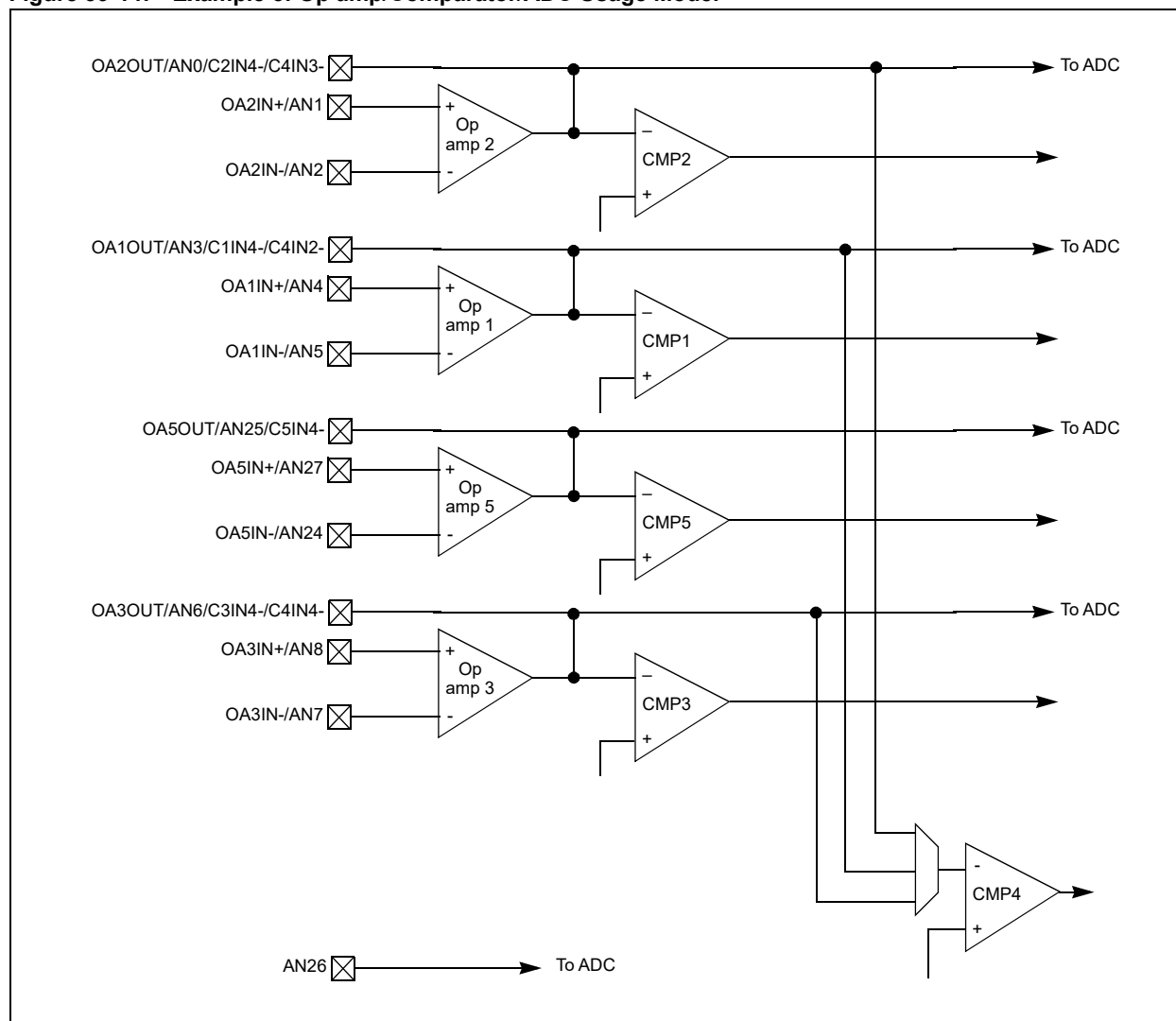
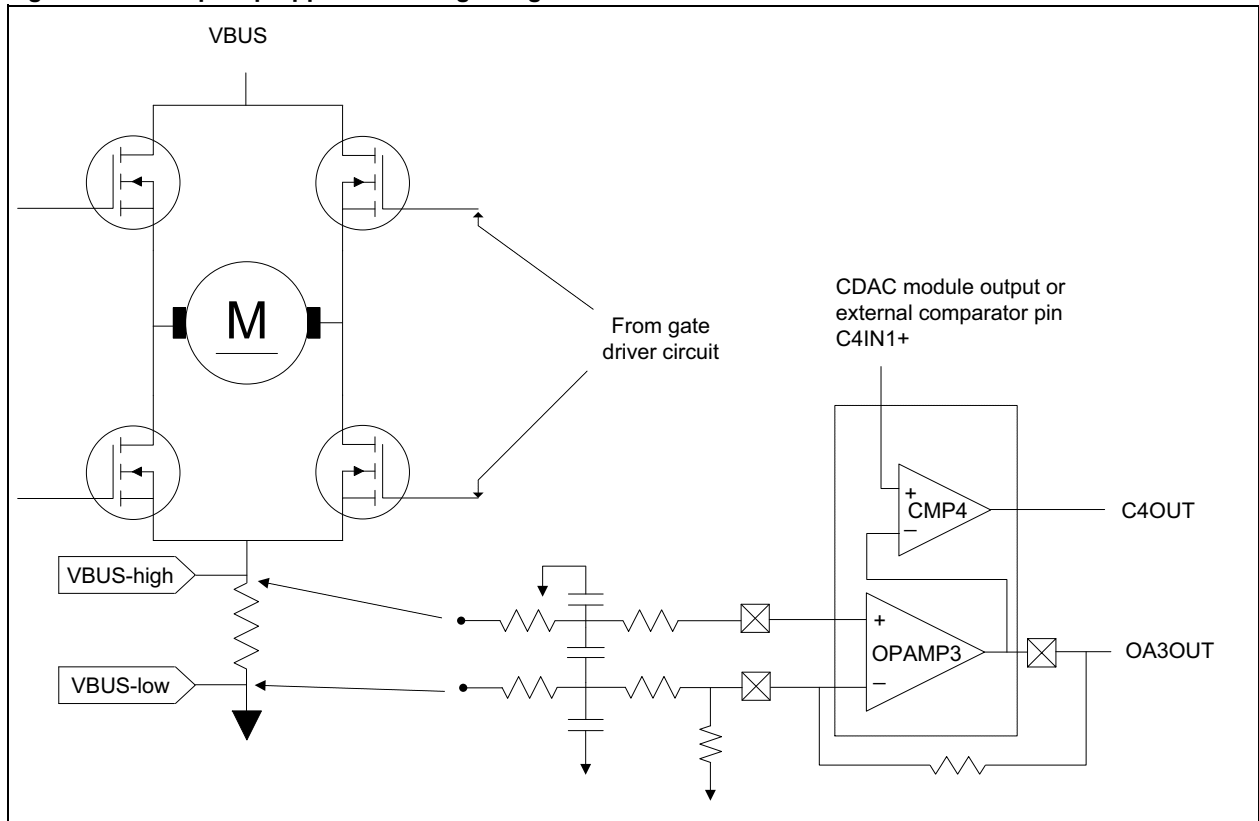


Figure 39-15 illustrates a typical example of an over-current detection in a motor control application utilizing the internal comparator connection to the op amps.

Figure 39-15: Op amp Application Usage Diagram



39.9 REVISION HISTORY

Revision A (March 2012)

This is the initial released version of this document.

Revision B (July 2017)

This revision includes extensive updates incorporated throughout the document.

Revision C (January 2020)

The following updates were incorporated during this release of the document:

Section	Updates
Section 39.1.1 “Features”	Updated Figure 39-1: “Op amp/Comparator Module Block Diagram”
Section 39.2 “Op amp/Comparator Registers”	- Corrected the CLPWR bit in the register summary to display LPWR - The following bits were added to the Register 39-4: “CMxCON: Op amp/Comparator Control Register for PIC32MKxxxGPK/MCM/GPG/MCJxxx Devices”: OPAON, ENPGA, HYSPOL, HYSSEL, and CEVT - Added a new note to the Register 39-4: “CMxCON: Op amp/Comparator Control Register for PIC32MKxxxGPK/MCM/GPG/MCJxxx Devices”
Section 39.3 “Comparator Operation”	- Updated values of VIN to VTH - Updated Figure 39-2: “Comparator Configuration for Devices with Symmetrical Hysteresis - VHYST” - Added a new Figure 39-3: “Comparator Configuration for Devices with Asymmetric Hysteresis - VHYST” - Updated Figure 39-4: “Output State Transitions”
Section 39.8 “Op amp Configuration”	- Updated Figure 39-11: “Op amp Configuration With Internal ADC Connection” with a new note - Added Section 39.8.2 “Op amp Low-Power Mode”

Revision D (April 2020)

The following updates were incorporated during this release of the document:

- Updated [Figure 39-2: “Comparator Configuration for Devices with Symmetrical Hysteresis - VHYST”](#) with a new Symmetric Hysteresis diagram
- Updated [Figure 39-3: “Comparator Configuration for Devices with Asymmetric Hysteresis - VHYST”](#) with a new Asymmetric Hysteresis diagram

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ISBN: 978-1-5224-5903-3

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