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Quartz Crystals and Microchip ICs

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INTRODUCTION

A quartz crystal is a very stable and accurate resonator. Quartz crystals have been used for almost a century to provide a frequency reference in electronic circuits. In the 1940s, the manufacturing of quartz crystals was industrialized due to a sudden need for reliable wireless communication during World War Two. Prior to that, crystals were mostly used by radio amateurs and it was with their assistance that the quartz crystal industry in the US was built-up during this time frame. At that time, natural quartz was used and only a few mines provided the required purity for a good-performing quartz crystal. Today, synthetic quartz - with its higher purity levels - has replaced natural quartz as a key component in timing and communication applications. This application note will explain how to choose or specify a quartz crystal for use with a Microchip timing IC (see Figure 1).

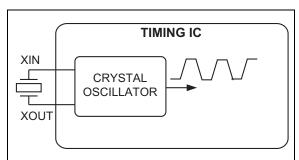


FIGURE 1: Example of Using a Crystal with a Microchip IC.

HOW THE CRYSTAL WORKS

The crystal itself is passive and needs an electronic circuit – a crystal oscillator – to create a reference clock signal. To get the crystal to vibrate, electrodes are placed on the quartz surface. Quartz has piezoelectric properties and a voltage between two electrodes makes the crystal change its shape. An alternative approach also works by applying pressure to the crystal to change its shape. This results in an electrical voltage appearing between two electrodes. This interaction between electrical voltage and mechanical shape causes useful electrical impedance behavior at

the mechanical resonance of the piece of quartz. The crystal absorbs electrical energy from an AC voltage at the mechanical resonance. In other words, the electrical impedance drops at the mechanical resonance so a crystal can be used as a filter to pass the resonance frequency through. An oscillator circuit uses this to build a reference clock signal at this resonance frequency.

An example of the traditional construction of a quartz crystal is illustrated in Figure 2. In this example, the quartz crystal has the shape of a round disk. An electrode is placed on both sides of the disk to apply an electrical voltage. To preserve the frequency accuracy, avoid letting the quartz crystal become dirty or letting the electrode oxidize. The crystal is typically placed in a hermetic enclosure to keep it clean. Figure 2 shows a metal can enclosure where the lid is removed. Surface-mountable ceramic enclosures with smaller dimensions have become much more common.



FIGURE 2: Traditional Construction of a Quartz Crystal.

Most crystals, including the crystal displayed above, vibrate the thickness of a disk. Note that the thinner the disk is, the higher the frequency at which it will vibrate. To manufacture a crystal with a specific frequency, the thickness must be carefully adjusted to achieve the target frequency. The final calibration is done by etching a small amount of metal, typically silver, away from the electrode to reduce its mass and force the rise in frequency. The crystal frequency is monitored during the etching – or ion beam tuning – and is stopped when it has reached its target.

MICROCHIP CRYSTALS

Many Microchip timing ICs use a quartz crystal for the frequency reference. There are specified parameters of a quartz crystal that need to match the parameters of the oscillator circuit in order to meet frequency accuracy and provide reliable operation. These parameters can be illustrated by the electrical model for the quartz crystal, simplified model for the crystal, and oscillator in Figure 3 below.

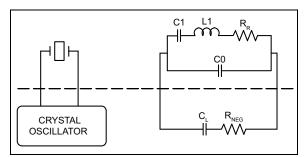


FIGURE 3: Electrical Model for Quartz Crystal/Simplified Model for Crystal Oscillator.

The parameters for Figure 3 are as follows:

- · C1 Crystal Motional Capacitance
- L1 Crystal Motional Inductance
- R_R Crystal Resonance Resistance
- C_L Oscillator Load Capacitance
- R_{NEG} Oscillator Gain, Presented as a Resistance with a Negative Value

TABLE 0-1: CRYSTAL PARAMETER TYPICAL VALUES

Parameter	Value	Notes
C1 (Motional Capacitance)	15 fF ~ 25 fF	Large metal can crystal.
	1 fF ~ 5 fF	Small ceramic sur- face-mount crystal or mesa crystal.
	0.1 fF ~ 2 fF	Overtone crystal.
C0 (Parallel Capacitance)	3 pF ~ 5 pF	Large metal can crystal.
	0.5 pF ~ 2 pF	Small ceramic sur- face-mount crystal or mesa crystal.
ESR (Effective Series Resistance)	5Ω ~ 25Ω	Large metal can crystal.
	15Ω ~ 60Ω	Small ceramic sur- face-mount crystal.
P _D (Drive Level)	500 μW (max.)	Large metal can crystal.
	100 μW (max.)	Small ceramic sur- face-mount crystal.
C _L (Load Capacitance)	12 pF ~ 20 pF	Low frequencies, 10 MHz ~ 25 MHz, fundamental mode.
	5 pF ~ 12 pF	Medium frequen- cies, 25 MHz ~ 50 MHz, fundamen- tal mode.
	3 pF ~ 5 pF	High frequencies up to ~200 MHz.

EXPLANATION OF PARAMETERS

C1 and L1

The motional capacitor (C1) represents the elasticity of quartz while the motional inductor (L1) represents the moving mass. As a result, the C1 and L1 circuit is the electrical resonating tank representation of the mechanical resonance in the quartz crystal. The value of C1 is important when trying to tune the frequency of the crystal through changing the load capacitance in the crystal oscillator. The larger the value of C1, the more frequency deviation from the same load capacitance variation will occur. For example, in a voltagecontrolled XTAL oscillator (VCXO), as in Microchip's PL500, PL502, PL520, or PL586 series of products, this is important because the VCXO needs to have a specific frequency tuning range. If no frequency tuning is present, the value of C1 is less important. For variations in the load capacitance to have less of an effect on the frequency, a smaller value for C1 may be desirable. The value of L1 is not often specified. Instead, the frequency is specified and we can calculate L1 from C1 and the frequency.

Microchip may specify C1 in the event it is important to achieve a certain frequency tuning range. Where it is not specified, it is left to the crystal manufacturer to choose the best value based upon manufacturability.

R_R, ESR, and R_{NEG}

The resonance resistor (R_R) represents the losses in the crystal when it is resonating. The crystal oscillator's negative resistance will settle at a value that exactly cancels the positive crystal resonance resistance, causing a perpetual oscillation. The values of R_{NEG} and R_R in this circuit are not identical because of C0. In typical crystal specifications, a value identified as equivalent series resistance (ESR) is noted. This value is the exact opposite (positive) of the R_{NEG} value in the circuit and can be calculated from the R_R , C0, and C_L values.

When the crystal oscillator is first turned on, the value of $R_{\mbox{\scriptsize NEG}}$ needs to be much larger than the ESR to grow the oscillation signal quickly. A good rule of thumb is to have the $R_{\mbox{\scriptsize NEG}}$ value equal to at least three times (3X) the crystal ESR value to ensure reliable start-up of the crystal oscillator. When the oscillation amplitude has reached a specific amplitude, the nonlinear properties of the oscillator amplifier will prevent the signal from growing further and the $R_{\mbox{\scriptsize NEG}}$ value is effectively reducing to equal the ESR value for perpetual oscillation. There are a variety of different methods for setting the oscillation amplitude where the crystal oscillator settles. Microchip can provide the value of $R_{\mbox{\scriptsize NEG}}$ in its timing ICs and can recommend the ESR or R_R to ensure a proper oscillator startup.

C₀

C0 is the parallel – or holder – capacitance of the crystal. It is typically generated by the electrodes in the crystal. At frequencies not near a mechanical resonance of the crystal, the quartz crystal behaves like an ordinary capacitor with a few pico-Farads (pF) of capacitance. The C0 is a parasitic capacitance in the crystal that only has a negative influence on the performance. Microchip will specify a maximum value so that C0 does not interfere too much with crystal oscillator startup or frequency tuning.

C_L

The load capacitance (C_L) is a property of the crystal oscillator. Its value influences the exact oscillation frequency and stability of the oscillator. To ensure frequency accuracy, crystals are calibrated to resonate at their nominal frequency with a specific load capacitance value. Microchip can specify the C_L value of the crystal oscillator circuit in its timing IC to ensure the proper crystal can be selected. Theoretically, a crystal manufacturer can make any C_L value, but the most popular values are readily available with most distributors. It is sometimes possible to make a small adjustment to match the C_L value with an additional capacitor in order to use a popular crystal with a particular C_L value. Contact Microchip for advice on exactly how much adjustment a certain timing IC can tolerate.

With programmable clock generators like Microchip's PL610, PL611, and PL611s series, C_L is programmable and can be customized to a specific crystal in combination with PCB trace capacitance. Typically it takes more gain and power to drive a large C_L .

F_L

 F_L represents the load frequency where the crystal oscillator will oscillate. In relation to the crystal, it is the oscillation frequency specified at a certain value for the C_L . The nominal frequency specified for a crystal will be this load frequency.

FS

The series resonance frequency (F_S) of the crystal is determined by C1 and L1. F_S is the frequency where the impedance of the crystal is the lowest and, therefore, easy to find with a 50 Ω impedance/network analyzer. Some oscillators can oscillate at this frequency, although it is not typical.

Parameter Interactions and Dependencies

The "perfect" crystal has a low R_R or ESR, a low C0 value, and a large C1 value in the event there is a need to tune the frequency. Unfortunately, this "perfect" crystal does not exist due to physical dependencies

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between the parameters. Increasing the size of the electrode effectively increases the value of C1 and decreases the value of $R_{\rm R}$ or ESR while also increasing the value of C0. The size of the electrode is also limited by the active area and total size of the quartz disc. The smallest SMD crystals are not well-suited for use in VCXOs due to the fact that their C1 values cannot be made large enough for adequate frequency tuning. By using larger crystals, a design can be created that provides for a larger electrode for VCXOs and a smaller electrode for non-tuning oscillators. With the smallest SMD crystals, the best that can be accomplished is optimization for a low $R_{\rm R}$ value.

There is a relatively constant ratio between C0 and C1, depending upon how efficiently the electrodes are driving the piezo properties of the quartz. The lower the C0/C1 ratio, the more efficiently the piezo properties are used. Large crystals usually have the best efficiency with a C0/C1 ratio, close to 200. Small, 2 mm x 1.6 mm or smaller, ceramic surface-mount crystals will be less "pullable", with a C0/C1 ratio around 400.

Overtones

An AT-cut quartz crystal can vibrate at a variety of different harmonics. The most common vibration is the "fundamental mode". This mode is the 1st harmonic and the lowest resonance frequency. With AT-cut quartz, overtones appear at odd multiples of the fundamental mode frequency. For example, there is a 3rd overtone, a 5th overtone, etc. Each overtone can be represented with an extra C1-L1-R_R branch in the crystal model. Generally, the higher the overtone, the higher the R_R will be for that overtone. This is most accurate at the lowest (3rd and 5th) overtones. Typically, a crystal oscillator has more oscillator gain (bigger negative resistance) at lower frequencies. With larger R_R values at overtones, the crystal oscillator will always oscillate at the fundamental mode frequency without any additional filtering. The simplest method to make the oscillator oscillate at the 3rd overtone is a high-pass filter to suppress the oscillator gain near the fundamental frequency. If there is sufficient oscillator gain at the 3rd overtone frequency to overcome the RR at the 3rd overtone, the oscillator will oscillate at the 3rd overtone frequency. To oscillate at the 5th or a higher overtone, it is recommended to work with a band-pass filter to suppress both higher and lower tones.

The crystal resonance frequency is a function of the quartz plate thickness. To increase frequency, the quartz plate thickness needs to be reduced. Thinner crystals can be more difficult to handle during the manufacturing process. Using the crystal at an overtone is a compromise that makes the crystal itself less expensive while making the oscillator circuit more complex.

The vibrating mass is the same at an overtone, making the L1 values of the overtones and the fundamental mode approximately the same. That makes the C1 values much smaller, making the frequency higher (theoretically, 9X smaller for the 3rd overtone, 25X smaller for the 5th overtone, etc.). This sort of overtone operation is not well suited for VCXO designs because of the high C0/C1 ratio.

Inverted Mesa Technology

The inverted mesa technology makes the crystal very thin in the middle portion of the crystal plate. The thicker outer edges allow for easy handling and the thinner center allows a high fundamental mode frequency when the electrodes are placed only inside the thin area.

The inverted mesa technology is relatively expensive, but some applications justify the cost (VCXO designs at high frequencies, for example). Microchip provides high-frequency VCXO ICs, such as the PL520 and PL586 series, that function well with inverted mesa crystals. Additionally, Microchip's PL686-05 and PL610-01 can also work with high-frequency inverted mesa crystals.

Drive Level

The power dissipated in the crystal is the drive level. Above a certain drive level, crystals can show nonlinear properties that can cause unwanted side effects. Coupling with unwanted modes can occur, resulting in frequency instabilities. Microchip will specify the typical IC drive level for the timing IC so that a properly functioning crystal can be selected.

Q-Factor

Q is a parameter that implies energy efficiency. Compared to a resonant tank circuit made with discrete components, quartz has a very large Q-factor. This parameter is usually not specified, but often expected, of the quartz crystal. The high Q-factor makes the frequency very stable, but another consequence of the high Q-factor is very low noise in the oscillator signal. The Q-factor of an AT quartz crystal can be above 20,000 to as high as 300,000.

CRYSTAL FREQUENCY ACCURACY AND STABILITY

The resonance frequency of a quartz crystal is very stable compared to alternative techniques such as an LC tank or other materials, like ceramic resonators. When used properly, a quartz crystal is a very accurate frequency reference for its cost and this is mostly why quartz crystals are so popular. The frequency accuracy and stability can be broken down into several items:

- Calibration Tolerance at Room Temperature:
 This is the accuracy of the frequency at nominal conditions. For purposes of identification, "easy" is ±50 ppm, "medium" is ±25 ppm, and "difficult" is ±10 ppm.
- **Temperature Drift:** Referenced to the frequency at nominal conditions, the frequency drifts with a particular temperature curve. The temperature curve can be modeled with a 3rd order polynomial equation and the crystal is usually designed to minimize the drift for a particular temperature range (see Figure 4). It is advised to select a crystal that is specified for the same temperature range as what the crystal oscillator circuit will be exposed to. The two most common temperature ranges are industrial (-40°C to +85°C) and commercial (0°C to +70°C). The wider industrial temperature range results in bigger drift numbers or can be more difficult to achieve certain drift requirements with. A less than ±20 ppm drift for the industrial range is considered "difficult", but it is relatively easy to achieve the same numbers using the commercial range. For the commercial range, a less than ±10 ppm drift is considered "difficult".
- Aging: The frequency of a quartz crystal slowly drifts with time due to aging. Mechanical stresses relax over time. Epoxy outgassing or moisture can react with the electrode and make the crystal heavier. Usually, frequency drifts down with aging. The crystal will age quickly in the first few years of use, slowing over time. Occasionally, a manufacturer will pre-age crystals at the factory to meet a very tight aging specification. A typical aging specification is 5 ppm per year. Sometimes a specification will read as 5 ppm for the first year and lower subsequently.
- Total Stability: This number includes all of the above and is actually the most popular method for specifying the frequency accuracy of a quartz crystal. It guarantees that the crystal oscillator frequency does not drift outside a certain range under all conditions and for the life of the device. Total frequency numbers like ±100 ppm are relatively easy, even with -40°C to +85°C temperature range. Medium is ±50 ppm and, below that, it quickly gets very difficult. Dealing with a total stability requirement, the crystal manufacturer can

optimize the frequency accuracy for each individual item for the best manufacturability.

Microchip ICs do not contribute significantly to the accuracy and stability of its output clocks. Frequency accuracy will be determined by the quartz crystal reference.

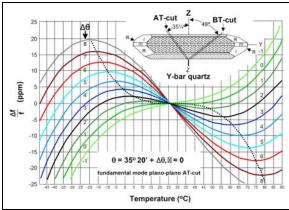


FIGURE 4: AT-Cut Crystals.

Temperature Behavior for

CRYSTAL OSCILLATOR MATHEMATICS

Equation 1 provides the relation between the ESR value and R_R value:

EQUATION 1:

$ESR = R_R \times (1 + (C0)/C_L)^2$		
Where:		
R_R	15Ω	
C0	3 pF	
CL	12 pF	

For the equation above, ESR works out to 23Ω . Equation 2 helps calculate frequency movements:

EQUATION 2:

$$F_L = F_S \times SQRT(1 + C1/[C0 + C_L])$$

Equation 2 can be used to find the frequency change as a result of load capacitance change.

If CL1 causes FL1 and CL2 causes FL2, see Equation 3.

EQUATION 3:

$$FL1/FL2 = SQRT([1 + C1/(C0 + CL1)]/[1 + C1/(C0 + CL2)])$$

Equation 4 is a simplified version of Equation 3.

EQUATION 4:

$$FL1/FL2 = 1 + 2 \times C1 \times (CL2 - CL1)/(C0 + CL1)/(C0 + CL2)$$

When CL1 and CL2 are close together, see Equation 5.

EQUATION 5:

$$dFL = 2000 \times C1 \times dCL/(C0 + C_L)^2$$

dFL is the frequency shift, in parts per million (ppm) caused by the load capacitance shift dCL. C1 is the motional capacitance in femto Farads (fF), dCL is the load capacitance shift in pico Farads (pF), C0 is the parallel capacitance in pF, and C_L is the nominal load capacitance in pF.

C_L Error Example

A crystal is calibrated for C_L = 12 pF and the IC spec also says C_L = 12 pF, but there is an additional 1 pF of parasitic capacitance in the PCB. How large is the frequency error because of the extra 1 pF? Additional information for the crystal: C1 = 8 fF and C0 = 2.5 pF. The frequency error is calculated in Equation 6.

EQUATION 6:

$$dFL = 2000 \times 8 \times 1/(2.5 + 12)^{2}$$

In this case, dFL = 76 ppm.

VCXO Example

The VCXO specification states that CL1 = 20 pF at $V_{CONTROL}$ = 0V; CL2 = 8 pF at $V_{CONTROL}$ = 1.65V; and CL3 = $V_{CONTROL}$ = 3.3V.

The crystal is calibrated for C_L = 8 pF, so the nominal frequency is achieved at $V_{CONTROL}$ = 1.65V.

The crystal's parameters are that C1 = 8 fF (or 0.008 pF) and C0 = 2.5 pF.

With the control voltage tuning between 0V and 3.3V, the frequency tuning range can be calculated by Equation 7 and Equation 8.

EQUATION 7:

$$FL1/FL2 = SQRT([1+0.008/(2.5+20)]/[1+0.008/(2.5+8)]) = 0.999797 = 1-203ppm$$

EQUATION 8:

$$FL3/FL2 = SQRT([1+0.008/(2.5+4)]/[1+0.008/(2.5+8)]) = 1.000234 = 1+234ppm$$

The frequency tuning range is -203/+234 ppm with 0 ppm in the center at $V_{CONTROL} = 1.65V$.

FINE TUNING THE LOAD CAPACITANCE

When the load capacitance of the timing IC is different from the load capacitance to which crystal was calibrated, the crystal oscillator will not oscillate at the intended nominal frequency of the crystal. That can be fixed by adding capacitors to the crystal oscillator circuit. For example, adding a capacitor in series with the crystal lowers the load capacitance of the oscillator circuit (see Figure 5).

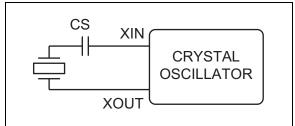


FIGURE 5: Crystal C_L Value is Smaller than Oscillator C_I Value.

In the event the crystal oscillator load capacitance (C_{LO}) is larger than the load capacitance the crystal is calibrated to (C_{LX}) , C_S can be added in series to lower the crystal oscillator load capacitance to match the crystal.

EQUATION 9:

$$C_S = C_{LO} \times C_{LX} / (C_{LO} - C_{LX})$$
 Where:
$$C_{LO} \qquad \qquad 14.32 \ \mathrm{pF}$$

$$C_{LX} \qquad \qquad 12 \ \mathrm{pF}$$

Using the given values, C_S calculates out to 74 pF.

When the error is only 2 pF or 3 pF, a capacitor can be added from X_{IN} to ground to increase the oscillator load capacitance. The problem with this method is that the oscillator gain reduces when adding a capacitor to ground. A more balanced approach is to add a capacitor to ground at both X_{IN} and X_{OUT} (see Figure 6).

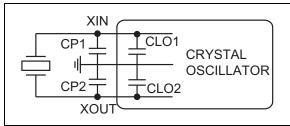


FIGURE 6: Crystal C_L Value is Larger than Oscillator C_L Value.

Contact Microchip to find out how much capacitance can be added safely in this fashion to a specific Microchip timing IC. The math is not so precise for this case due to there being various ratios for CLO1/CLO2. However in most cases one can assume the values for CLO1 and CLO2 are quite close to one another.

To correct the load capacitance 1 pF up with CP1 only, CP1 = 4 pF (approximately) must be added. To correct the load capacitance 1 pF up with CP1 and CP2, CP1 = CP2 = 2 pF (approximately) must be added. Using both CP1 and CP2 is the better method and affects the oscillator gain the least.

USING A REFERENCE CLOCK SIGNAL INSTEAD OF A CRYSTAL

Most crystal oscillators allow the X_{IN} pin to be driven with a reference clock signal instead of using a crystal. Although this method is acceptable, there are a few items to consider before implementing it:

- The usual signal at X_{IN} is a sine wave with a peak-to-peak signal swing smaller than V_{DD}. When applying a square wave to X_{IN}, higher frequency harmonics will couple through CLO1 (see Figure 7) to the ground rail and can interfere with other parts of the circuit. When issues such as deterministic jitter or spurs in the phase noise arise, try and slow down the edges on the reference clock square wave with another series resistor. A value of 100Ω is a good first try.
- Most crystal oscillators have DC biasing inside the IC. When using a large signal reference clock with rail-to-rail signal swing, the X_{IN} pin can be directly driven. Conversely, when the reference clock has a smaller signal swing a TCXO clipped sine wave, for example it is advisable to use a series coupling capacitor to allow the DC biasing to settle at the intended level. The phase noise performance of the reference oscillator will affect synthesizer phase noise performance within the PLL loop bandwidth. Signal edge rate and amplitude will also have an effect.

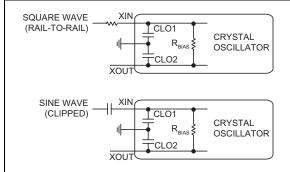


FIGURE 7: Driving X_{IN} with External Reference Clock.

CRYSTAL SELECTION CHECKLIST

When selecting a crystal for a Microchip timing ICs, use the following checklist:

- · Select the correct nominal frequency.
- · Select the desired package type.
- Select the correct load capacitance. Attempt to find a crystal with a load capacitance as close as possible to the load capacitance of the oscillator. Potential frequency error can be calculated from the difference between the crystal oscillator load capacitance and the selected crystal load capacitance. When this error is unacceptable, then tuning the load capacitance with capacitors may be needed. Alternatively, one can have the correct load capacitance crystal made to the correct CL specification.
- Select the required frequency accuracy and stability items in combination with the required temperature range and life time of the device.
- Verify that other parameters of the crystal meet the crystal oscillator requirements:
 - Maximum ESR
 - Maximum drive level
 - Maximum C0
 - In case of VCXO frequency tuning, there can be a C1, motional capacitance requirement and/or a maximum C0/C1 ratio requirement.

SPECIFIC MICROCHIP IC RECOMMENDATIONS

The following is a list of Microchip ICs with specific notes about the crystal used with these ICs:

- SM802xxx: The FLEX SM802xxx products use fundamental mode crystals in the range of 12 MHz to 30 MHz. The load capacitance of the oscillator is 10 pF. This is a common value and crystals with this load capacitance will be available on the market. Crystals up to C_L = 12 pF can be tuned in by adding capacitors from X_{IN} and X_{OUT} to ground. Decreasing the C_L value to 8 pF or lower with a capacitor in series with the crystal is acceptable.
- SM803xxx: The FLEX2 SM803xxx products use fundamental mode crystals in the range of 12 MHz to 60 MHz. The load capacitance of the oscillator is 12 pF. This is a common value. With this oscillator it is not recommended to increase the C_L value with capacitors to ground but decreasing the C_L value to 10 pF or 8 pF with a capacitor in series with the crystal is acceptable.
- PL135-XX: The PL135 products are fanout XOs.
 There will be multiple clock outputs with the crystal frequency. The C_L value for the PL135-27 is 12 pF, for the PL135-37 is 8 pF and for the PL135-47 and PL135-67 is 15 pF. The crystal frequency range is 10 MHz to 40 MHz.
- PL500-17: The PL500-17 is a VCXO. The nominal load capacitance at the nominal control voltage is 8 pF, at the lowest control voltage is 15 pF and at the highest control voltage is 5.2 pF. For the frequency to be at the nominal value with the nominal control voltage the crystal C_L value needs to be 8 pF. The value of the motional capacitance C1 of the crystal determines the frequency tuning range. Formulas from the Crystal Oscillator Mathematics section can be used to calculate the frequency tuning range. The PL500-17 can work with crystals between 17 MHz and 36 MHz.
- PL500-37: The PL500-37 is a VCXO similar to the PL500-17, but designed for higher-frequency crystals in the range 36 MHz to 130 MHz. Above about 60 MHz the crystals are too thin to handle with the common design and it becomes more practical to use inverted mesa technology. The load capacitance at the nominal control voltage is 5.1 pF, at the lowest control voltage is 9.5 pF, and at the highest control is 3.3 pF.
- PL502-3X: The PL502-3X products are VCXOs with additional PLL to multiply the crystal frequency with up to x32. There is also an output divider that can divide down the crystal frequency, down to divide by 16. The load capacitance at the nominal control voltage is 9.5 pF, at the lowest control voltage is 21 pF, and at the highest control voltage is 6.0 pF. The PL502-3X can work with

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- crystals between 12 MHz and 25 MHz.
- PL520-XX: The PL520 products are VCXOs that work with high-frequency crystals. The PL520-20 uses 100 MHz to 200 MHz crystals, the PL520-30 uses 65 MHz to 130 MHz crystals and the PL520-80 uses 19 MHz to 65 MHz crystals.
- PL586-XX: The PL586 products are high frequency VCXOs that were designed for super low phase noise. The different ICs work with crystal frequencies between 75 MHz and 170 MHz with inverted mesa technology. The nominal load capacitance is close to 5 pF. These ICs are sold unpackaged and integrated with a quartz crystal into the same hermetically sealed package and the crystal frequency is calibrated when already connected to the IC. This makes it less important to know the exact load capacitance.
- PL602-2X, PL60203X: PCIe clock generator ICs that use a 25 MHz crystal with a load capacitance of 12 pF.
- PL602-37: Similar to the PL502-37, but without the VCXO. The crystal oscillator load capacitance is 20 pF. This is relatively large but smaller C_L values can be achieved by adding a capacitor in series with the crystal.
- PL602041, PL60208X: PCle clock generator ICs that use a 25 MHz crystal with a load capacitance of 10 pF.
- PL6070XX: PCIe clock generator ICs that use a 25 MHz crystal with a load capacitance of 15 pF.
- PL610-01: This clock generator is customizable (factory programmable) and one of the programmable items is the load capacitance for the crystal. The value can be chosen between 8 pF and 12 pF. The crystal frequency can be between 5 MHz and 60 MHz.
- PL610-32: This is a special low-power clock generator for making an RTC 32.768 MHz clock using a 16.777 MHz crystal. The load capacitance is only 3 pF to keep the power consumption low. Please contact the factory about using larger values.
- PL611-XX: Customizable clock generators with PLL. The load capacitance of the crystal oscillator can be programmed between 5 pF and 20 pF. The crystal frequency can be between 10 MHz and 30 MHz.
- PL611s-XX: Customizable clock generators with PLL, similar to PL611-XX, but smaller and lower power. The load capacitance of the crystal oscillator can be programmed between 8 pF and 12 pF and the crystal frequency can be between 10 MHz and 50 MHz.
- PL613-XX: Customizable clock generators with multiple PLLs and multiple outputs. The load capacitance is fixed to 15 pF (not programmable). The crystal frequency can be between 10 MHz

- and 50 MHz.
- PL671-XX: EMI reduction clock generators that can use a crystal between 10 MHz and 40 MHz. The load capacitance of the crystal oscillator is 15 pF.
- PL686-XX: Super low phase noise clock generators that use inverted mesa crystals in the range 75 MHz to 170 MHz. These ICs are sold unpackaged for integration together with the crystal in a low phase noise clock module.
- SY89529: Clock generator that uses a 16.66 MHz crystal and the crystal oscillator is a series mode type that runs the crystal near the series resonance. A certain load capacitance value can be achieved with a capacitor in series with the crystal.
- SY8953X: Clock generators that use crystals between 14 MHz and 18 MHz. The crystal oscillator is a series mode type that runs the crystal near the series resonance frequency. Add a capacitor in series to achieve a certain load capacitance value.
- SM8400XX: Clock generators that use a 25 MHz crystal. This crystal oscillator needs external capacitors from X_{IN} to ground and X_{OUT} to ground to operate properly. The capacitance in the IC is only 2 pF and 2 × 20 pF external makes C_L = 12 pF or 2 × 30 pF external makes C_L = 18 pF. Do not increase above C_I = 18 pF.
- SM843256, SM844256: Clock generators that use crystals between 18 MHz and 25 MHz with a load capacitance of 10 pF.
- SY898535: LVPECL fanout buffer that can also use a crystal for the frequency reference input.
 The crystal frequency can be between 12 MHz and 40 MHz.

Note the following details of the code protection feature on Microchip devices:

- · Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our
 knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data
 Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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