DS0115
Datasheet
SmartFusion2 Pin Descriptions

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 16.0

Added pin A1 designator in all the figures in Bank Location Diagrams, page 4.

1.2 Revision 15.0

The following is a summary of the changes in revision 15.0 of this document.

- In the “Bank 8” row of Table 1, page 17, removed SERDES 0 in “VFG784 M2S060” and “FG676 M2S060” columns.
- Added Table 6, page 23.

1.3 Revision 14.0

Table 5, page 22 has been updated and a footnote has been added to indicate that there is a limitation regarding the assignment of LVDS to DDRIOs.

1.4 Revision 13.0

The following is a summary of the changes in revision 13.0 of this document.

- Updated all the cross references in the document with the Microchip website migrated links.
- Added Figure 3, page 5.
- Updated Table 1, page 17.
- Updated Table 12, page 30.
- Updated Table 12, page 30 with the following row. M2S060T-VF400 D18 MSI47NB2/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI46NB1 is an input only pin.
- Updated with VFG784 package in Bank Location Diagrams, page 4 and Mechanical Drawings, page 35.
- Added Figure 29, page 35 to Figure 52, page 58.

1.5 Revision 12.0

The following is a summary of the changes in revision 12.0 of this document.

- Information about unused conditions was added, see Table 10, page 28, Table 11, page 29, Table 12, page 30, and Table 13, page 30.
- Information about VPPNVM and VSSNVM was added to table note of Supply pins, see Table 9, page 26.

1.6 Revision 11.0

The following is a summary of the changes in revision 11.0 of this document.

- Updated Table 5, page 22, Table 9, page 26, Table 10, page 28 and Table 12, page 30.
- Added reference to PD3068: Package Mechanical Drawings for all the package devices. For more information, see Mechanical Drawings, page 35.
- Updated Programming SPI, page 29.

1.7 Revision 10.0

The following is a summary of the changes in revision 10.0 of this document.

- Added Figure 20, page 14.
- Added MDDR/FDDR Interface, page 25.

1.8 Revision 9.0

The following is a summary of the changes in revision 9.0 of this document.

- Added Figure 8, page 8.
- Updated Table 1, page 17 and Table 2, page 19.
- Added Figure 28, page 22.
- Updated Programming SPI, page 29.
- Updated Supply Pins, page 26.
- Updated Table 15, page 32.

1.9 Revision 8.0

The following is a summary of the changes in revision 8.0 of this document.

- Added Figure 5, page 6, Figure 6, page 7, Figure 13, page 10, and Figure 14, page 11.
- Removed all instances of and references to M2S100 device from Table 1, page 17.
- Replaced VQ144 with TQ144 from Table 3, page 19.
- Removed GPIO or USB_DIR_C from Table 16, page 33.

1.10 Revision 7.0

The following is a summary of the changes in revision 7.0 of this document.

- Updated Notes for Bank Location figures.
- Added Figure 24, page 16, Figure 25, page 16, Figure 26, page 17, and Figure 27, page 17.
- Modified Table 1 • Organization of I/O Banks in SmartFusion2 Devices - FC1152, FCS536, FCV484, FG896, FG676, and FG484 by moving VF400 and FCS 325 devices to Table 2 • Organization of I/O Banks in SmartFusion2 Devices - VF400, FCS325, VF256, and TQ144 (SAR 58291).
- Added VF256 and VQ144 devices to Table 2 • Organization of I/O Banks in SmartFusion2 Devices - VF400, FCS325, VF256, and TQ144 (SAR 58291).
- Modified notes in Table 9, page 26.
- Modified Table 9, page 26 by adding 'x' to supply pin names and deleting the individual pin names.
- Added Table 15, page 32.

1.11 Revision 6.0

The following is a summary of the changes in revision 6.0 of this document.

- Modified Notes for the following figures: Figure 1, page 4, Figure 2, page 5, and Figure 7, page 7.
- Added Figure 19, page 13, Figure 23, page 15, and Figure 27, page 17.
- Updated Table 1, page 17 and Table 2, page 19.
- Note added for VPP and VPPNVM for 090, 100, and 150 devices in Table 9, page 26.
- Added descriptions for TMATCH pins to Table 14, page 31.

1.12 Revision 5.0

The following is a summary of the changes in revision 5.0 of this document.

- Table 5, page 22 was corrected to change LVDS to LVDS2V5.
- Updated description column in Table 5, page 22. Also added a Note for default state of I/Os.
- Updated description column for VREF0 and VREF5 inTable 9, page 26. Also modified pin name from MDDR_PLL_VDDA to MSS_MDDR_PLL_VDDA.
- Updated description column in Table 12, page 30 for DEVRST_N.
- Added Figure 1, page 4, Figure 4, page 6, Figure 7, page 7, Figure 12, page 10, Figure 22, page 15, Figure 18, page 13, Figure 21, page 14

1.13 Revision 4.0

The following is a summary of the changes in revision 4.0 of this document.

- Added Figure 13, page 10, Figure 14, page 11, Figure 15, page 11, Figure 16, page 12, and Figure 17, page 12 for the VF400 package.
- Updated Bank names in Table 1, page 17 and Table 2, page 19.

- VF400 was added to Table 3, page 19.
- Deleted incorrect references to 1.8 V from Reference Resistors.
- Several table notes were revised in Table 9, page 26. Added recommendation for SERDES VDDAPLL supply when SERDESIF is unused. Added VDD_2V5 as a supply with range 1.2 V to 2.5 V.
- Updated the XTL pin names in Table 12, page 30. Added description for DEVRST_N stating that “It is a dedicated I/O of type MSIO (3.3 V capable)”.
- Table 14, page 31 was expanded to include additional pins. Moved details for VDD_2V5 to Table 9, page 26.
- Updated the Pin Table for the FG484, page 47 package with M2S090.
- Added VF400, page 49 section.
- The Board Design Guidelines application note has been released and references to it in this document are now hyper-linked to its location on the Microsemi website.

1.14 Revision 3.0

The following is a summary of the changes in revision 3.0 of this document.

- The SmartFusion2 Pin Descriptions, page 4 section has been separated from the rest of the SmartFusion2 datasheet and is now published separately. Pin tables have been removed from the document and replaced by links to sortable pin tables in an Excel spreadsheet. Pin tables for non-T devices are being reworked and will be included in a future release of the document (SAR 45184). The contents of the document have been reorganized (SAR 45275).
- Table 1, page 17 and Table 2, page 19 were corrected to change MSIOD to MSIO for bank 4 and bank 7, M2S010T and M2S025T devices on the FG484 package.
- Notes were added to Table 11, page 29 and Table 12, page 30 giving instructions on how to handle pins if unused.
- Added Special Pins, page 31 section.
- Connection information for some of the SERDES pins was clarified in the notes to Table 13, page 30.

1.15 Revision 2.0

The document was revised extensively, including major changes to Table 9, page 26, new bank location diagrams, renaming of many pins and new pin tables for FG484 and FG896.

1.16 Revision 1.0

The following is a summary of the changes in revision 1.0 of this document.

- Table 9, page 26 was revised to clarify instructions for unused pins.
- Figure 1, page 4 was revised. The number of pairs in bank 1 was corrected to 10 (was 11) and the number of pairs in bank 3 was corrected to 23 (was 25).
- Added Table 2, page 19.
- The description for the FLASH_GOLDEN pin in Table 11, page 29 was corrected to reverse the conditions for High and Low.
- Table 13, page 30 was revised to clarify handling of pins with and without transceiver.
- Added FG484, page 47, including pin tables for M2S010T, M2S025T, and M2S050T.

1.17 Revision 0.0

Revision 0.0 was the first publication of this document.

2 SmartFusion2 Pin Descriptions

2.1 User I/Os

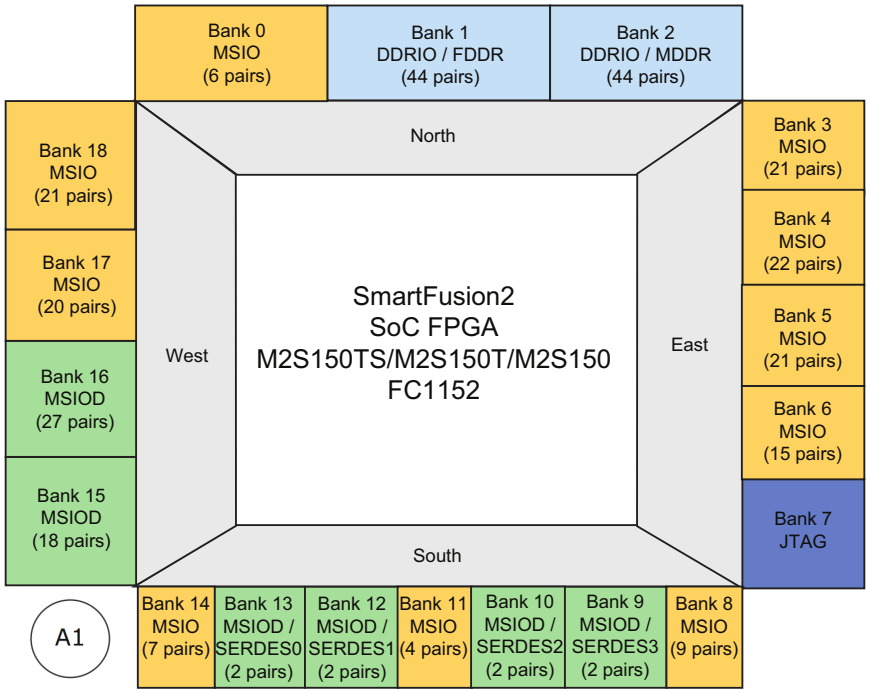
SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) devices feature a flexible I/O structure that supports a range of mixed voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V) through bank selection. The MSIO, MSIOD, and DDRIO can be configured as differential I/Os or two single-ended I/Os. These I/Os use one I/O slot to implement single-ended standards and two I/O slots for differential standards. The DDRIO is shared between fabric logic and MDDR/FDDR whereas MSIO/MSIOD is shared between MSS peripherals and fabric logic. When an MDDR/FDDR controller or MSS peripheral is not used, the respective I/Os are available to fabric logic.

For functional block diagrams of MSIO, MSIOD, and DDRIO, refer to the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.
For supported I/O standards, refer to the "Supported Voltage Standards" table in the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

2.2 Bank Location Diagrams

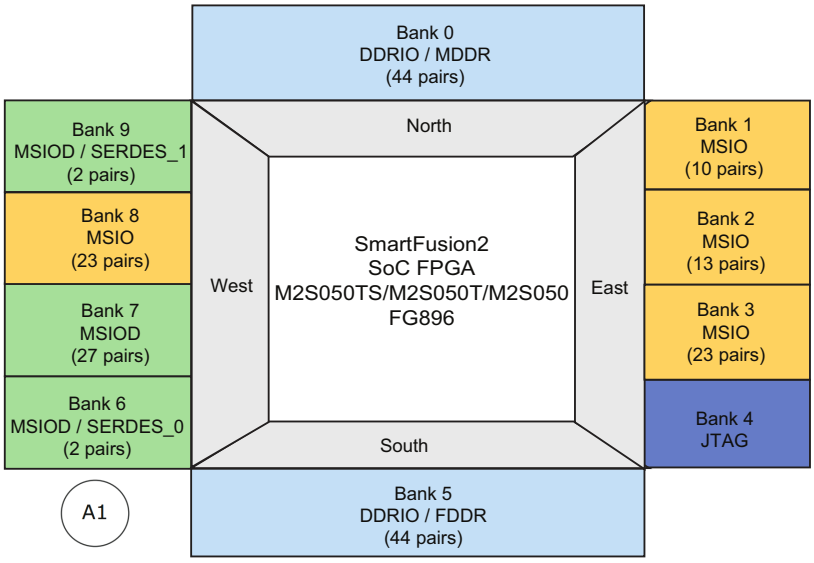
I/Os are grouped on the basis of I/O voltage standard. The grouped I/Os of each voltage standard form an I/O bank. Each I/O bank has dedicated I/O supply and ground voltages. Because of these dedicated supplies, only I/Os with compatible standards can be assigned to the same I/O voltage bank.

Figure 1 • **SmartFusion2 M2S150TS/M2S150T/M2S150-FC1152 I/O Bank Locations**



Note: For M2S150-FC1152 device, SERDES blocks are not available in bank 9, 10, 12, and 13.

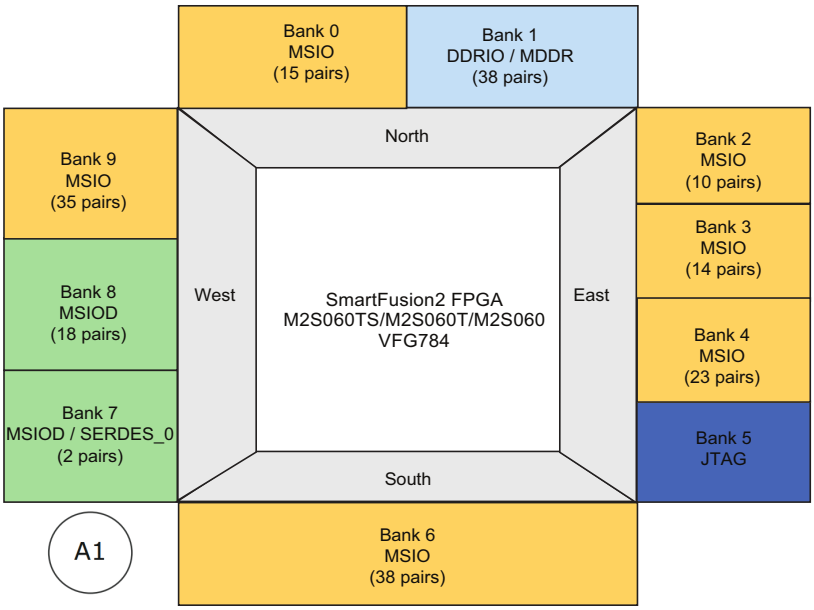
Figure 2 • **SmartFusion2 M2S050TS/M2S050T/M2S050-FG896 I/O Bank Locations**



Note: In bank 1, there are 21 single-ended user I/Os. Pin H27, MSI46NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI46NB1 is an input only pin.

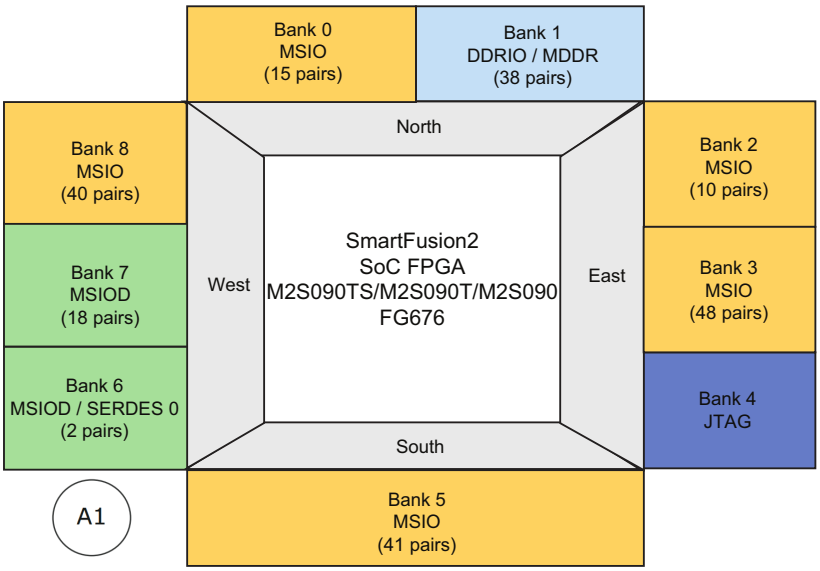
Note: For M2S050-FG896 device, SERDES blocks are not available in bank 6 and bank 9.

Figure 3 • **SmartFusion2 M2S060TS/M2S060T/M2S060-VFG784 I/O Bank Locations**



Note: In bank 2, there are 21 single-ended user I/Os. Pin C26 and MSI47NB2 is an input only when used to connect to the FPGA fabric.

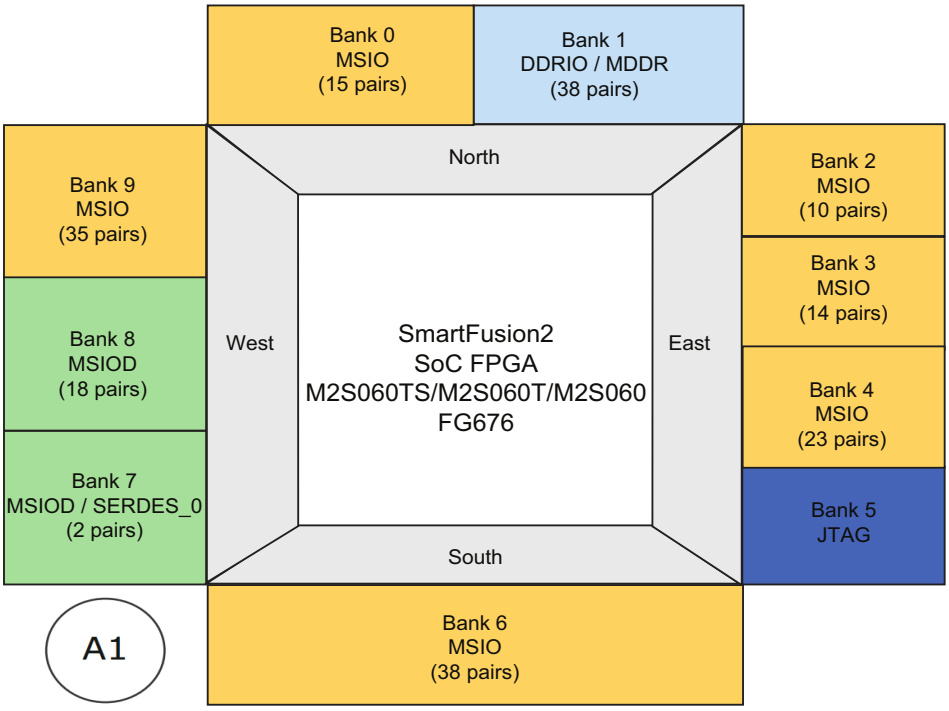
Figure 4 • **SmartFusion2 M2S090TS/M2S090T/M2S090-FG676 I/O Bank Locations**



Note: In bank 2, there are 21 single-ended user I/Os. Pin D23, MSI59NB2/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI59NB2 is an input only pin.

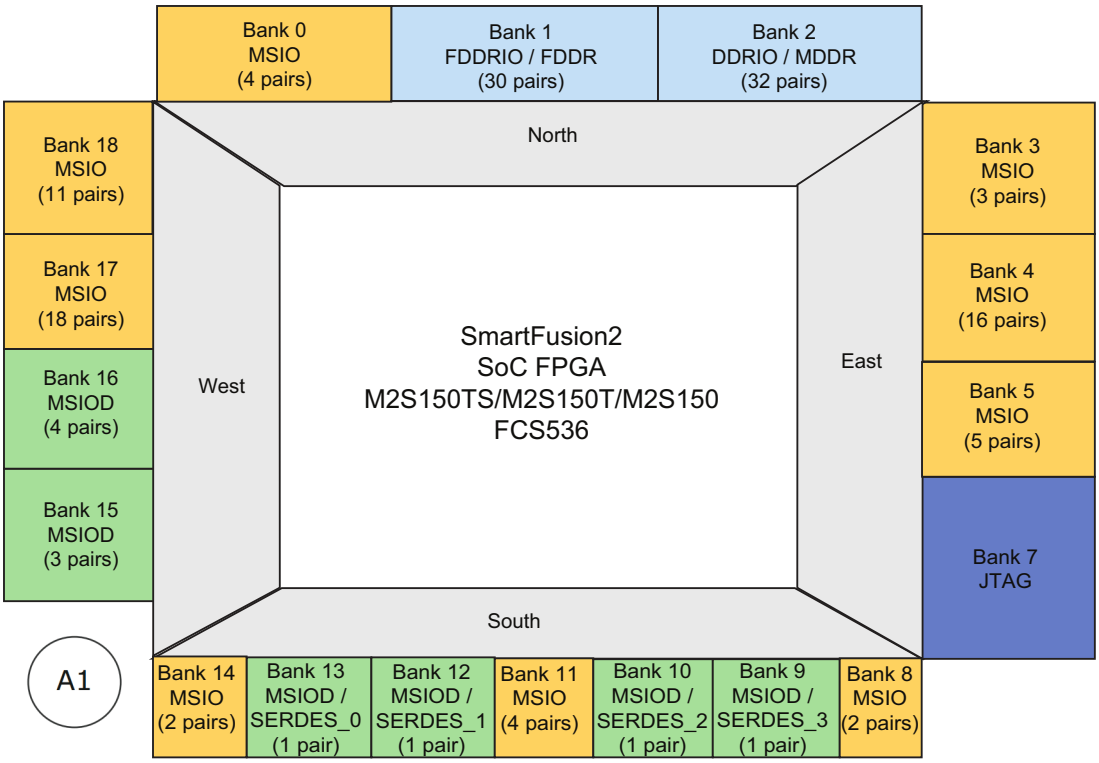
Note: For M2S090-FG676 device, the SERDES block is not available in bank 6.

Figure 5 • **SmartFusion2 M2S060TS/ M2S060T/M2S060-FG676 I/O Bank Locations**



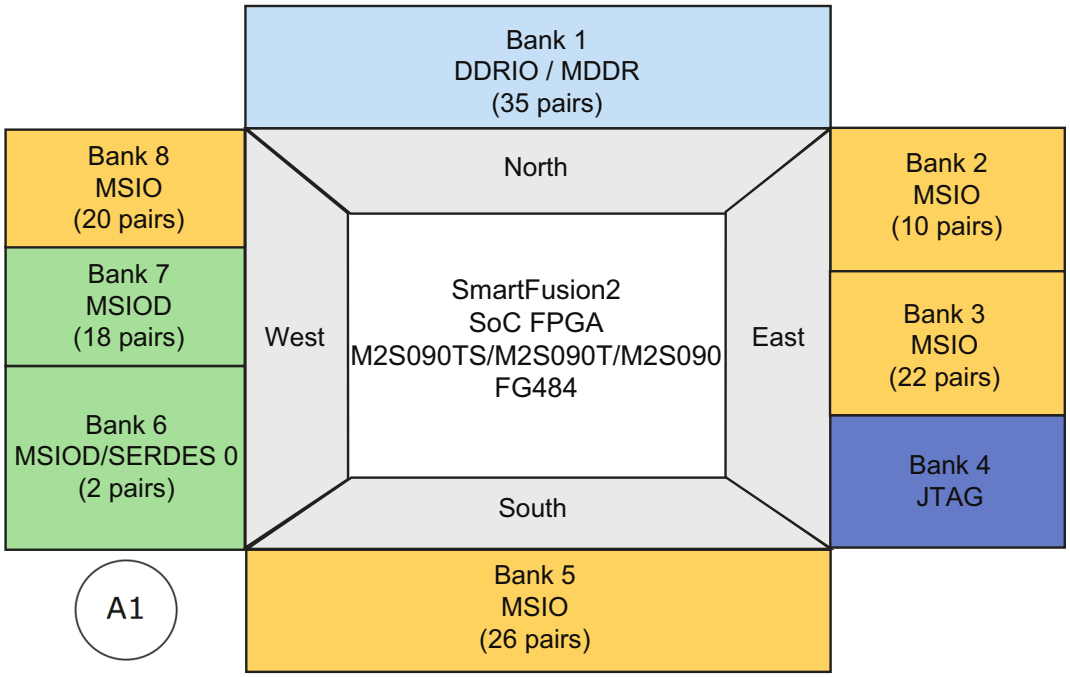
Note: For the M2S060-FG676 device, SERDES block is not available in bank 7.

Figure 6 • **SmartFusion2 M2S150TS/M2S150T/M2S150-FCS536 I/O Bank Locations**



Note: For the M2S150-FCS536 device, SERDES interface is not available in bank 9, 10, 12, and 13.

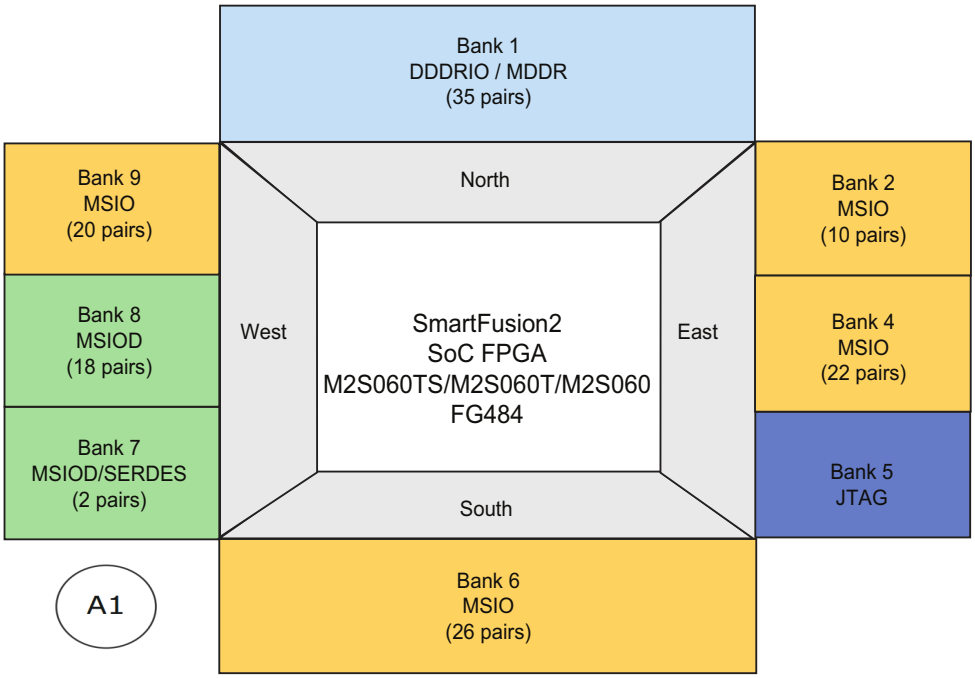
Figure 7 • **SmartFusion2 M2S090TS/M2S090T/M2S090-FG484 I/O Bank Locations**



Note: In bank 2, there are 21 single-ended user I/Os. Pin D21, MSI59NB2/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI59NB2 is an input only pin.

Note: For M2S090-FG484 device, SERDES block is not available in bank 6.

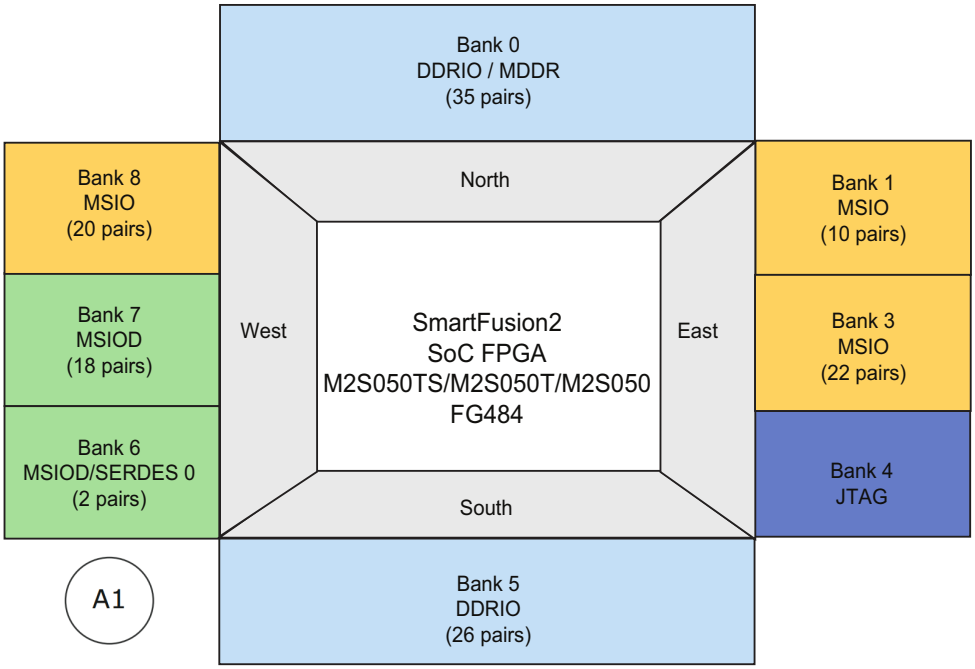
Figure 8 • **SmartFusion2 M2S060TS/M2S060T/M2S060-FG484 I/O Bank Locations**



Note: For the M2S060S-FG484 and M2S060-FG484 devices, SERDES block is not available in bank 7.

Note: In bank 2, there are 21 single-ended user I/Os. Pin D21, MSI47NB2/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI47NB2 is an input only pin.

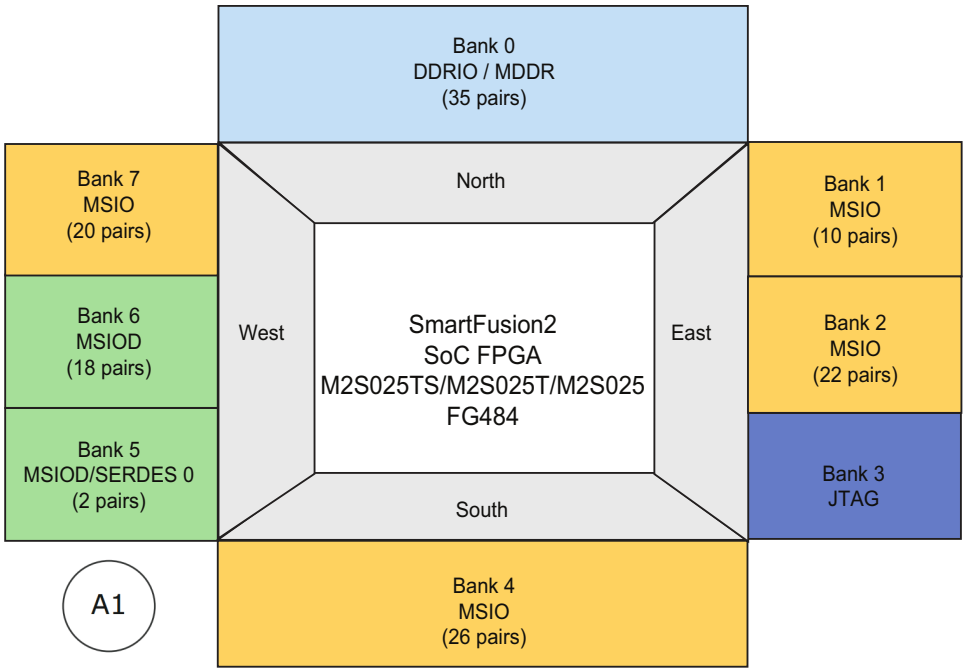
Figure 9 • **SmartFusion2 M2S050TS/M2S050T/M2S050-FG484 I/O Bank Locations**



Note: In bank 1, there are 21 single-ended user I/Os. Pin D21, MSI46NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI46NB1 is an input only pin.

Note: For M2S050-FG484 device, SERDES block is not available in bank 6.

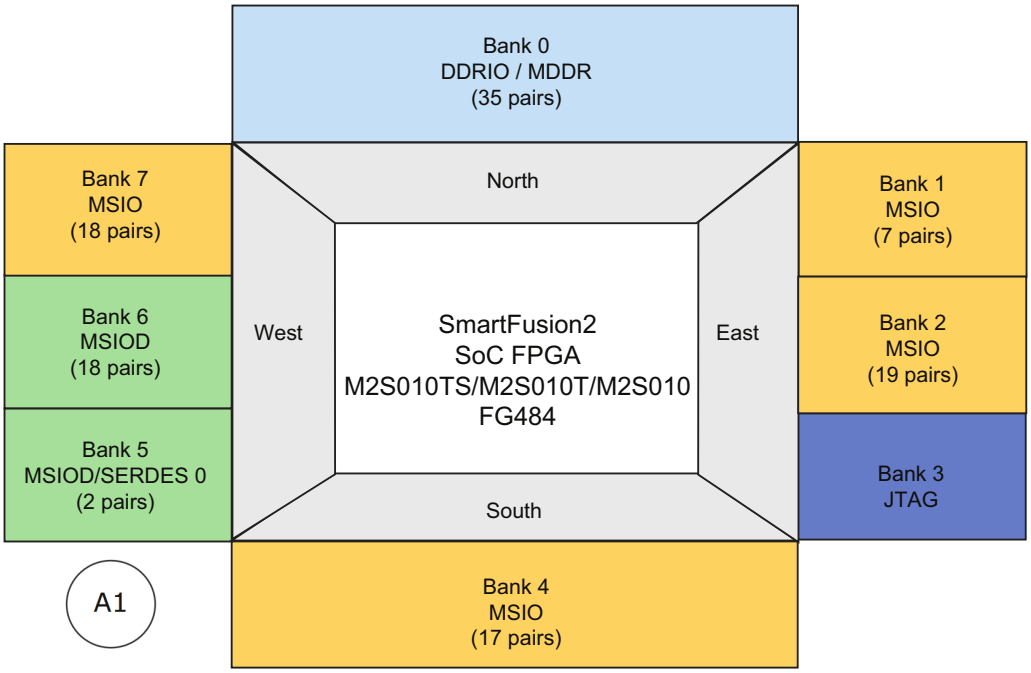
Figure 10 • **SmartFusion2 M2S025TS/M2S025T/M2S025-FG484 I/O Bank Locations**



Note: In bank 1, there are 21 single-ended user I/Os. Pin D21, MSI32NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI32NB1 is an input only pin.

Note: For M2S025-FG484 device, SERDES block is not available in bank 5.

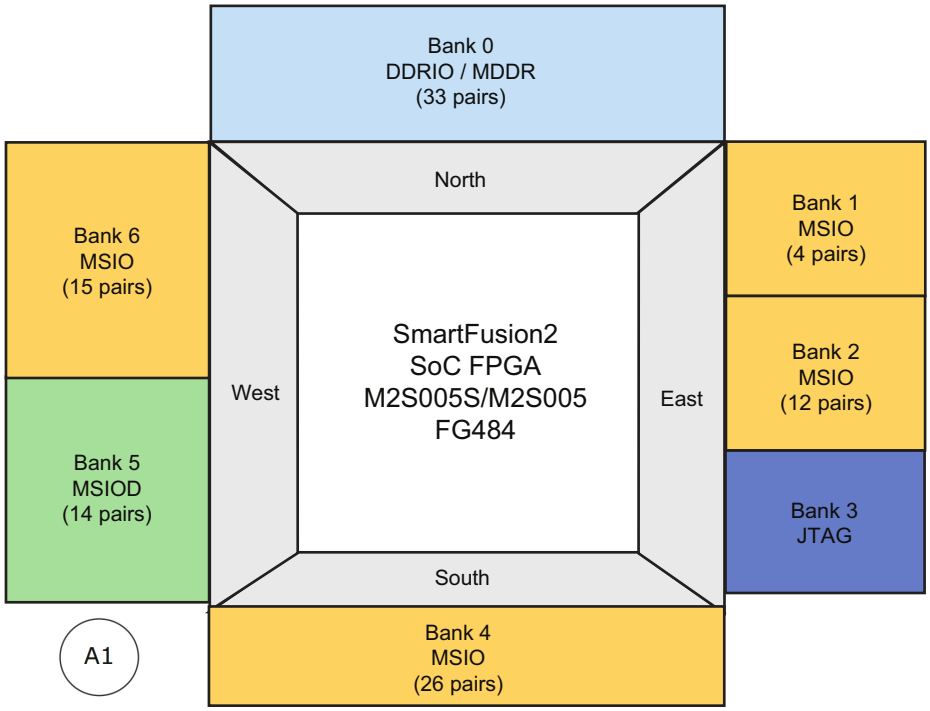
Figure 11 • **SmartFusion2 M2S010TS/M2S010T/M2S010-FG484 I/O Bank Locations**



Note: In bank 1, there are 15 single-ended user I/Os. Pin D21, MSI26NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI32NB1 is an input only pin.

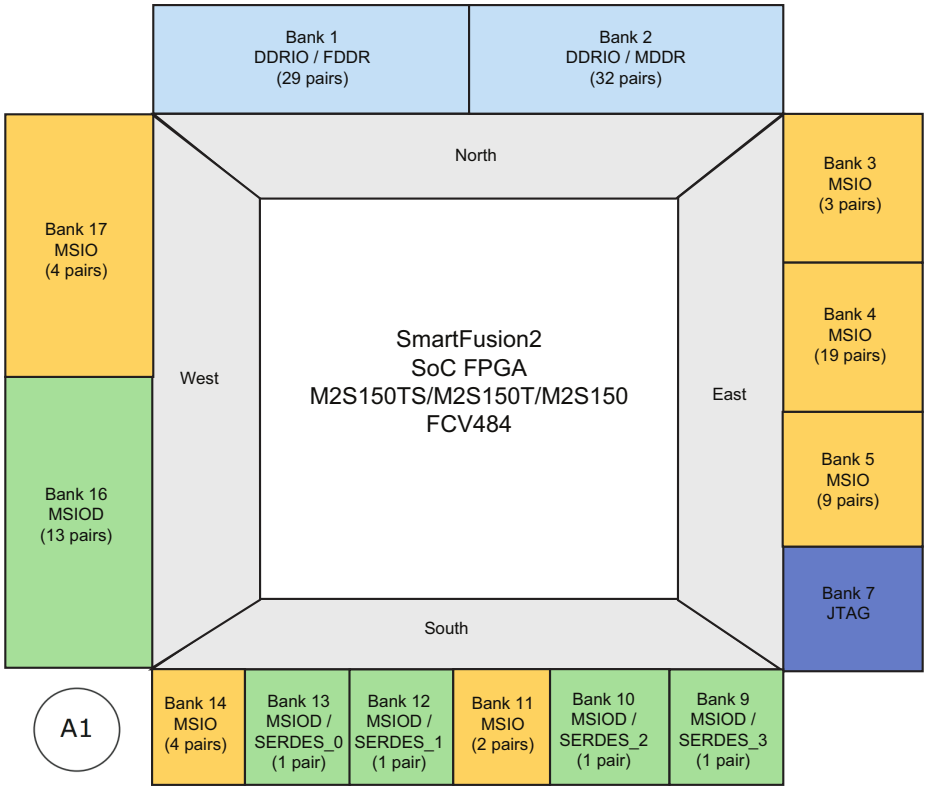
Note: For M2S010-FG484 device, SERDES block is not available in bank 5.

Figure 12 • **SmartFusion2 M2S005S/M2S005-FG484 I/O Bank Locations**



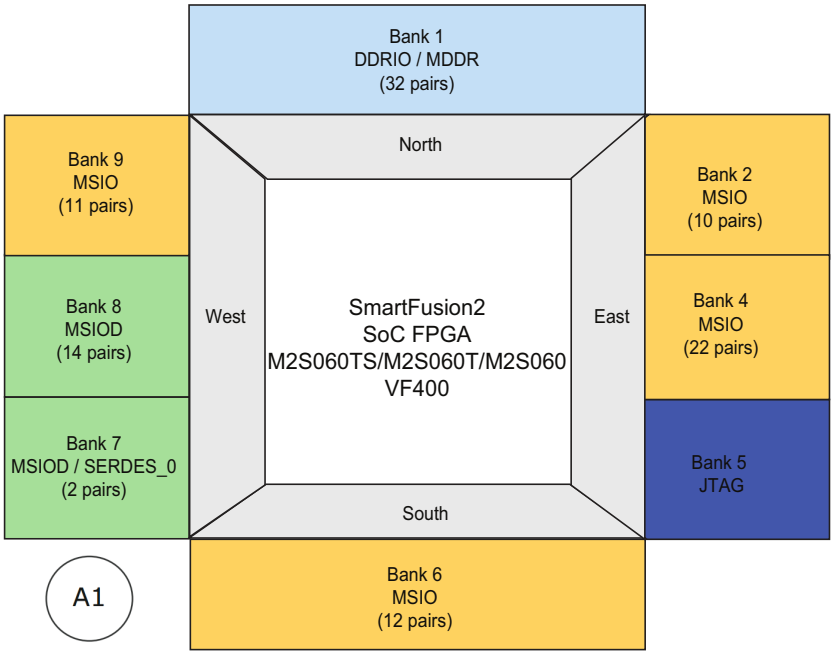
Note: In bank 1, there are 9 single-ended user I/Os. Pin D21, MSI16NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI16NB1 is an input only pin.

Figure 13 • **SmartFusion2 M2S150TS/M2S150T/M2S150-FCV484 I/O Bank Locations**



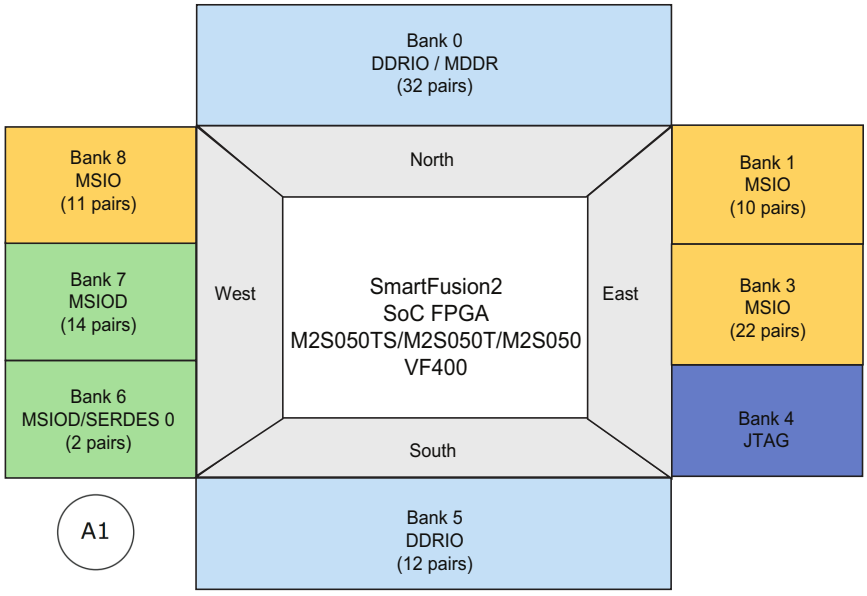
Note: For the M2S150-FCV484 device, SERDES block is not available in banks 9, 10, 12, and 13.

Figure 14 • **SmartFusion2 M2S060TS/M2S060T/M2S060-VF400 I/O Bank Locations**



Note: For the M2S060-VF400 device, SERDES block is not available in bank 7.

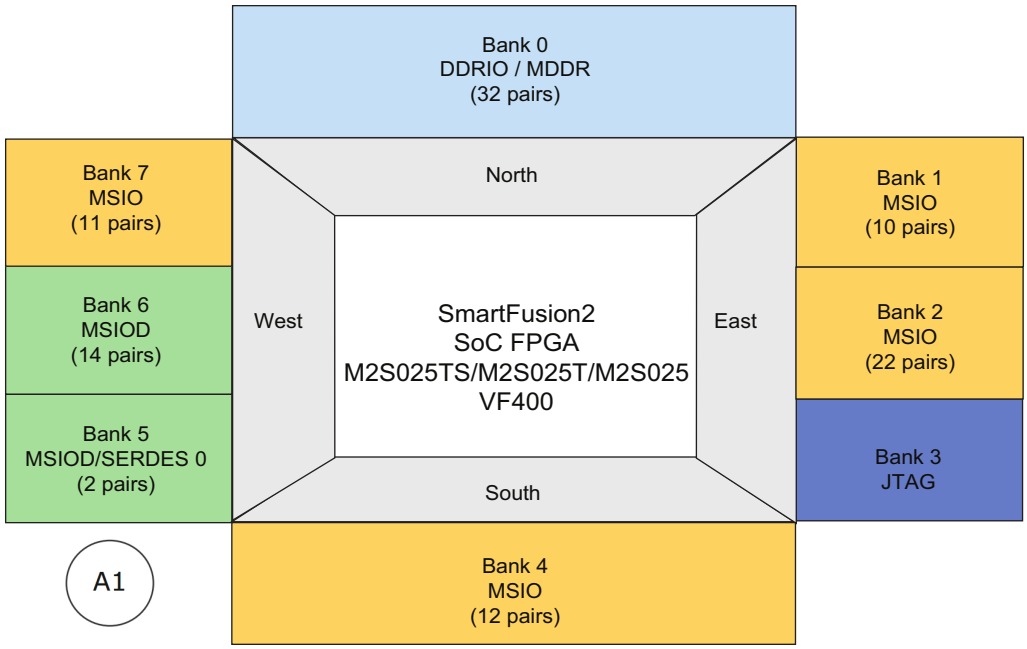
Figure 15 • **SmartFusion2 M2S050TS/M2S050T/M2S050-VF400 I/O Bank Locations**



Note: In bank 1, there are 21 single-ended user I/Os. Pin D18, MSI46NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI46NB1 is an input only pin.

Note: For M2S050-VF400 device, SERDES block is not available in bank 6.

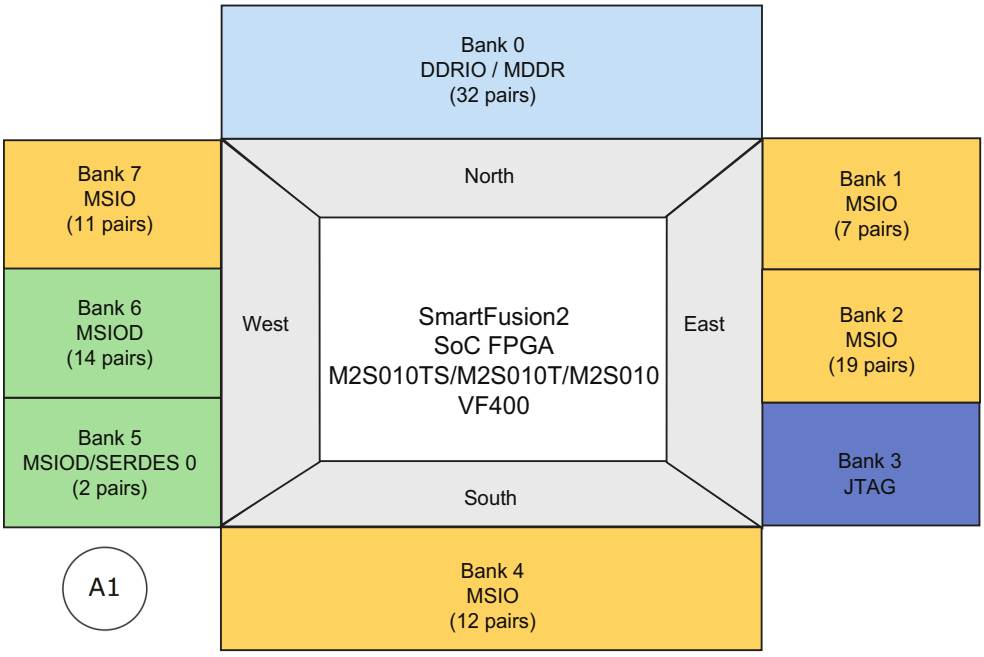
Figure 16 • **SmartFusion2 M2S025TS/M2S025T/M2S025-VF400 I/O Bank Locations**



Note: In bank 1, there are 21 single-ended user I/Os. Pin D18, MSI32NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI32NB1 is an input only pin.

Note: For M2S025-VF400 device, SERDES block is not available in bank 5.

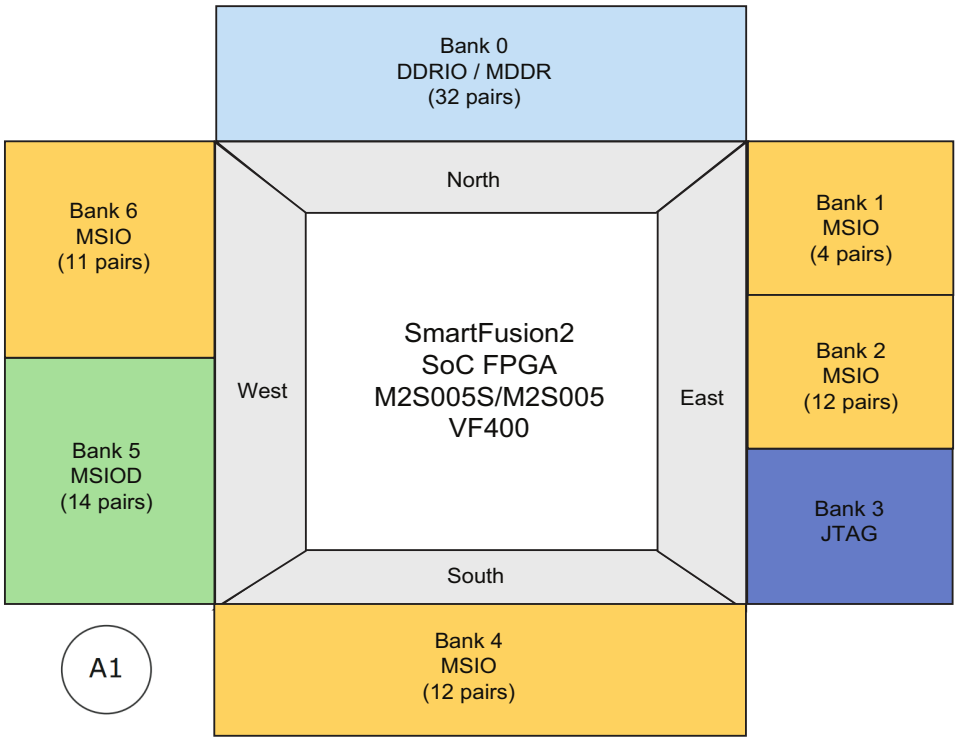
Figure 17 • **SmartFusion2 M2S010TS/M2S010T/M2S010-VF400 I/O Bank Locations**



Note: In bank 1, there are 15 single-ended user I/Os. Pin D18, MSI26NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI26NB1 is an input only pin.

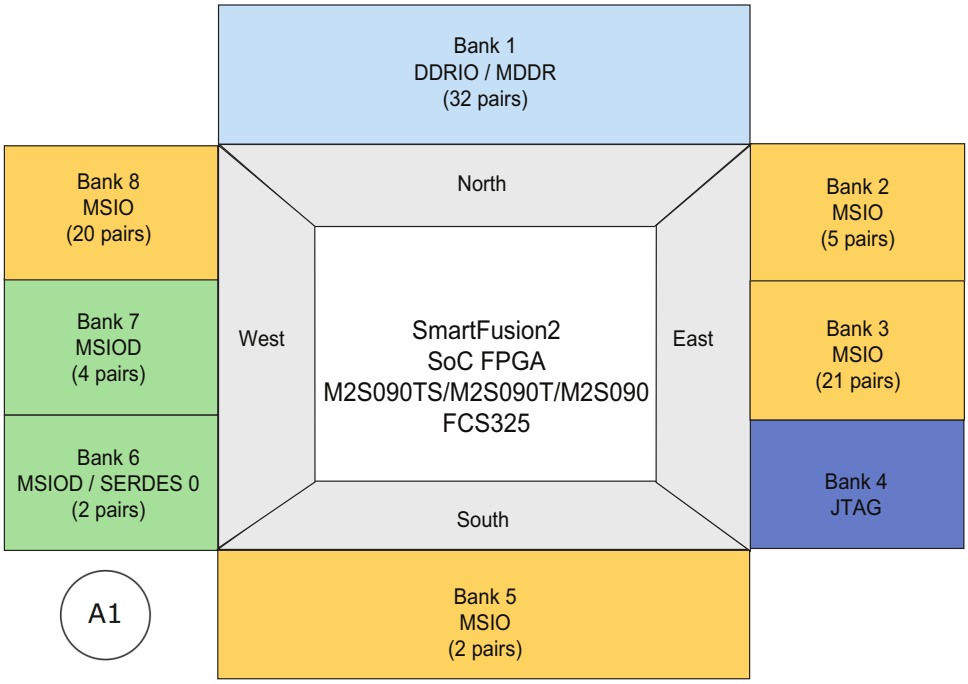
Note: For M2S010-VF400 device, SERDES block is not available in bank 5.

Figure 18 • **SmartFusion2 M2S005S/M2S005-VF400 I/O Bank Locations**



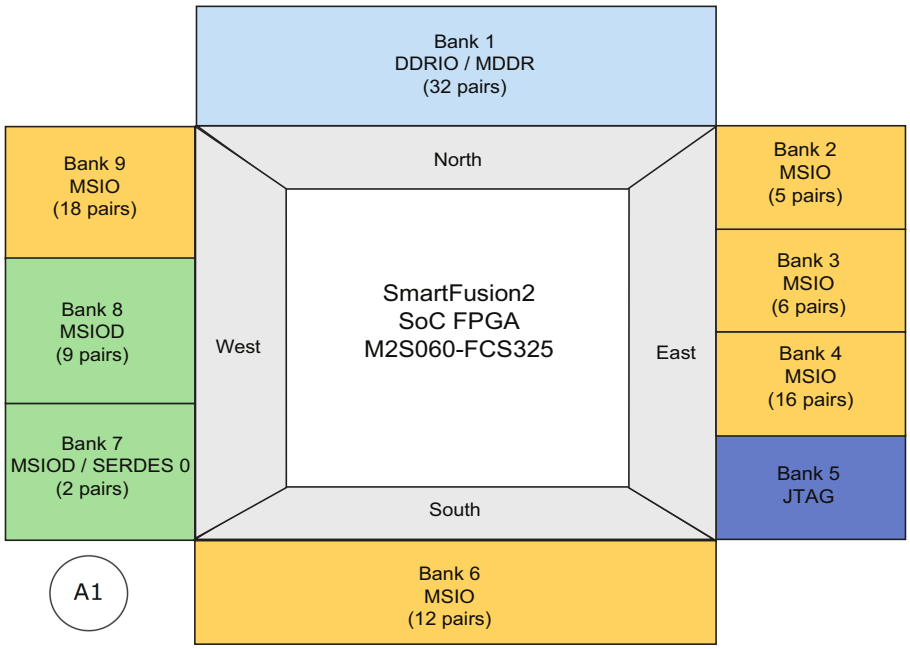
Note: In bank 1, there are 9 single-ended user I/Os. Pin D18, MSI16NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI16NB1 is an input only pin.

Figure 19 • **SmartFusion2 M2S090TS/M2S090T/M2S090-FCS325 I/O Bank Locations**



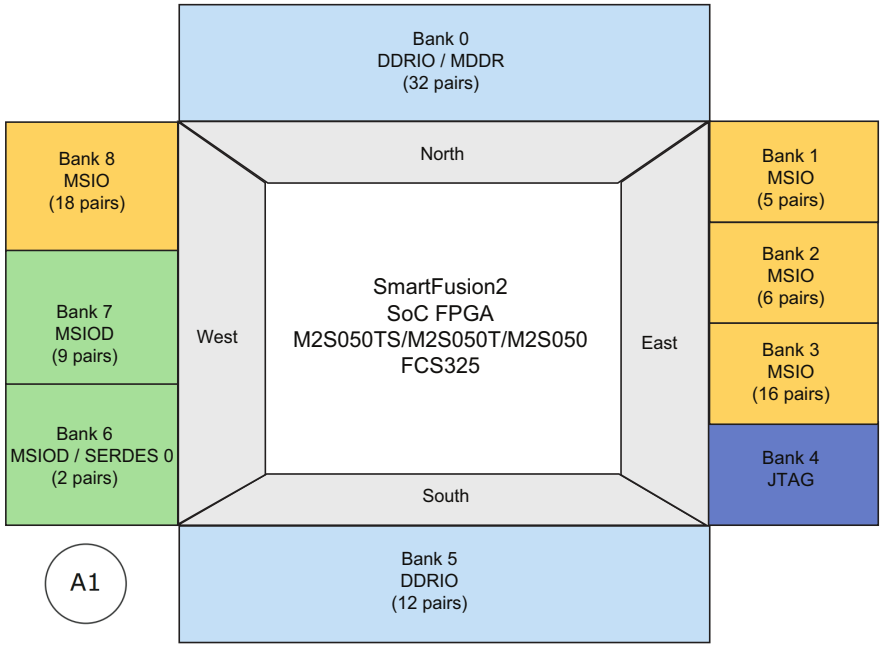
Note: For M2S090-FCS325 device, SERDES block is not available in bank 6.

Figure 20 • **SmartFusion2 M2S060-FCS325 I/O Bank Locations**



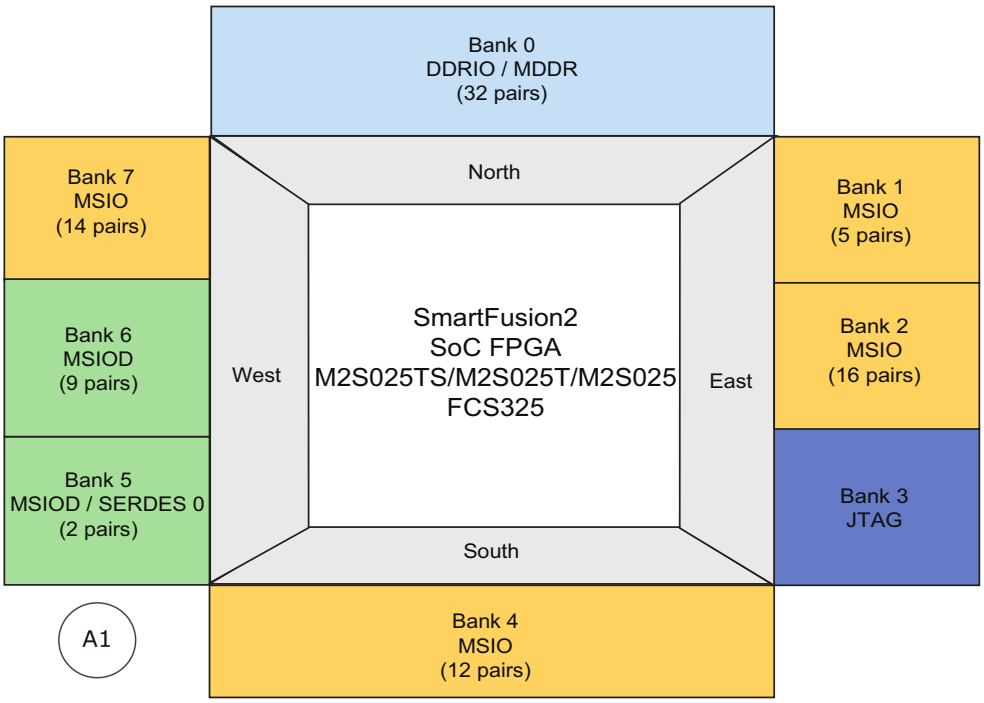
Note: For M2S060-FCS325 device, SERDES block is not available in bank 7.

Figure 21 • **SmartFusion2 M2S050TS/M2S050T/M2S050-FCS325 I/O Bank Locations**



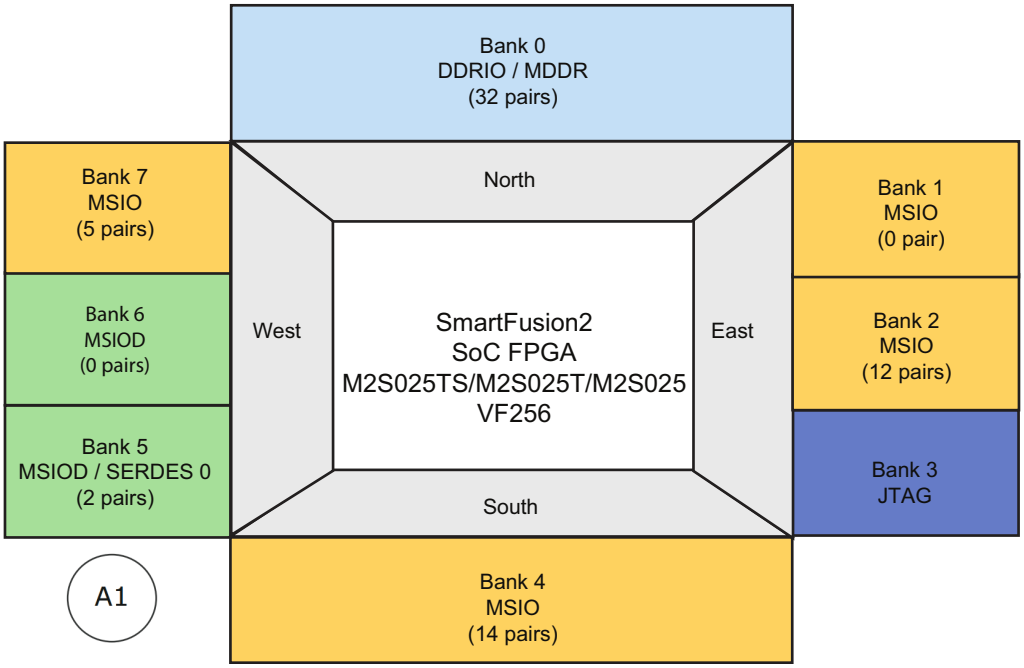
Note: For M2S050-FCS325 device, SERDES block is not available in bank 6.

Figure 22 • **SmartFusion2 M2S025TS/M2S025T/M2S025-FCS325 I/O Bank Locations**



Note: For M2S025-FCS325 device, SERDES block is not available in bank 5.

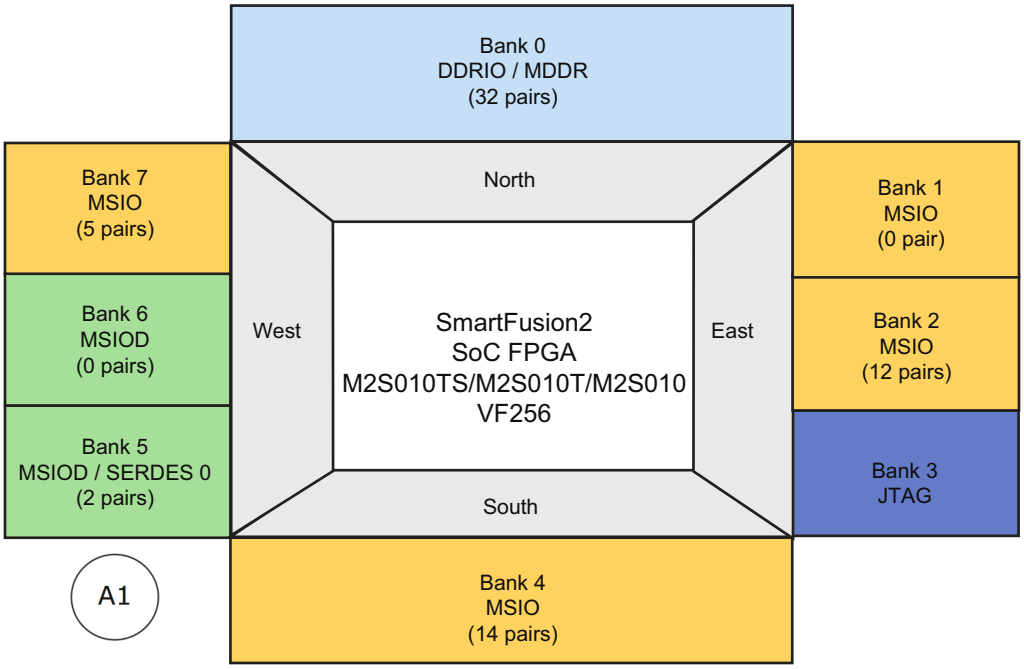
Figure 23 • **SmartFusion2 M2S025TS/M2S025T/M2S025-VF256 I/O Bank Locations**



Note: In bank 1, there are 4 single-ended user I/Os. Pin G12, MSIO32NB1/MMUART_0_TXD/GPIO_27_B, cannot be configured as differential. The function MSI32NB1 is an input only pin.

Note: For M2S025-VF256 device, SERDES block is not available in bank 5.

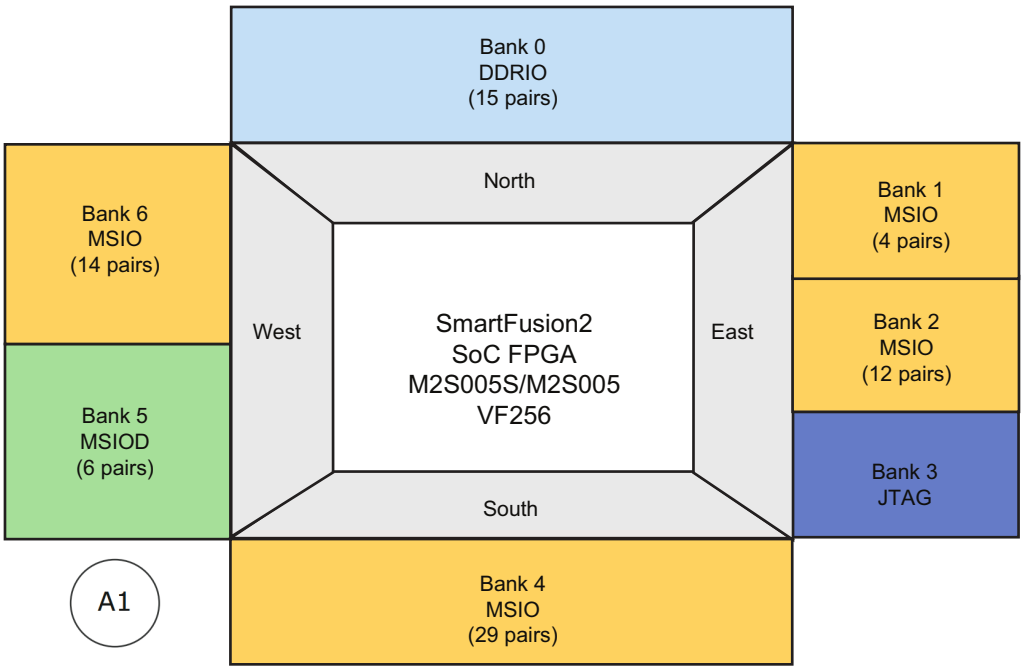
Figure 24 • **SmartFusion2 M2S010TS/M2S010T/M2S010-VF256 I/O Bank Locations**



Note: In bank 1, there are 4 single-ended user I/Os. Pin G12, MSI26NB1/MMUART_0_TXD/GPIO_27_B, cannot be configured as differential. The function MSI26NB1 is an input only pin.

Note: For M2S010-VF256 device, SERDES block is not available in bank 5.

Figure 25 • **SmartFusion2 M2S005S/M2S005-VF256 I/O Bank Locations**



Note: In bank 1, there are 9 single-ended user I/Os. Pin D12, MSI16NB1/MMUART_0_TXD/GPIO_27_B, cannot be configured as differential. The function MSI16NB1 is an input only pin.

Figure 26 • **SmartFusion2 M2S010-TQ144 I/O Bank Locations**

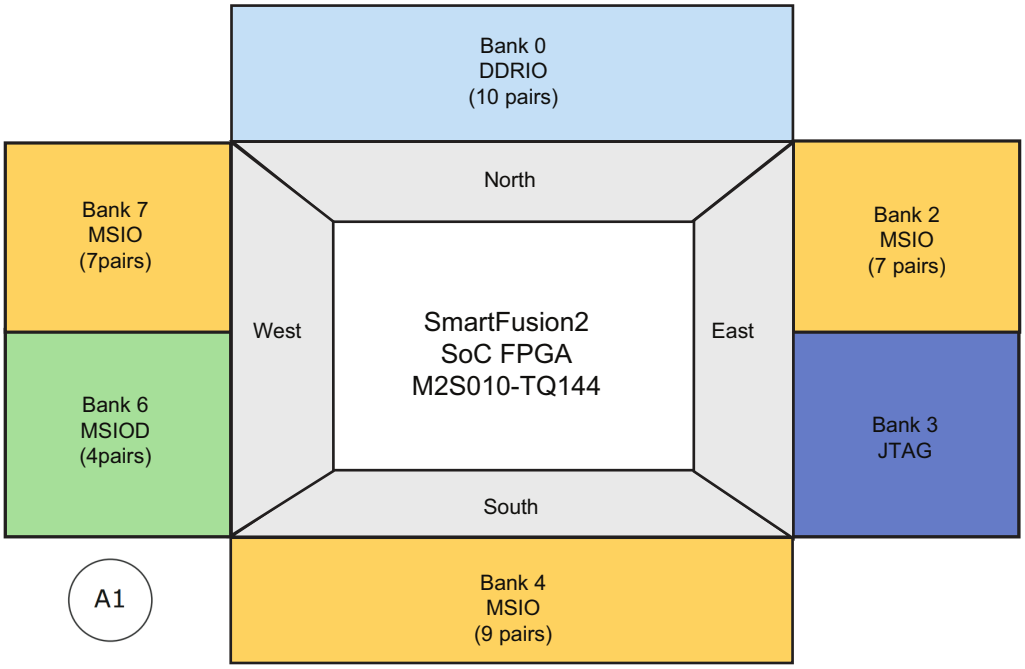


Figure 27 • **SmartFusion2 M2S005S/M2S005-TQ144 I/O Bank Locations**

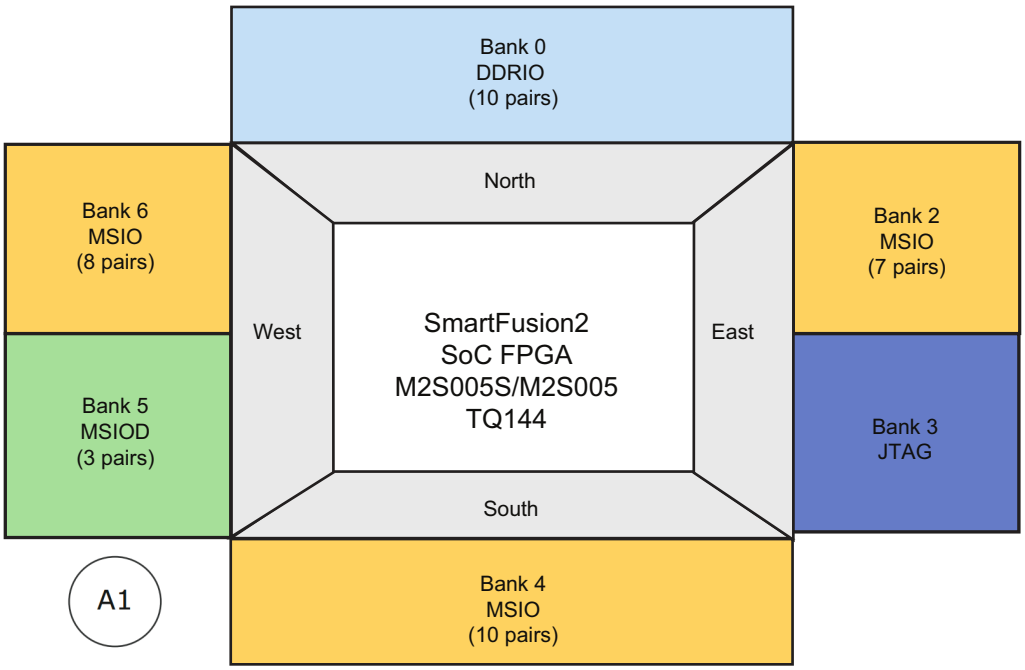


Table 1 • **Organization of I/O Banks in SmartFusion2 Devices—FC1152, FCS536, FCV484, FG896, and FG676[1]**

	FC1152	VFG784	FCS536	FCV484	FG896	FG676	
Bank No.	**M2S150TS M2S150T M2S150**	**M2S060TS M2S060T M2S060**	**M2S150TS M2S150T M2S150**	**M2S150TS M2S150T M2S150**	**M2S050TS M2S050T M2S050**	**M2S090TS M2S090T M2S090**	**M2S060TS M2S060T M2S060**
Bank 0	MSIO: fabric	MSIO: fabric	MSIO: fabric	–	DDRIO: MDDR or fabric	MSIO: fabric	MSIO: fabric

Table 1 • **Organization of I/O Banks in SmartFusion2 Devices—FC1152, FCS536, FCV484, FG896, and FG676[1]**

	FC1152	VFG784	FCS536	FCV484	FG896	FG676	
Bank No.	**M2S150TS M2S150T M2S150**	**M2S060TS M2S060T M2S060**	**M2S150TS M2S150T M2S150**	**M2S150TS M2S150T M2S150**	**M2S050TS M2S050T M2S050**	**M2S090TS M2S090T M2S090**	**M2S060TS M2S060T M2S060**
Bank 1	DDRIO: FDDR or fabric	DDRIO: MDDR or fabric	DDRIO: FDDR or fabric	DDRIO:FDDR or fabric	MSIO: MSS or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric
Bank 2	DDRIO: MDDR or fabric	MSIO: fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: fabric
Bank 3	MSIO: MSS or fabric	MSIO: fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: fabric
Bank 4	MSIO: MSS or fabric	MSIO: fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	JTAG/SWD	JTAG/SWD	MSIO: fabric
Bank 5	MSIO: MSS or fabric	JTAG/ SWD	MSIO: MSS or fabric	MSIO: MSS or fabric	DDRIO: FDDR or fabric	MSIO: fabric	JTAG/SWD
Bank 6	MSIO: fabric	MSIO: fabric	–	MSIO: fabric	MSIOD: SERDES 0 or fabric	MSIOD: SERDES 0 or fabric	MSIO: fabric
Bank 7	JTAG/ SWD	MSIOD: SERDES 0 or fabric	JTAG/ SWD	JTAG/ SWD	MSIOD: fabric	MSIOD: fabric	MSIOD: SERDES 0 or fabric
Bank 8	MSIO: fabric	MSIOD: fabric	MSIO: fabric	–	MSIO: fabric	MSIO: fabric	MSIOD: fabric
Bank 9	MSIOD: SERDES 3 or fabric	MSIO: fabric	MSIOD: SERDES 3 or fabric	MSIOD: SERDES 3 or fabric	MSIOD: SERDES 1 or fabric	–	MSIO: fabric
Bank 10	MSIOD: SERDES 2 or fabric	–	MSIOD: SERDES 2 or fabric	MSIOD: SERDES 2 or fabric	–	–	–
Bank 11	MSIO: fabric	–	MSIO: fabric	MSIO: fabric	–	–	–
Bank 12	MSIOD: SERDES 1 or fabric	–	MSIOD: SERDES 1 or fabric	MSIOD: SERDES 1 or fabric	–	–	–
Bank 13	MSIOD: SERDES 0 or fabric	–	MSIOD: SERDES 0 or fabric	MSIOD: SERDES 0 or fabric	–	–	–
Bank 14	MSIO: fabric	–	MSIO: fabric	MSIO: fabric	–	–	–
Bank 15	MSIOD: fabric	–	MSIOD: fabric	–	–	–	–
Bank 16	MSIOD: fabric	–	MSIOD: fabric	MSIOD: fabric	–	–	–
Bank 17	MSIO: fabric	–	MSIO: fabric	MSIO: fabric	–	–	–
Bank 18	MSIO: fabric	–	MSIO: fabric	–	–	–	–

1. Banks that are shaded should always be powered with the appropriate VDDI bank supplies.

Table 2 • **Organization of I/O Banks in SmartFusion2 FG484 Device[1]**

Bank No.	M2S090TS M2S090T M2S090	M2S060TS M2S060T M2S060	M2S050TS M2S050T M2S050	M2S025TS M2S025T M2S025	M2S010TS M2S010T M2S010	M2S005S
Bank 0	–	–	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric
Bank 1	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric
Bank 2	MSIO: MSS or fabric	MSIO: fabric	–	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric
Bank 3	MSIO: MSS or fabric	–	MSIO: MSS or fabric	JTAG/SWD	JTAG/SWD	JTAG/SWD
Bank 4	JTAG/SWD	MSIO: fabric	JTAG/SWD	MSIO: fabric	MSIO: fabric	MSIO: fabric
Bank 5	MSIO: fabric	JTAG/SWD	DDRIO: FDDR or fabric	MSIOD: SERDES 0 or fabric	MSIOD: SERDES 0 or fabric	MSIOD: fabric
Bank 6	MSIOD: SERDES 0 or fabric	MSIO: fabric	MSIOD: SERDES 0 or fabric	MSIOD: fabric	MSIOD: fabric	MSIO: fabric
Bank 7	MSIOD: fabric	MSIOD: SERDES 0 or fabric	MSIOD: fabric	MSIO: fabric	MSIO: fabric	–
Bank 8	MSIO: fabric	MSIOD: fabric	MSIO: fabric	–	–	–
Bank 9	–	MSIO: fabric	–	–	–	–
Bank 10	–	–	–	–	–	–
Bank 11	–	–	–	–	–	–
Bank 12	–	–	–	–	–	–
Bank 13	–	–	–	–	–	–
Bank 14	–	–	–	–	–	–
Bank 15	–	–	–	–	–	–
Bank 16	–	–	–	–	–	–
Bank 17	–	–	–	–	–	–
Bank 18	–	–	–	–	–	–

1. Banks that are shaded should always be powered with the appropriate VDDI bank supplies.

Table 3 • **Organization of I/O Banks in SmartFusion2 Devices—VF400 and TQ144[1]**

	VF400					TQ144	
Bank No.	M2S060TS M2S060T M2S060	M2S050TS M2S050T M2S050	M2S025TS M2S025T M2S025	M2S010TS M2S010T M2S010	M2S005S	M2S010	M2S005S
Bank 0	–	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: fabric	DDRIO: fabric
Bank 1	DDRIO: MDDR or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric		

Table 3 • **Organization of I/O Banks in SmartFusion2 Devices—VF400 and TQ144[1] *(continued)***

	VF400					TQ144	
Bank No.	**M2S060TS M2S060T M2S060**	**M2S050TS M2S050T M2S050**	**M2S025TS M2S025T M2S025**	**M2S010TS M2S010T M2S010**	**M2S005S**	**M2S010**	**M2S005S**
Bank 2	MSIO: fabric		MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric
Bank 3	–	MSIO: MSS or fabric	JTAG/SWD	JTAG/SWD	JTAG/SWD	JTAG/SWD	JTAG/SWD
Bank 4	MSIO: fabric	JTAG/SWD	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric
Bank 5	JTAG/SWD	DDRIO: FDDR or fabric	MSIOD: SERDES 0 or fabric	MSIOD: SERDES 0 or fabric	MSIOD: fabric	–	MSIOD: fabric
Bank 6	MSIO: fabric	MSIOD: SERDES 0 or fabric	MSIOD: fabric	MSIOD: fabric	MSIO: fabric	MSIOD: fabric	MSIO: fabric
Bank 7	MSIOD: SERDES 0 or fabric	MSIOD: fabric	MSIO: fabric	MSIO: fabric	–	MSIO: fabric	–
Bank 8	MSIOD: fabric	MSIO: fabric	–	–	–	–	–
Bank 9	MSIO: fabric	–	–	–	–	–	–

1. Banks that are shaded should always be powered with the appropriate VDDI bank supplies.

Table 4 • **Organization of I/O Banks in SmartFusion2 Devices—FCS325 and VF256[1]**

	FCS325					VF256	
Bank No.	**M2S090TS M2S090T M2S090**	**M2S060TS M2S060T M2S060**	**M2S050TS M2S050T M2S050**	**M2S025TS M2S025T M2S025**	**M2S025TS M2S025T M2S025**	**M2S010TS M2S010T M2S010**	**M2S005S**
Bank 0	–	–	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: fabric
Bank 1	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric
Bank 2	MSIO: fabric	MSIO: fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric	MSIO: MSS or fabric
Bank 3	MSIO: fabric	MSIO: fabric	MSIO: MSS or fabric	JTAG/SWD	JTAG/SWD	JTAG/SWD	JTAG/SWD
Bank 4	JTAG/SWD	MSIO: fabric	JTAG/SWD	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric
Bank 5	MSIO: fabric	JTAG/SWD	DDRIO: FDDR or fabric	MSIOD: SERDES 0 or fabric	MSIOD: SERDES 0 or fabric	MSIOD: SERDES 0 or fabric	MSIOD: fabric
Bank 6	MSIOD: SERDES 0 or fabric	MSIO: fabric	MSIOD: SERDES 0 or fabric	MSIO: fabric	MSIOD: fabric	MSIOD: fabric	MSIO: fabric

Table 4 • **Organization of I/O Banks in SmartFusion2 Devices—FCS325 and VF256[1] *(continued)***

	FCS325					VF256	
Bank No.	**M2S090TS M2S090T M2S090**	**M2S060TS M2S060T M2S060**	**M2S050TS M2S050T M2S050**	**M2S025TS M2S025T M2S025**	**M2S025TS M2S025T M2S025**	**M2S010TS M2S010T M2S010**	**M2S005S**
Bank 7	MSIOD: fabric	MSIOD: SERDES 0 or fabric	MSIOD: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	–
Bank 8	MSIO: fabric	MSIOD: fabric	MSIO: fabric	–	–	–	–
Bank 9	–	MSIO: fabric	–	–	–	–	–

1. Banks that are shaded should always be powered with the appropriate VDDI bank supplies.

Table 5 • **User I/O Types**

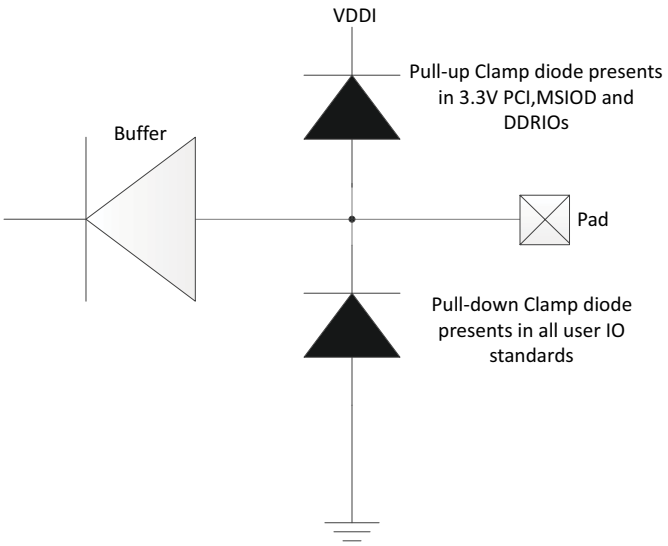
Name	Type	Description
MSIOxyBz	In/Out	MSIOs provide programmable drive strength, weak pull-up, and weak-pull-down. In single ended mode, the I/O pair operates as two separate I/Os named P and N. Some of these pins are also multiplexed with integrated peripherals in the MSS (I^2C, USB, SPI, UART, CAN, and fabric I/Os).This allows MSIO pins to be multiplexed as I/Os for the FPGA fabric, the ARM Cortex-M3 processor, or for given integrated MSS peripherals. MSIOs can be routed to dedicated I/O buffers (MSSIOBUF) or in some cases to the FPGA fabric interface through an IOMUX. SmartFusion2 I/O ports also support ESD protection. MSIO I/O cells operate at up to 3.3 V and are capable of high-speed LVDS2V5 and LVDS3V3 operation.
MSIODxyBz	In/Out	MSIOD is very similar to MSIO, but drops 3.3 V and hot-plug support and adds pre-emphasis, in order to achieve higher speeds. MSIODs provide programmable drive strength, weak pull-up, and weak pull-down. MSIOD I/O cells operate at up to 2.5 V and are capable of high-speed LVDS2V5 operation. Some of these pins are also multiplexed with the SERDES interface. SmartFusion2 I/O ports support ESD protection.
DDRIOxyBz	In/Out	The double data input output (DDRIO) is a multi-standard I/O optimized for LPDDR/DDR2/DDR3 performance. In SmartFusion2 devices there are two DDR subsystems: the fabric DDR and MSS DDR controllers. All DDRIOs can be configured as differential I/Os[1] or two single-ended I/Os. If you select MDDR/FDDR, Libero SoC automatically connects MDDR/FDDR signals to the DDRIOs. DDRIOs can be connected to the respective DDR subsystem PHYs or can be used as user I/Os. Depending on the memory configuration, only the required DDRIOs are used by Libero SoC. The unused DDRIOs are available to connect to the fabric. DDRIO supports a maximum of 2.5 V and does not support 3.3 V.

1. LVDS, RSDS, mini LVDS, BUSLVDS, MLVDS, and SUBLVDS are not supported with DDRIOs.

Note: For more information on I/O status of MSIO, MSIOD and DDRIO pins during power up/down and default conditions, refer to *AC396: SmartFusion2 and IGLOO2 in Hot Swapping and Cold Sparing Application Note*.

All user I/Os have internal clamp diode control circuitry. A pull-up clamp diode must not be present in the I/O circuitry if the hot-swap feature is used. The 3.3 V PCI standard requires a pull-up clamp diode on the I/O, so it cannot be selected if hot-swap capability is required.

Figure 28 • **Internal Clamp Diode Control Circuitry**



The following table lists I/O Banks that have clamp diodes.

Table 6 • **I/O Banks with Clamp Diode**

I/O Bank	I/O Standard	Clamp Diode
MSIO	PCI	Present
MSIO	All non-PCI standards	Not present
MSIOD	All I/O standards	Present
DDR	All I/O standards	Present

2.3 Naming Conventions

2.3.1 User I/O Naming Conventions

The naming convention used for each FPGA user I/O is **IOxyBz**, where:

IO is the type of I/O—MSIO, MSIOD, or DDRIO.

x refers the I/O pair number in bank z.

y is P (positive) or N (negative). In single-ended mode, the I/O pair operates as two separate I/Os named P and N. Differential mode is implemented with a fixed I/O pair and cannot be split with an adjacent I/O.

B is bank.

z refers to bank number (0–9 for M2S050-FG896).

Differential standards are implemented as true differential outputs and complementary single-ended outputs for SSTL/HSTL. In the single-ended mode, the I/O pair operates as two separate I/Os named P and N. All the configuration and data inputs/outputs are then separate and use names ending in P and N to differentiate between the two I/Os.

For more information, refer to the "I/Os" chapter of the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

2.3.2 Dedicated Global I/O Naming Conventions

Dedicated global I/Os are dual-use I/Os which can drive the global blocks either directly or through clock conditioning circuits (CCC) or virtual clock conditioning circuits (VCCC). They can also be used as regular user I/Os. These global I/Os are the primary source for bringing in the external clock inputs into the SmartFusion2 device.

In the M2S050T-FG896 device, there are 16 global blocks located in the center of the fabric and 32 global I/Os located 8 each on the north, east, south, and west sides of the fabric. There are 6 CCC blocks, located 2 each on northwest, northeast, and southwest side of the fabric and 2 VCCC blocks on the southeast side of the fabric.

Dedicated global I/Os that drive the global blocks (GB) directly are named as **GBn,** where

n is 0 to 15.

Dedicated global I/Os that drive GBs through CCCs are named as **CCC_xyz_CLKIw**, where:

xy is the location—NE, SW, or NW.

z is 0 or 1.

I represents input clock

w refers to one of the four possible output clocks of the associated CCC_xyz—GL0, GL1, GL2, or GL3.

Dedicated global I/Os that drive GBs through VCCCs are named as **VCCC_SEz**, where:

SE is southeast.

z is 0 or 1.

Unused dedicated global I/Os behave similarly to unused regular User I/Os (MSIO, MSIOD, DDRIO). Libero configures unused User I/Os as input buffer disabled, output buffer tri-stated with weak pull-up.

For further details, refer to the "Fabric Global Routing Resources" chapter of the *UG0449: SmartFusion2 SoC FPGA and IGLOO2 FPGA Clocking Resources User Guide*.

2.3.3 Multi-Function I/Os

Certain I/Os can have more than one function. Users select the functionality through Libero configuration tools.

The name of a pin shows the functionalities for which that pin can be configured and used.

Example pin name: **MSIO48NB1/I2C_0_SCL/GPIO_31_B/USB_DATA1_C**

This I/O port is multi-purpose and can be configured as MSIO, I2C0 clock, fabric I/O, or USB_DATA1_C.

2.4 MDDR/FDDR Interface

SmartFusion2 devices have MDDR/ FDDR blocks. The DDR subsystems are hardened ASIC blocks for interfacing the LPDDR, DDR2, and DDR3 memories. It supports 8-/16-/32-bit data bus width modes. The DDRIO uses fixed impedance calibration for different drive strengths. These values can be programmed using Libero SoC software for the selected I/O standard. The values are fed to the pull-up/pull-down reference network to match the impedance with an external resistor. For more information about reference resistor values (for different drive modes), refer to the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

2.4.1 DDR Controller Pins

The following table lists the DDR Controller pins.

Table 7 • **DDR Controller Pins[1]**

Pin Name	Type	Reference Resistor (Ω)
xDDR_CAS_N	Output	DRAM CASN.
xDDR_CKE	Output	DRAM Clock enable.
xDDR_CLK	Output	DRAM single-ended clock for differential pads.
xDDR_CLK_N	Output	DRAM single-ended clock for differential pads.
xDDR_CS_N	Output	DRAM Chip select.
xDDR_ODT	Output	DRAM on-die termination (ODT). 0: Termination Off 1: Termination On
xDDR_RAS_N	Output	DRAM RASN.
xDDR_RESET_N	Output	DRAM reset for DDR3.
xDDR_WE_N	Output	DRAM Write enable
xDDR_ADDR[15:0]	Output	DRAM address bits.
xDDR_BA[2:0]	Output	DRAM bank address.
xDDR_DM_RDQS[3:0]	Input/Output	DRAM data mask from bidirectional pads.
xDDR_DQS[3:0]	Input/Output	DRAM single-ended data strobe output for bidirectional pads.
xDDR_DQS[3:0]_N	Input/Output	DRAM single-ended data strobe output for bidirectional pads.
xDDR_DQ[31:0]	Input/Output	DRAM data input or output for bidirectional pads.
xDDR_DQ_ECC[3:0]	Input/Output	DRAM data input or output for SECDED.
xDDR_DM_RDQS_ECC	Input/Output	DRAM single-ended data strobe output for bidirectional pads.
xDDR_DQS_ECC	Input/Output	DRAM single-ended data strobe output for bidirectional pads.
xDDR_DQS_ECC_N	Input/Output	DRAM data input or output for bidirectional pads.
xDDR_TMATCH_[0/1]_IN	Input	DQS enable input for timing match between DQS and system clock. For simulations, tie to xDDR_TMATCH_[0/1]_OUT.

Table 7 • **DDR Controller Pins[1] *(continued)***

xDDR_TMATCH_[0/1]_OUT	Output	DQS enable output for timing match between DQS and system clock. For simulations, tie to xDDR_TMATCH_[0/1]_IN.
xDDR_TMATCH_ECC_IN	Input	DQS enable input for timing match between DQS and system clock. For simulations, tie to xDDR_TMATCH_ECC_OUT.
xDDR_TMATCH_ECC_OUT	Output	DQS enable output for timing match between DQS and system clock. For simulations, tie to xDDR_TMATCH_ECC_IN.
xDDR_IMP_CALIB	Ref	Pull-down with resistor depending on voltage/standard: DDR2 - 150 Ω DDR3 (1.5 V) - 240 Ω LPDDR - 150 Ω

1. Though calibration is not required, it is recommended to use corresponding resistor placeholder to connect the xDDR_IMP_CALIB to the ground with or without a resistor. x represents Fabric or MSS DDR.

For more information about DDR memory calibration, refer to the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

For DDR termination details refer *AN4153 Board and Layout Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs*.

2.4.2 I/O Standards

The following table lists the supported I/O standards for different DDR memories.

Table 8 • **Supported I/O Standards for Different DDR Memories**

Memory Type	I/O Standard
DDR3	SSTL15I, SSTL15II
DDR2	SSTL18I, SSTL18II
LPDDR	LVCMOS18

2.5 Supply Pins

SmartFusion2 devices support multi-standard I/Os (MSIOs), MSIODs, double data rate I/Os (DDRIOs), microcontroller serial interfaces, high speed serial interfaces, and a debugging JTAG interface. SmartFusion2 devices require the power supplies listed in the following table.

Table 9 • **Supply Pins**

Name	Type	Description
VDD	Supply	DC core supply voltage. Must always power this pin.
VPP	Supply[1]	Power supply for charge pumps (for normal operation and programming). Must always power this pin.
VPPNVM	Supply[1]	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP.
VDDIx	Bank power supplies[2]	VDDIx, Bank x power
VREFx	Supply[3]	Reference voltage for MDDR/FDDR signals which is powered through the corresponding Bank Supply (VDDIx). When **unused**, VREFx can be DNC or grounded (VSS).

Table 9 • **Supply Pins *(continued)***

Name	Type	Description
CCC_NE0_PLL_VDDA	PLL power supplies[4]	Analog power pad for PLL0
CCC_NE1_PLL_VDDA		Analog power pad for PLL1
CCC_NW0_PLL_VDDA		Analog power pad for PLL2
CCC_NW1_PLL_VDDA		Analog power pad for PLL3
CCC_SW0_PLL_VDDA		Analog power pad for PLL4
CCC_SW1_PLL_VDDA		Analog power pad for PLL5
MSS_MDDR_PLL_VDDA		Analog power pad for PLL of MDDR and MSS
FDDR_PLL_VDDA		Analog power pad for PLL of FDDR
SERDES_x_VDD	SERDESx power supplies[5]	It is a +1.2 V supply and for few devices SERDES_x_VDD is internally shorted to core VDD. For example, M2S150-FCV484 device.
SERDES_x_L01_VDDAIO		Tx/Rx analog I/O voltage. Low voltage power for Lane0 and Lane1 of SERDESIFx, located on the left side. It is a +1.2 V SERDES PMA supply.
SERDES_x_L23_VDDAIO		Tx/Rx analog I/O voltage. Low voltage power for Lane2 and Lane3 of SERDESIFx, located on the right side. It is a +1.2 V SERDES PMA supply.
SERDES_x_L01_VDDAPLL		Analog power for SERDESx PLL of Lane0 and Lane1. In used condition, it must be connected to +2.5 V. In unused condition, it can be connected to either +2.5 V or VDD (1.2 V).
SERDES_x_L23_VDDAPLL		Analog power for SERDESx PLL of Lane2 and Lane3. In used condition, it must be connected to +2.5 V. In unused condition, it can be connected to either +2.5 V or VDD (1.2 V).
SERDES_x_L01_REFRET		Local on-chip ground return path for SERDES_x_L01_VDDAPLL for Lane0 and Lane1 of SERDESIF0, located on the left side. If unused, it must be grounded (VSS).
SERDES_x_L23_REFRET		Local on-chip ground return path for SERDES_x_L23_VDDAPLL for Lane2 and Lane3 of SERDESIF0, located on the right side. If unused, it must be grounded (VSS).
SERDES_x_PLL_VDDA		High supply voltage for PLL SERDESx. It can be +2.5 V or +3.3 V.
SERDES_x_PLL_VSSA		VDDA to on-die VSSA high pass filter connection for PLL SERDESx. If unused, it must be grounded (VSS).
CCC_NE0_PLL_VSSA	PLL return paths[6]	Return path for corresponding analog PLL VDDA supply. High frequency noise should be eliminated by placing the R-C filter circuitry in between VDDA and VSSA pins.
CCC_NE_PLL_VSSA		
CCC_NW0_PLL_VSSA		
CCC_NW1_PLL_VSSA		
CCC_SW0_PLL_VSSA		
CCC_SW1_PLL_VSSA		
MSS_MDDR_PLL_VSSA		Analog ground pad for PLL of MDDR and MSS
FDDR_PLL_VSSA		Analog ground pad for PLL of FDDR
VSS	Ground	Ground pad for core and I/Os. Must always connect to ground.
VSSNVM		Analog sense circuit ground of eNVM. Must always connect to ground.

1. Lower pin count packages. The VPPNVM and VSSNVM pins are internal shorted to VPP and VSS, respectively and are not bonded out of silicon, for example, M2S150TS. For more information about VPP and VPPNVM power supplies, refer to Recommended Operating Conditions of *the IGLOO 2 FPGA and SmartFusion® 2 SoC FPGA Datasheet.*
2. For details on bank power supplies, refer to the “Recommendation for Unused Bank Supplies" table in the *AN4153 Board and Layout Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs.* For more details on user I/O pins (MSIO, MSIOD, DDRIO) and supported voltage standards, refer to the Supported Voltage Standards table in the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide.*
3. Reference voltages should be powered with the appropriate bank supplies through voltage divider circuitry. If I/O banks are being used as single-ended I/Os (and MDDR or FDDR functionalities are not being used), then VREFx can be left floating (DNC) even though the VDDIx powered to the corresponding supplies.
4. If used as PLL, the supply must be connected over resistor and capacitors (filter circuitry) to a common PLL supply (2.5 V or 3.3 V) to the corresponding on-board PLL return path. If PLL is unused or used as divider, the supply must connect directly to either 2.5 V or 3.3 V (without filter circuitry). Libero does not allow setting of 2.5 V and 3.3 V PLL supply for different kinds of PLL. Use either 2.5 V or 3.3 V PLL supply for all the PLL in the board as per the setting used in the Libero.
5. If used, all SERDES PLL pins must be powered through resistor and capacitors (filter circuitry) to the correct appropriate supply to the corresponding on-board return path. If unused must connect directly to the appropriate supplies (without filter circuitry).
6. If used, all CCC PLL pins must be powered through resistor and capacitors (filter circuitry) to the appropriate supply to the corresponding on-board return path on-board. If unused must connect directly to the Ground (without filter circuitry).

Note: For M2S090T(S), M2GL090T(S), M2S150T(S), and M2GL150T(S) devices, the VPP and VPPNVM must be connected to a 3.3 V supply.

2.5.1 Additional Notes on Supply Pins

- As an alternative to leaving unused positive and ground level supplies floating (not connected, open), they can be shorted to VSS on-board. This could be considered a better practice in avionics, so that floating supplies do not pick up charge from radiation.
- For on-board connectivity solutions, refer to the *AN4153 Board and Layout Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs*.

2.6 JTAG Pins

JTAG pins can operate at any voltage—1.2 V / 1.5 V / 1.8 V / 2.5 V / 3.3 V (nominal). The debug port is implemented using a serial wire JTAG debug port (SWJ-DP) rather than a serial wire debug port (SW-DP). This enables either the M3 JTAG or the SW protocol to be used for debugging.

Table 10 • **JTAG Pin Names and Descriptions**

Name	Type	Description	Unused Conditions
JTAGSEL	Input	JTAG controller selection. If JTAGSEL is pulled High, an external TAP controller connects to the JTAG interface—system controller TAP. If JTAGSEL is pulled Low, an external TAP controller connects to either the Cortex-M3 JTAG TAP (if debug is enabled) or an auxiliary TAP (if debug is disabled).	Pull-up to VDDI (JTAG bank) through a 1 KΩ resistor.
JTAG_TCK/ M3_TCK	Input	Test clock. Serial input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/pull-down resistor. If JTAG is not used, Microsemi recommends tying it off. Connect TCK through the 1 KΩ resistor to GND or +3.3 V through a resistor placed close to the FPGA pin.	Connect to either VDDI# (JTAG) or VSS through a 200 KΩ to 1 KΩ resistor.
JTAG_TDI/ M3_TDI	Input	Test data. Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.	Do not connect (DNC)
JTAG_TDO/ M3_TDO/ M3_SWO	Output	Test data. Serial output for JTAG boundary scan, ISP, and UJTAG usage. The TDO pin does not have an internal pull-up/-down resistor. M3_SWO: Serial Wire Viewer output	DNC

Table 10 • **JTAG Pin Names and Descriptions *(continued)***

Name	Type	Description	Unused Conditions
JTAG_TMS/ M3_TMS/ M3_SWDIO	Input	Test mode select. There is an internal weak pull-up resistor on the TMS pin. M3_SWDIO: Serial Wire Debug data input/output	DNC
JTAG_TRSTB/ M3_TRSTB	Input	Boundary scan reset pin. The TRSTB pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRSTB pin. In critical applications, an upset in the JTAG circuit could allow entering an undesired JTAG state. In such cases, Microsemi recommends that you tie off TRSTB to GND through a resistor (1 k) placed close to the FPGA pin.	DNC or pull-down to VSS through a 1 KΩ resistor for upset immunity.

2.7 Programming SPI

The system controller contains a dedicated SPI block for programming. The SPI is operated in Slave mode. In Master mode, the SmartFusion2 device is interfaced with an external SPI flash device and the programming data is downloaded from it to the FPGA. In Slave mode, it is communicated with a remote device that initiates download of the programming data to the FPGA. SC_SPI interface can not be used to program the device in Master mode except for M2S050. SC_SPI work in Master and slave mode for M2S050 device. SC_SPI can be configured only in Slave mode. SPI_0 is used in SPI master mode.

Table 11 • **Programming SPI Interface**

Name	Type	Description	Unused Conditions
SC_SPI_SS	Output	SPI slave select	DNC
SC_SPI_SDO	Output	SPI data output	DNC
SC_SPI_SDI	Input	SPI data input	DNC
SC_SPI_CLK	Output	SPI clock	DNC
FLASH_GOLDEN_N	Input	If pulled Low, this indicates that the device is to be re-programmed from an image in the external SPI flash attached to the SPI interface. If pulled High, the SPI is put into slave mode. Add an external pull-up resistor value of 10 kΩ to VDDI (Bank).	Pull-up to VDDI# through a 10 KΩ resistor.

Note: If unused, SPI programming pins must be left floating.

Note: For more details related to reset, clock, and programming, refer to *the AN4153 Board and Layout Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs.*

Note: For more information on remaining programming modes, refer to *the UG0451: SmartFusion2 and IGLOO2 Programming User Guide.*

2.8 Dedicated I/Os

Dedicated I/Os (Table 12, page 30 and Table 13, page 30) can be used for a single purpose such as SERDES, device reset, or clock functions. SmartFusion2 dedicated I/Os:

- Device reset pins
- Crystal oscillator pins
- SERDES I/Os
- Programming SPI pins

Table 12 • **Device Reset and Crystal Oscillator Pin Types and Descriptions**

Pin	Type	Description	Unused Conditions
Device Reset I/Os			
DEVRST_N	Input	Device reset; active Low and powered by VPP. It is an asynchronous signal and Schmitt trigger input with the maximum slew rate must not exceed 1 µs. When DEVRST_N is asserted, all user IOs are fully tri-stated. In unused condition, pull up to VPP through 10 kΩ resistor. Use the 3.3 V I/O standards specification. Any of the 3.3 V I/O standards like LVTTL/LVCMOS is applicable for DEVRST.	Pull-up to VPP through a 10 KΩ resistor.
Crystal Oscillator I/Os[1]			
XTLOSC_[MAIN/AUX]_EXTAL	Input	Crystal connection or external RC network.	DNC. Nominal 50 KΩ internal weak pull-up to VPP.
XTLOSC_[MAIN/AUX]_XTAL	Input	Input clock from the main/auxiliary crystal oscillator	

1. The M2S050 device has only a main crystal oscillator.

2.9 SERDES I/Os

The SERDES I/Os available in SmartFusion2 devices are dedicated for high speed serial communication protocols. The SERDES I/Os support protocols such as PCI Express 2.0, XAUI, serial gigabit media independent interface (SGMII), serial rapid IO (SRIO), and any user-defined high speed serial protocol implementation in fabric. Refer to the *AN4153 Board and Layout Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs* for further information.

Table 13 • **SERDES I/O Port Names and Descriptions**

Port Name	Type	Description	Unused Conditions
Data / Reference Pads			
SERDES_x_RXD[0:3]_P	Input	Receive data. SERDES differential input for each lane.	Pull-down to VSS through a 10 kΩ resistor. This is to improve latch-up immunity.
SERDES_x_RXD[0:3]_N			
SERDES_x_TXD[0:3]_P	Output	Transmit data. SERDES differential output for each lane.	DNC
SERDES_x_TXD[0:3]_N			

Table 13 • **SERDES I/O Port Names and Descriptions *(continued)***

Port Name	Type	Description	Unused Conditions
Common I/O Pads per SERDES Interface			
SERDES_x_L01_REXT	Reference	External reference resistor connection to calibrate TX/RX termination value.	DNC
SERDES_x_L23_REXT			DNC
SERDES_x_REFCLK[0:1]_P	Clock	Reference clock differential.	DNC
SERDES_x_REFCLK[0:1]_N	Clock	Reference clock differential.	DNC

2.10 Special Pins

The two live probe I/O cells are dual-purpose. If live probe functionality will never be used on these I/Os, the user can configure the I/O as an input, output, or bidirectional. However, if the intent is to perform live switching between the user I/O and probe functionality, then use the I/O only as an output. If it were configured as an input during general use, then as soon as it is switched over to live probe operation, the probe circuitry would drive out onto this I/O, potentially causing device damage.

Table 14 • **Special Pins**

Name	Type	Description
PROBE_A	Input/ Output	The two live probe I/O cells are dual-purpose—Live probe functionality and user I/O
PROBE_B		
CCC_xyz_CLKI0	Input	Input clock from dedicated input pad 0. The xy portion refers to the CCC location (NE, SW, SE, or NW) and z represents the CCC number (0 or 1).
CCC_xyz_CLKI1	Input	Input clock from dedicated input pad 1. The xy portion refers to the CCC location (NE, SW, SE, or NW) and z represents the CCC number (0 or 1).
CCC_xyz_CLKI2	Input	Input clock from dedicated input pad 2. The xy portion refers to the CCC location (NE, SW, SE, or NW) and z represents the CCC number (0 or 1).
CCC_xyz_CLKI3	Input	Input clock from dedicated input pad 3. The xy portion refers to the CCC location (NE, SW, SE, or NW) and z represents the CCC number (0 or 1).
GBx	Input	GB is a multiplexer that generates an independent global signal. The GBs can be driven from multiple sources such as dedicated global I/Os, fabric CCCs, VCCCs, and fabric routing
xDDR_TMATCH_[0/1]_IN	Input	DQS enable input for timing match between DQS and system clock. TMATCH_IN and TMATCH_OUT pins need to be looped back with the trace length as short as possible.
xDDR_TMATCH_[0/1]_OUT	Output	DQS enable output for timing match between DQS and system clock.
DNC	–	Do not connect. This pin should not be connected to any signals on the PCB; leave this pin unconnected.
NC	–	Do not connect. This pin is not connected to circuitry within the device. This pin can be driven to any voltage or can be left floating with no effect on the operation of the device.

2.11 Input Only Pins

These pins are differentially paired with Flash_golden_n (input only pin) and are input only when used to connect to the FPGA fabric. These pins can be used as output for the listed MSS peripherals.

Table 15 • **Input Only Pins**

Device	Pin	Description
M2S050T-FG896	H27	MSI46NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI46NB1 is an input only pin.
M2S060-VFG784	C26	MSI47NB2 is an input only when used to connect to the FPGA fabric.
M2S090T-FG676	D23	MSI59NB2/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI59NB2 is an input only pin.
M2S090T-FG484	D21	MSI59NB2/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI59NB2 is an input only pin.
M2S060T-FG484	D21	MSI47NB2/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI47NB2 is an input only pin.
M2S050T-FG484	D21	MSI46NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI46NB1 is an input only pin.
M2S025T-FG484	D21	MSI32NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI32NB1 is an input only pin.
M2S010T-FG484	D21	MSI26NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI32NB1 is an input only pin.
M2S005-FG484	D21	MSI16NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI16NB1 is an input only pin.
M2S060T-VF400	D18	MSI47NB2/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI46NB1 is an input only pin.
M2S050T-VF400	D18	MSI46NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI46NB1 is an input only pin.
M2S025T-VF400	D18	MSI32NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI32NB1 is an input only pin.
M2S010T-VF400	D18	MSI26NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI26NB1 is an input only pin.
M2S005-VF400	D18	MSI16NB1/MMUART_0_TXD/GPIO_27_B/USB_DIR_C, cannot be configured as differential. The function MSI16NB1 is an input only pin.
M2S025T-VF256	G12	MSI26NB1/MMUART_0_TXD/GPIO_27_B, cannot be configured as differential. The function MSI26NB1 is an input only pin.
M2S010T-VF256	G12	MSI26NB1/MMUART_0_TXD/GPIO_27_B, cannot be configured as differential. The function MSI26NB1 is an input only pin.
M2S005-VF256	D12	MSI16NB1/MMUART_0_TXD/GPIO_27_B, cannot be configured as differential. The function MSI16NB1 is an input only pin.

2.12 Microcontroller Subsystem (MSS)

Table 16 • **MSS Pin Names and Descriptions**

Name	Type	Description
Inter-Integrated Circuit (I^2C) Peripherals		
I2C_0_SCL	Input/Output	I^2C bus serial clock output.
I2C_0_SDA	Input/Output	I^2C bus serial data input/output.
I2C_1_SCL	Input/Output	I^2C bus serial clock output.
I2C_1_SDA	Input/Output	I^2C bus serial data input/output.
Universal Asynchronous Receiver/Transmitter (UART) Peripherals		
MMUART_0_CLK	Output	UART clock.
MMUART_0_TXD	Output	UART transmit data.
MMUART_0_RXD	Input	UART receive data.
MMUART_0_CTS	Input	UART clear to send.
MMUART_0_RTS	Output	UART request to send.
MMUART_0_DTR	Output	Modem data terminal ready.
MMUART_0_DCD	Input	Modem data carrier detects.
MMUART_0_DSR	Input	Modem data set ready.
MMUART_0_RI	Input	Modem ring indicator.
MMUART_1_CLK	Output	UART Clock.
MMUART_1_TXD	Output	UART transmit data.
MMUART_1_RXD	Input	UART receive data.
MMUART_1_CTS	Input	UART clear to send.
MMUART_1_RTS	Output	UART request to send.
MMUART_1_DTR	Output	Modem data terminal ready.
MMUART_1_DCD	Input	Modem data carrier detects.
MMUART_1_DSR	Input	Modem data set ready.
MMUART_1_RI	Input	Modem ring indicator.
Serial Peripheral Interface (SPI) Controllers		
SPI_0_SS0	Output	SPI slave select0.
SPI_0_SS1	Output	SPI slave select1.
SPI_0_SS2	Output	SPI slave select2.
SPI_0_SS3	Output	SPI slave select3.
SPI_0_SS4	Output	SPI slave select4.
SPI_0_SS5	Output	SPI slave select5.
SPI_0_SS6	Output	SPI slave select6.
SPI_0_SS7	Output	SPI slave select7.
SPI_0_CLK	Output	SPI clock.
SPI_0_SDO	Output	SPI data output.
SPI_0_SDI	Input	SPI data input.

Table 16 • **MSS Pin Names and Descriptions** ***(continued)***

Name	Type	Description
SPI_1_SS0	Output	SPI slave select0.
SPI_1_SS1	Output	SPI slave select1.
SPI_1_SS2	Output	SPI slave select2.
SPI_1_SS3	Output	SPI slave select3.
SPI_1_SS4	Output	SPI slave select4.
SPI_1_SS5	Output	SPI slave select5.
SPI_1_SS6	Output	SPI slave select6.
SPI_1_SS7	Output	SPI slave select7.
SPI_1_CLK	Output	SPI clock.
SPI_1_SDO	Output	SPI data output.
SPI_1_SDI	Input	SPI data input.

Note: All the pins can also be used as Fabric I/Os as all MSS pins are muxed with Fabric I/Os.

2.13 I/O Programmable Features

SmartFusion2 devices support different I/O programmable features for MSIO, MSIOD, and DDRIO. Each I/O pair (P, N) supports the following programmable features:

- Programmable drive strength
- Programmable weak pull-up and pull-down
- Configurable ODT and driver impedance
- Programmable input delay
- Programmable Schmitt input and receiver

For more information on SmartFusion2 I/O programmable features, refer to the "SmartFusion2 I/O Features" table of the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

2.14 Mechanical Drawings

The following illustrations show the top, bottom, and side views, and dimensions for the SmartFusion2.

2.14.1 FC1152

Figure 29 • **FC1152 Package Top-View and Side-View**

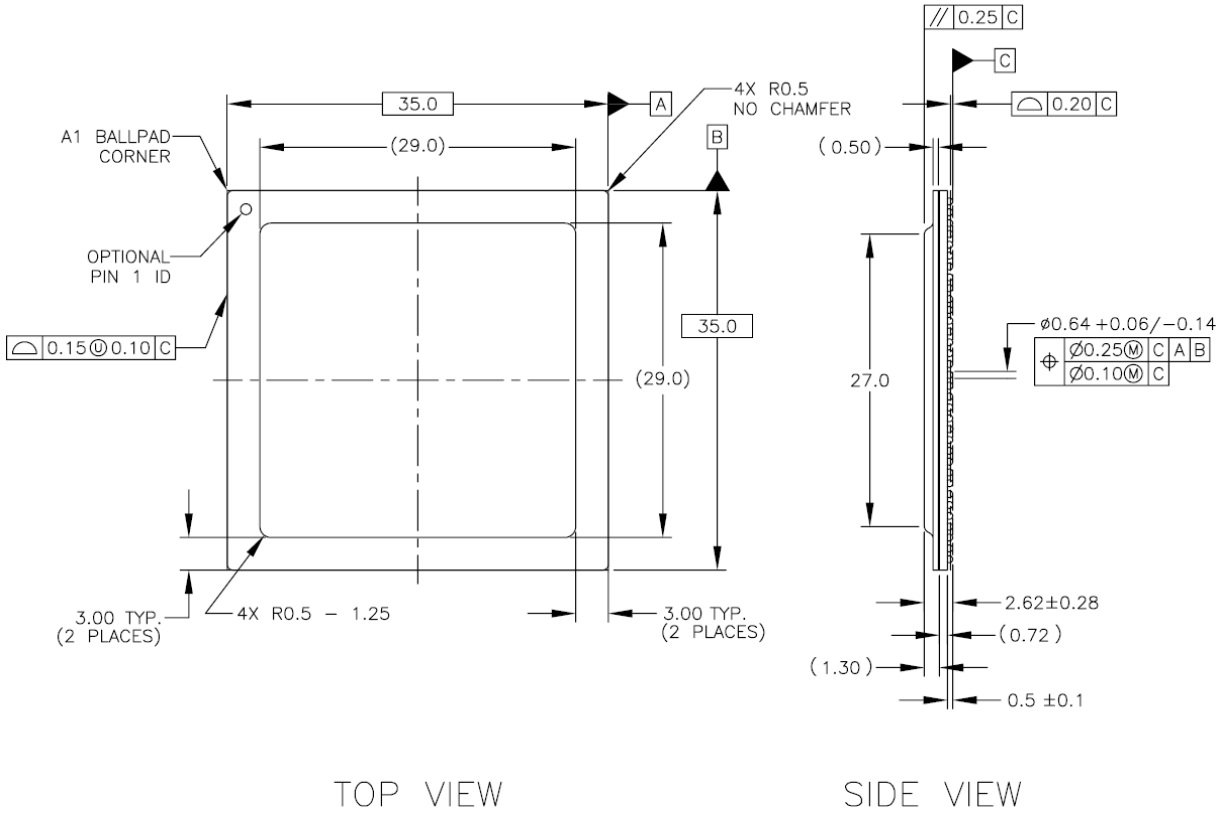
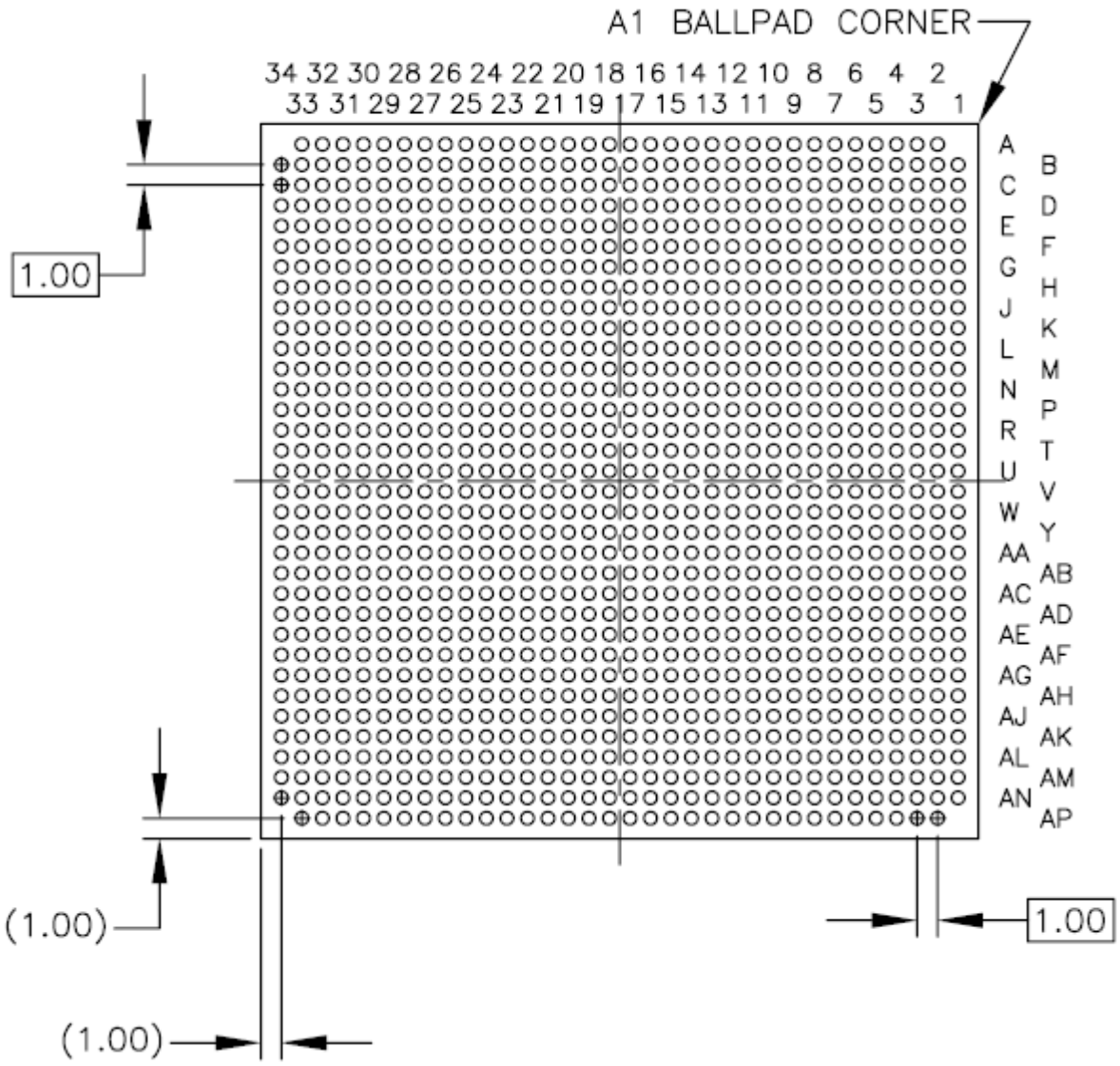


Figure 30 • **FC1152 Package Bottom-View**



2.14.1.1 Pin Tables

Pin tables for the FC1152 package depicted in the preceding figure are found in the Excel spreadsheet located here:

SmartFusion2 FC1152 Pinouts

The following devices are available in the FC1152: M2S150(T), (TS)

For more information on Layout Guidelines, see the *AN4153 Board and Layout Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs*.

2.14.2 FG896

Figure 31 • **FG896 Package Top-View and Side-View**

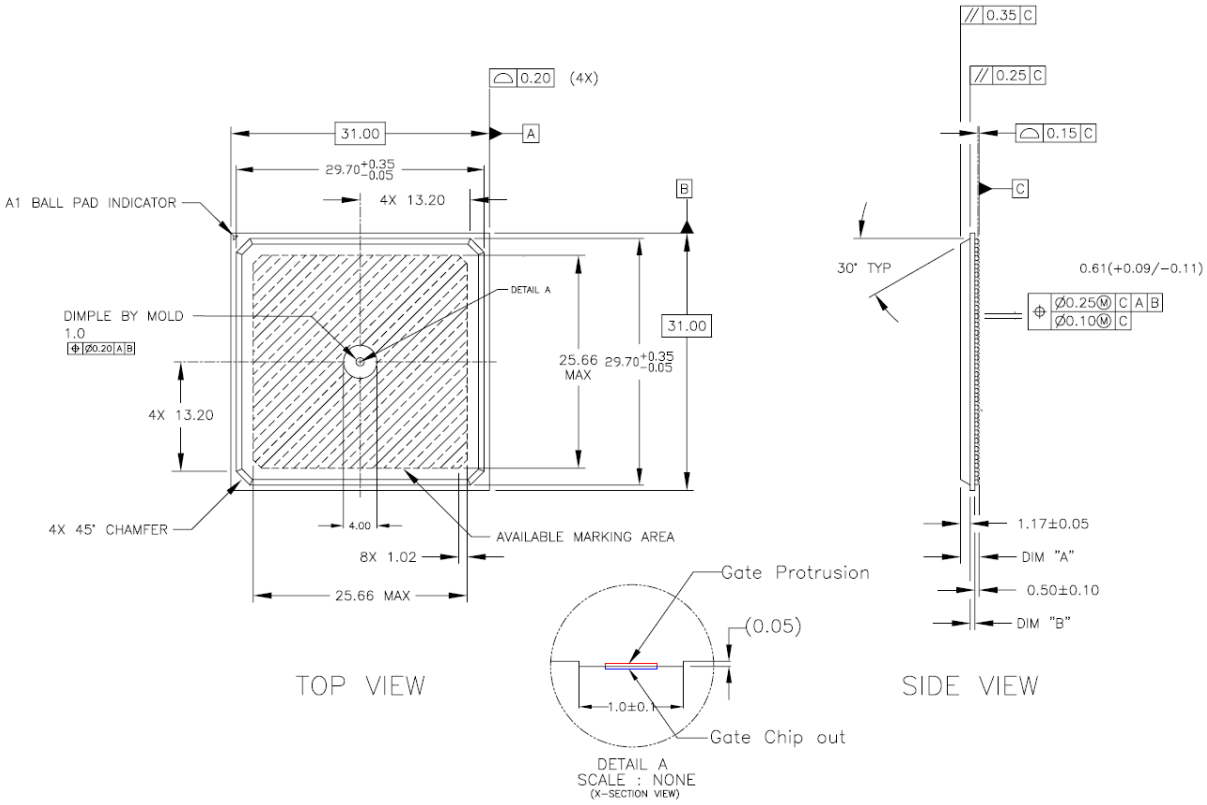
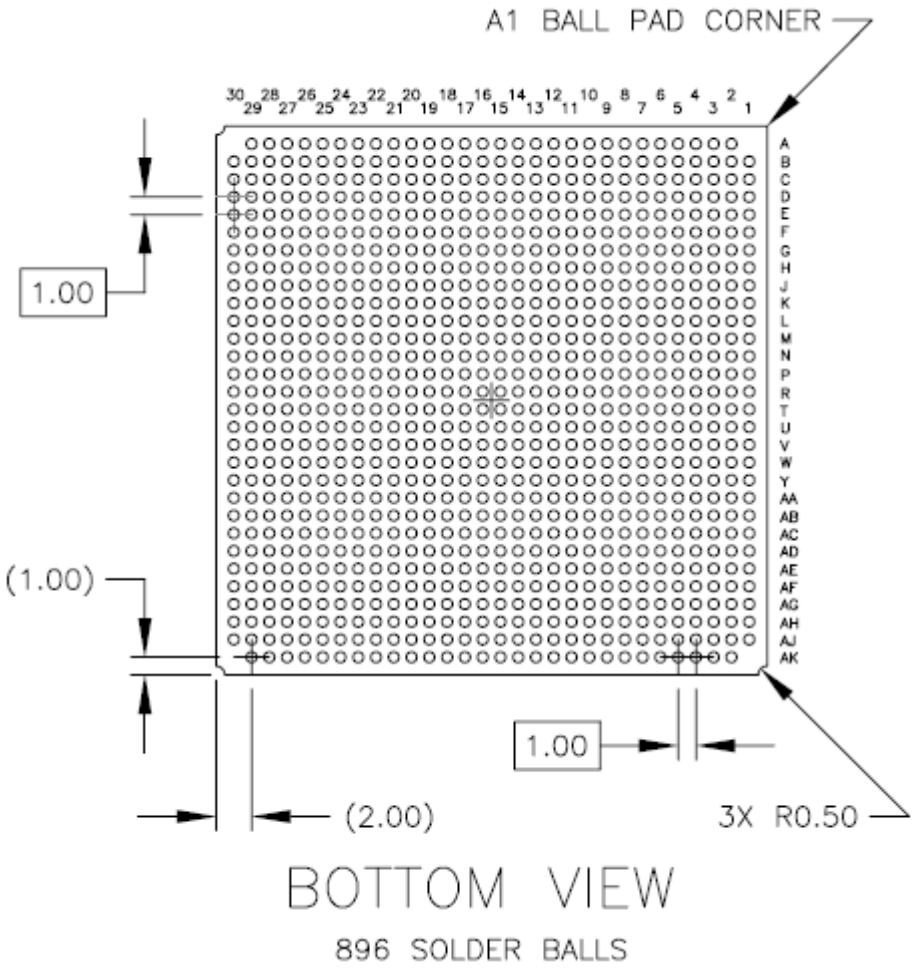


Figure 32 • **FG896 Package Bottom-View**



2.14.2.1 Pin Tables

Pin tables for the FG896 package depicted in the preceding figure are found in the Excel spreadsheet located here:

SmartFusion2 FG896 Pinouts

The following devices are available in the FG896: M2S050(T), (TS)

For more information on Layout Guidelines, see the *AN4153 Board and Layout Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs*.

2.14.3 VFG784

Figure 33 • **VFG784 Package Top-View and Side-View**

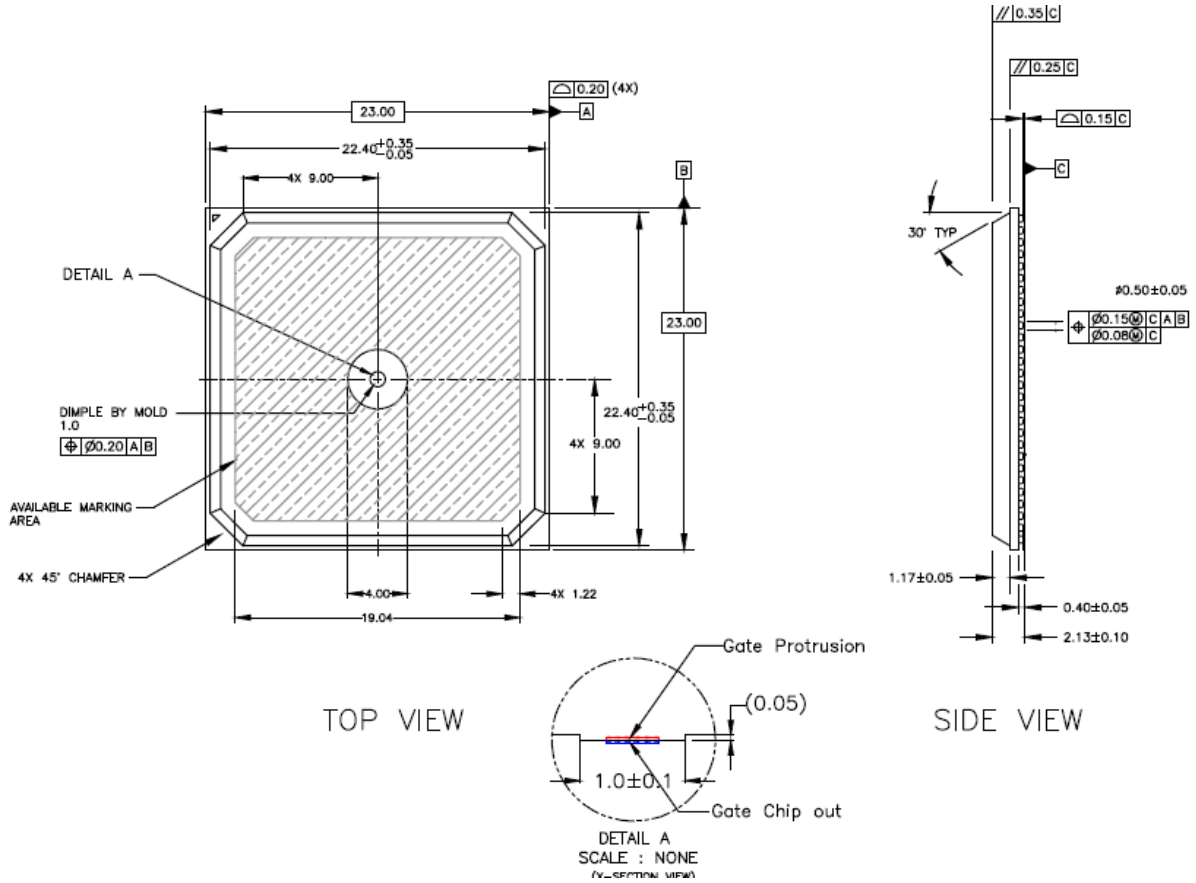
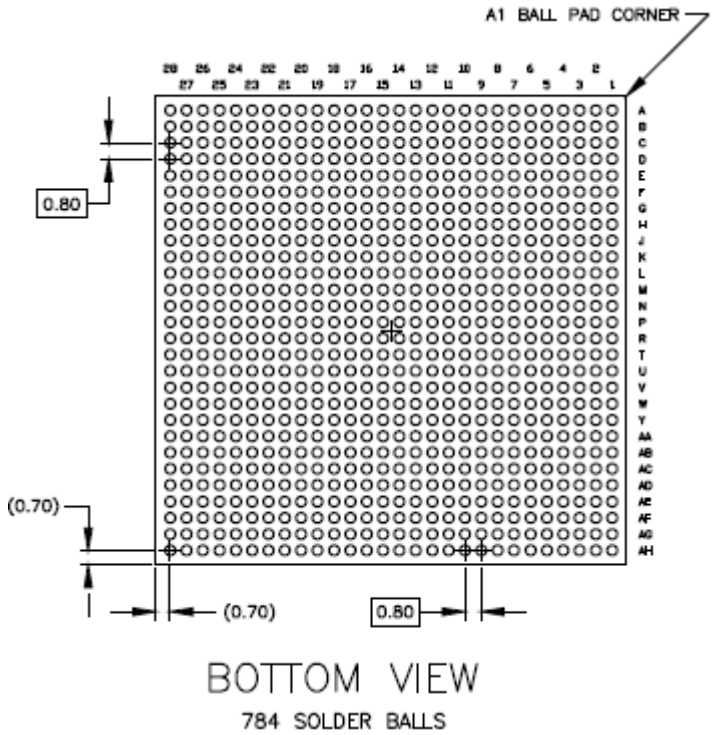


Figure 34 • **VFG784 Package Bottom-View**



2.14.3.1 Pin Tables

Pin tables for the VFG784 package depicted in the preceding figure are found in the Excel spreadsheet located here:

SmartFusion2 VFG784 Pinouts

The following devices are available in the VFG784: M2S060(T), (TS)

For more information on Layout Guidelines, see the *AN4153 Board and Layout Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs*.

2.14.4 FG676

Figure 35 • **FG676 Package Top-View and Side-View**

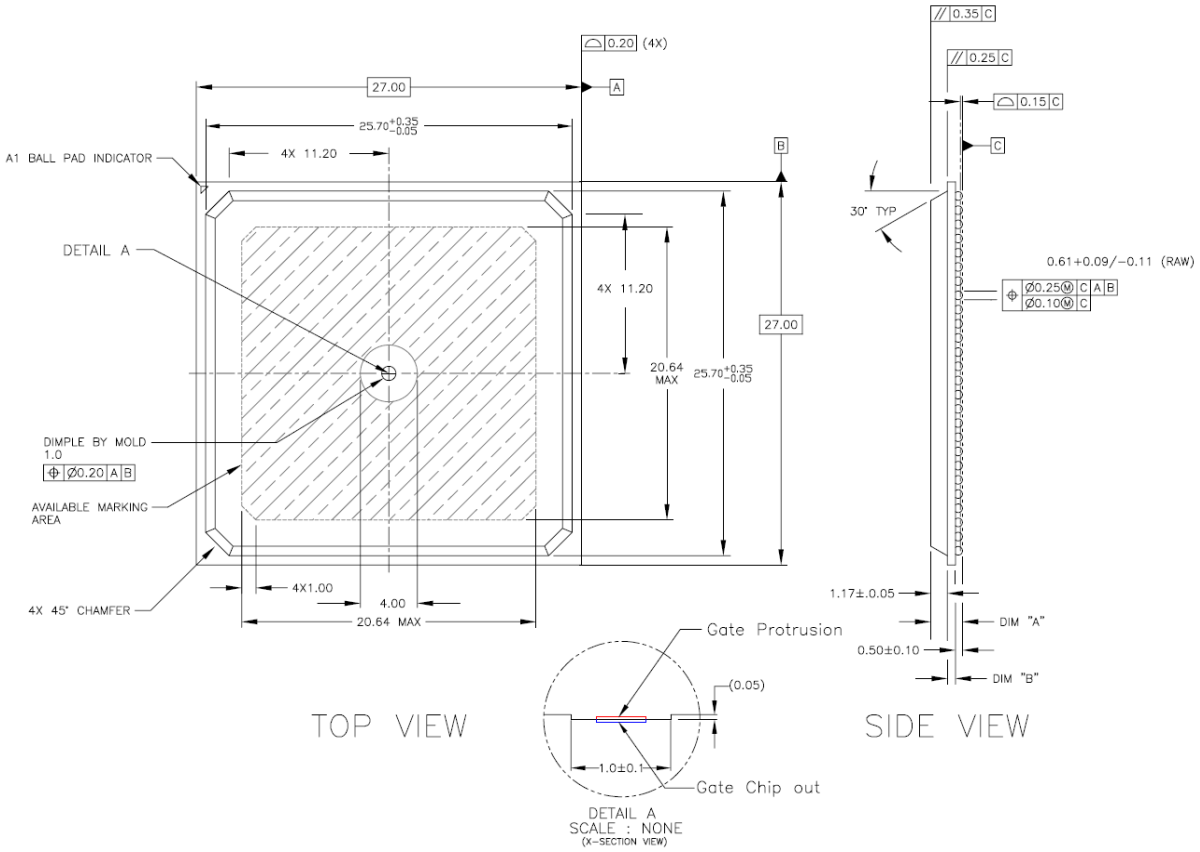
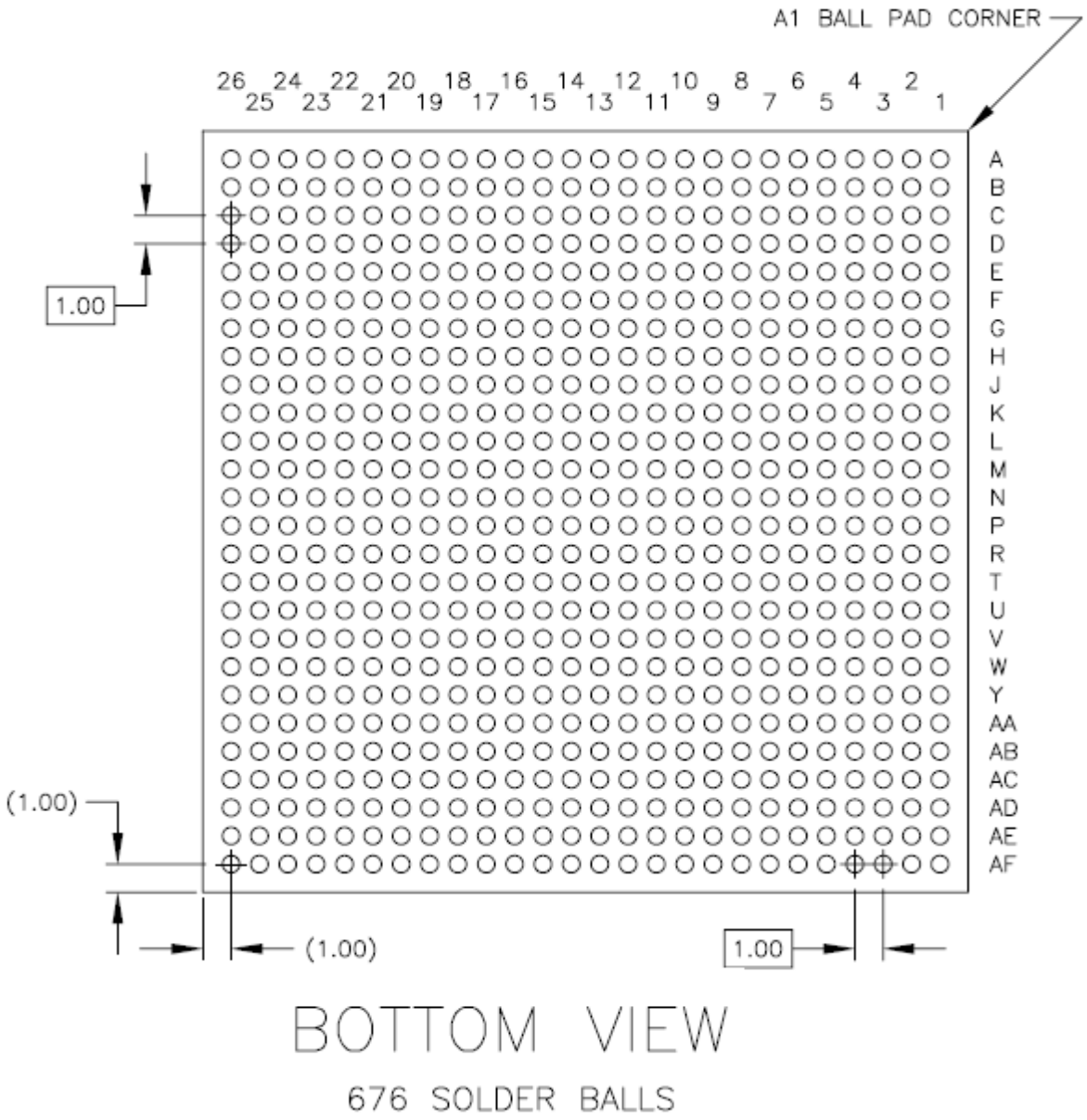


Figure 36 • **FG676 Package Bottom-View**



2.14.4.1 Pin Tables

Pin tables for the FG676 package depicted in the preceding figure are found in the Excel spreadsheet located here:

SmartFusion2 FG676 Pinouts

The following devices are available in the FG676: M2S090(T), (TS) and M2S060(T), (TS)

For more information on Layout Guidelines, see the *AN4153 Board and Layout Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs*.

2.14.5 FCS536

Figure 37 • **FCS536 Package Top-View and Side-View**

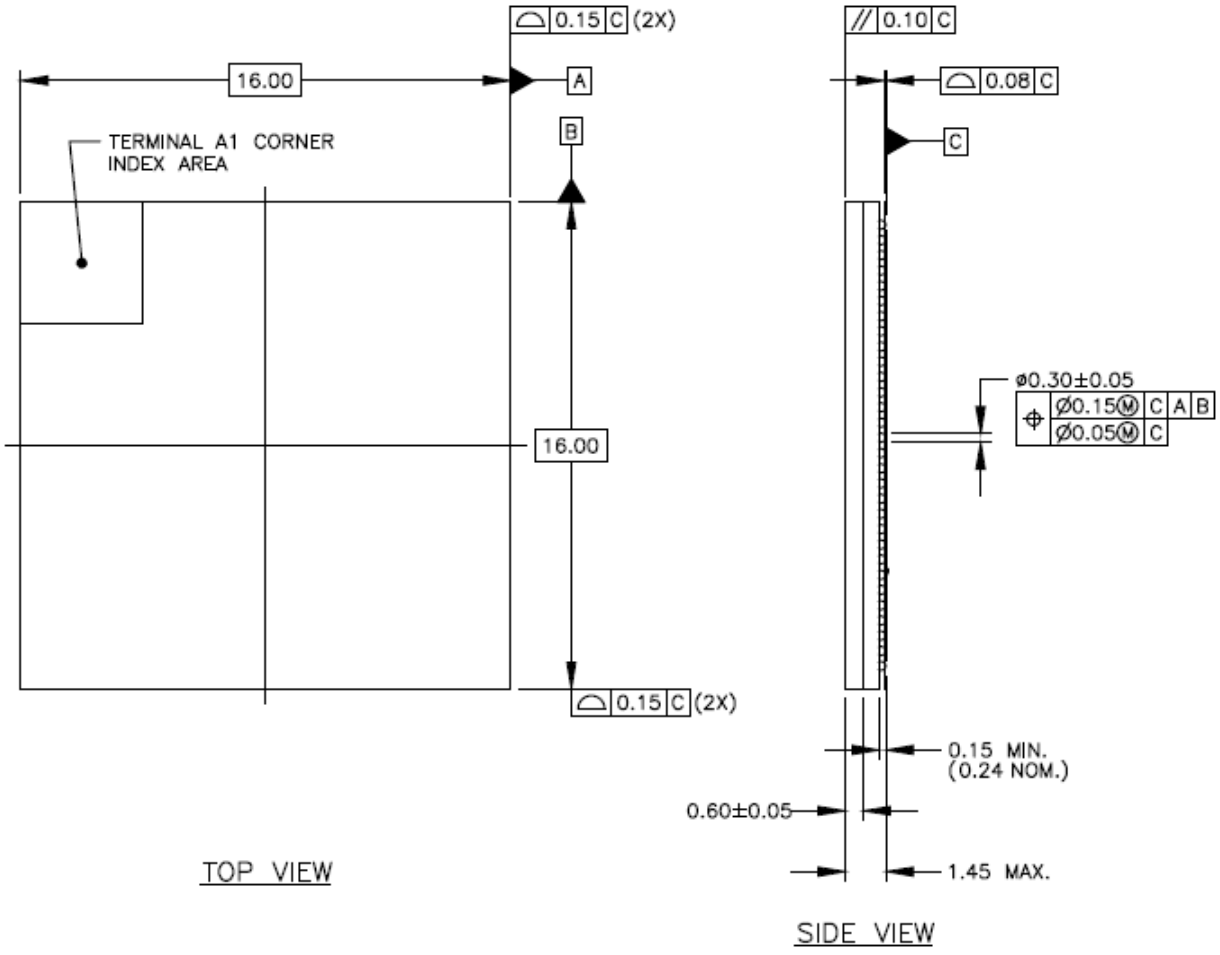
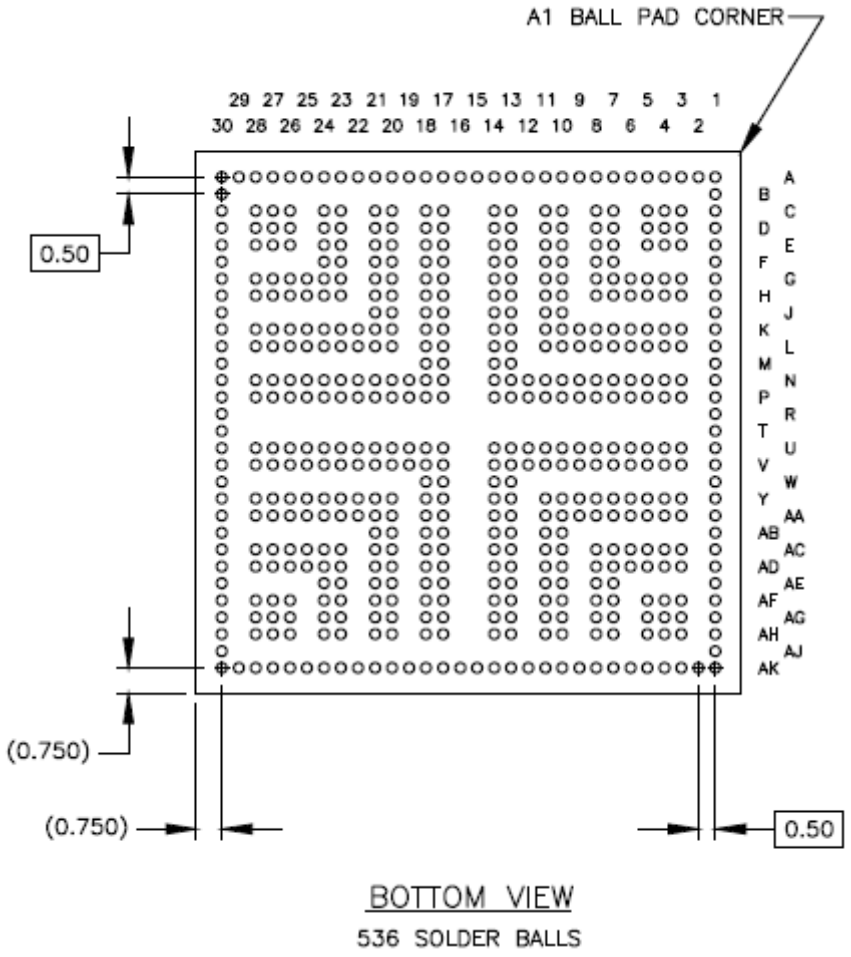


Figure 38 • **FCS536 Package Bottom-View**



2.14.5.1 Pin Tables

Pin tables for the FCS536 package depicted in the preceding figure are found in the Excel spreadsheet located here:

SmartFusion2 FCS536 Pinouts

The following devices are available in the FCS536: M2S150(T), (TS)

For more information on Layout Guidelines, see the *AN4153 Board and Layout Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs*.

2.14.6 FCV484

Figure 39 • **FCV484 Package Top-View and Side-View**

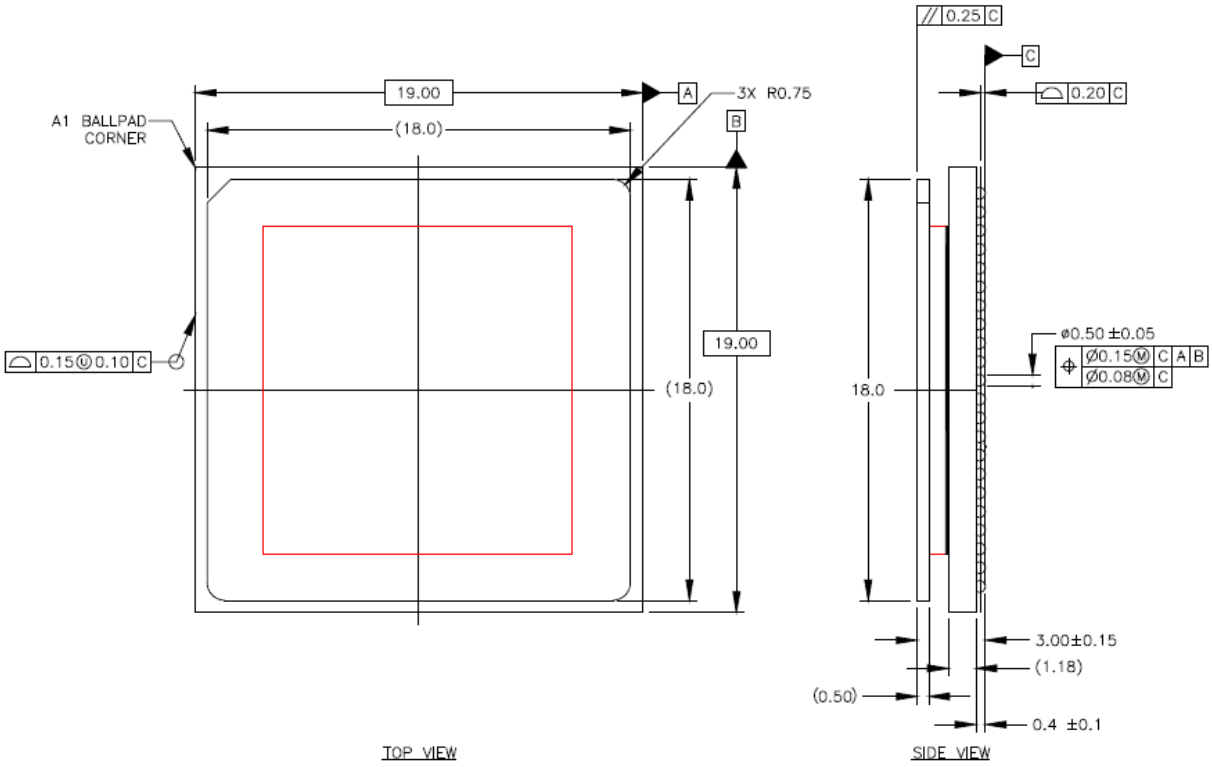
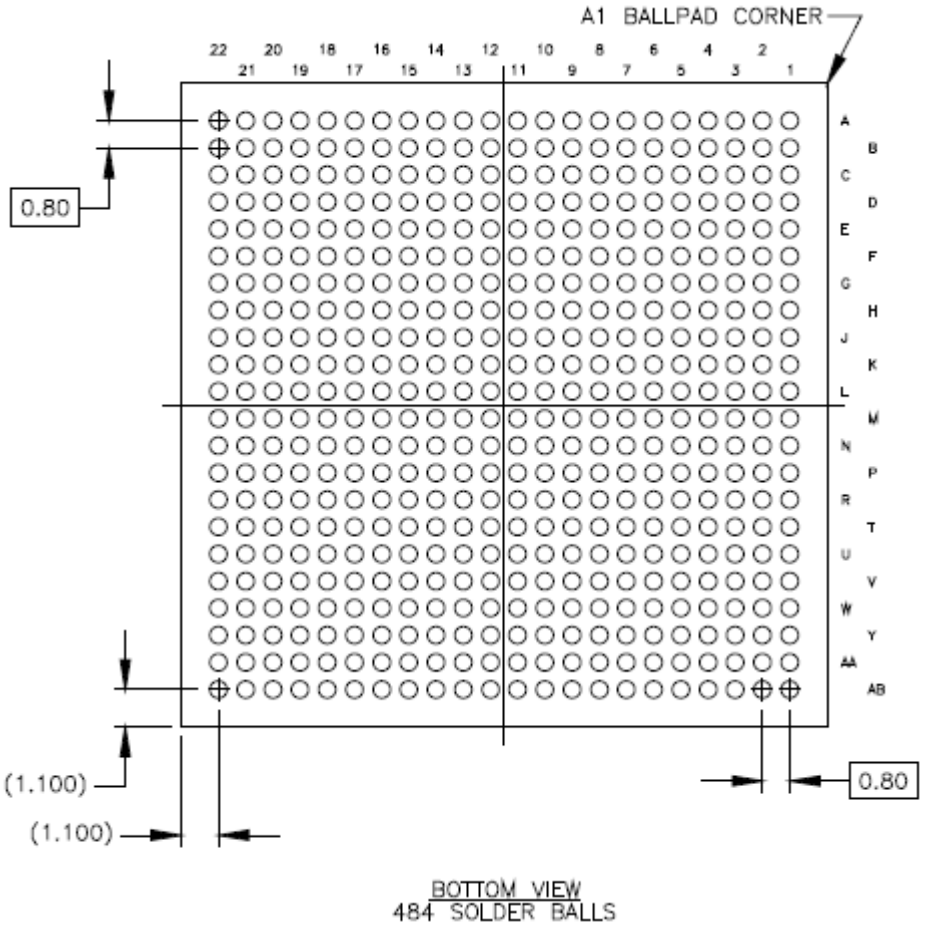


Figure 40 • **FCV484 Package Bottom-View**



2.14.6.1 Pin Tables

Pin tables for the FCV484 package depicted in the preceding figure are found in the Excel spreadsheet located here:

SmartFusion2 FCV484 Pinouts

The following devices are available in the FCV484: M2S150(T), (TS)

For more information on Layout Guidelines, see the *AN4153 Board and Layout Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs*.

2.14.7 FG484

Figure 41 • **FG484 Package Top-View and Side-View**

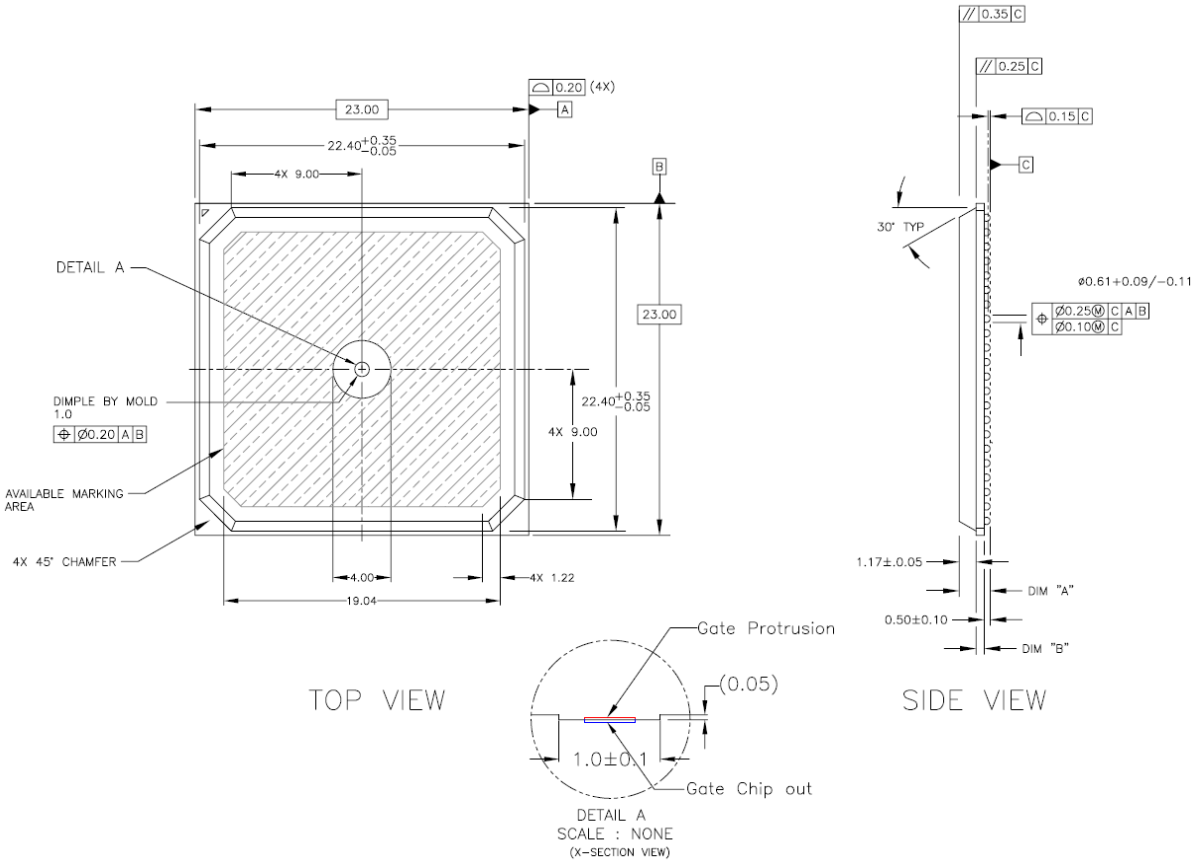
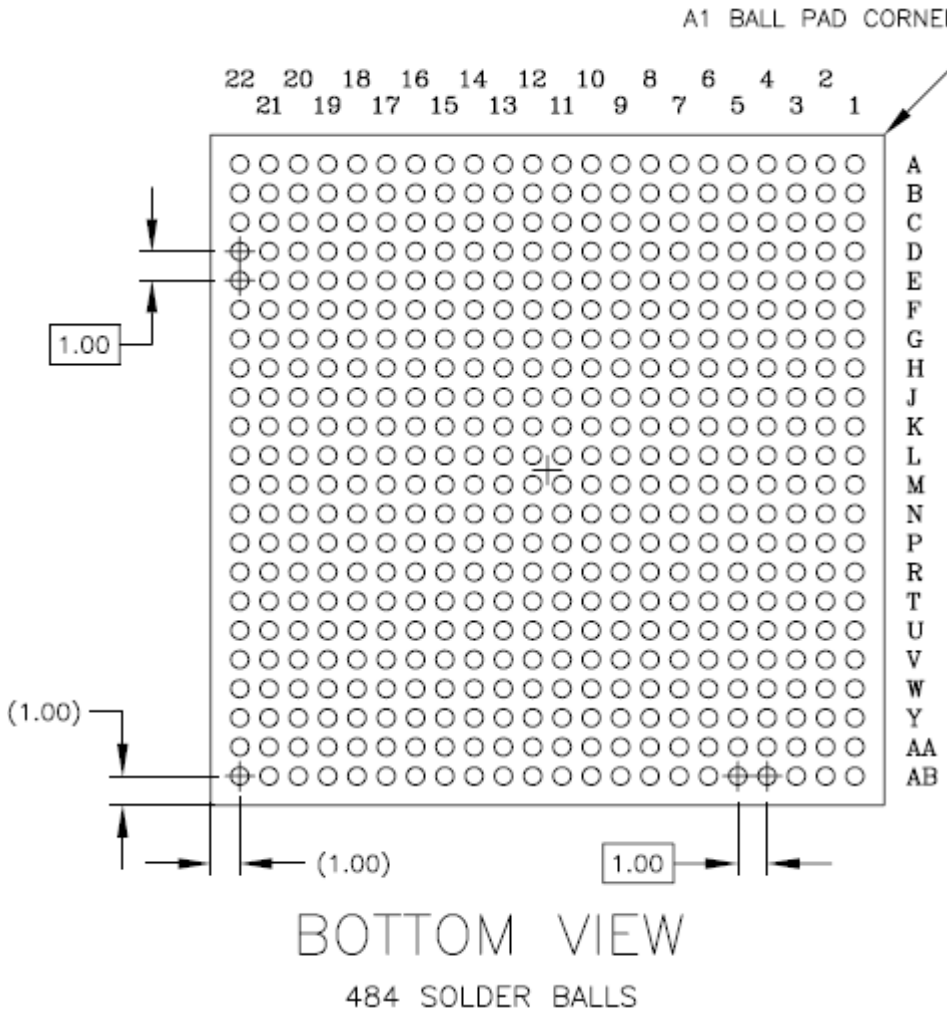


Figure 42 • **FG484 Package Bottom-View**



2.14.7.1 Pin Tables

Pin tables for the FG484 package depicted in the preceding figure are found in the Excel spreadsheet located here:

SmartFusion2 FG484 Pinouts

The following devices are available in the FG484:

- M2S005(S)
- M2S010(T), (TS)
- M2S025(T), (TS)
- M2S050(T), (TS)
- M2S060(T), (TS)
- M2S090(T), (TS)

For more information on Layout Guidelines, see the *AN4153 Board and Layout Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs*.

2.14.8 VF400

Figure 43 • **VF400 Package Top-View and Side-View**

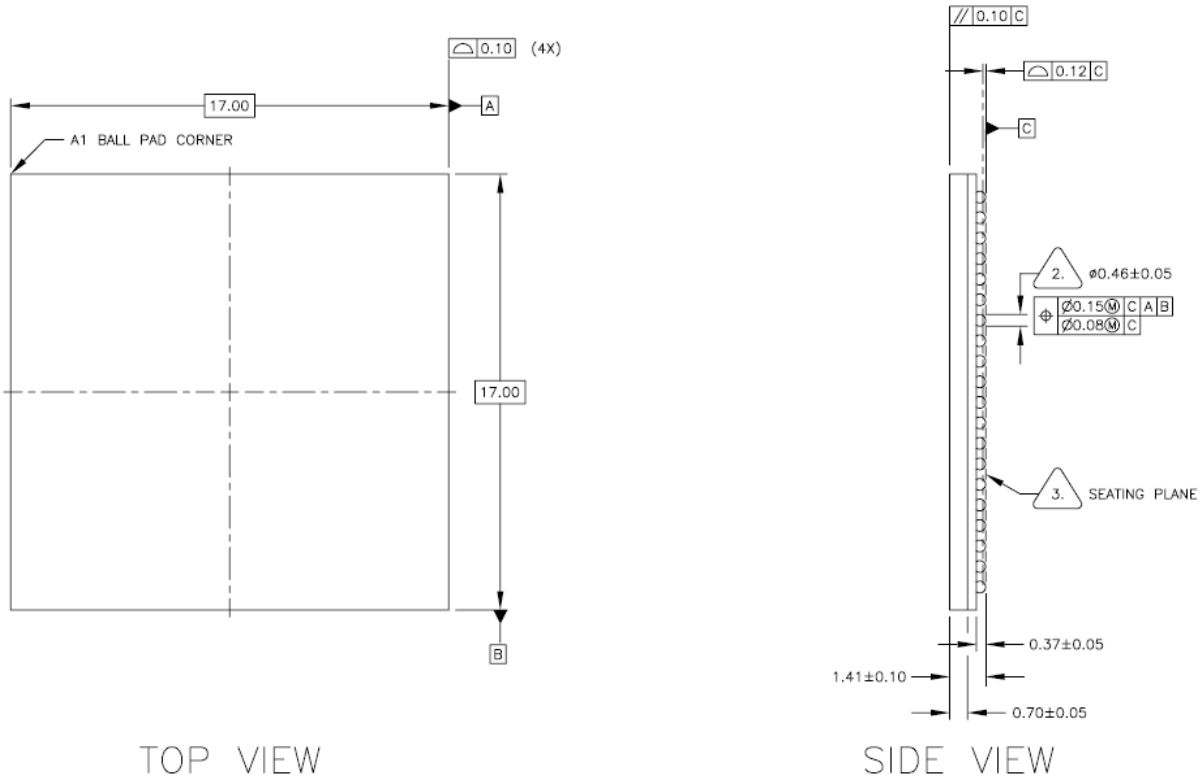
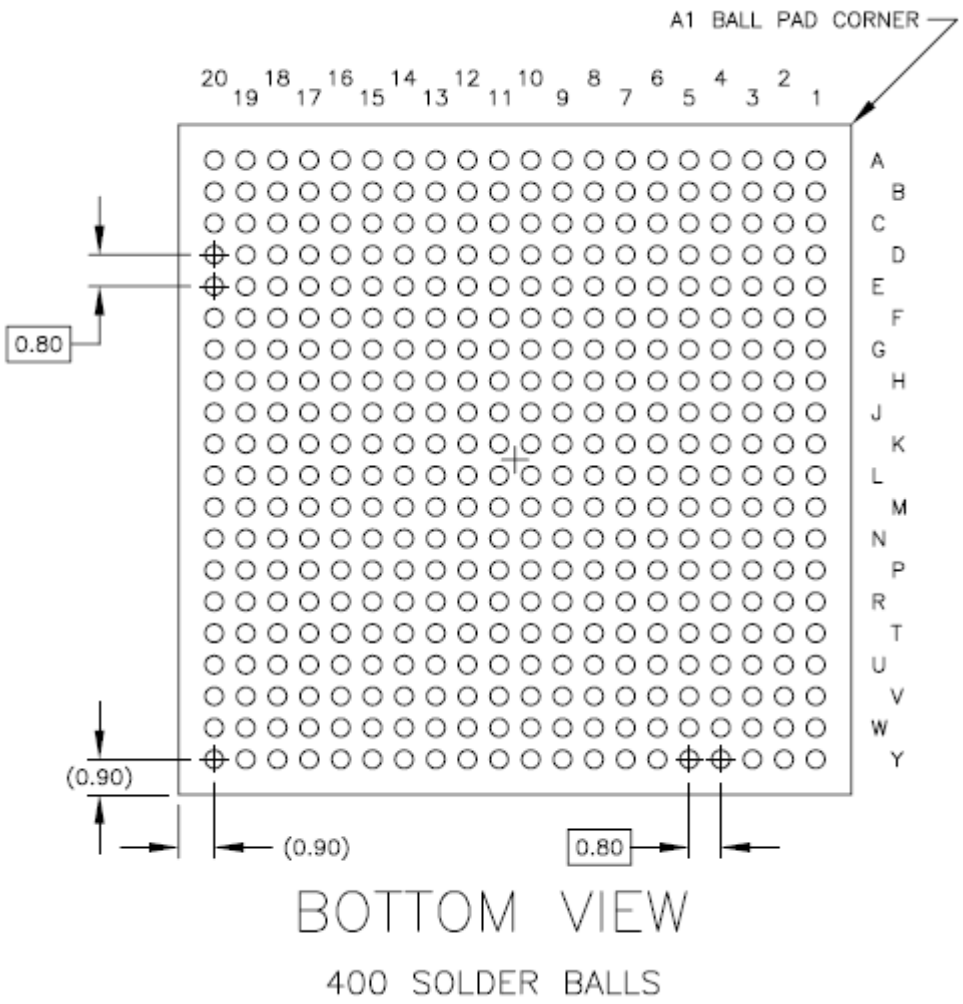


Figure 44 • **VF400 Package Bottom-View**



2.14.8.1 Pin Tables

Pin tables for the VF400 package depicted in the preceding figure are found in the Excel spreadsheet located here:

SmartFusion2 VF400 Pinouts

The following devices are available in the VF400:

- M2S005(S)
- M2S010(T), (TS)
- M2S025(T), (TS)
- M2S050(T), (TS)
- M2S060(T), (TS)

For more information on Layout Guidelines, see the *AN4153 Board and Layout Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs*.

2.14.9 FCS325

Figure 45 • **FCS325 Package Top-View and Side-View**

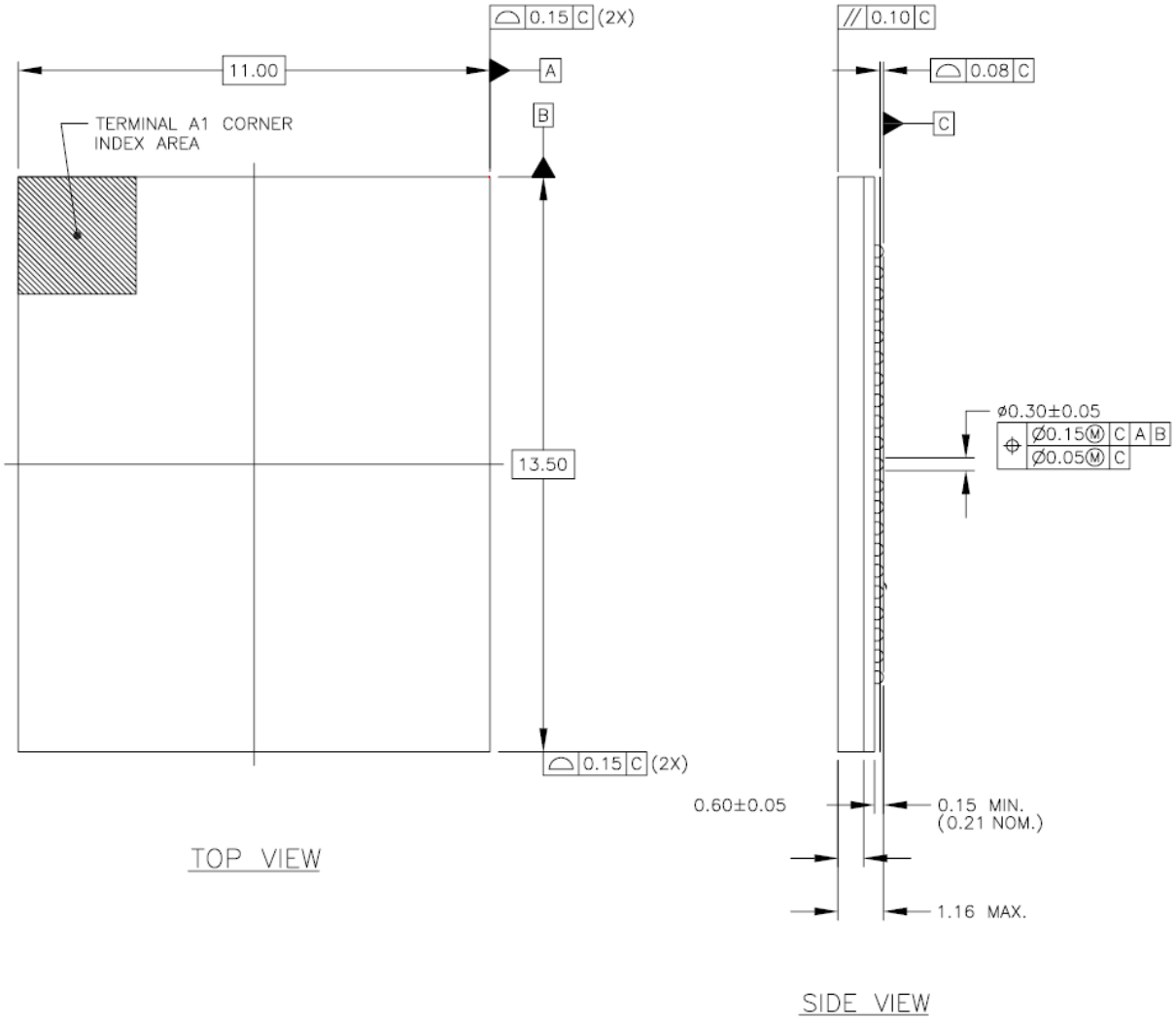
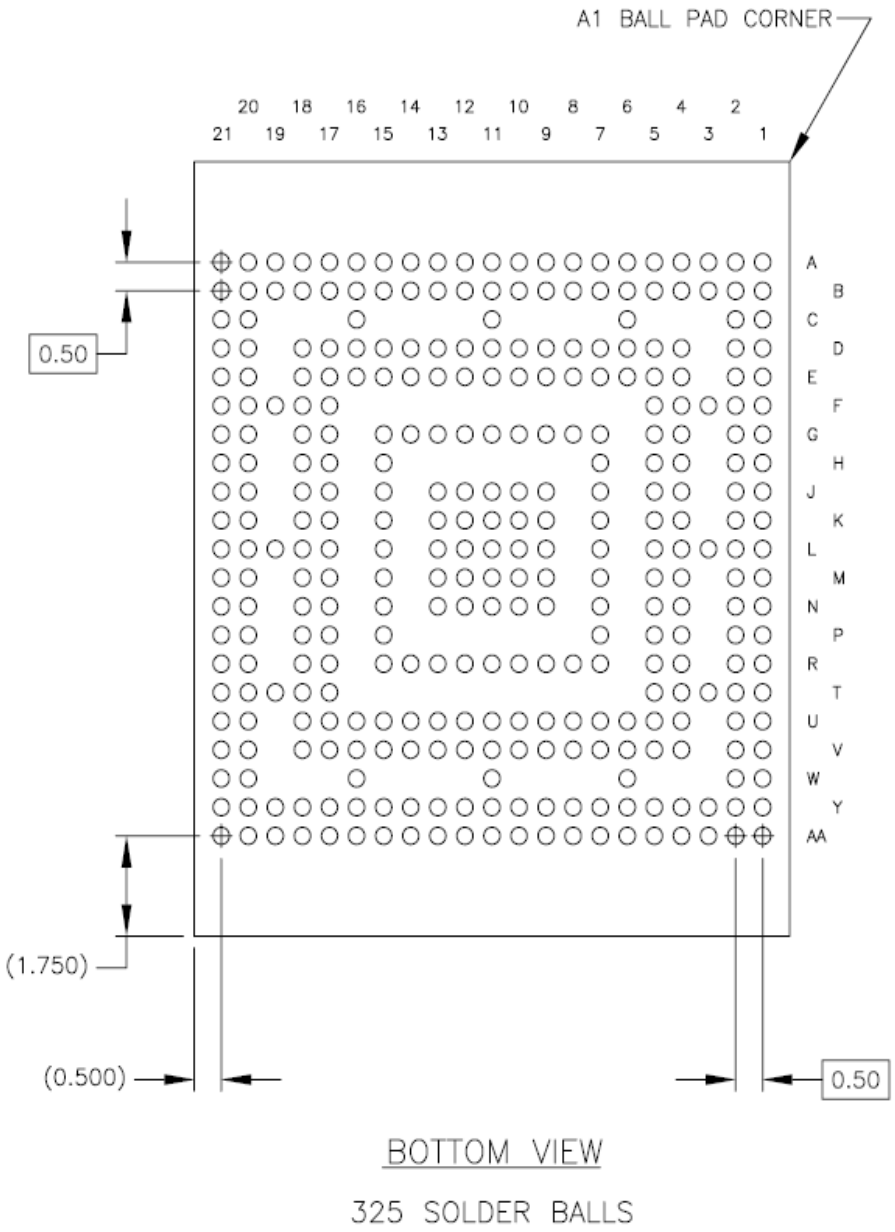


Figure 46 • **FCS325 Package Bottom-View**



2.14.9.1 Pin Tables

Pin tables for the FCS325 package depicted in the preceding figure are found in the Excel spreadsheet located here:

SmartFusion2 FCS325 Pinouts

The following devices are available in the FCS325:

- M2S090(T), (TS)

For more information on Layout Guidelines, see the *AN4153 Board and Layout Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs*.

2.14.10 FCS325 (11mm X 11mm)

Figure 47 • **FCS325 (11mm X 11mm) Package Top-View and Side-View**

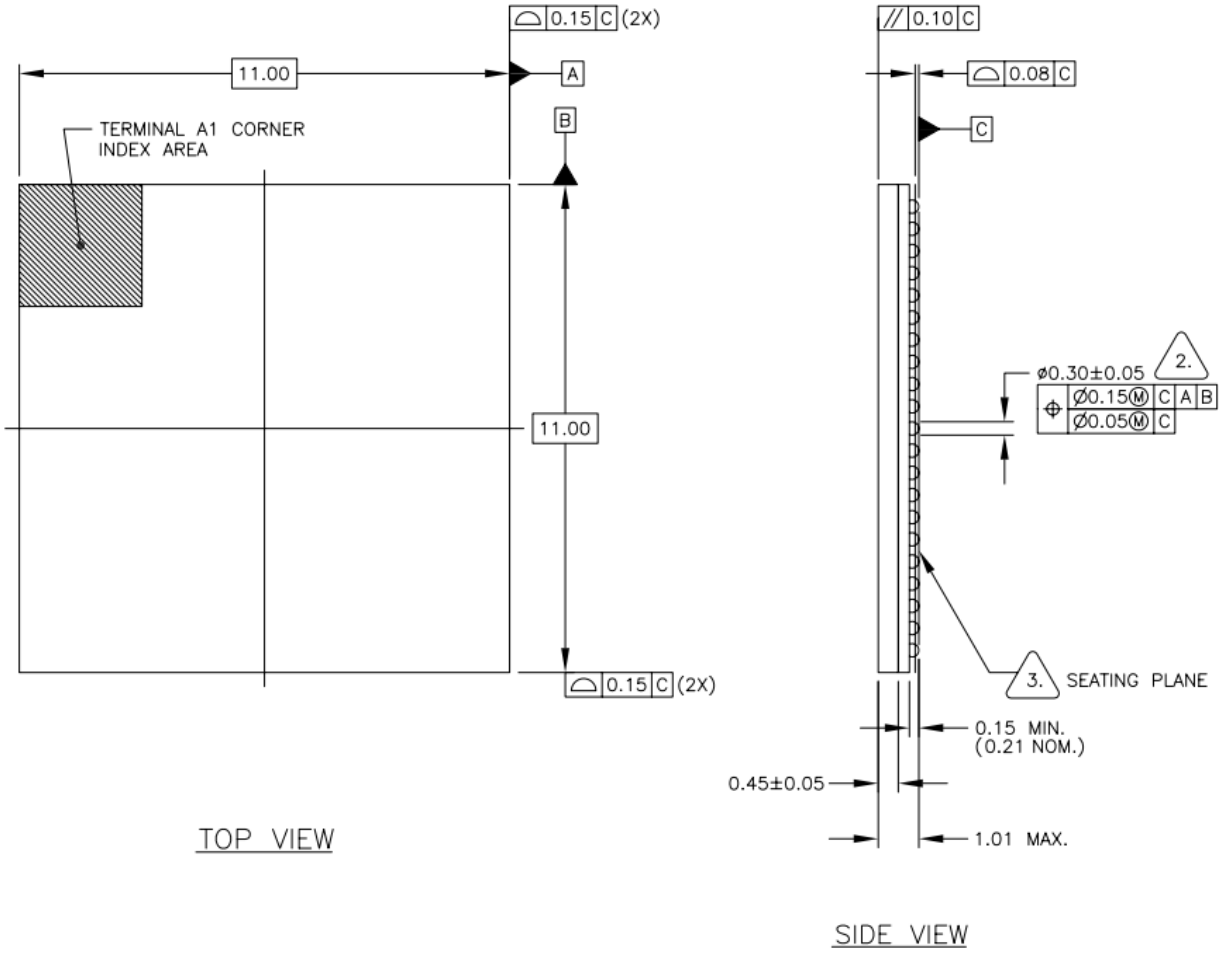
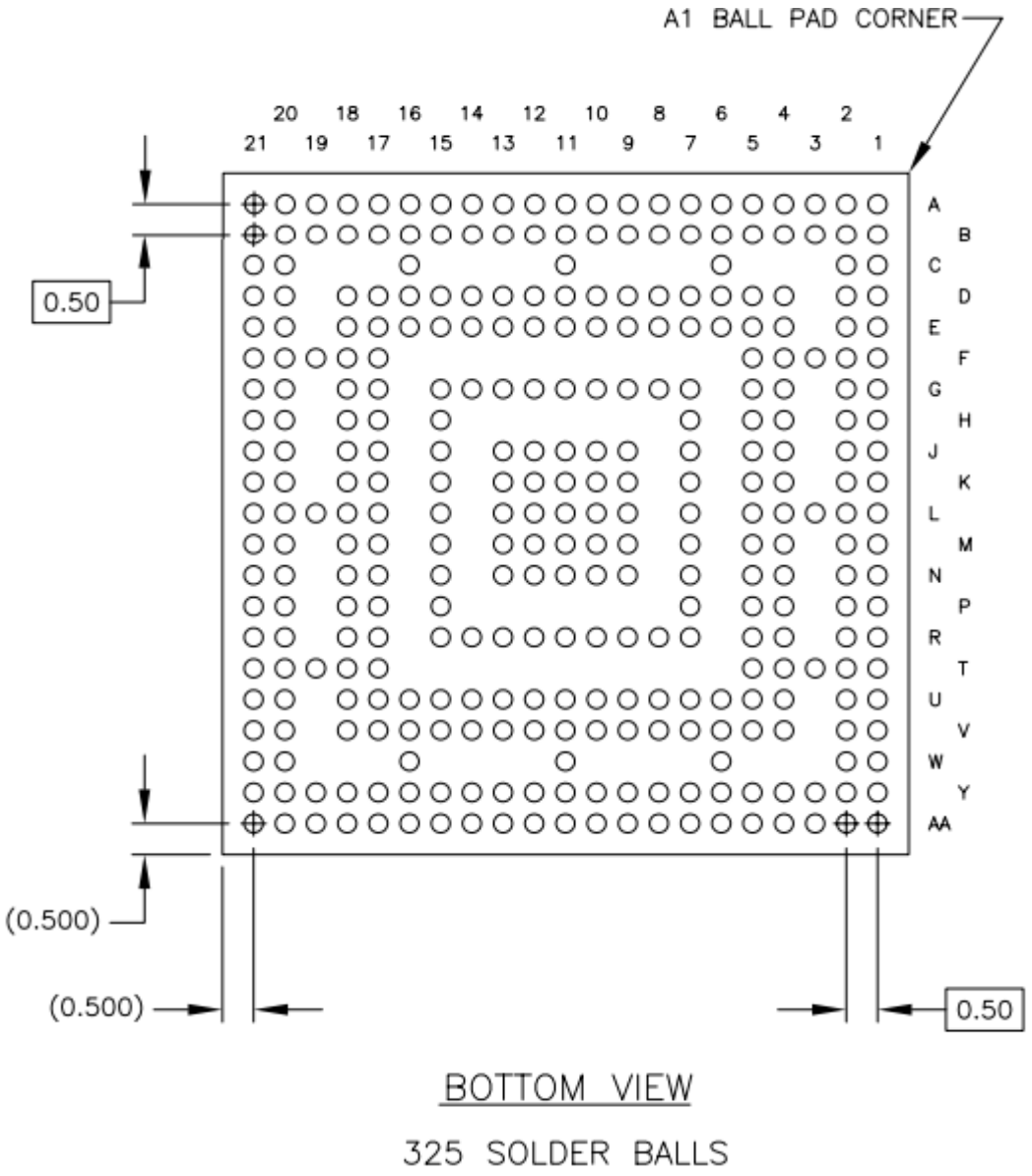


Figure 48 • **FCS325 (11mm X 11mm) Package Bottom-View**



2.14.10.1 Pin Tables

Pin tables for the FCS325 package depicted in the preceding figure are found in the Excel spreadsheet located here:

IGLOO2 FCS325 Pinouts

The following devices are available in the FCS325:

- M2S025(T), (TS)
- M2S050(T), (TS)

For more information on Layout Guidelines, see the *AN4153 Board and Layout Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs*.

2.14.11 VF256

Figure 49 • **VF256 Package Top-View and Side-View**

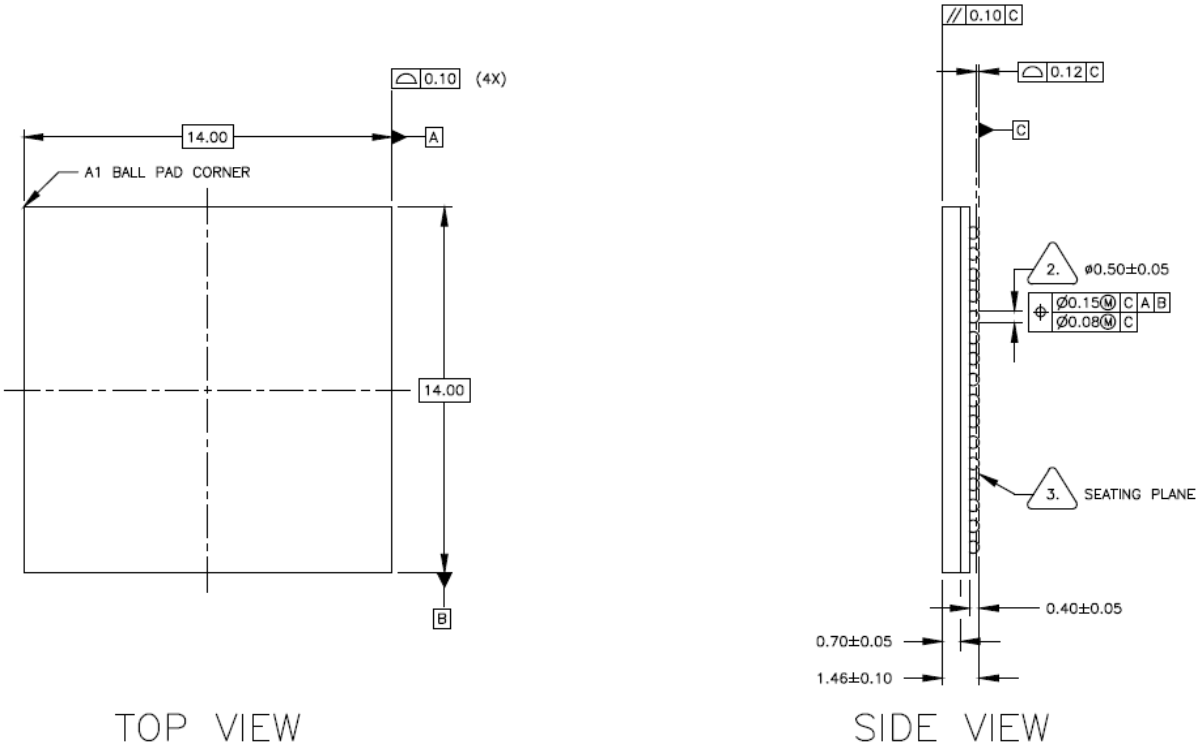
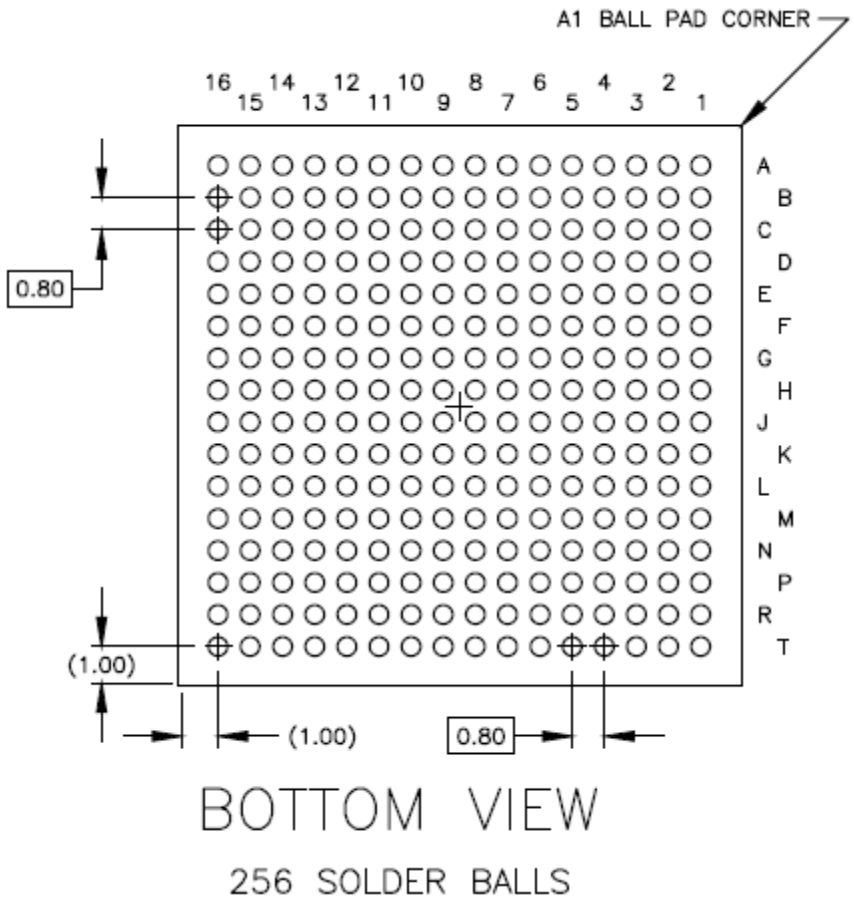


Figure 50 • **VF256 Package Bottom-View**



2.14.11.1 Pin Tables

Pin tables for the VF256 package depicted in the preceding figure are found in the Excel spreadsheet located here:

SmartFusion2 VF256 Pinouts

The following devices are available in the VF256:

- M2S005(S)
- M2S010(T), (TS)
- M2S025(T), (TS)

For more information on Layout Guidelines, see the *AN4153 Board and Layout Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs*.

2.14.12 FCS158

Figure 51 • **FCS158 Package Top-View and Side-View**

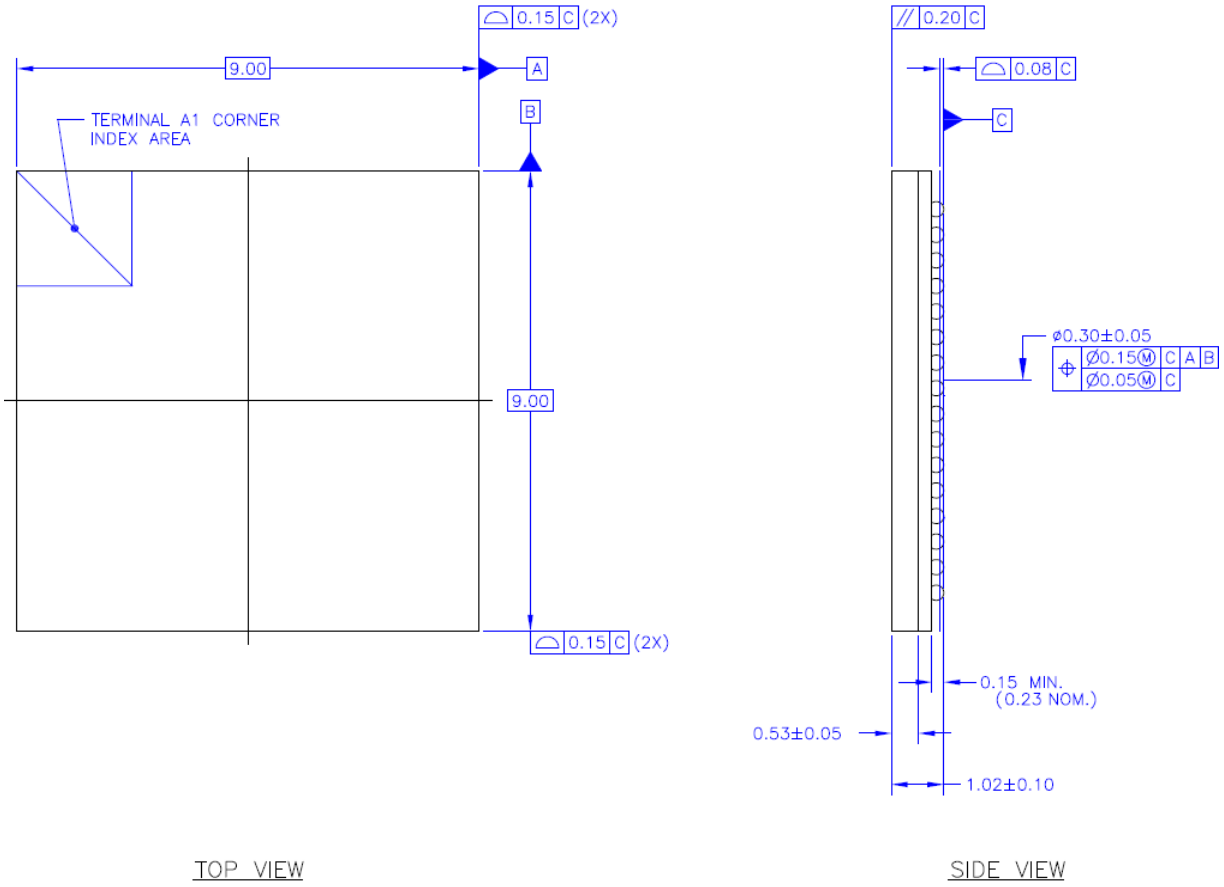
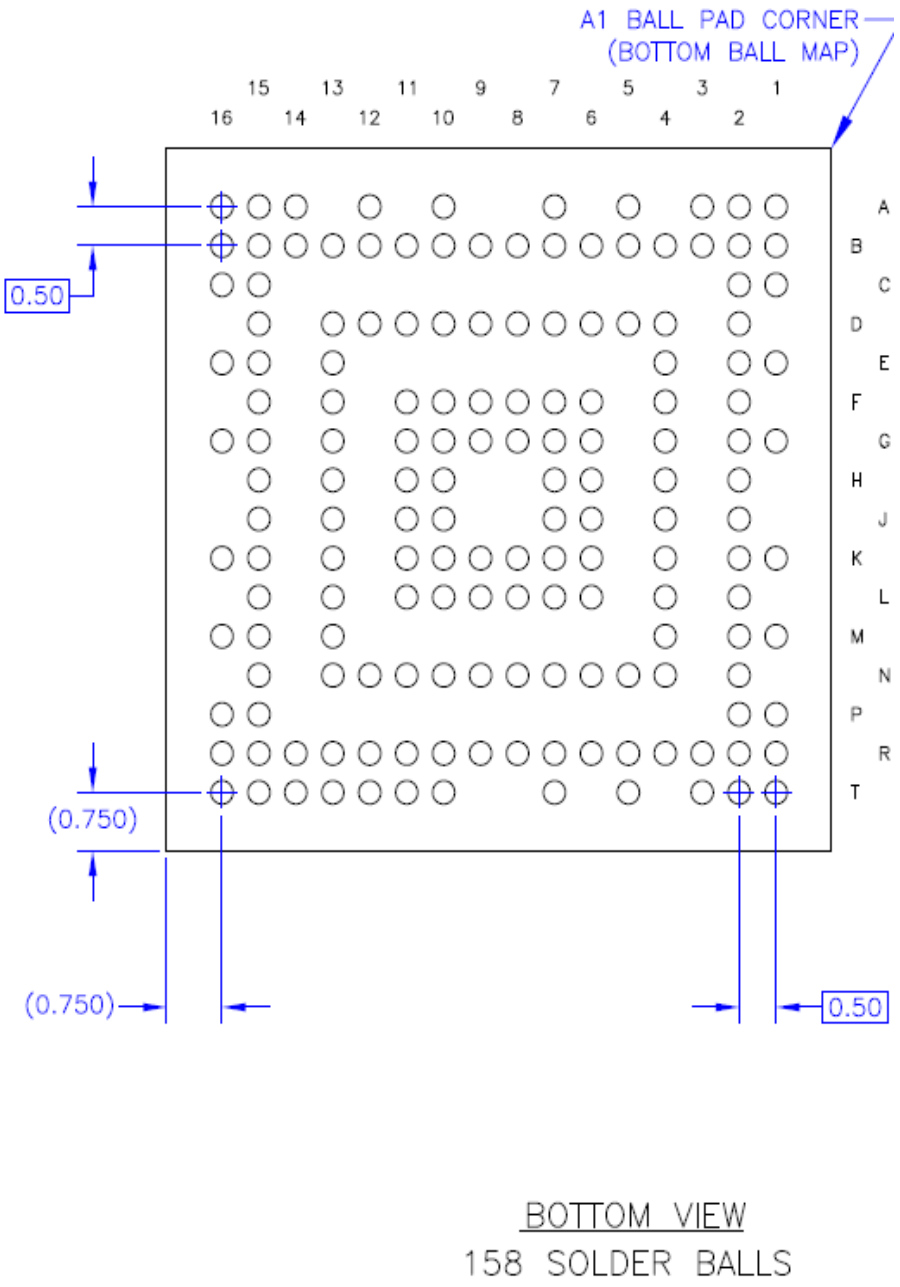


Figure 52 • **FCS158 Package Bottom-View**



2.14.12.1 Pin Tables

Pin tables for the FCS158 package depicted in the preceding figure are found in the Excel spreadsheet located here:

SmartFusion2 FCS158 Pinouts

The following devices are available in the FCS158:

- M2S025(S)
- M2S025(T), (TS)

For more information on Layout Guidelines, see the *AN4153 Board and Layout Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs*.

2.14.13 TQ144

Figure 53 • **TQ144 Package Top-View and Side-View**

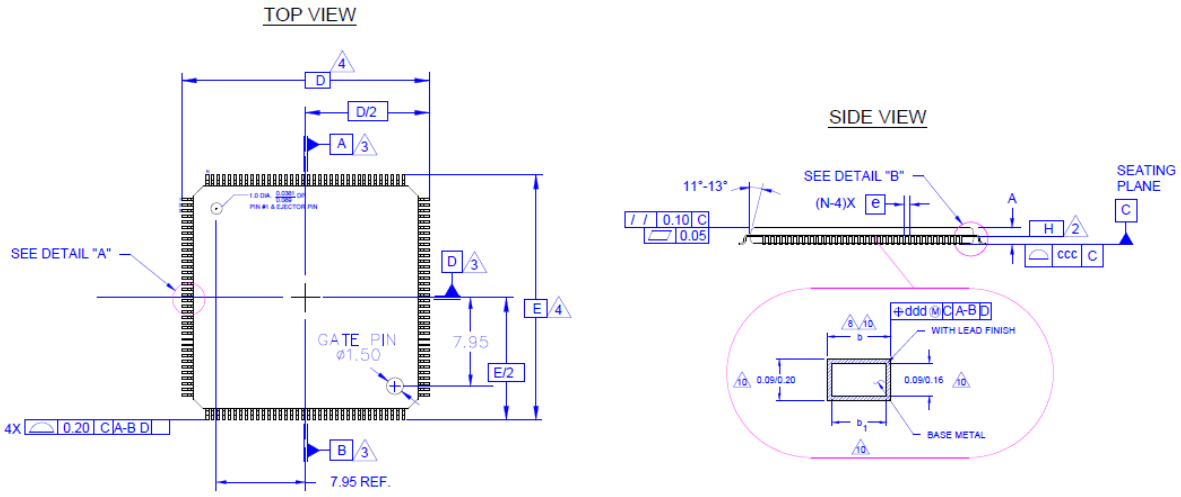
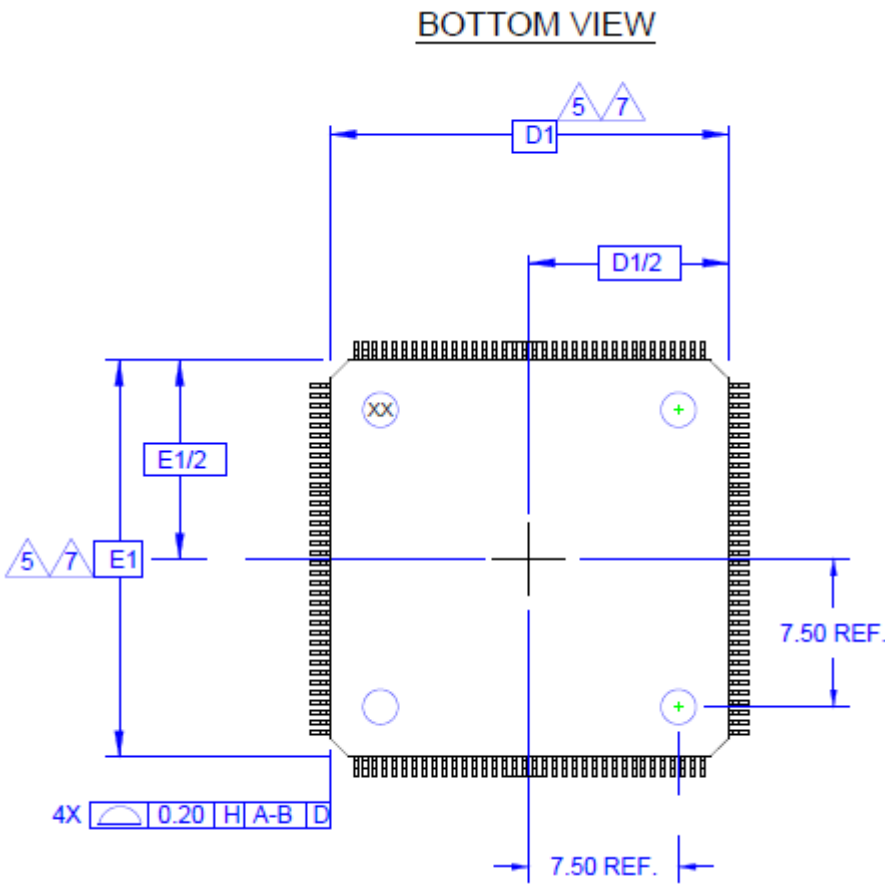


Figure 54 • **TQ144 Package Bottom-View**



Note:

1. All dimensioning and tolerances confirm to ASME Y14.5-1994.
2. Datum plane H located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.

3. Datums A-B and D to be determined at centerline between leads where leads exit plastic body at datum plane H.
4. To be determined at seating plane C.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254 mm per side. Dimension D1 and E1 include mold mismatch and are determined at datum plane H.
6. N is number of terminals.
7. Package top dimensions are smaller than bottom dimensions by 0.10 millimeters and top of package will not overhang bottom of package.
8. Dimension b does not include damber protrusion. Allowable damber protrusion shall be not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Damber can not be located on the lower radius or the foot.
9. All dimensions are in millimeters.
10. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
11. This drawing conforms to JEDEC registered outline m2s-026-c, variation BFB.
12. A1 is defined as the distance from the seating plane to the lowest point of the package body.

2.14.13.1 Pin Tables

Pin tables for the TQ144 package depicted in the preceding figure are found in the Excel spreadsheet located here:

SmartFusion2 TQ144 Pinouts

The following devices are available in the TQ144: M2S010 and M2S005 (S)

For more information on Layout Guidelines, see the *AN4153 Board and Layout Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs*.