Atmel 8-bit and 32-bit Microcontrollers

AVR127: Understanding ADC Parameters

APPLICATION NOTE

Introduction

This application note explains the basic concepts of analog-to-digital converter (ADC) and the parameters that determine the performance of an ADC. These ADC parameters determine the accuracy of the output available from the ADC.

The introduction to ADC terminologies is followed by the description on various performance parameters of the ADC. Static performance parameters such as Gain Error, Offset Error, Full Scale Error, and Linearity Error are explained in detail. Dynamic performance parameters such as Signal-to-Noise-Ratio (SNR), Total Harmonic Distortion (THD), Signal Noise and Distortion (SINAD), and Effective Number of Bits (ENOB) are also explained.

Features

- Getting introduced to ADC concepts
- Understanding various ADC parameters
- Understanding the effect of ADC parameters on the performance of ADC

Table of Contents

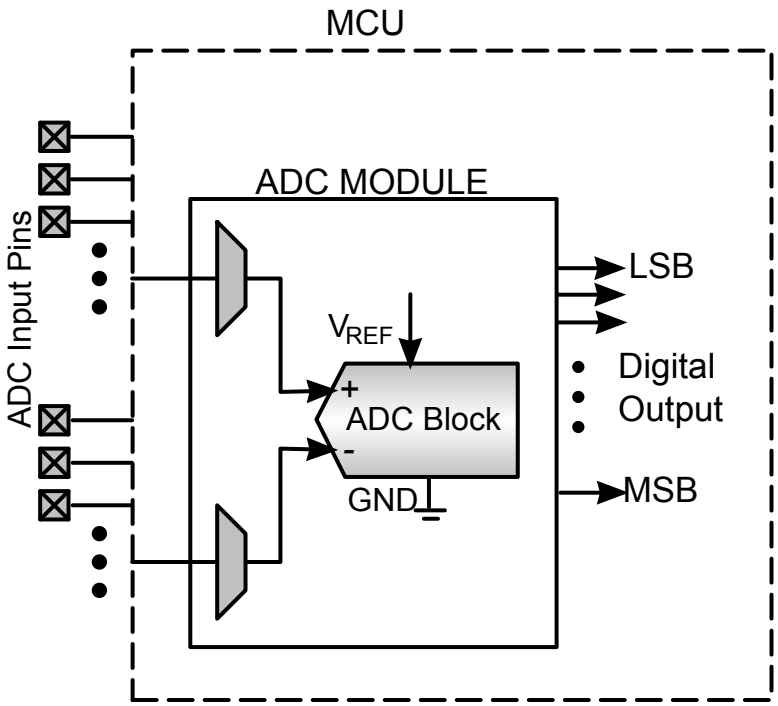
1. Abbreviations

ADC	Analog to Digital Converter
CPU	Central Processing Unit
dB	Decibel
DNL	Differential Non-Linearity
ENOB	Effective Number of Bits
GND	Ground
INL	Integral Non-Linearity
kHz	kiloHertz
LSB	Least Significant Bit
MHz	megaHertz
MSB	Most Significant Bit
mV	milliVolt
RMS	Root Mean Square
SINAD	Signal Noise and Distortion
SNR	Signal to Noise Ratio
THD	Total Harmonic Distortion
TUE	Total Unadjusted Error

2. ADC - Basics

An ADC is an electronic system or a module that has an Analog Input ($\mathbf{V_{IN}}$), Reference Voltage Input ($\mathbf{V_{REF}}$) and Digital Outputs. The ADC converts the analog input signal to a digital output value that represents the magnitude or value of the analog input in comparison with the reference voltage. It samples the input analog voltage and produces an output digital code for each sample measured. Basic symbol of an ADC with input and output signals are as shown in the following diagram.

Figure 2-1. Basic ADC Module



Let us understand a few basic terminologies and concepts used in the ADC before attempting to understand the working principle of an ADC.

2.1. Reference Voltage

The Reference Voltage ($\mathbf{V_{REF}}$) is the standard voltage against which the Analog Input Voltage must be measured. $\mathbf{V_{REF}}$ can be an input voltage provided through external pin. Some ADCs are capable of generating $\mathbf{V_{REF}}$ for the ADC module from the Analog $\mathbf{V_{CC}}$ of the MCU device. The range of $\mathbf{V_{REF}}$ varies among different devices and the respective device datasheet must be referred to know the exact value. Typically, $\mathbf{V_{REF}}$ can be selected by configuring the bit field of the corresponding register.

2.2. Analog Input Voltage

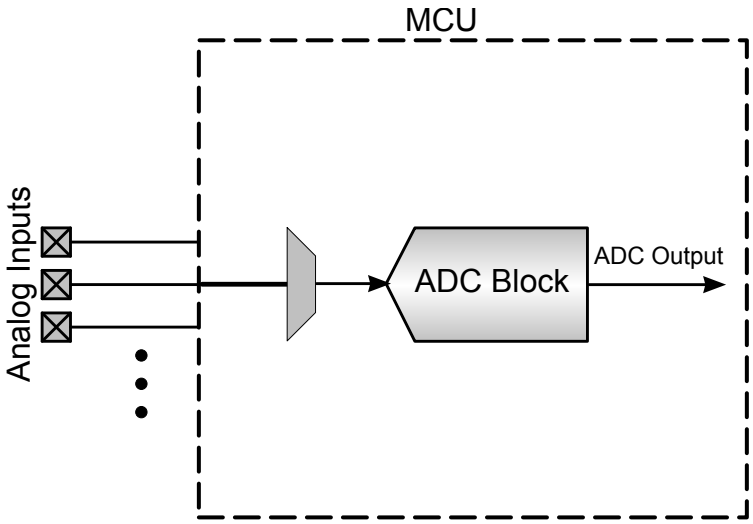
The Analog Input Voltage ($\mathbf{A_{IN}}$) is the voltage to be measured and converted into a digital value. The input voltage should always be less than $\mathbf{V_{REF}}$ to avoid saturation of the ADC. The input voltage range is also called as conversion range.

ADC modules can be classified based on the number of Analog Inputs used as follows:

1. Single-ended Input
2. Differential Input

In single-ended input[1], the ADC sampling and conversion is performed only on one analog input signal. The basic block diagram of a single-ended input is as shown below.

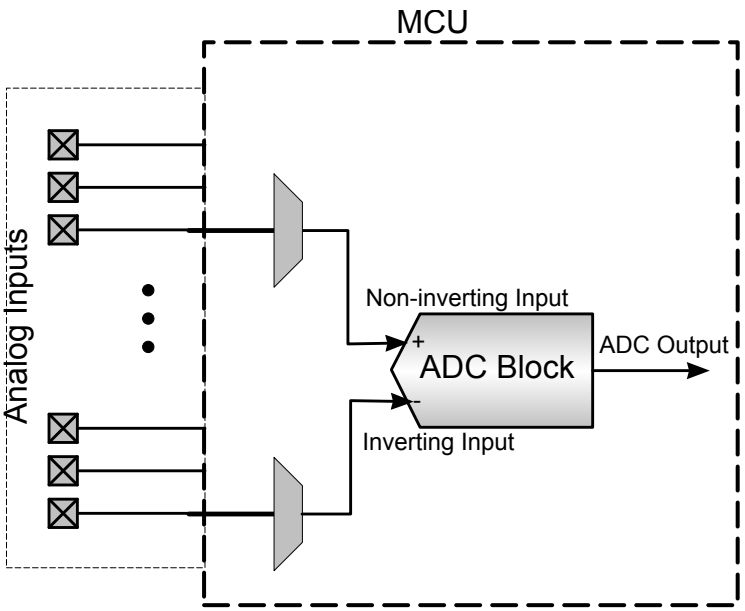
Figure 2-2. Single-ended Input



In differential input, the difference in voltage of two analog inputs is applied to the ADC module. This can be done either directly or after performing some amplification using suitable gain stages. Differential conversions are usually operated in signed mode, where the MSB of the output code acts as the sign bit. When using differential mode, offset error can be measured easily by setting up the positive and negative input on the same pin and the offset can be measured directly as the ADC does not require the Ground (GND) level as a reference.

For example, when two Analog Inputs are provided, A_{IN1} = 1.5V & A_{IN2} = 0.5V, the digital value of differential output (A_{IN1} - A_{IN2} = 1V) is expected.

Figure 2-3. Differential Input



Most ADCs can operate only using a positive input voltage. The ADCs whose $\mathbf{A_{IN}}$ falls in the positive range ($\mathbf{0 < A_{IN} < V_{REF}}$) are called as **Unipolar ADC**. ADCs capable of accepting both positive and negative input voltages are called as **Bipolar ADC**[1]. For example, in a Unipolar ADC, if the V_{REF} = 2V, then 0 < A_{IN} < 2V should always be maintained to get expected output.

Note:

1. Refer the respective device datasheet to know the input type, polarity, and input range supported by the device.
2. For details about Signed / Unsigned conversion modes of Atmel® AVR® XMEGA® devices, refer to the AVR1300: Using the Atmel AVR XMEGA ADC.

2.3. Resolution

The entire input voltage range (0V to V_{REF}) is divided into a number of sub-ranges called *Step*. Each step is assigned a single output digital code. A step is also called LSB (least significant bits) and the number of such steps is usually in powers of two (2^n). Here, n is called the *Resolution* of the ADC and 2^n provides the step count. For a specific V_{REF}, the step size is determined by the resolution (V_{REF} / 2^n).

For example, an ADC with Resolution = 3-bits and V_{REF} = 2V, total number of steps are 8 and the step size is 250mV.

2.4. Quantization

Quantization is the process where the sampled analog input voltage will be replaced with an approximation from a finite set of discrete values. It is also called as *rounding*. The LSB is determined if input analog voltage lies in the lowest step of the input voltage range.

For example, when V_{REF} = 2V, Resolution = 3-bits, the whole range is divieded into 8 steps. Analog Input voltage from 0V to 250mV is assigned to the same output digital code 000 and voltages from 251mV to 500mV is assigned 001. This process is called as *Quantization*.

2.5. Ideal ADC

When the resolution of a specific ADC is infinite, it is called an ideal ADC. In other words, the resolution of an ideal ADC is equal to its Effective Number of Bits (ENOB). In an ideal ADC, every possible analog input value provides a unique digital output from the ADC within the specified conversion range. It is considered as a theoretical concept that cannot be realized. An ideal ADC can be described mathematically using a linear transfer function, as shown in the following graphical illustrations.

Figure 2-4. Single Ended Ideal ADC

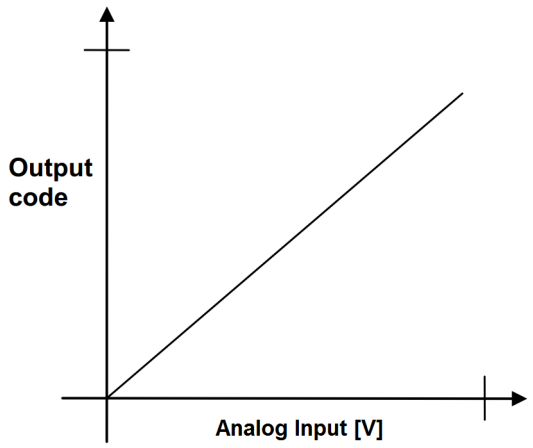
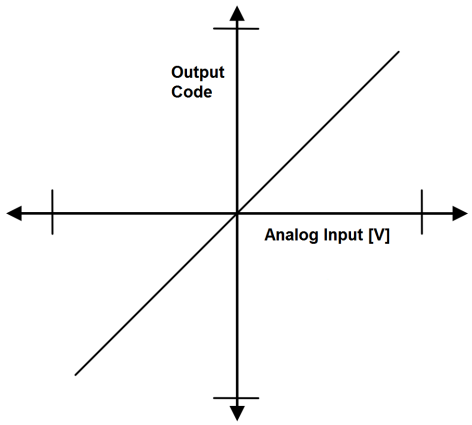


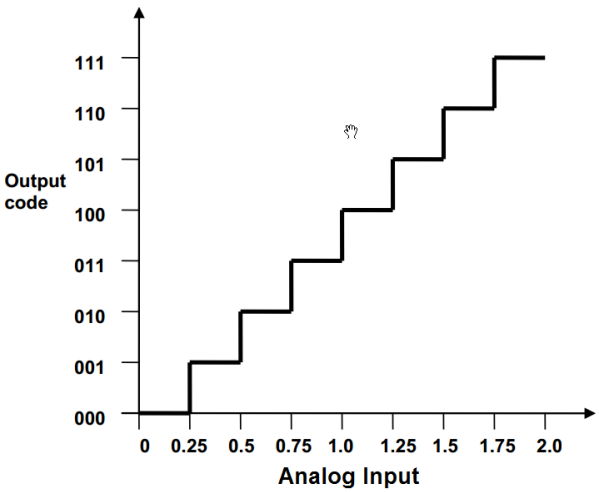
Figure 2-5. Differential Ideal ADC



2.6. Perfect ADC

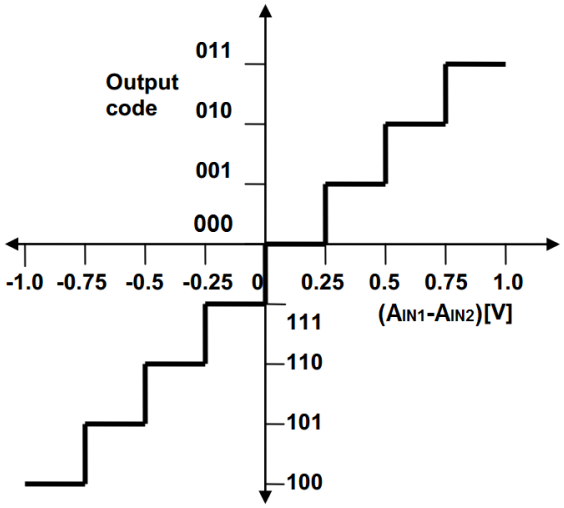
Since ADC generates digital output, it is not possible to provide continuous output values. The perfect ADC performs the process of quantization during conversion. This results in a staircase transfer function where each step represents one LSB.

Figure 2-6. Perfect ADC in Single-ended Mode (Unadjusted Quantization)



Consider an example with V_{REF} = 2V and Resolution = 3-bits, the step size is 250mV (1 LSB). The input analog voltage ranges from 0V to 250mV will be assigned the digital output code 000 and the input analog voltage range from 251mV to 500mV will be assigned the digital code 001 and so on. This is depicted in Figure 2-6 Perfect ADC in Single-ended Mode (Unadjusted Quantization) which shows the transfer function of a perfect 3-bit ADC operating in single ended mode. Figure 2-7 Perfect ADC in Differential Mode (Unadjusted Quantization), shows the transfer function of a perfect 3-bit ADC operating in differential mode.

Figure 2-7. Perfect ADC in Differential Mode (Unadjusted Quantization)



Note: In the above example, the differential analog input voltage can vary from -1V to +1V and the MSB acts as sign bit.

From the Figure 2-6 Perfect ADC in Single-ended Mode (Unadjusted Quantization), it is obvious that an input voltage of 0V produces an output code 000. At the same time, an input voltage of 250mV also produces the same output code 000. This explains the quantization error due to the process of quantization. As the input voltage rises from 0V, the quantization error also rises from 0LSB and reaches a maximum quantization error of 1LSB at 250mV. Again, the quantization error increases from 0 to 1LSB as the input rises from 250mV to 500mV. This maximum quantization error of 1LSB can be reduced to ±0.5LSB by shifting the transfer function towards left through 0.5LSB.

Figure 2-8. Perfect ADC in Single-ended Mode (Adjusted Quantization)

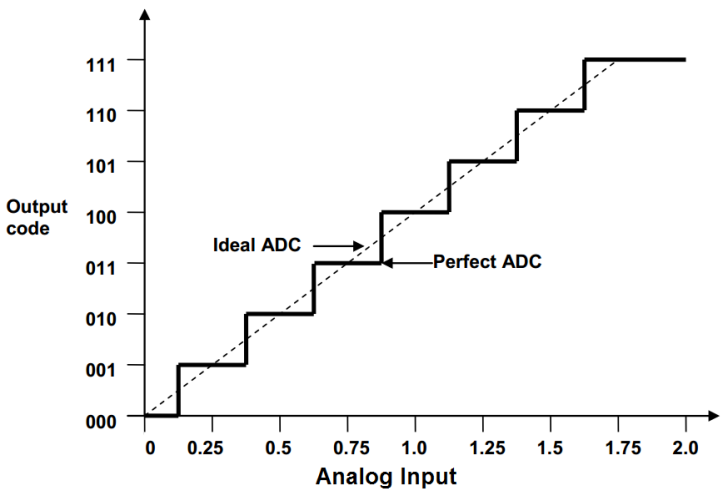
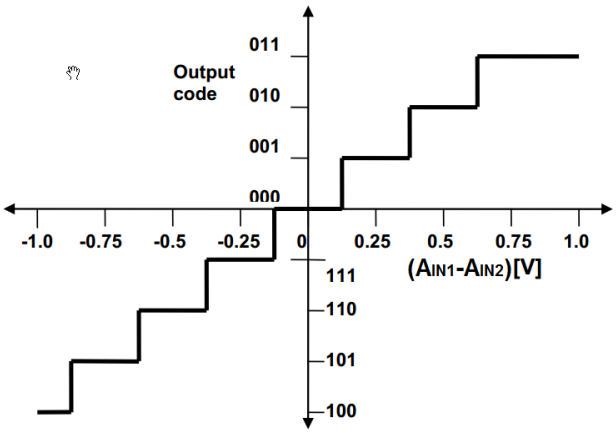


Figure 2-8 Perfect ADC in Single-ended Mode (Adjusted Quantization) depicts the quantization adjusted perfect transfer function together with the ideal transfer function. As seen on the figure, the perfect ADC equals the ideal ADC on the exact midpoint of every step. This means that the perfect ADC essentially rounds input values to the nearest output step value. Similarly, Figure 2-9 Perfect ADC in Differential Mode (Adjusted Quantization) is for differential ADC.

Figure 2-9. Perfect ADC in Differential Mode (Adjusted Quantization)



The Quantization error is only considered in a model such as a Perfect ADC. However, in real-time the actual ADC has several other errors apart from quantization error. These errors are explained in the upcoming sections.

3. ADC Errors

To understand the performance of an ADC, it is important to understand various errors that affects the ADC output. The static errors that affect the performance of an ADC are explained in the following topics.

3.1. Offset Error

The offset error is defined as the deviation of the actual ADC's transfer function from the perfect ADC's transfer function at the point of zero to the transition measured in the LSB bit.

When the transition from output value 0 to 1 does not occur at an input value of 0.5LSB, then we say that there is an offset error. With positive offset errors, the output value is larger than 0 when the input voltage is less than 0.5LSB from below. With negative offset errors, the input value is larger than 0.5LSB when the first output value transition occurs. In other words, if the actual transfer function lies below the ideal line, there is a negative offset and vice versa. Transfer functions of Positive and negative offsets for Ideal, Perfect, and Actual ADCs are shown in the following images:

Figure 3-1. Positive Offset Error

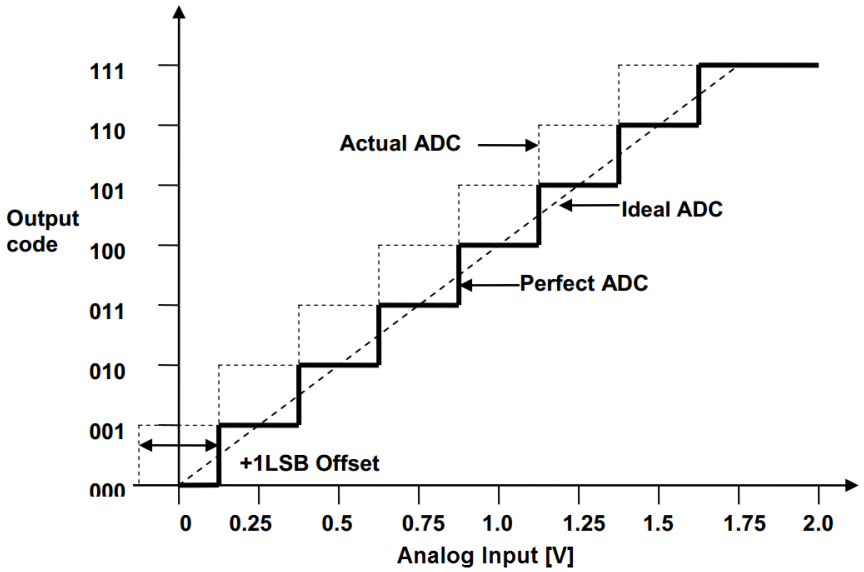
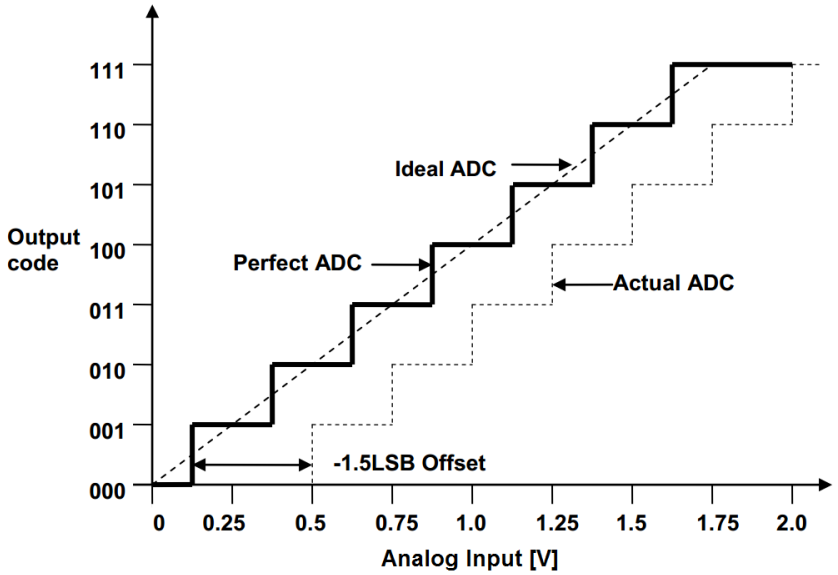


Figure 3-2. Negative Offset Error



In Figure 3-1 Positive Offset Error, the first transition occurs at 0.5LSB and the transition is from 1 to 2. But 1 to 2 transitions should occur at 1.5LSB for perfect case. So the difference (Perfect – Actual = 1.5LSB – 0.5LSB = +1LSB) is the offset error.

In the Figure 3-2 Negative Offset Error, the first transition occurs at 2LSB and the transition is from 0 to 1. But 0 to 1 transition should occur at 0.5LSB for perfect case. So the difference (Perfect – Actual = 0.5LSB – 2LSB = -1.5LSB) is the offset error.

Note: Offset errors limit the available range for the ADC. A large positive offset error causes the output value to saturate at maximum before the input voltage reaches maximum. A large negative offset error gives output value as 000 for the smallest input voltages.

3.2. Gain Error

The gain error is defined as the deviation of the midpoint of the last step of the actual ADC from the midpoint of the last step of the ideal ADC, after compensated for offset error. After compensating for offset errors, applying an input voltage of 0V will always give an output value of 000. However, gain errors cause the actual transfer function slope to deviate from the ideal slope. This gain error can be measured and compensated by scaling the output values. The Transfer function of Positive and Negative gain errors for a 3-bit ADC is shown as follows:

Figure 3-3. Positive Gain Error

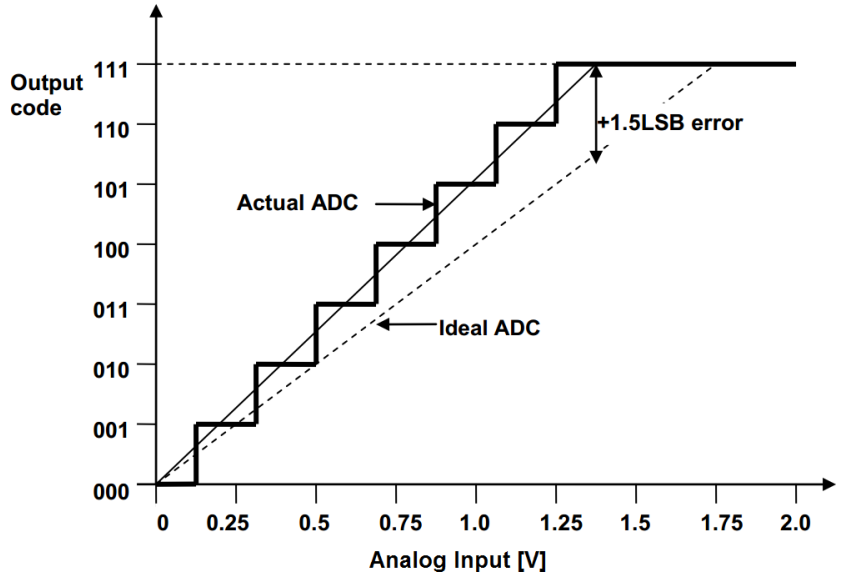
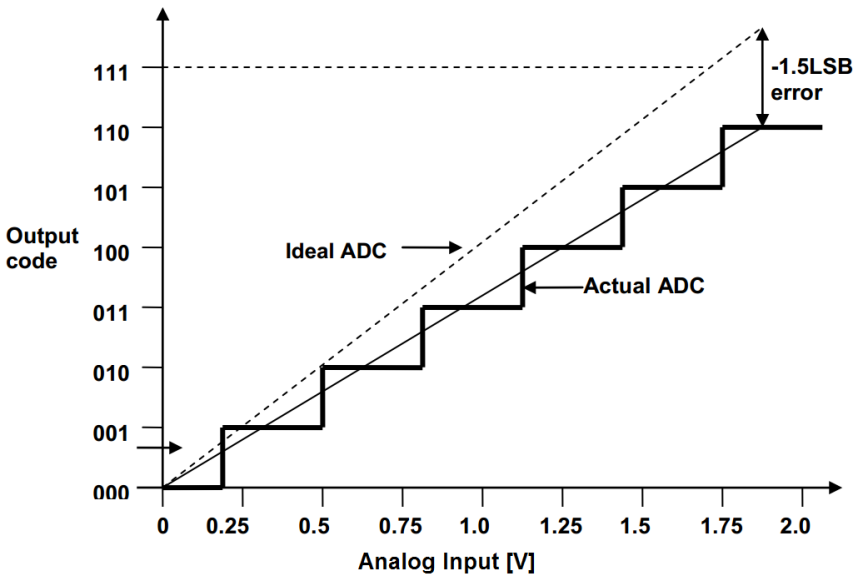


Figure 3-4. Negative Gain Error



If the transfer function of the actual ADC occurs above the ideal straight line, then it produces positive gain error and vice versa. The gain error is calculated as LSBs from a vertical straight line drawn between the midpoint of the last step of the actual transfer curve and the ideal straight line.

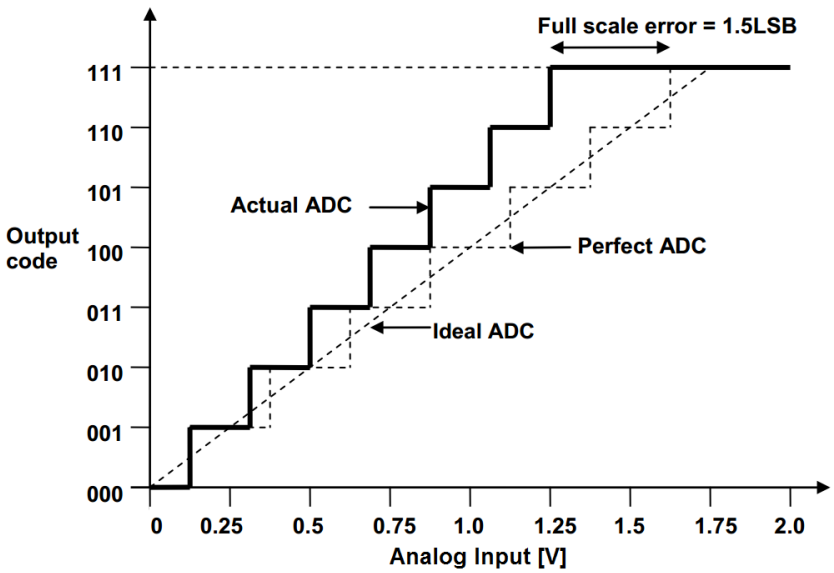
In Figure 3-3 Positive Gain Error, the output value saturates before the input voltage reaches its maximum. The vertical arrow shows the midpoint of the last output step.

In Figure 3-4 Negative Gain Error, the output value has only reached six when the input voltage is at its maximum. This results in a negative deviation for the actual transfer function.

3.3. Full Scale Error

Full scale error is the deviation of the last transition (full scale transition) of the actual ADC from the last transition of the perfect ADC, measured in LSB or volts. Full scale error is due to both gain and offset errors.

Figure 3-5. Full Scale Error



The gain and offset errors of the ADC can be measured and compensated using calibration procedures. For more specific details on calibration methods, refer to AVR120: Characterization and Calibration of the ADC on an AVR.

3.4. Non-Linearity

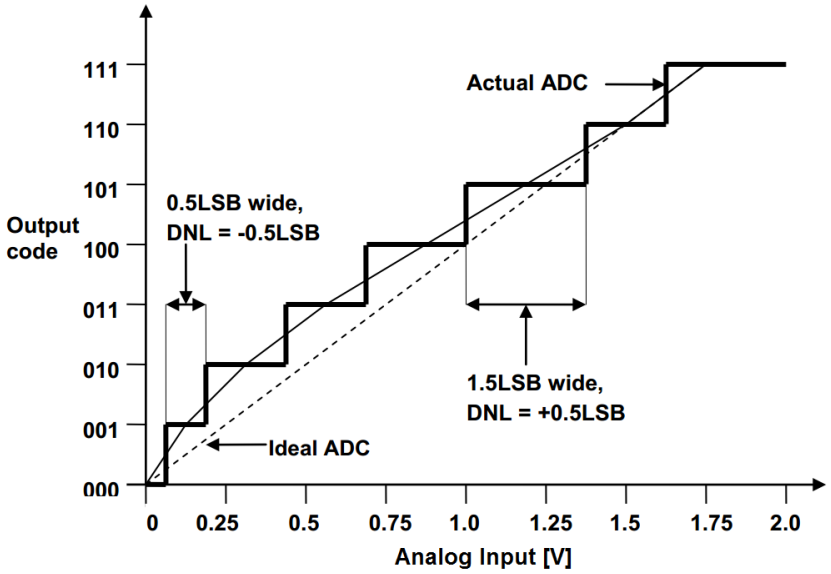
When offset and gain errors are compensated for, the actual transfer function should now be equal to the transfer function of perfect ADC. However, non-linearity in the ADC may cause the actual curve to deviate slightly from the perfect curve, even if the two curves are equal around 0V and at the point where the gain error was measured.

There are two major types of non-linearity that degrade the performance of ADC. They are differential non-linearity (DNL) and integral non-linearity (INL).

3.4.1. Differential Non-Linearity (DNL)

Differential non-linearity (DNL) is defined as the maximum and minimum difference in the step width between actual transfer function and the perfect transfer function. Non-linearity produces quantization steps with varying widths.

Figure 3-6. Differential Non-Linearity (DNL)

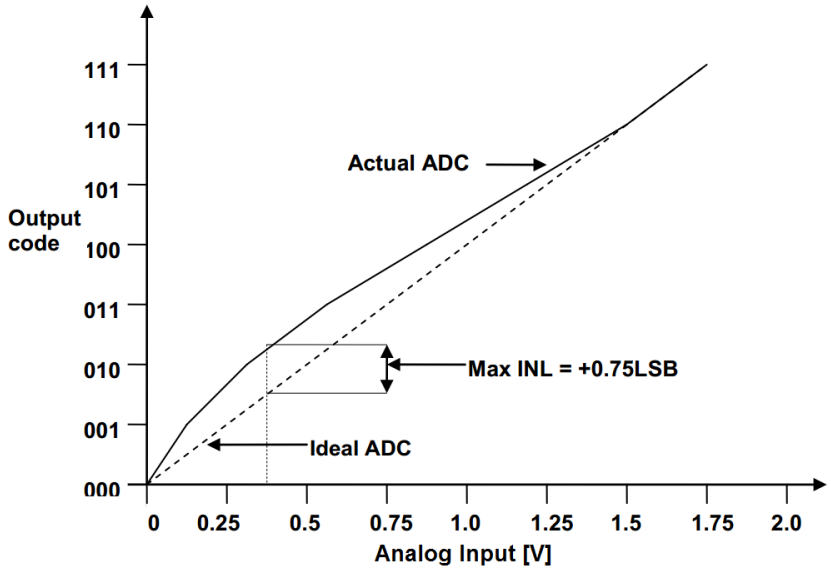


For the case of Perfect ADC, the step width must be 1LSB. But an ADC with DNL shows step widths which are not exactly 1LSB. In Figure 3-6 Differential Non-Linearity (DNL), in a maximum case the width of the step with output value 101 is 1.5LSB which should be 1LSB. The DNL in this case would be +0.5LSB. Whereas in a minimum case, the width of the step with output value 001 is only 0.5LSB which is 0.5LSB less than the expected width. Now, the DNL would be ±0.5LSB.

3.4.2. Integral Non-Linearity (INL)

Integral non-linearity (INL) is defined as the maximum vertical difference between the actual and the ideal curve. It indicates the amount of deviation of the actual curve from the ideal transfer curve. INL can be interpreted as a sum of DNLs. For example, several consecutive negative DNLs raise the actual curve above the ideal curve as shown in Figure 3-7 Integral Non-Linearity (INL) and the INL in this case would be positive. Negative INLs indicate that the actual curve is below the ideal curve. This means that the distribution of the DNLs determines the integral linearity of the ADC.

Figure 3-7. Integral Non-Linearity (INL)

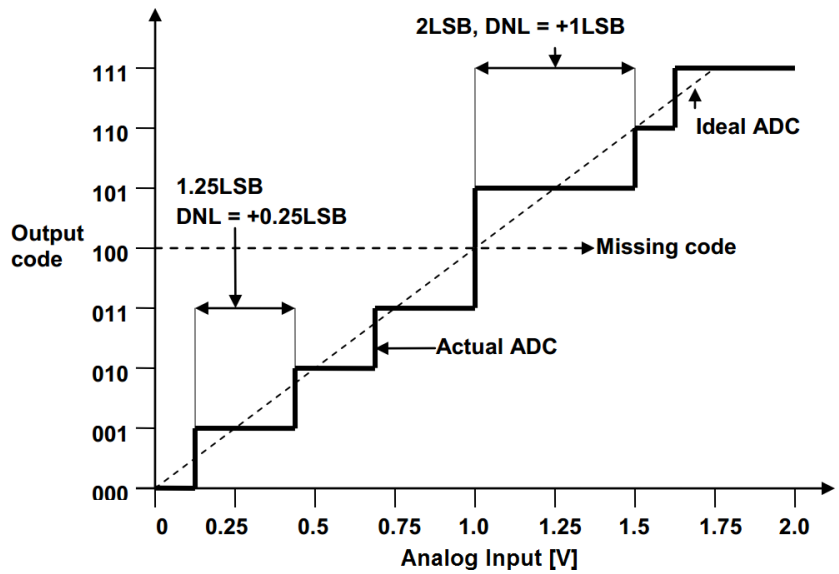


The INL can be measured by connecting the midpoints of all output steps of the actual ADC and finding the maximum deviation from the ideal curve in terms of LSBs. In the example shown, we can note that the maximum INL is +0.75LSB.

3.4.3. Missing code

There are some special cases where the actual transfer function of the ADC appears as shown in following graphic.

Figure 3-8. Missing Code shown in 3-bit ADC



In the following example, the first code transition (from 000 to 001) occurs when the value of input changes by 250mV. This is exactly as expected. The second transition, from 001 to 010 has an input change that is 1.25LS. So it is larger by 0.25LSB. The change in the input for the third transition is exactly the right size. The digital output remains constant when the input voltage changes from 1000mV to 1500mV and the code 100 can never appear at the output. It is missing. The higher the resolution of the

ADC, lesser the severity of the missing code is. An ADC with DNL error less than ±1LSB guarantees no missing code.

3.5. Total Unadjusted Error (TUE)

The Total Unadjusted Error or Absolute error is the total uncompensated error that includes Quantization, Offset, Gain and Non-Linearity Errors. In other words, it is the maximum deviation between ideal expected value and actual value obtained from the ADC for any input voltage. In a perfect case, the TUE is 0.5LSB which is due to the quantization error. The gain and offset errors are more significant contributors to the absolute error.

As seen from earlier sections, offset and gain error reduces the effective ADC range. The Total Unadjusted Error represents a reduction in the ADC range. Applications prone to higher TUE should have some margins against the minimum and maximum input values to avoid the TUE impact.

4. Noise Parameters

4.1. Signal to Noise Ratio (SNR)

SNR is defined as the ratio of the output signal voltage level to the output noise level. It is usually represented in decibels (dB) and calculated using the following formula.

$$SNR(dB) = 20\log\left(\frac{V_{RMS(Signal)}}{V_{RMS(Noise)}}\right)$$

For example if the output signal amplitude is 1V(RMS) and the output noise amplitude is 1mV(RMS), then the SNR value would be 60dB. The above formula is a general definition for SNR. The SNR value of an ideal ADC is calculated using the following formula:

SNR (dB) = 6.02N+1.76(dB)

where N is the resolution (no. of bits) of the ADC. For example an ideal 10-bit ADC will have an SNR of approximately 62dB.

Note: In practical applications, to achieve better performance, the SNR value of an ADC should be higher.

4.2. Total Harmonic Distortion (THD)

Whenever an input signal of a particular frequency passes through a non-linear device, additional content is added at the harmonics of the original frequency. For example, assume an input signal having frequency f. Then the harmonic frequencies are 2f, 3f, 4f, etc. So non-linearity in the converter will produce harmonics that were not present in the original signal. These harmonic frequencies usually distort the output which degrades the performance of the system. This effect can be measured using the term called total harmonic distortion (THD).

THD is defined as the ratio of the sum of powers of the harmonic frequency components to the power of the fundamental/original frequency component. In terms of RMS voltage, the THD is given by,

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + \ldots + V_n^2}}{V_1}$$

The THD value increases with the increase in the frequency. The THD should have minimum value for less distortion. As the input signal amplitude increases, the distortion also increases.

Note: In practical applications, to achieve better performance, the THD value of an ADC should be lesser.

4.3. Signal to Noise and Distortion (SINAD)

Signal to noise and distortion (SINAD) is a combination of SNR and THD parameters. It is defined as the ratio of the RMS value of the signal amplitude to the RMS value of all other spectral components, including harmonics, but excluding DC. For representing the overall dynamic performance of an ADC, SINAD is a good choice since it includes both the noise and distortion components.

SINAD can be calculated with SNR and THD by

$$SINAD = -10\log\left(10^{-SNR/10} + 10^{-THD/10}\right)$$

Note: In practical applications, to achieve better performance, the SINAD value of an ADC should be higher.

4.4. Effective Number Of Bits (ENOB)

Effective number of bits (ENOB) is the number of bits with which the ADC behaves like a perfect ADC. It is another way of representing the signal to noise ratio and distortion (SINAD) and can be derived from the following formula.

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Note: In practical applications, to achieve better performance, the ENOB value of an ADC should be as close as possible to the resolution of the ADC.

5. Oversampling

Oversampling is a process of sampling the analog input signal at a significantly higher sampling rate than the Nyquist sampling rate. The main advantages of oversampling are:

1. It avoids the aliasing problem, since the sampling rate is higher compared to the Nyquist sampling rate.
2. It provides a way of increasing the resolution of the ADC. For example, to implement a 14-bit converter, it is enough to have a 10-bit converter which can run at 256 times the target sampling rate. Averaging a group of 256 consecutive 10-bit samples adds four bits to the resolution of the average, producing a single sample with 14-bit resolution.
3. The number of samples required to get additional **n** bits is = 2^{2n}.
4. It improves the SNR of the ADC.

More samples are measured to increase the resolution, which leads to reduced throughput of the ADC module. For example, a 10-bit converter with a capacity of sampling 1 kilo samples per second can be used as a 14-bit converter with a throughput of 4 samples per second.

6. ADC Timings

Basically, an ADC requires some time for startup, sampling, and holding and for conversion. The startup time is higher in the ADCs available in complex microcontrollers that operate at higher frequencies.

6.1. Startup Time

Startup time contains the minimum time (in clock cycles) required to guarantee the best converted value after the ADC has been enabled either for the first time or after a wake up from specific sleep modes.

6.2. Sample and Hold Time

After triggering an ADC to start a conversion, it takes some time (in clock cycles) to charge the internal capacitor to a stable value in order to get accurate conversion results. This time is called as *Sample Time*. When multiple channels are used for conversion, this sample time must be carefully considered. A minimum time (in clock cycles) is required to ensure the proper conversion of the value between two ADC channel switching. The number of clock cycles required to convert the charge or the voltage across the internal sampling capacitor into corresponding digital code is called the *Hold Time*.

6.3. Settling Time

When multiple channels are used, there may be scenarios where each channel may have different gain and offset configurations. Switching between these channels requires a specific amount of time, before beginning the sample and hold phase, in order to have accurate results. Especially care should be taken when switching between differential channels. When a differential channel is selected, the ADC must wait for some time for some of the analog circuits (for example the automatic offset cancellation circuitry) to stabilize to the new value. This duration is called as *Settling Time*. If ADC conversion is started before the settling time it will produce an erroneous output.

The settling time must be observed for the first differential conversion after changing the ADC reference.

6.4. Conversion Time

The combination of the sampling time and the hold time, is called conversion time. This is usually represented in number of clock cycles. The conversion time is the primary parameter in deciding the speed of the ADC.

The startup time, sample time, hold time, and the settling time are all software configurable in ADC's of some high end microcontrollers.

6.5. Sampling Rate, Bandwidth and Throughput Rate

Sampling rate is defined as the number of samples acquired in one second. The Bandwidth represents the maximum frequency of the input analog signal that can be provided to the ADC. The sampling rate and bandwidth follow Nyquist sampling theorem. According to this theorem, the sampling rate must be at least twice the bandwidth of the input signal.

Consider the case of single ended conversion where one conversion takes 13 ADC clock cycles. Assuming the ADC clock frequency to be 1MHz, then approximately 77k samples will be converted in one second. That means the sampling rate is 77k. According to Nyquist theorem, the maximum frequency of

the analog input signal is limited to 38.5kHz, which represents the bandwidth of the ADC in single ended mode.

Similarly, if 1MHz is the maximum clock frequency that can be applied to an ADC which takes at least 13 ADC clock cycles for converting one sample, then 77k samples per second is the maximum throughput rate of the ADC.

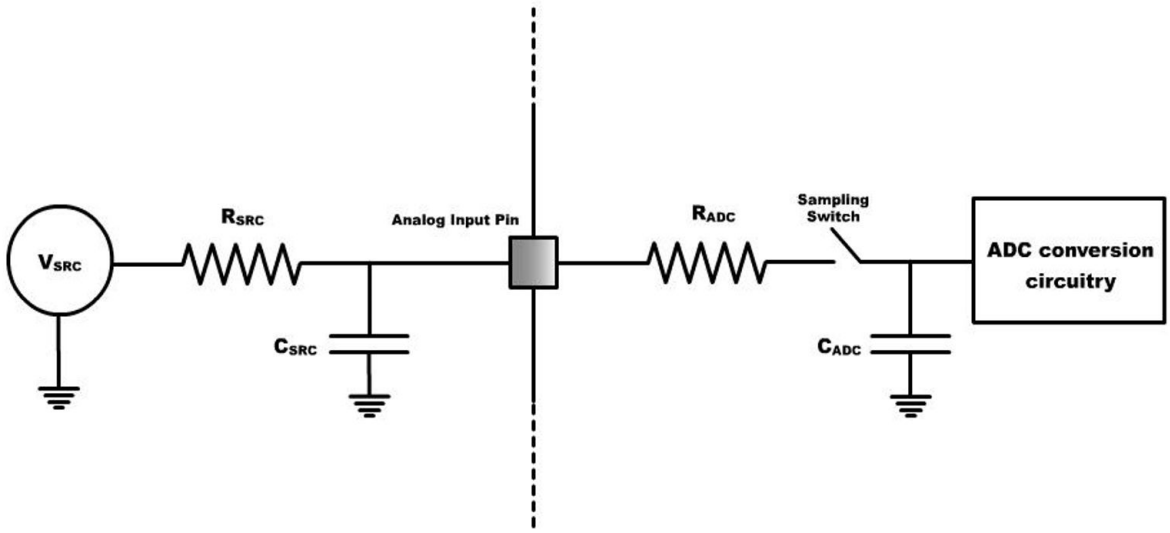
While using differential mode, the bandwidth is also limited to the frequency of the internal differential amplifier. Before providing the analog input to the ADC, any frequency component beyond the specified bandwidth must be filtered using an external filter to avoid any non-linearity.

7. Impedances and Capacitances of ADC

Inside an ADC, the sample and hold circuit of the ADC contains a resistance-capacitance (R_{ADC} and C_{ADC}) pair in a low pass filter arrangement. The C_{ADC} is also called as sampling capacitor. Whenever an ADC start conversion signal is issued, the sampling switches between the R_{ADC} – C_{ADC} pair is closed so that the analog input voltage charges the sampling capacitor through the resistance R_{ADC}.

The following figure depicts the equivalent circuit of an ADC system.

Figure 7-1. Equivalent Circuit of an ADC System



The input impedance of the ADC is the combination of R_{ADC} and the impedance of the capacitor. As the sampling capacitor gets charged to the input voltage, the current through R_{ADC} reduces and ends up with a minimum value when voltage across the sampling capacitor equals the input voltage. So the minimum input impedance of the ADC equals R_{ADC}.

In the source side, the ideal source voltage is subject to some resistance called the source resistance (R_{SRC}) and some capacitance called source capacitance (C_{SRC}) present in the source module. Because of the presence of R_{SRC}, the current entering the sample and hold circuit reduces. So this reduction in current increases the time to charge the sampling capacitance thereby reducing the speed of the ADC. Also the presence of C_{SRC} makes the source to first charge it completely before charging the sampling capacitor. This reduces the accuracy of the ADC since the sampling capacitor may not be completely charged.

Note:

1. R_{ADC} and C_{ADC} are a part of the ADC specification. Refer the device datasheet for more information.
2. R_{SRC} and C_{SRC} directly affects the operating speed and accuracy of ADC module. In the practical applications, R_{SRC} and C_{SRC} of the input signal must be considered while selecting the ADC parameters.

8. Revision History

Doc. Rev.	Date	Comments
8456D	05/2016	General improvements of descriptions.
8456C	10/2013	Updated typo in list item 3 in section Oversampling 2^2n corrected to 2^{2n}
8456B	07/2013	General improvements in regards of descriptions.
8456A	11/2011	Initial revision

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