AN3589

Using Sigma-Delta Analog-to-Digital Converter (SDADC) on a SAMC MCU with MPLAB Harmony v3

Introduction

The Sigma-Delta Analog-to-Digital Converter (SDADC) converts analog signals to digital values. The SDADC has 16-bit resolution at 1ksps and is capable of converting up to 1.5 Msps divided by the data over sampling ratio (OSR).

The input selection has up to three differential analog channels. The SDADC provides signed results. ADC measurements can be started by either application software or an incoming event from another peripheral in the device. ADC measurements can be started with predictable timing and without software intervention. The SDADC also integrates a Sleep mode and a conversion sequencer. These features reduce power consumption and processor intervention. A set of reference voltages are generated internally.

This document describes the SDADC in ATSAMC21N device is configured in differential mode and the SDADC results are displayed on a console. It also provides example code for both interrupt and polling methods, developed using MPLAB® X IDE and MPLAB Harmony v3 Configurator for reference.

Features

- Sigma-Delta converter with 16-bit resolution at 1 ksps
  - Three external analog differential input pairs
- Conversion range 0V to a wide range of VREF options
  - Hardware gain, offset, and shift compensation

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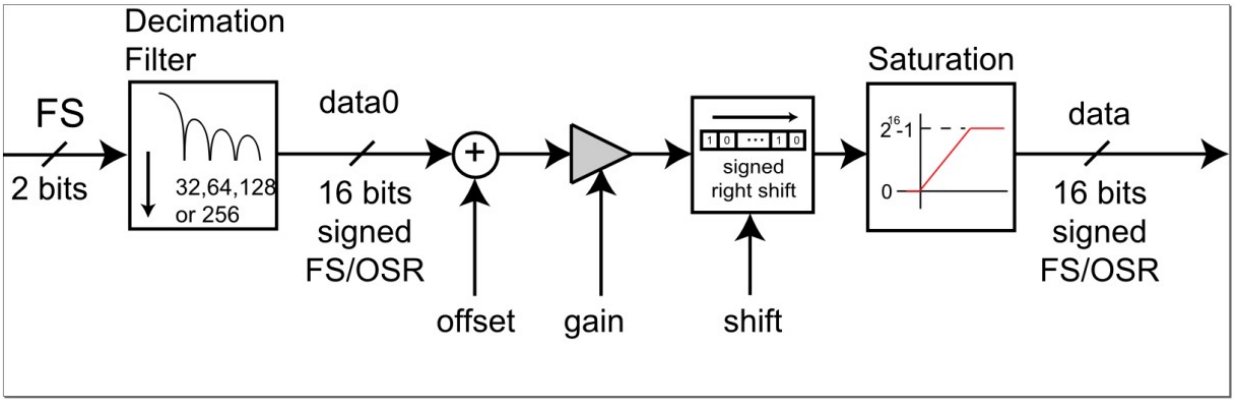
1. Module Overview

1.1 Description

The Sigma-Delta Analog-to-Digital Converter (SDADC) converts an analog voltage to a signed 16-bit value by integrating and decimating the output of a sigma-delta modulator. The filtering and decimation are done using a sinc-based filter that has zeros placed to minimize the aliasing effects of the decimation. This is a 3rd order sinc filter with an adjustable Oversampling Ratio (OSR) to achieve higher throughput, as shown in the figure below. For example, an OSR of 64 will provide an output at 23 ksps while an OSR of 1024 will produce an output at a sample rate of 1.4 ksps.

Figure 1-1. Cascaded Integrator-Comb (CIC) Decimation Filter

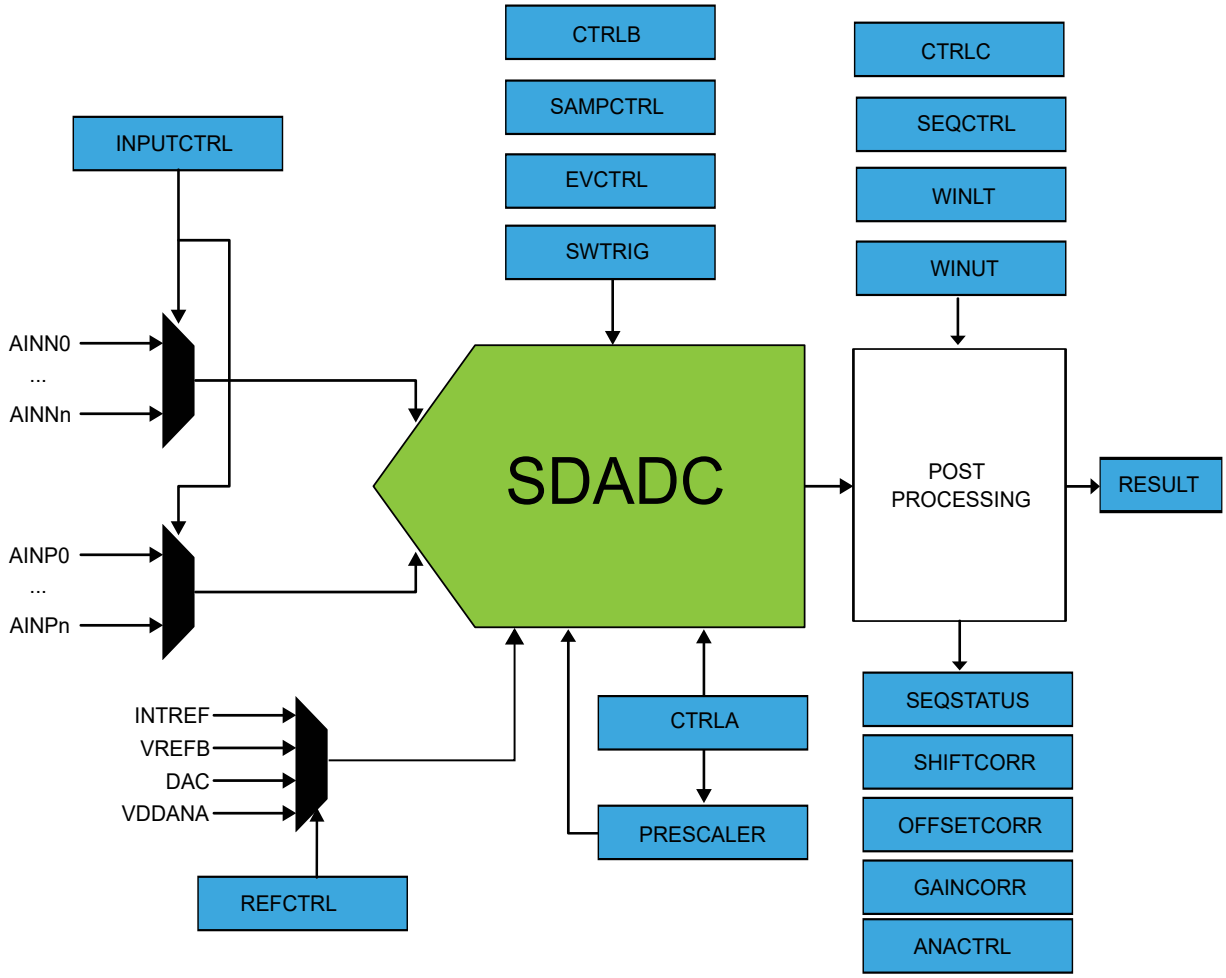


The SDADC provides a signed result in a 24-bit register to allow for gain and offset correction without overflow in hardware. Because the result is in 2's complement format, the SDADC result is signed 16-bit (maximum) using ±VREF. Using the internal VREF set at 1.024V, the SDADC will produce codes for ±1.024V. The internal VREF can be configured to supply a reference of 1.024V, 2.048V, and 4.096V.

Note: The range selected in the REFSEL register must match the supplied VREF and must be set independently of the internal VREF, if not it will result in incorrect readings.

1.2 Register Interface

Figure 1-2. SDADC Register Interface



2. Functional Description

The Sigma Delta Analog-to-Digital Converter (SDADC) can be used for high-resolution ADC measurements, and these measurements can include: Temperature sensors, Thermocouples, Cold-Junction Compensation, 3-4 Wire RTD sensors, 4-20 mA current loops, current (Shunt), as well as scales and load cells. The Sigma-Delta architecture provides a low-cost solution for these precision measurements that requires only a simple R-C lo-pass filter for anti-aliasing.

A generic clock (GCLK_SDADC) is used to generate the CLK_SDADC through a 7-bit prescaler. The GCLK must be configured and enabled before using the SDADC. The sampling clock is derived from the CLK_SDADC/4. Therefore, the maximum CLK_SDADC is 6 MHz, as the maximum sampling frequency is 1.5 MHz. The GCLK_SDADC is asynchronous to the APB bus clock, therefore, writes to registers require synchronization. This generic clock allows configuring CLK_SDADC to run in sleep modes based on the values of RUNSTDBY (Run in Standby), ONDEMAND (On Demand Control) and ENABLE (Enable) bits of the CTRLA (Control A) register. The 7-bit prescaler enables flexible sampling frequency adjustment.

The SDADC supports differential measurements on three analog input channels which can be used sequentially. The measurements are done using any one of four references: internal bandgap, external voltage on VREFB (Voltage Reference) pin, Digital-to-Analog Converter (DAC) output, or VDD Analog (VDDANA). The voltage reference has a selectable buffer to offer higher input impedance to the external reference.

The SDADC filters and decimates the sigma-delta output bit stream at 16-bit (signed) with programmable rates of CLK_SDADC_FS (prescaled SDADC clock frequency) divided by 64 to 1024. The Output rate is set by modifying the programmable Over Sampling Ratio (OSR). The result is a 2’s compliment 24-bit result with programmable gain and offset correction.

The SDADC peripheral supports three interrupts:

- Result Ready Interrupt (RESRDY) - The RESRDY can trigger a DMA transfer or event.
- Overrun Interrupt (OVERRUN) - The OVERRUN flag is set when the previous result is not read before a new result is ready.
- Window Monitor Interrupt (WINMON) - The WINMON can generate an event by setting the WINMONEO bit in the EVCTRL register.

Automatic sequences can be configured to enable multiple samples from a single start of conversion request. The order of this conversion is from the lower positive input pair to the upper positive input pair (AINN0, AINP0, AINN1, AINP1 ...).

Note: If the SEQCTRL register has no bits set to ‘1’, the conversion is done with the selected INPUTCTRL input (MUXSEL). Window Monitor can be used to define a threshold and trigger the WINMON flag (or interrupt).

2.1 Basic Operation

2.1.1 Initialization

The SDADC must be configured with the peripheral disabled. The register setting sequence to configure and enable the SDADC is as follows where the notations are stated in the form <register.bit(s)>:

- Enable the Generic Clock
- Select the Voltage Reference and Range
  - REFCTRL.REFRANGE
  - REFCTRL.REFSEL
- Set the Conversion Rate and Resolution
  - GCLK_SDADC
  - CTRLB.PRESCALER (SDADC_CLK)
  - CTRLB.OSR (Over Sampling Ratio)
- Select trigger source or interrupts
  - SWTRIG.START (Software Trigger)
  - Free Run Mode

  - DMA/Event
  - Timers
- Sequence Control
  - Automatic Sequences (SEQCTRL)
  - Lower-to-Upper Positive Pairs
  - The SEQSTATUS.SEQBUSY bit will be set when a conversion is initiated and cleared when sequence is complete
  - The input number is stored with the RESULT
- Window Monitor Control
  - RESULT compared to threshold
  - WINUT/WINLT (Upper and Lower Thresholds)
  - WINCTRL.WINMODE (Inside/Outside window)
  - INTFLAG.WINMON (Interrupt flag)
- Configure Input Pins
  - INPUTCTRL.MUXSEL[3:0]
- Configure Interrupts
  - INTENSET.RESRDY (Conversion ready)
  - INTENSET.WINMON (Threshold reached)
  - INTENSET.OVERRUN (previous result not read)

2.1.2 Reading the Results

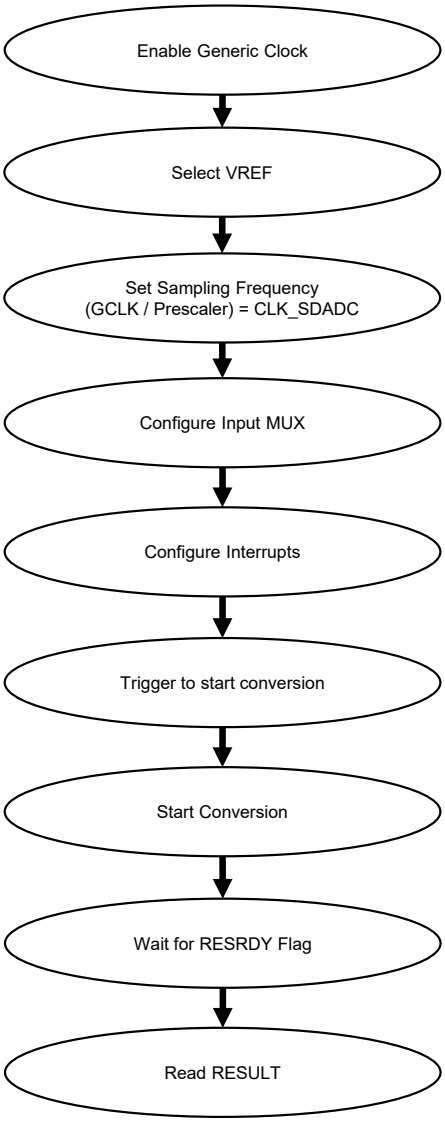
The SDADC result ready flag (RESRDY) will be set when a conversion is complete. When the peripheral is first initialized, the results are only valid after the 3rd conversion. To automate this limitation in hardware, the register set includes the skip count field in CTRLB register (CTRLB.SKPCNT[3:0]) to automatically skip the first ‘n’ results. When in free running mode, the application must read the result prior to the next result being ready. If this does not happen, the overrun flag will be set.

The result is read from the RESULT register.

2.2 Usage Summary

The following flowchart explains the procedure of configuring the SDADC for reading the SDADC Result.

Figure 2-1. Reading the SDADC Result Flow Chart



3. Firmware Implementation

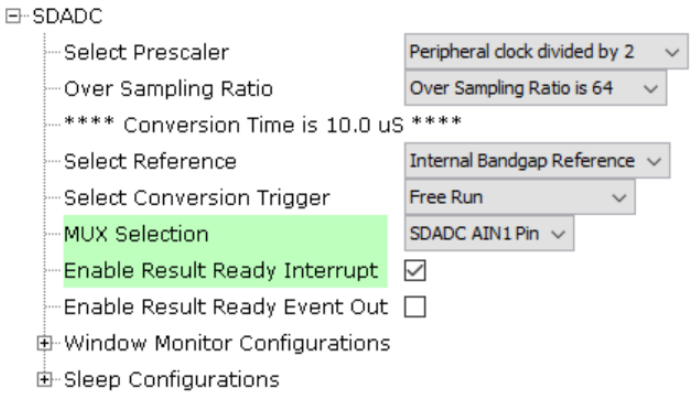
With the MPLAB Harmony Configurator (MHC), the required peripheral library (PLIB) files are generated by configuring the respective components. Easy to use APIs have been provided to use the peripheral. This example demonstrates the basic use of the SDADC in interrupt and polling modes.

3.1 MPLAB Harmony v3 Configurator SDADC Configurations

The default configurations made in the MPLAB Harmony Configurator for the SDADC peripheral are as follows, and it is shown in the following figure.

- Over Sampling Ratio = 64
- Internal Bandgap Reference = 4.096V
- Interrupts Enabled

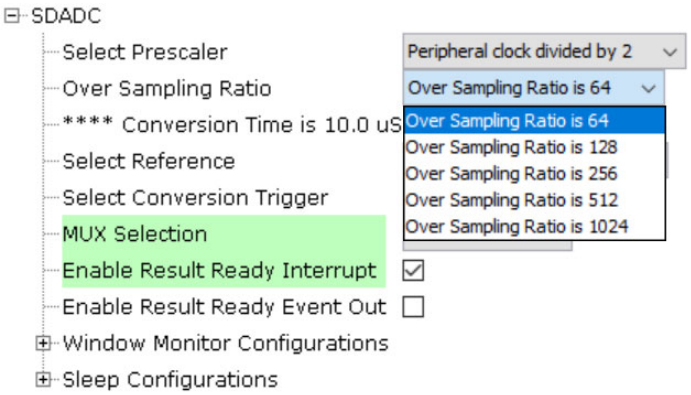
Figure 3-1. SDADC Configurations in MPLAB Harmony v3 Configurator



The above default configurations can be changed in the MPLAB Harmony v3 Configurator, by following these steps:

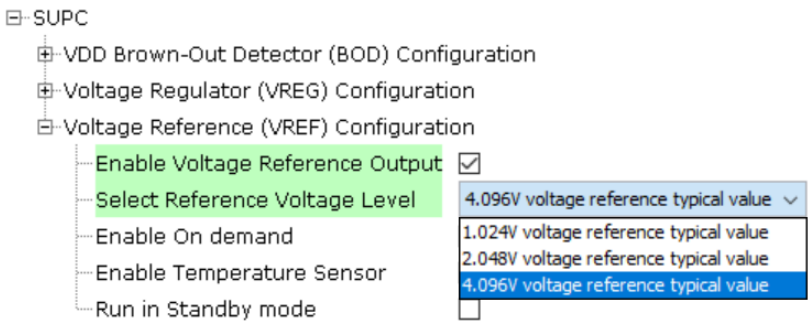
1. In MPLAB X IDE, navigate to the *Tools* > *Embedded* > *MPLAB Harmony v3 Configurator*.
2. To change the Over Sampling Ratio, click on the **SDADC** module and select the desired value from the **Over Sampling Ratio** drop-down list as shown in the following figure.

   Figure 3-2. OSR Drop-Down List in MPLAB Harmony v3 Configurator



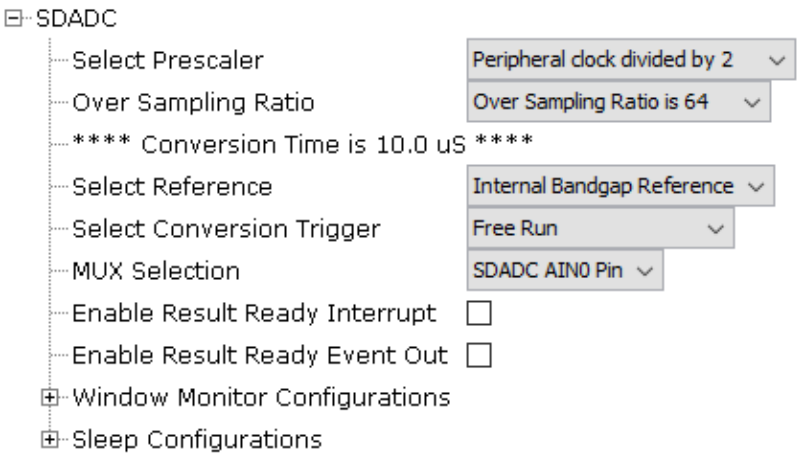
3. To change the Interval Voltage Reference value, in the Project Graph, click on the **SUPC** module.
4. Select the desired voltage reference value from the Select Reference Voltage Level drop-down list as shown in the following figure.

Figure 3-3. Reference Voltage Level Drop-Down List in MPLAB Harmony v3 Configurator



5. The interrupt can be disabled to work with polling method. Click on the **SDADC** module and clear the **Enable Result Ready Interrupt** option and generate the code.

Figure 3-4. SDADC Result Ready Interrupt Disabled in MPLAB Harmony v3 Configurator



6. In the `plib_sdadc.c` file generated for polling mode, the `bool SDADC_ConversionResultIsReady( void )` function will be added. This API returns a Boolean value as a status to confirm if the results are ready.
7. In the `main.c` file, check for this status and proceed to read when the results are ready. Refer to the polling mode project, where this has been implemented.
8. Save the configurations and generate the code by selecting *MHC* > *Generate Code*.
9. Update the `plib` files with appropriate changes taken into consideration.

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3.2 Peripheral Library (PLIB) APIs

MPLAB Harmony v3 provides the PLIB APIs for the SDADC in `plib_sdadc.c`. The following APIs allow for the configuration, initialization, and reading the SDADC:

- `void SDADC_Initialize(void)`
- `int16_t SDADC_ConversionResultGet(void)`
- `bool SDADC_ConversionResultIsReady (void );`

3.3 Callback APIs

In addition to the PLIB APIs, the following callback APIs are included:

- `void SDADC_CallbackRegister(SDADC_CALLBACK callback, uintptr_t context)`

3.4 Support APIs

The SAMC21N supports a variety of voltage references to support different measurement requirements when using the SDADC peripheral. The following support API provides the application of the examples.

- `void App_SDADC_Config(void)`
- For more information on SDADC APIs, refer to:
  microchip-mplab-harmony.github.io/csp/frames.html?frmname=topic&frmfile=06665.html

3.5 SDADC Example

This document is accompanied by example firmware, which is listed as follows.

- `sdadc_conversion_polling`: Demonstrates the SDADC conversion in polling mode
- `sdadc_conversion_interrupt`: Demonstrates the SDADC conversion in interrupt mode

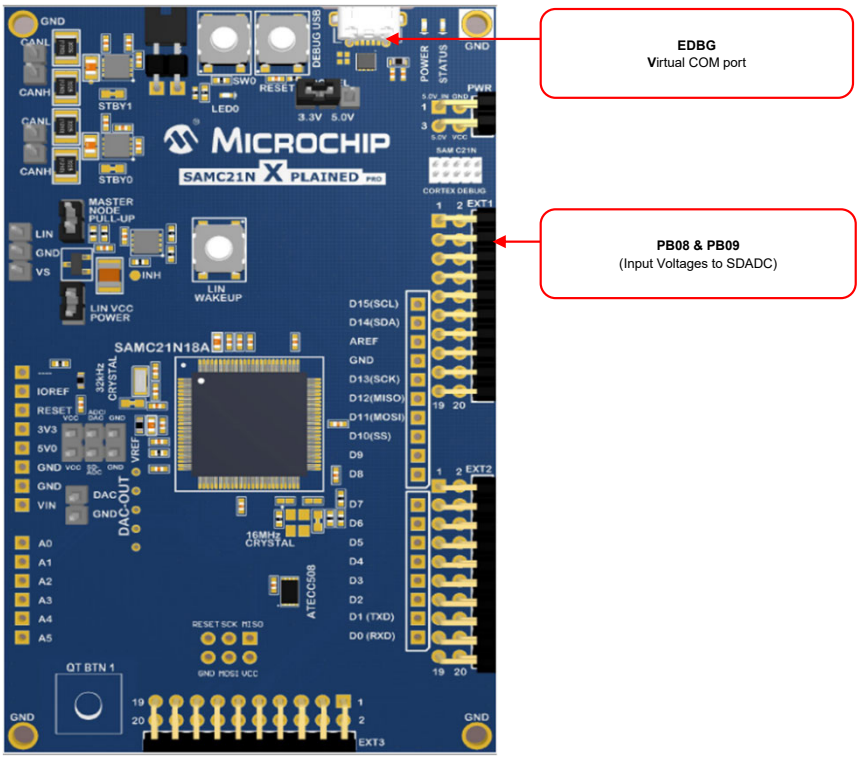
3.5.1 Requirements

- MPLAB X IDE version 5.40 or higher
  www.microchip.com/mplab/mplab-x-ide
- MPLAB X C32 Compiler v2.41 or higher
  www.microchip.com/mplabx/compilers
- MPLAB Harmony Configurator Plugin v3.5.0 or higher
- MPLAB Harmony v3 "csp" repo v3.7.1 or higher
  github.com/Microchip-MPLAB-Harmony/csp/releases/tag/v3.7.1
- MPLAB Harmony v3 "dev_packs" repo v3.7.0 or higher
  github.com/Microchip-MPLAB-Harmony/dev_packs
- MPLAB Harmony v3 "mhc" repo v3.4.0 or higher
  github.com/Microchip-MPLAB-Harmony/mhc
- SAMC21N Xplained Pro evaluation kit
  www.microchip.com/DevelopmentTools/ProductDetails/PartNO/ATSAMC21N-XPRO
- Stable Voltage Source to INN[1] and INP[1] pins, or PB08 and PB09.

3.5.2 Description

The example firmware initializes the SDADC on the SAMC21N Xplained Pro board to use Input Channel one . This is a differential measurement, therefore ensure that both the positive (INP) and negative (INN) pins are connected to a voltage source. The firmware also initializes the USART to communicate with a terminal program through the on-board EDBG Virtual COM port. Settings are 115200, 8, N, 1.

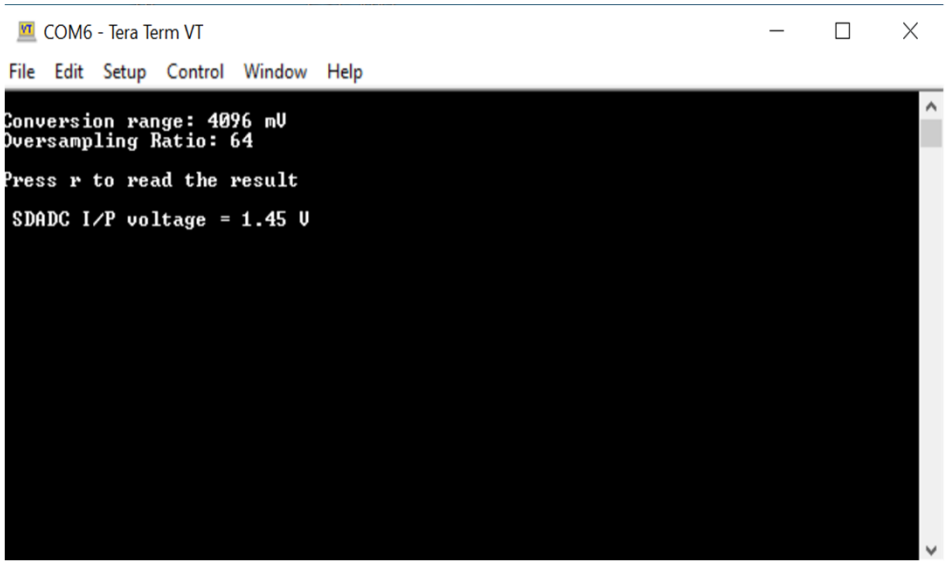
Figure 3-5. SAMC21N Xplained Pro Evaluation Kit



The SDADC is configured to use the internal VREF, and the range is set to 4.096 V full scale and the default setting of the OSR is 64.

Pressing the ‘r’ key will read the result and display it in a form scaled to mV.

Figure 3-6. Output Displayed on Terminal Window



4. Conclusion

This document was intended to emphasize the usage of MPLAB Harmony v3 Configurator and has described the procedure for configuring the SDADC of the ATSAMC21N. The Differential mode of this 16-bit resolution SDADC has been used and the results are displayed on a console. The user can directly program the code to the device and view the result on the terminal console.

5. References

- MPLAB Harmony v3:
  www.microchip.com/mplab/mplab-harmony
- SAM C20/C21 Family Data Sheet:
  ww1.microchip.com/downloads/en/DeviceDoc/SAMC20_C21_%20Family_Data_%20Sheet_DS60001479D.pdf
- SAM C21N Xplained Pro:
  ww1.microchip.com/downloads/en/DeviceDoc/70005318A.pdf
- AT10294: Using the Sigma-Delta Analog to Digital Converter on SAMC MCU (SDADC):
  ww1.microchip.com/downloads/en/DeviceDoc/Atmel-42467-Using-the-Sigma-Delta-Analog-to-Digital-Converter-on-SAMC-MCU-(SDADC)_ApplicationNote_AT10294.pdf
- SAM C21 Getting Started Training Module:
  microchipdeveloper.com/harmony3:samc21-getting-started-training-module
- Clock System Configuration Technical Brief:
  ww1.microchip.com/downloads/en/DeviceDoc/Clock_System_Configuration_Usage_on_SAMC2x(Cortex%20M0+)_%20Devices_DS90003227A.pdf

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