
USB to SPI Bridging with Microchip USB 2.0 Hubs

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INTRODUCTION

The USB to SPI bridging feature of Microchip hubs provides system designers with expanded system control and potential BOM reductions. When using Microchip's USB hubs, a separate USB to SPI device is no longer required and a downstream USB port is not lost, as occurs when a standalone USB to SPI device is implemented. This feature is available on Microchip hubs which contain the internal Hub Feature Controller and a SPI Interface. These hubs include USB3613, USB3813, USB4604, and USB4624.

Commands may be sent from the USB Host to the internal Hub Feature Controller device in the Microchip hub to perform the following functions:

- Enable SPI Pass-Through Interface
- SPI Write/Read
- Disable SPI Pass-Through Interface

SECTIONS

[Section 1.0, General Information](#)

[Section 2.0, Part Number Specific Information](#)

[Section 3.0, SDK Implementation](#)

[Section 4.0, Manual Implementation](#)

REFERENCES

Consult the following documents for details on the specific parts referred to in this document:

- *USB3613 Data Sheet*
- *USB3813 Data Sheet*
- *USB4604 Data Sheet*
- *USB4624 Data Sheet*
- *AN 26.18 Configuration of the USB253x / USB3x13 / USB46x4*

1.0 GENERAL INFORMATION

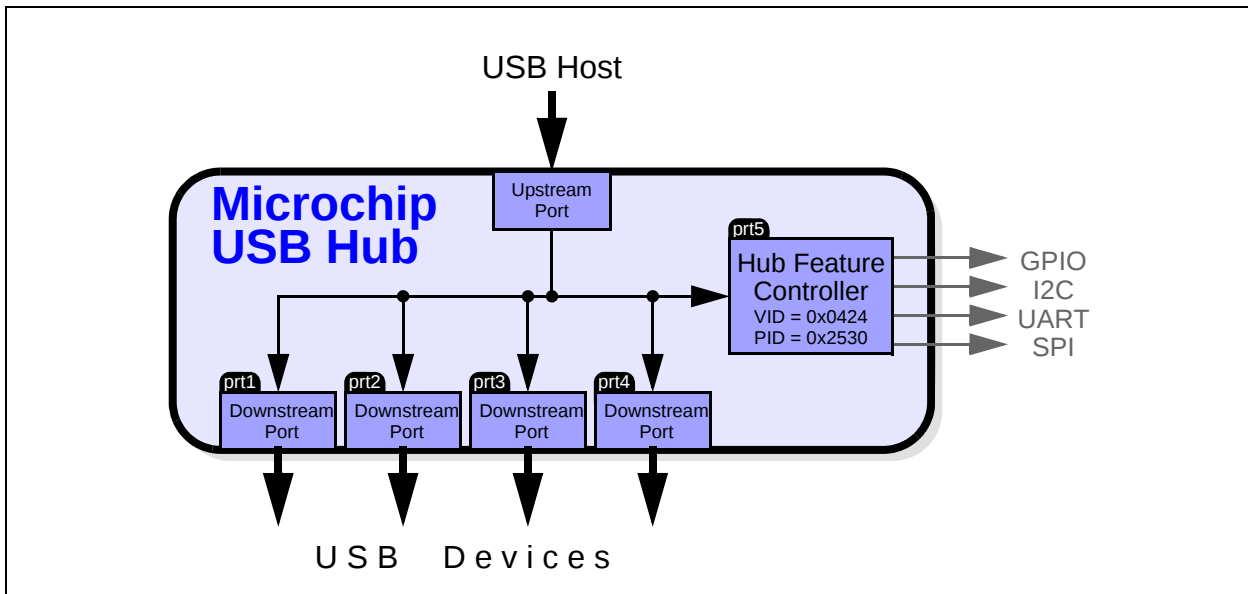
Microchip's USB hub bridging features operate via host commands which are sent to an embedded Hub Feature Controller located on an additional internal USB port. In order for the bridging features to work correctly, this internal Hub Feature Controller must be enabled by default. See the table below for details on default Hub Feature Controller settings by part.

TABLE 1: DEFAULT SETTINGS FOR HUB FEATURE CONTROLLER ENABLE

Part Number	Part Summary	Hub Controller Default Setting
USB2532	2-Port USB 2.0 Hub	Disabled (enable via config)
USB2533	3-Port USB 2.0 Hub	Disabled (enable via config)
USB2534	4-Port USB 2.0 Hub	Disabled (enable via config)
USB3613	3-Port USB 2.0 Mobile Hub (HSIC Upstream / 1 HSIC Downstream Port)	Disabled (enable via config)
USB3813	3-Port USB 2.0 Mobile Hub (1 HSIC Downstream Port)	Disabled (enable via config)
USB4604-1080	4-Port USB 2.0 Hub (USB or HSIC Upstream)	Enabled
USB4604-1070	4-Port USB 2.0 Hub (USB or HSIC Upstream)	Disabled (order 1080 SKU)
USB464-1080	4-Port USB 2.0 Hub (USB or HSIC Upstream / 2 Downstream HSIC Ports)	Enabled
USB4624-1070	4-Port USB 2.0 Hub (USB or HSIC Upstream / 2 Downstream HSIC Ports)	Disabled (order 1080 SKU)

The Hub Feature Controller is connected to an extra internal port in the hub. For example, in a four port hub, the Hub Feature Controller is connected to port 5. The Product ID (PID) for the Hub Feature Controller is 0x2530. All bridging commands are addressed to the Hub Feature Controller, not the Hub.

FIGURE 1-1: MICROCHIP HUB FEATURE CONTROLLER BLOCK DIAGRAM



1.1 SPI Bridging Commands

The following SPI Functions are supported:

- Enable SPI Pass-Through Interface
- SPI Write/Read
- Disable SPI Pass-Through Interface

1.1.1 ENABLE THE SPI PASS-THROUGH INTERFACE

A single command to enable the SPI interface is required before performing any SPI Write or Read commands. The SPI interface may operate at either 30MHz or 60MHz (based on pin-strapping).

1.1.2 SPI WRITE/(READ)

The SPI interface works as a complete pass-through. This means that the host must properly arrange data payloads in the appropriate SPI compatible format and bit order, including the SPI slave device address. Up to 256 Bytes of data payload may be sent per SPI write command sequence.

Data may also be read from a SPI device via the SPI Write command. Up to 512 bytes of data may be read from the SPI device per read. The read data is stored in the internal registers of the hub starting at register 0x4A10. To retrieve the data, you must use a USB to Register Read command. Further details can be found in *AN 26.18 Configuration of the USB253x / USB3x13 / USB46x4*.

1.1.3 DISABLE THE SPI PASS-THROUGH INTERFACE

The SPI interface may be disabled after writing/reading to the device is complete.

1.2 SPI Interface Setup Requirements

1.2.1 SPI MASTER INTERFACE

The SPI Interface always acts as a SPI master.

1.2.2 SELECTING SPI FREQUENCY

The SPI Interface may operate at either 30MHz or 60MHz. The speed is selected by pin strapping the SPI_SPD_SEL pin (also the SPI_DO pin during runtime) and is detected at power on or reset. The strapping options are:

- GND (Logical 0) = 30MHz
- 3.3V (Logical 1) = 60MHz

When running in 30MHz mode, the SPI_DO/SPI_SPD_SEL pin will drive to 0V during a suspend state. When running in 60MHz mode, the SPI_DO/SPI_SPD_SEL pin will tri-state during a suspend state.

1.2.3 SPI MODES OF OPERATION

Both SPI Modes 0 and 3 are supported:

- Mode 0: Clock Polarity = 0, Clock Edge = 1
- Mode 3: Clock Polarity = 1, Clock Edge = 0

Dual Output Enable mode is also supported.

The default mode of operation is Mode 0 with Dual Output Enable mode disabled. If the mode of operation is to be modified, a register write to the SPI_CONTROL register must be performed. See *AN 26.18 Configuration of the USB253x / USB3x13 / USB46x4* for details on how to modify that register.

2.0 PART NUMBER SPECIFIC INFORMATION

2.1 Part Summary

The following tables display the SPI interface pins by part number as well as any notes on those pins.

2.2 USB3613 and USB3813

TABLE 2: USB3613 AND USB3813 SPI INTERFACE PINS

Pin #	Name	Notes
E2	SPI_DI	-
E1	SPI_CE_EN	-
D3	SPI_DO	This pin is also the SPI_SPD_SEL Strap which selects between 30MHz and 60MHz speed of operation.
D2	SPI_CLK	-

2.3 USB4604 and USB4624

TABLE 3: USB4604 AND USB4624 SPI INTERFACE PINS

Pin #	Name	Notes
31	SPI_DI	-
25	SPI_CE_EN	-
26	SPI_DO	This pin is also the SPI_SPD_SEL Strap which selects between 30MHz and 60MHz speed of operation.
27	SPI_CLK	-

3.0 SDK IMPLEMENTATION

The simplest method for implementing the USB to SPI bridging functions is to use the publicly available USB2530 SDK (Software Development Kit). The SDK is available for Windows and Linux operating systems. Visit the product page for any of the hubs listed in this document on microchip.com to download the SDK package for the desired Operating System. Using the libraries available in the SDK, the bridging features can be implemented in C-code.

The SDK package contains the following:

- User's Manual: Detail description of how to use the SDK and call each function
- Release Notes:
- Library Files:
 - For Windows: A ".dll" and a ".lib" file
 - For Linux: a ".cpp" file that can be built into a ".a" file
- Example code

3.1 Commands included in the SDK

- **MchpUsbSpiSetConfig:** Enables or Disables the SPI interface.
- **MchpUsbSpiWrite:** Write up to 255 Bytes of data to an SPI slave device.
- **MchpUsbSpiRead:** Read up to 255 Bytes of data from an SPI slave device.

For additional details on how to use the SDK to implement USB to SPI bridging, download the SDK package and read the User's Manual.

4.0 MANUAL IMPLEMENTATION

The USB to SPI bridging features may be implemented at the lowest level if you have the ability to build USB packets. This approach is required if you are not using a Windows or Linux host system and cannot use the SDK.

The details of the SPI pass-through control packets are shown below.

4.1 Enable SPI Pass-Through Interface Command

The following SETUP packet command is required to enable the SPI pass-through interface. The interface must be enabled before any Write or Read commands may be performed. Note that there is no data phase to this USB transaction,

TABLE 4: USB SETUP COMMAND

Setup Parameter	Value	Description
bmRequestType	0x41	Vendor specific command, Host-to-device data transfer
bRequest	0x60	Register read command: CMD_SPI_ENTER_PASSTHRU
wValue	0x0000	Reserved
wIndex	0x0000	Reserved
wLength	0x00	No data stage

4.2 SPI Write Command

This command is used to write data to or read data from a SPI peripheral connected to the USB hub.

TABLE 5: USB SETUP COMMAND

Setup Parameter	Value	Description
bmRequestType	0x41	Vendor specific command, Host-to-device data transfer
bRequest	0x61	Register read command: CMD_SPI_WRITE
wValue	0XXXXX	The total length of data to be sent to the SPI peripheral (the size of the data following the SETUP packet).
wIndex	0x0000	Reserved
wLength	0xNN	The number of bytes the SPI interface will return for the command sent

The maximum amount of data that can be read from one USB command is 512 Bytes by specifying wValue = 517 and wLength = 5.

The maximum amount of data that can be written to a SPI peripheral is 256 Bytes by specifying wValue = wLength = 260.

4.2.1 SPI WRITE USB TRANSACTION SEQUENCE:

1. SETUP PACKET: To send 'Write Enable' OpCode to SPI ROM (wValue = wLength = 1)
2. DATA: 0x06 (opcode for 'Write Enable').
3. STATUS: An IN-Zero Length Packet is sent from hub.
4. SETUP PACKET: To send data payload
5. DATA: EP0 Data to SPI ROM with 0x02 + 24bit SPI address + Data Stream
6. STATUS: If an IN-Zero Length Packet is sent from hub, transfer was a success. If an IN-STALL packet is sent from hub, there was an error during transfer.

4.2.2 SPI READ USB TRANSACTION SEQUENCE:

1. SETUP PACKET: As defined above.
2. DATA: EP0 OUT Data to SPI ROM with 0x0B + 24Bit SPI Address + 0x00 (dummy byte).
3. STATUS: If an IN-Zero Length Packet is sent from hub, transfer was a success. If an IN-STALL packet is sent from hub, there was an error during transfer, likely due to missing ACK from the SPI slave.
4. Perform Configuration Register Read on hub starting at register 0x4A10 to retrieve read data. See *AN 26.18 Configuration of the USB253x / USB3x13 / USB46x4*

4.3 Disable SPI Pass-Through Interface Command

The following SETUP packet command is required to disable the SPI pass-through interface. Note that there is no data phase to this USB transaction,

TABLE 6: USB SETUP COMMAND

Setup Parameter	Value	Description
bmRequestType	0x41	Vendor specific command, Host-to-device data transfer
bRequest	0x62	Register read command: CMD_SPI_ENTER_PASSTHRU
wValue	0x0000	Reserved
wIndex	0x0000	Reserved
wLength	0x00	No data stage

5.0 EXAMPLES

5.1 Write 512 Bytes to a SPI ROM

1. Enable the SPI Pass-Through Interface

TABLE 7: ENABLE SPI INTERFACE SETUP COMMAND

Setup Parameter	Value
bmRequestType	0x41
bRequest	0x60
wValue	0x0000
wIndex	0x0000
wLength	0x00

2. Send a SPI Write/Read Command to read 512 Bytes of data.

TABLE 8: SPI WRITE SETUP COMMAND

Setup Parameter	Value
bmRequestType	0x41
bRequest	0x61
wValue	0x0205 (517)
wIndex	0x0000
wLength	0x0005

3. EP0 OUT data = 0x0B, 0xXX, 0xYY, 0xZZ, 0x00, 0xXX, 0xYY, 0xZZ.

Note: 0xXX, 0xYY, 0xZZ is the 24 Bit physical SPI address of the SPI peripheral.

4. Read response via USB to Configuration Register Read from register 0x4A10. Further details can be found in *AN 26.18 Configuration of the USB253x / USB3x13 / USB46x4*.
5. Do one of the following:
 - Close the SPI Interface with the Disable SPI Pass-Through Command
 - Wait for the manufacturer specified time before performing another Read/Write command.
 - Send RDSR commands until the BUSY field is cleared before performing another Read/Write command.

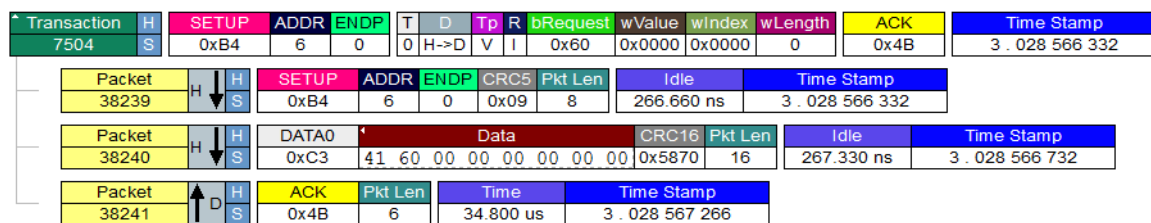
5.2 Enable the SPI Pass-Through Interface

1. **Command Phase (SETUP Transaction):** Send the following SETUP Register Read Command to Endpoint 0 of the Hub Feature Controller to enable the SPI pass-through interface:

TABLE 9: EXAMPLE SPI WRITE SETUP PACKET

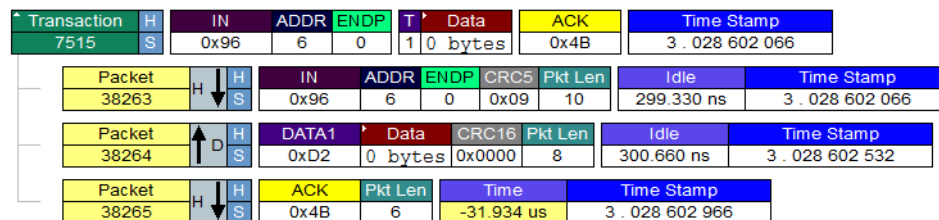
Field	Value	Note
bmRequestType	0x41	
bRequest	0x60	
wValue	0x0000	
wIndex	0x0000	
wLength	0x0000	

FIGURE 1: SETUP TRANSACTION EXAMPLE



2. **Status (IN Transaction):** The host sends an IN packet to the Hub Feature Controller, to which the Hub Feature controller replies with a zero data length packet. The host ACKs to complete the bridging command.

FIGURE 2: IN TRANSACTION EXAMPLE



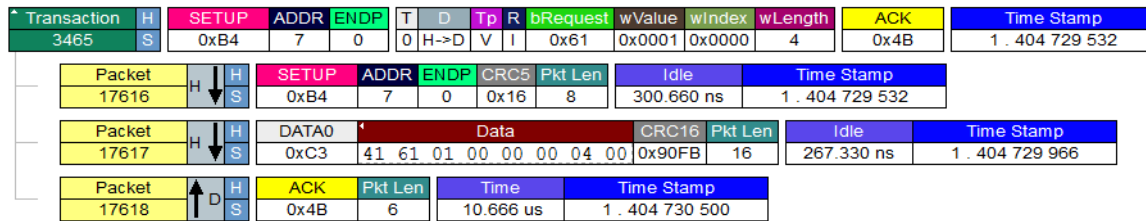
5.3 Read the JEDEC ID from an attached SPI Device

- Command Phase 1 (SETUP Transaction 1):** The JEDEC ID gives manufacturer information and memory information. This example shows how to read the JEDEC ID from an attached SPI device. Send the following SETUP Register Read Command to Endpoint 0 of the Hub Feature Controller send a SPI Write command to the attached SPI device.

TABLE 10: SPI JEDEC ID READ SETUP PACKET EXAMPLE

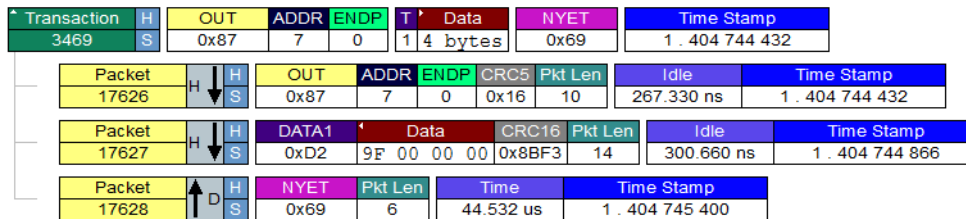
Field	Value	Note
bmRequestType	0x41	
bRequest	0x61	
wValue	0x0001	
wIndex	0x0000	
wLength	0x0004	

FIGURE 3: SPI JEDEC ID READ SETUP TRANSACTION EXAMPLE



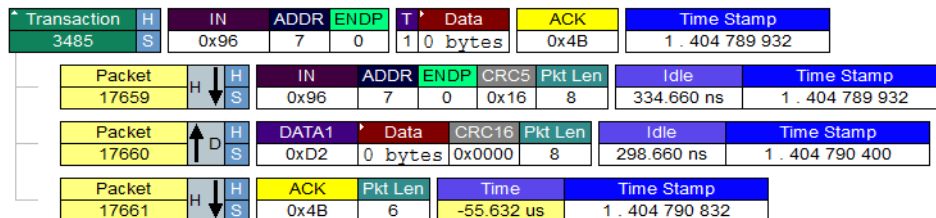
- Data Phase 1 (OUT Transaction 1):** Host sends an OUT packet followed by the data bytes of length wLength. In this example, the 0x9F data is the opcode for reading a JEDEC ID in a SPI device. Hub Feature Controller responds with a NYET after receiving the data.

FIGURE 4: SPI JEDEC ID OUT TRANSACTION EXAMPLE



- Status Phase 1 (IN Transaction 1):** Host sends an IN packet to complete the USB Transfer. Hub Feature Controller responds with a zero length data packet. The host ACKs to complete the bridging command.

FIGURE 5: SPI JEDEC ID IN TRANSACTION EXAMPLE

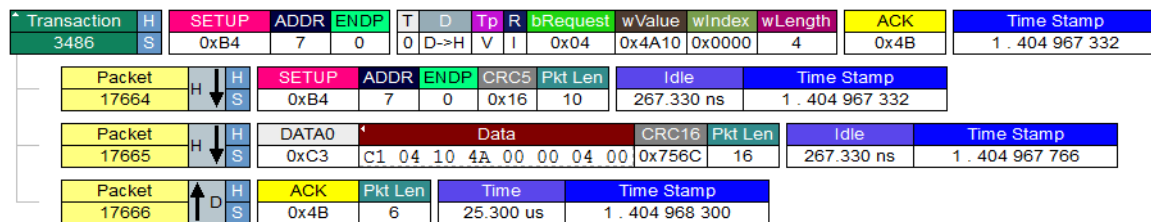


4. **Retrieve the Returned Data (SETUP Transaction 2):** The SPI device will respond to the opcode command and the returned data will be stored in the hub's internal register starting at address 0x4A10. A USB to Register Read command can retrieve the data. This command is setup as:

TABLE 11: SPI JEDEC ID REGISTER READ SETUP PACKET EXAMPLE

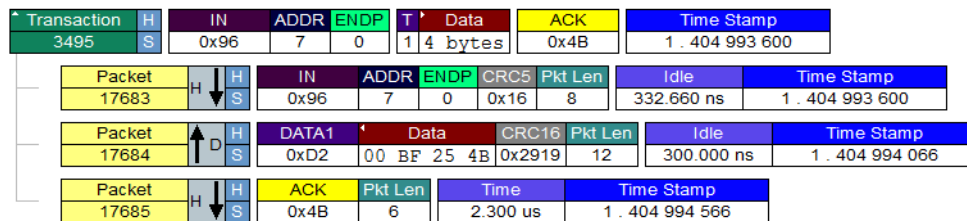
Field	Value	Note
bmRequestType	0xC1	
bRequest	0x04	
wValue	0x4A10	The hub's internal register address
wIndex	0x0000	
wLength	0x0004	A JEDEC ID request will return 4 bytes. The first byte will be a dummy 0x00.

FIGURE 6: SPI JEDEC ID REGISTER READ SETUP TRANSACTION EXAMPLE



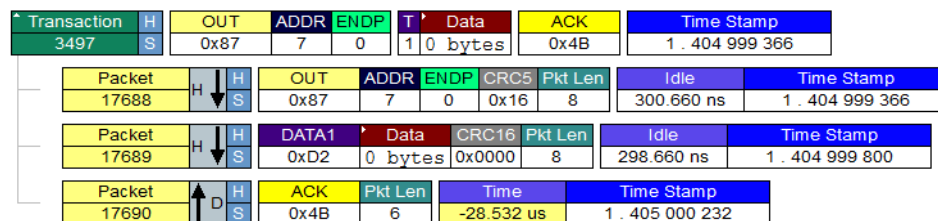
5. **Data Phase 2 (IN Transaction 2):** Host sends an IN packet to retrieve the data from the 0x4A10 register. In this example, the JEDEC ID that is returned is 0xBF, 0x25, 0x4B. The host replies with an ACK after receiving the data.

FIGURE 7: SPI JEDEC ID REGISTER READ IN TRANSACTION EXAMPLE



6. **Status Phase 2 (OUT Transaction 2):** Host sends an OUT packet followed by a zero length data packet. The Hub Feature Controller ACKs to complete the bridging command.

FIGURE 8: SPI JEDEC ID REGISTER READ OUT TRANSACTION EXAMPLE



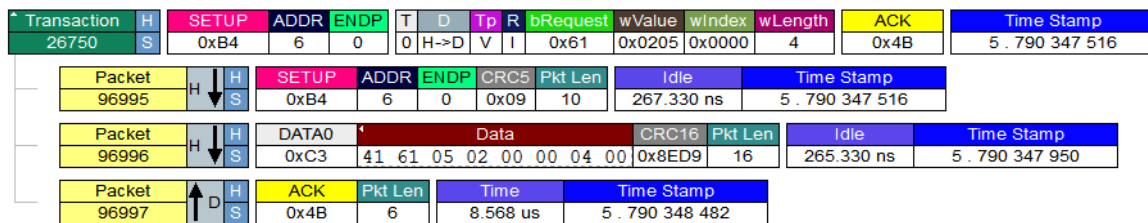
5.4 Read 512 Bytes from an attached SPI Device

1. **Command Phase 1 (SETUP Transaction 1):** This example shows how to perform a block read of 512 bytes (the maximum number of bytes per command) from an attached SPI device. Send the following SETUP Register Read Command to Endpoint 0 of the Hub Feature Controller send a SPI Write command to the attached SPI device

TABLE 12: SPI BLOCK READ COMMAND SETUP PACKET EXAMPLE

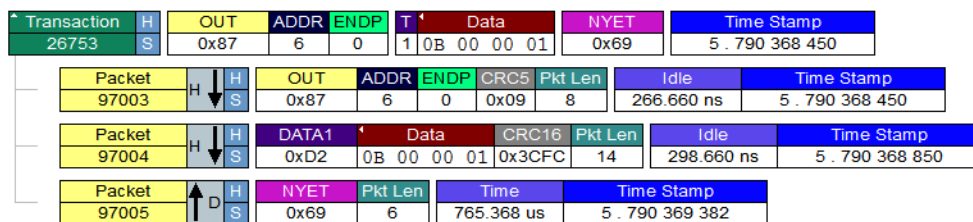
Field	Value	Note
bmRequestType	0x41	
bRequest	0x61	
wValue	0x0205 (517)	The first 5 Bytes of any SPI read must be ignored; Therefore, 5 must be added to the number of Bytes to be read.
wIndex	0x0000	
wLength	0x0004	

FIGURE 9: SPI BLOCK READ COMMAND SETUP TRANSACTION EXAMPLE



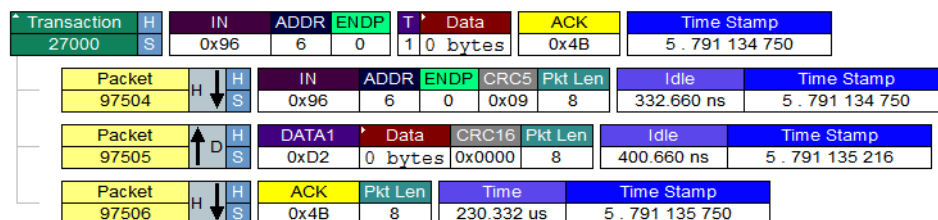
2. **Data Phase 1 (OUT Transaction 1):** Host sends an OUT packet followed by the data bytes of length wLength. In this example, the 0x0B is the opcode for a block read in this specific SPI device, the next 0x00,0x00,0x01 is the register address to begin reading from the SPI device. The Hub Feature Controller responds with a NYET after receiving the data.

FIGURE 10: SPI BLOCK READ COMMAND OUT TRANSACTION EXAMPLE



3. **Status Phase 1 (IN Transaction 1):** Host sends an IN packet to complete the USB Transfer. Hub Feature Controller responds with a zero length data packet. The host ACKs to complete the bridging command.

FIGURE 11: SPI BLOCK READ COMMAND IN TRANSACTION EXAMPLE



4. **Retrieve the Returned Data (SETUP Transaction 2):** The SPI device will respond to the opcode command and the returned data will be stored in the hub's internal register starting at address 0x4A10. For a SPI Block Read, the first 5 bytes must be ignored. A USB to Register Read command can retrieve the data. This command is setup as:

TABLE 13: REGISTER READ SETUP PACKET EXAMPLE

Field	Value	Note
bmRequestType	0xC1	
bRequest	0x04	
wValue	0x4A10	The hub's internal register address
wIndex	0x0000	
wLength	0x0205	517 Bytes will be read (512 + 5 dummy bytes)

FIGURE 12: REGISTER READ SETUP TRANSACTION EXAMPLE

Transaction	H	SETUP	ADDR	ENDP	T	D	TP	R	bRequest	wValue	wIndex	wLength	ACK	Time Stamp
27001	S	0xB4	6	0	0	D→H	V	I	0x04	0x4A10	0x0000	517	0x4B	5 . 791 366 082

Packet	H	SETUP	ADDR	ENDP	CRC5	Pkt Len	Idle	Time Stamp
97509	S	0xB4	6	0	0x09	10	267.330 ns	5 . 791 366 082

Packet	H	DATA0	Data						CRC16	Pkt Len	Idle	Time Stamp
97510	S	0xC3	C1 04 10 4A 00 00 05 02						0x74E6	16	267.330 ns	5 . 791 366 516

Packet	D	ACK	Pkt Len	Time	Time Stamp
97511	S	0x4B	6	91.100 us	5 . 791 367 050

5. **Data Phase 2 (IN Data Payload Transaction):** Hub sends a series of IN packets (64 Bytes per packet) until all 517 bytes are read. The first 5 bytes should always be ignored.

FIGURE 13: REGISTER READ IN TRANSACTION EXAMPLE

Transaction 27028	IN	ADDR	ENDP	T	Data	ACK	Time	Time Stamp
	0x96	6	0	1	0: 00 00 00 00 01 00 02 48 BE 75 C8 10 22 FF 02 4F C5 90 09 54 E4 F0 30 25 04 E0 44 02 F0 22 02 32: 6D 39 02 46 A0 FF FF 02 67 38 FF FF FF 02 78 B0 90 08 0A E0 44 04 F0 78 BD E6 90 24 00 F0	0x4B	78.466 us	5 . 791 458 150
Transaction 27051	IN	ADDR	ENDP	T	Data	ACK	Time	Time Stamp
	0x96	6	0	0	0: 90 08 2F B0 44 30 F0 90 08 2E B0 44 02 F0 22 02 20 78 8B 2D BA 2E 89 2F 8C 30 8D 31 C2 2C 75 34 32: 40 D3 E5 33 95 31 B5 32 95 30 50 08 85 32 30 85 33 31 80 12 E5 34 FD 7C 00 AE 30 AF 31 12 11 70	0x4B	77.300 us	5 . 791 536 616
Transaction 27076	IN	ADDR	ENDP	T	Data	ACK	Time	Time Stamp
	0x96	6	0	1	0: ED 4C 70 02 D2 2C E5 31 45 30 70 03 30 2C 73 90 33 40 E0 30 E0 07 90 33 43 E0 30 E0 F2 90 33 43 32: 74 01 F0 C3 E5 34 95 31 E4 95 30 AF 31 50 02 AF 34 8F 35 20 2B 28 E4 FF EF C3 95 35 50 20 AB 2D	0x4B	77.400 us	5 . 791 613 916
Transaction 27103	IN	ADDR	ENDP	T	Data	ACK	Time	Time Stamp
	0x96	6	0	0	0: 05 2F E5 2F AA 2E 70 02 05 2E 14 F9 12 10 F6 FE E4 2F F5 82 E4 34 33 F5 83 EE F0 0F 80 DA 90 33 32: 41 E5 35 F0 90 33 40 E0 44 01 F0 E5 31 45 30 70 02 C2 2C C3 E5 31 95 35 F5 31 E5 30 94 00 F5 30	0x4B	76.666 us	5 . 791 691 316
Transaction 27128	IN	ADDR	ENDP	T	Data	ACK	Time	Time Stamp
	0x96	6	0	1	0: 80 84 22 FF 75 81 BD 12 35 00 90 24 00 E0 30 E7 51 90 44 00 74 90 F0 A3 74 24 F0 A3 74 00 F0 A3 32: 74 E0 F0 A3 74 54 F0 A3 74 F7 F0 A3 74 F0 A3 74 90 F0 A3 74 24 F0 A3 74 03 F0 A3 74 74 F0 A3	0x4B	76.400 us	5 . 791 768 182
Transaction 27153	IN	ADDR	ENDP	T	Data	ACK	Time	Time Stamp
	0x96	6	0	0	0: 74 0B F0 A3 74 F0 F0 A3 74 22 F0 90 08 42 74 10 F0 74 01 A3 F0 12 80 00 90 08 42 74 88 F0 A3 74 32: 81 F0 90 24 00 E0 44 02 F0 75 F9 98 00 00 12 6D 74 12 69 87 02 7C 8F 02 7C 8F 02 2C 78 82 E6 78	0x4B	79.184 us	5 . 791 844 582
Transaction 27180	IN	ADDR	ENDP	T	Data	ACK	Time	Time Stamp
	0x96	6	0	1	0: B8 F6 E6 12 13 62 02 9B 00 03 82 01 03 74 02 02 9B 03 02 C3 04 03 5D 05 02 0C 06 02 17 07 02 27 32: 08 01 F8 09 02 A9 10 04 1A 20 04 49 21 04 78 22 04 BC 23 05 0C 24 05 AE 25 05 62 26 05 C1 28 07	0x4B	77.300 us	5 . 791 923 766
Transaction 27205	IN	ADDR	ENDP	T	Data	ACK	Time	Time Stamp
	0x96	6	0	0	0: 19 2A 07 19 2B 07 6D 2C 02 A9 30 07 8D 31 07 91 32 02 A9 40 02 A9 41 02 CD 42 02 A9 50 02 75 60 32: 02 7F 61 02 7A 62 02 A9 63 02 51 70 02 A9 71 03 00 72 02 56 73 02 5B 74 07 95 80 00 00 07 84 12	0x4B	12.666 us	5 . 792 001 066
Transaction 27209	IN	ADDR	ENDP	T	Data	ACK	Time	Time Stamp
	0x96	6	0	1	73 52 79 B0 7A	0x4B	3.434 us	5 . 792 013 732

6. **Status Phase 2 (OUT Transaction 2):** Host sends an OUT packet followed by a zero length data packet. The Hub Feature Controller ACKs to complete the bridging command.

FIGURE 14: REGISTER READ OUT TRANSACTION EXAMPLE

Transaction	H	OUT	ADDR	ENDP	T	Data	ACK	Time Stamp	
27211	S	0x87	6	0	1	0 bytes	0x4B	5 . 792 019 800	
Packet	H	H	OUT	ADDR	ENDP	CRC5	Pkt Len	Idle	Time Stamp
97942	S	↓	0x87	6	0	0x09	8	266.660 ns	5 . 792 019 800
Packet	H	H	DATA1	Data	CRC16	Pkt Len	Idle	Time Stamp	
97943	S	↓	0xD2	0 bytes	0x0000	8	332.660 ns	5 . 792 020 200	
Packet	H	H	ACK	Pkt Len	Time	Time Stamp			
97944	S	↑	0x4B	6	2.165 sec	5 . 792 020 666			

7. After completing the SPI Read, do one of the following:
- Close the SPI Interface with the Disable SPI Pass-Through command.
 - Wait for the manufacturer specified time before performing another Read/Write command.
 - Send RDSR commands until the BUSY field is cleared before performing another Read/Write command.

5.5 Write 256 Bytes to an attached SPI Device

1. **Command Phase 1 (SETUP Transaction 1):** This example shows how to perform a block write of 256 bytes to an attached SPI device. Send the following SETUP Register Read Command to Endpoint 0 of the Hub Feature Controller to enable the SPI write feature.

TABLE 14: SPI WRITE ENABLE SETUP PACKET EXAMPLE

Field	Value	Note
bmRequestType	0x41	
bRequest	0x61	
wValue	0x0001	
wIndex	0x0000	
wLength	0x0001	

FIGURE 15: SPI WRITE ENABLE SETUP TRANSACTION EXAMPLE

Transaction	H	SETUP	ADDR	ENDP	T	D	Tp	R	bRequest	wValue	wIndex	wLength	ACK	Time Stamp
98000	S	0xB4	6	0	0	H→D	V	I	0x61	0x0001	0x0000	1	0x4B	19 . 101 512 616

Packet	H	SETUP	ADDR	ENDP	CRC5	Pkt Len	Idle	Time Stamp
340086	S	0xB4	6	0	0x09	10	267.330 ns	19 . 101 512 616

Packet	H	DATA0	Data					CRC16	Pkt Len	Idle	Time Stamp			
340087	S	0xC3	41	61	01	00	00	00	01	00	0x50F1	16	265.330 ns	19 . 101 513 050

Packet	D	ACK	Pkt Len	Time	Time Stamp
340088	S	0x4B	6	14.200 us	19 . 101 513 582

2. **Data Phase 1 (OUT Transaction 1):** Host sends an OUT packet followed by a single byte data payload of 0x06. 0x06 is the SPI write enable command. The Hub Feature Controller responds with a NYET after receiving the data.

FIGURE 16: SPI WRITE ENABLE TRANSACTION EXAMPLE

Transaction	H	OUT	ADDR	ENDP	T	Data	NYET	Time Stamp	
98006	S	0x87	6	0	1	06	0x69	19 . 101 531 182	
Packet	H	OUT	ADDR	ENDP	CRC5	Pkt Len	Idle		Time Stamp
340100	S	0x87	6	0	0x09	10	267.330 ns		19 . 101 531 182
Packet	H	DATA1	Data	CRC16	Pkt Len	Idle		Time Stamp	
340101	S	0xD2	06	0x03BD	10	299.330 ns		19 . 101 531 616	
Packet	D	NYET	Pkt Len	Time		Time Stamp			
340102	S	0x69	6	38.100 us		19 . 101 532 082			

3. **Status Phase 1 (IN Transaction 1):** Host sends an IN packet to complete the USB Transfer. Hub Feature Controller responds with a zero length data packet. The host ACKs to complete the bridging command.

FIGURE 17: SPI WRITE DATA IN TRANSACTION EXAMPLE

Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time Stamp
98019	S	0x96	6	0	1	0 bytes	0x4B	19 . 101 570 182
Packet	H	IN	ADDR	ENDP	CRC5	Pkt Len	Idle	Time Stamp
340127	S	0x96	6	0	0x09	8	334.660 ns	19 . 101 570 182
Packet	H	DATA1	Data	CRC16	Pkt Len	Idle	Time Stamp	
340128	S	0xD2	0 bytes	0x0000	8	398.660 ns	19 . 101 570 650	
Packet	H	ACK	Pkt Len	Time	Time Stamp			
340129	S	0x4B	8	-53.400 us	19 . 101 571 182			

4. **Send the SPI Write Data Payload (SETUP Transaction 2):** The SPI device is now ready to receive the data payload. For a SPI Block Write of 256 bytes, the SETUP command is:

TABLE 15: SPI WRITE DATA SETUP PACKET EXAMPLE

Field	Value	Note
bmRequestType	0x41	
bRequest	0x61	
wValue	0x0104 (260)	The 256 byte data payload + 4 extra command bytes
wIndex	0x0000	
wLength	0x0100 (256)	The 256 byte data payload

FIGURE 18: SPI WRITE DATA TRANSACTION EXAMPLE

Transaction	H	SETUP	ADDR	ENDP	T	D	TP	R	bRequest	wValue	wIndex	wLength	ACK	Time Stamp
98020	S	0xB4	6	0	0	H->D	V	I	0x61	0x0104	0x0000	256	0x4B	19 . 101 803 650
Packet 340132	H	SETUP	ADDR	ENDP	CRC5	Pkt Len	Idle	Time Stamp						
	S	0xB4	6	0	0x09	8	266.660 ns	19 . 101 803 650						
Packet 340133	H	DATA0	Data	CRC16	Pkt Len	Idle	Time Stamp							
	S	0xC3	41 61 04 01 00 00 00 01	0xEF52	18	266.000 ns	19 . 101 804 050							
Packet 340134	H	ACK	Pkt Len	Time	Time Stamp									
	S	0x4B	6	11.034 us	19 . 101 804 616									

5. **Data Phase 2 (OUT Data Payload Transaction):** Host sends a series of OUT packets (64 Bytes per packet) until all 256 + 4 command bytes are sent. The first 4 bytes must be 0x02, 0xXX, 0xYY, 0xZZ where 0xXX, 0xYY, 0xZZ is the 24 bit physical address of the SPI Flash. In this example, the SPI address is 0x111111.

FIGURE 19: SPI WRITE DATA OUT TRANSACTIONS EXAMPLE

Transaction	H	OUT	ADDR	ENDP	T	Data
98025	S	0x87	6	0	1	0: 02 11 11 11 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11 12 13 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F 20 21 22 23 24 25 26 27 28 29 2A 2B 2C 2D 2E 2F 30 31 32: 1C 1D 1E 1F 20 21 22 23 24 25 26 27 28 29 2A 2B 2C 2D 2E 2F 30 31 32
Transaction	H	OUT	ADDR	ENDP	T	Data
98050	S	0x87	6	0	0	0: 3C 3D 3E 3F 40 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 4E 4F 50 51 52 53 54 55 56 57 58 59 5A 5B 5C 5D 5E 5F 60 61 62 63 64 65 66 67 68 69 6A 6B 6C 6D 6E 6F 70 71 72 73 74 75 76 77 78 79 7A 7B 7C 7D 7E 7F 80 81 82 83 84 85 86 87 88 89 8A 8B 8C 8D 8E 8F 90 91 92 93 94 95 96 97 98 99 9A 9B 9C 9D 9E 9F A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 AA AB AC AD AE AF B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 BA BB BC BD BE BF C0 C1 C2 C3 C4 C5 C6 C7 C8 C9 CA CB CC CD CE CF D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 DA DB DC DD DE DF E0 E1 E2 E3 E4 E5 E6 E7 E8 E9 EA EB EC ED EE EF F0 F1 F2 F3 F4 F5 F6 F7 F8 F9 FA FB FC FD FE FF
Transaction	H	OUT	ADDR	ENDP	T	Data
98072	S	0x87	6	0	1	0: 6C 6D 6E 6F 70 71 72 73 74 75 76 77 78 79 7A 7B 7C 7D 7E 7F 80 81 82 83 84 85 86 87 88 89 8A 8B 8C 8D 8E 8F 90 91 92 93 94 95 96 97 98 99 9A 9B 9C 9D 9E 9F A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 AA AB AC AD AE AF B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 BA BB BC BD BE BF C0 C1 C2 C3 C4 C5 C6 C7 C8 C9 CA CB CC CD CE CF D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 DA DB DC DD DE DF E0 E1 E2 E3 E4 E5 E6 E7 E8 E9 EA EB EC ED EE EF F0 F1 F2 F3 F4 F5 F6 F7 F8 F9 FA FB FC FD FE FF
Transaction	H	OUT	ADDR	ENDP	T	Data
98093	S	0x87	6	0	0	0: AC AD AE AF B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 BA BB BC BD BE BF C0 C1 C2 C3 C4 C5 C6 C7 C8 C9 CA CB CC CD CE CF D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 DA DB DC DD DE DF E0 E1 E2 E3 E4 E5 E6 E7 E8 E9 EA EB EC ED EE EF F0 F1 F2 F3 F4 F5 F6 F7 F8 F9 FA FB FC FD FE FF

6. **Status Phase 2 (IN Transaction 2):** Host sends an IN packet and the hub responds with a zero length data packet. The Host ACKs to complete the bridging command.

FIGURE 20: SPI WRITE DATA IN TRANSACTION EXAMPLE

Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time Stamp
98343	S	0x96	6	0	1	0 bytes	0x4B	19 . 102 743 066
Packet	H	IN	ADDR	ENDP	CRC5	Pkt Len	Idle	Time Stamp
340790	S	0x96	6	0	0x09	8	300.660 ns	19 . 102 743 066
Packet	D	DATA1	Data	CRC16	Pkt Len	Idle	Time Stamp	
340791	S	0xD2	0 bytes	0x0000	8	432.660 ns	19 . 102 743 500	
Packet	H	ACK	Pkt Len	Time	Time Stamp			
340792	S	0x4B	8	-935.950 us	19 . 102 744 066			

7. After completing the SPI Write, do one of the following:
- Close the SPI Interface with the Disable SPI Pass-Through command.
 - Wait for the manufacturer specified time before performing another Read/Write command.
 - Send RDSR commands until the BUSY field is cleared before performing another Read/Write command.

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00001971B (04-22-16)	Section 1.2.2, "Selecting SPI Frequency"	Corrected pin name typo to "SPI_SPD_SEL"
	Table 2, "USB3613 and USB3813 SPI Interface Pins", Table 3, "USB4604 and USB4624 SPI Interface Pins", Table 9, "Example SPI Write Setup Packet"	Corrected table title typo: "I2C" changed to "SPI"
	Section 4.1, "Enable SPI Pass-Through Interface Command"	Corrected typo in first sentence: "follow" changed to "following"
	Section 4.2.1, "SPI Write USB Transaction Sequence:"	Corrected typo in step 2: Added end quotation mark to "Write Enable"
	Section 4.3, "Disable SPI Pass-Through Interface Command"	Corrected typos in first sentence: "follow" changed to "following", "enable" changed to "disable"
	Figure 4, Figure 10	Changed title "IN" to "OUT"
	Figure 5, Figure 11, Figure 17	Changed title "OUT" to "IN"
DS00001971A (06-17-15)	All	Initial release.

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