PolarFire FPGA 1G Ethernet Loopback Using IOD CDR

AN4623

Introduction (Ask a Question)

PolarFire® FPGAs support 1G (1000BASE-T) Ethernet solutions for various networking applications. In PolarFire devices, 10/100/1000 Mbps (1G) Ethernet is implemented using the CoreTSE Media Access Control (MAC) soft IP core. The CoreTSE IP implements a Serial Gigabit Media-Independent Interface (SGMII) with an Ethernet PHY. This Ethernet interface can be implemented in the FPGA by using either a transceiver or a GPIO with Clock and Data Recovery (CDR) capability. Both these features are provided by the PF_XCVR and the PF_IOD_CDR IP cores.

GPIOs in PolarFire devices operate at speeds of up to 1.066 Gbps for single-ended standards and 1.25 Gbps for differential standards. Each I/O has an I/O digital (IOD) logic block that supports gearing up of the output data rate and gearing down of the input data rate. The IOD block with CDR circuitry (PF_IOD_CDR IP) deserializes high-speed Ethernet input data and transfers it to the FPGA fabric at lower speeds. It also serializes the lower-speed Ethernet data from the FPGA fabric and transfers to the high-speed Ethernet PHY.

Note: The protocol standard uses “Master” and “Slave.” The equivalent Microchip terminology used in this document is **Initiator** and **Target**, respectively.

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1. Design Description (Ask a Question)

This document describes how to run the 1G Ethernet loopback demo design, which is a reference design created to demonstrate 1G Ethernet loopback using GPIO on a PolarFire Evaluation Board. The demo design is built using the PF_IOD_CDR_CCC, the PF_IOD_CDR, the CoreTSE, and the Mi-V soft processor IP cores. The reference design is for a single SGMII lane (single RJ45 cable). For information about how to build a multi-lane (multiple links) design, see 6. Appendix 3: Multi-Lane 1G IOD CDR Design.

You can program the demo design using either of the following options:

- Using the pre-generated `.job` file: To program the device using the `.job` file provided along with the demo design files, see 4. Appendix 1: Programming the Device Using FlashPro Express.
- Using Libero SoC: To program the device using Libero SoC, see 2. Libero Design Flow.

A license is required to use the CoreTSE IP core. To request a license, contact FPGA_marketing@microchip.com.

1.1 Design Requirements (Ask a Question)

The following table lists the hardware and software requirements for running the demo design.

Table 1-1. Design Requirements

Requirement	Version
Hardware	
PolarFire® Evaluation Kit (POLARFIRE-EVAL-KIT) – PolarFire Evaluation Board – 12V/5A AC power adapter and cord – USB 2.0A to mini-B cable for UART and programming	Rev D
RJ45 cable to connect the board with the host PC	—
Host PC	Windows® 10
Software	
Cat Karat (Ethernet packet generator)	To install the appropriate version, refer PacketBuilder website. Cat Karat version 1.51.200 is used in this demo.
FlashPro® Express	See the `readme.txt` file provided in the design files for the software versions used with this reference design.
Libero® SoC Design Suite	

Important: Libero SmartDesign and configuration screen shots shown in this application note are for illustration purpose only. Open the Libero design to see the latest updates.

1.2 Prerequisites (Ask a Question)

The following is a list of prerequisites for the design demo:

- Download the demo design files from this link: www.microchip.com/en-us/application-notes/AN4623
- Download and install Libero SoC (as indicated in the website for this design) on the host PC from the following location:
  Libero SoC Documentation
- If you already purchased a Gold license and received a Software ID from Microchip, generate your Gold License using the following link: www.microchipdirect.com/fpga-software-products?_ga=2.129591884.1509868822.1656915164-94450803.1634639592
- Download Cat Karat.

Important:

- The latest versions of ModelSim and Synplify Pro are included in the Libero SoC PolarFire installation package. Make sure you have a Libero Gold license for design evaluation on MPF300 device. A one year Gold software License is included with the Evaluation kit.
- The Cat Karat version 1.51.200 is used in this application note.

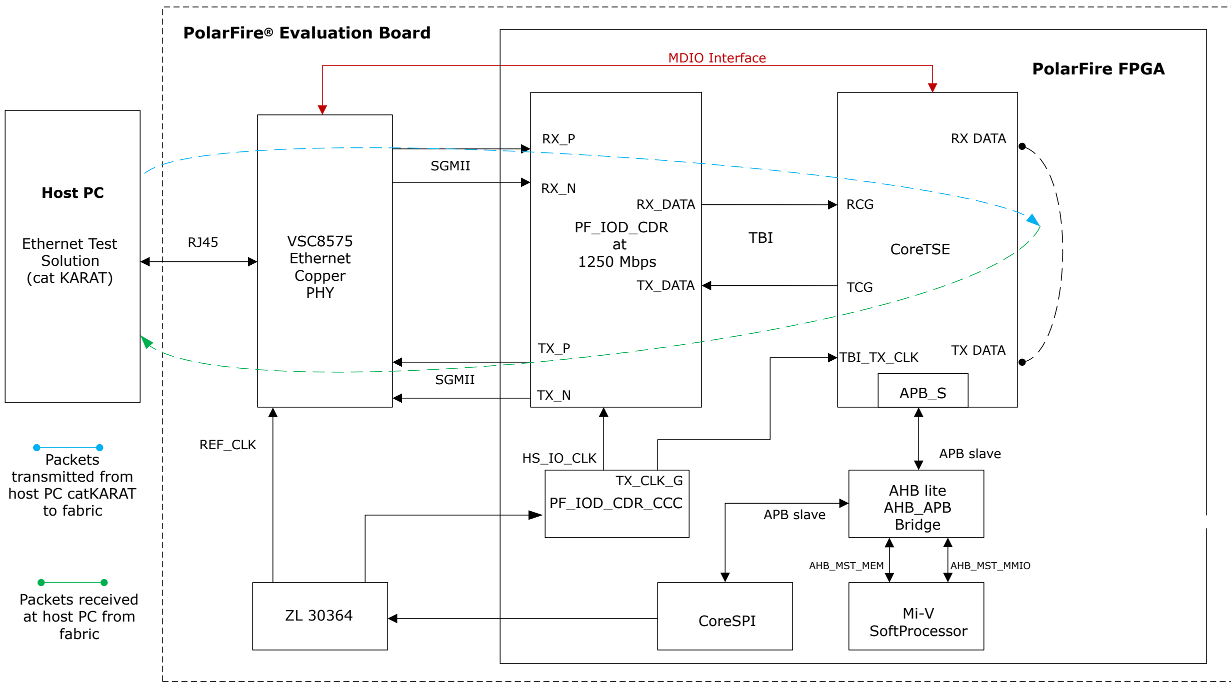
1.3 Demo Design (Ask a Question)

The following is the data flow for the 1G Ethernet loopback demo design:

1. PF_CCC_0 provides the clock to the Mi-V processor and other APB peripherals.
2. PF_IOD_CDR_CCC_C0 generates:
   - The fabric transmit clock ((TX_CLK_G)) for the CoreTSE block
   - The high-speed bank clocks, and drives the high-speed clocks (HS_IO_CLKs) of the PF_IOD_CDR_C0 block for clock recovery
3. PF_IOD_CDR_CCC_C0 also generates Delay codes for the PVT compensation.
4. Mi-V performs the following functions:
   - Executes the application from Tightly Coupled Memory (TCM)
   - Configures the ZL30364 clock generation hardware through the CoreSPI IP to generate reference clocks for the VSC PHY and the IOD CDR fabric module
   - Configures the Management registers of CoreTSE and VSC PHY
   - Sends a request to the CoreTSE IP to negotiate with the on-board VSC8575 PHY
5. CoreTSE IP implements 1G Ethernet MAC and is configured in Ten Bit Interface mode (TBI) to interface with the PF_IOD_CDR_C0. The CoreTSE IP has an inbuilt MDIO interface to exchange control and status information with the VSC PHY
6. PF_IOD_CDR IP does the following:
   - Interfaces with the on-board VSC8575 PHY and forms the SGMII link
   - Recovers the data and clock from the incoming RX_P and RX_N ports
   - Sends the recovered clock (RX_CLK_R) to the CoreTSE block
   - Deserializes the recovered data and sends 10-bit parallel data to CoreTSE
   - Receives Ethernet data through the RX_P and the RX_N input pads, gears down the receive data rate, and deserializes the data
   - Sends the deserialized data from PF_IOD_CDR_C0:RX_DATA [9:0] to CoreTSE IP: RCG [9:0]
   - Loops back the received data at the CoreTSE IP, and sends CoreTSE IP:TCG[9:0] to PF_IOD_CDR_C0:TX_DATA [9:0]
   - PF_IOD_CDR_C0 serializes the data, gears up the transmit data rate, and transmits the data to the on-board VSC PHY through the TX_P and TX_N output pads

The following figure shows the hardware implementation of the demo design.

Figure 1-1. Block Diagram



1.3.1 About PF_IOD_CDR (Ask a Question)

The PF_IOD_CDR IP core provides an asynchronous receive and transmit interface that supports up to 1.6 Gbps speed for serial data transfers. It supports the SGMII interface. PF_IOD_CDR uses the DDRX5 IO Gearing mode for the SGMII interface with a 10:1 digital ratio to provide 10-bit data width for both transmit and receive. The clock recovery circuit, which is part of this PF_IOD_CDR, keeps the receive clock centered in the data eye.

The PF_IOD_CDR interface is compatible with the CoreTSE, the CoreTSE_AHB, and the CoreSGMII IP cores configured in TBI mode. In this demo, the CoreTSE (Non-AMBA) MAC is used in the TBI mode to transmit and receive the Ethernet packets.

1.3.1.1 Receive interface (Ask a Question)

The PF_IOD_CDR IP includes the clock recovery block, which generates the recovered clock for sampling the incoming data stream. This IP uses the four clocks of phases 0, 90,180, and 270 degrees for the clock recovery. The recovered clock (RX_CLK_R) is used by the fabric for sampling the Rx data from PF_IOD_CDR IP. The CoreTSE logic also uses this clock.

For more information about PF_IOD_CDR and its blocks, see PolarFire FPGA and PolarFire SoC FPGA User I/O User Guide.

1.3.1.2 Transmit Interface (Ask a Question)

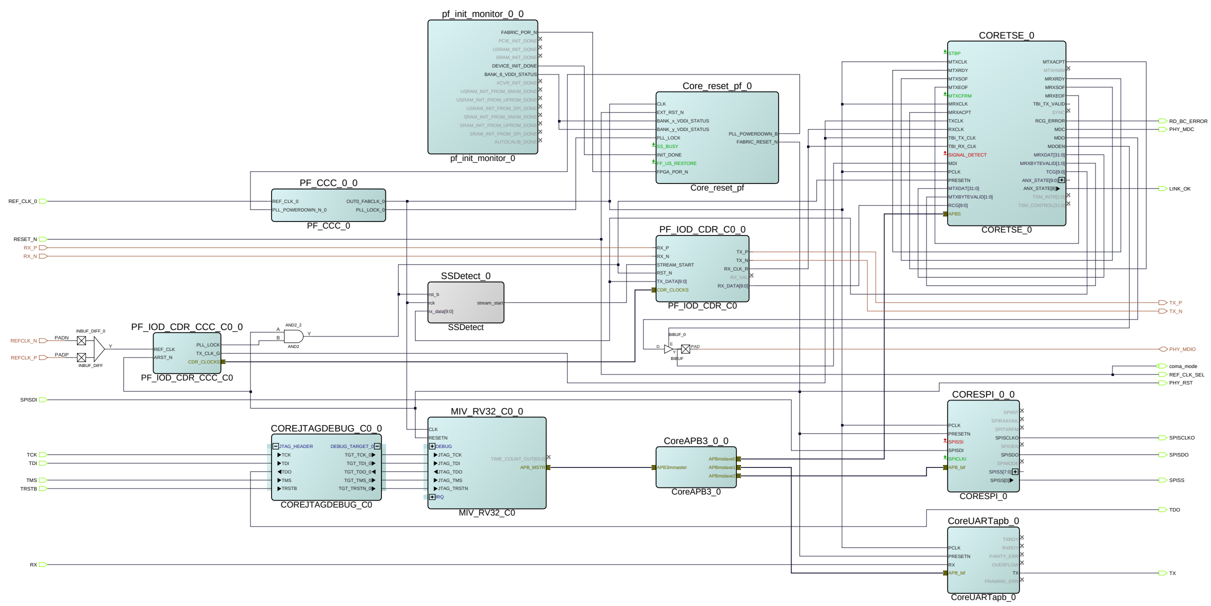
The PF_IOD_CDR transmit interface receives the parallel data (TX_DATA [9:0]), converts it into a serial data stream using the IOD interface, and then transmits it through the I/O ports of TX_P and TX_N. The 625 MHz clock generated by PF_IOD_CDR_CCC is used by the PF_IOD_CDR transmit interface to transmit the data serially on the TX_P/TX_N ports.

For more information about PF_IOD_CDR, see PolarFire FPGA and PolarFire SoC FPGA User I/O User Guide.

1.3.2 Design Implementation (Ask a Question)

The following figure shows the top-level Libero implementation of the demo design.

Figure 1-2. Top-Level Libero® Implementation



The following table lists the important I/O signals of the design.

Table 1-2. I/O Signals

Signal	Direction	Description
RX_P, RX_N	Input	IOD CDR receive signals connected to the VSC PHY transmit data signals
TX_P, TX_N	Output	IOD CDR transmit signals connected to the VSC PHY receive data signals
REFCLK_N, REFCLK_P	Input	Receives 125 MHz input clock from the on-board ZL30364 and feeds to NWC_PLL_0
RESET_N	Input	Active low Mi-V reset Asserted by pressing the on-board K22 push-button.
REF_CLK_0	Input	Receives 50 MHz input clock from the on-board 50 MHz oscillator and feeds to PF_CCC_0
TCK, TDI, TMS, TRSTB	Input	JTAG signals interface to the soft processor for debugging
LINK_OK	Output	Link status indicator Provides the link up or down status with the on-board PHY. This signal is mapped to on-board LED7. The LED ON state indicates that the link is up.
PHY_RST	Output	Active high reset signal to the on-board VSC8575 PHY
PHY_MDC	Output	Management Data IO clock is fed to the on-board VSC8575 PHY
PHY_MDIO	Output	Management Data IO Interface for accessing the on-board VSC8575 PHY registers
coma_mode	Output	Signal is held low to keep the VSC PHY fully active when it is out of reset
REF_CLK_SEL	Output	Reference clock speed pin of the VSC PHY. Held high for selecting the 125 MHz reference clock speed.
RD_BC_ERROR	Output	CoreTSE receive error signal This LED signal indicates the receive code group error. This signal is synchronous to RX_CLK_R, and it is mapped to LED4 on the board. When the LED is in ON state, there is an error in the received code group. When the LED is in OFF state, there is no error.
SPISCLKO, SPISS, SPISDO, SPISDI	Output	Serial Peripheral Interface (SPI) controller signals to interface with the ZL30364 clock generation hardware

...........continued		
Signal	**Direction**	**Description**
TDO	Output	JTAG test data output Serial data output from tap.

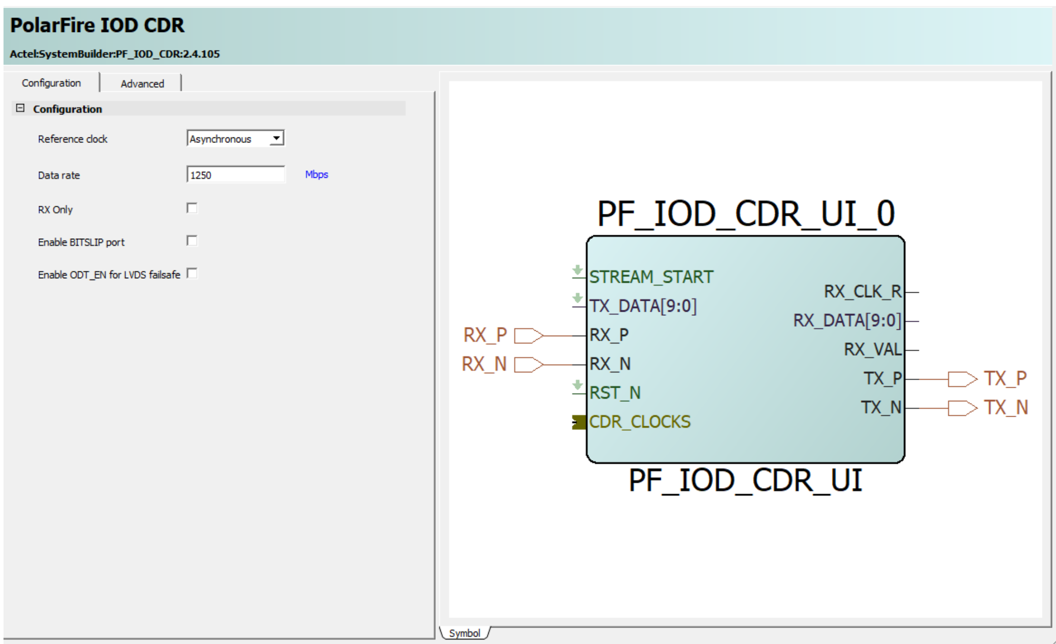
1.3.3 IP Configuration (Ask a Question)

This section describes the IP blocks and user-defined blocks instantiated in the demo design.

1.3.3.1 PF_IOD_CDR_C0_0 (Ask a Question)

The PF_IOD_CDR_C0_0 (PF_IOD_CDR) block is configured for 1250 Mbps. The data rate is set to 1250 Mbps because the SGMII interface operates at this speed. The **Enable BITSLIP port** check box is not selected because the CoreTSE IP has a built-in word alignment logic. The following figure shows the configuration of the PF_IOD_CDR_C0 block.

Figure 1-3. PF_IOD_CDR Configurator

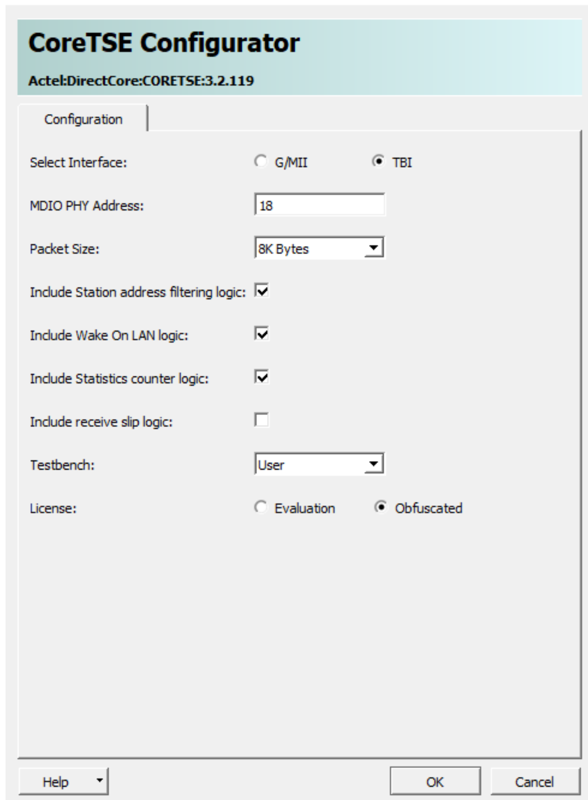


The **Advanced** tab includes the **Jump step size** option that specifies the precision of the clock adjustment during clock recovery. The supported step sizes are: 2 or 3; this demo uses a step size of 3.

1.3.3.2 CORETSE_0 (Ask a Question)

The CORETSE_0 (CoreTSE) block is used to implement the Ethernet MAC. This block is configured in the Ten-bit Interface (TBI) mode to interface with the VSC PHY using the SGMII interface, as shown in the following figure. The **MDIO PHY Address** value is used by the Mi-V soft processor to read and write to the management registers of the CoreTSE IP. The **Include receive slip logic** check box is not selected because the CoreTSE IP has a built-in word alignment logic in TBI mode.

Figure 1-4. CORETSE_0 Configurator



1.3.3.3 PF_INIT_MONITOR_0 (Ask a Question)

The pf_init_monitor_0 (PF_INIT_MONITOR) block is used to issue a reset signal to the user logic (FABRIC_RESET_N). To ensure a glitch-free reset, the DEVICE_INIT_DONE signal is connected to the CORERESET_PF IP with a lock signal from PF_CCC macro.

This IP retains the default configuration.

1.3.3.4 Core_reset_pf_0 (Ask a Question)

The Core_reset_pf_0 (CORERESET_PF) block handles the sequencing of reset signals in the PolarFire device. The CORERESET_PF block synchronizes the reset of all the blocks to which it is connected when the PolarFire device is powered up.

1.3.3.5 core_jtag_debug_0 (Ask a Question)

The CoreJTAGDebug IP is used to debug the Mi-V soft processor. This IP retains the default configuration.

1.3.3.6 Mi-V Soft Processor (Ask a Question)

The Mi-V soft processor supports RISC-V processor-based designs. It configures the ZL30364 clock generation hardware through the CoreSPI IP and the VSC PHY through the CoreTSE MDIO interface. It also configures the CoreTSE registers using the APB interface.

The following figures show the Mi-V soft processor configuration where the **Reset Vector Address** is set to 0x8000_0000. This is because in the Mi-V processor memory map, the memory range used for the APB interface is 0x6000_0000 to 0x6FFF_FFFF, and the memory range used for TCM is 0x8000_0000 to 0x8000_FFFF.

Figure 1-5. Mi-V Configurator—Configuration Tab

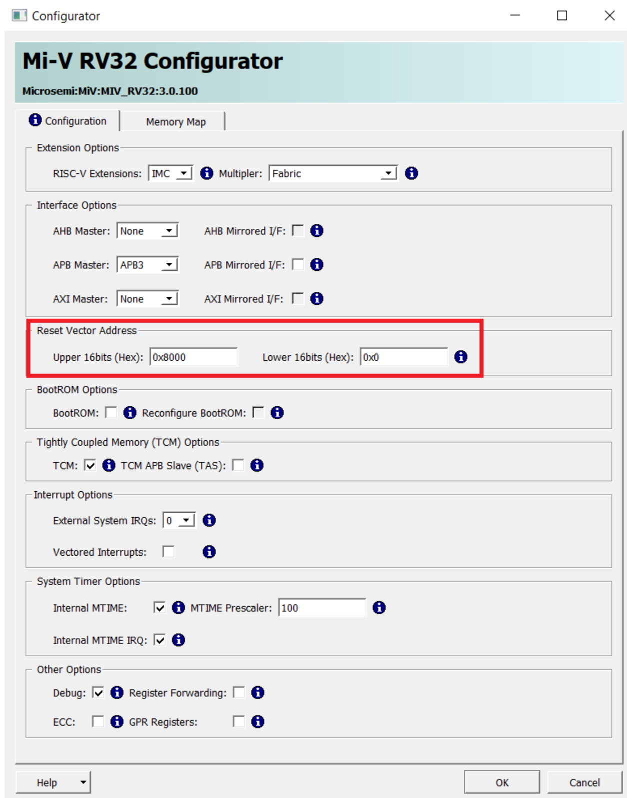
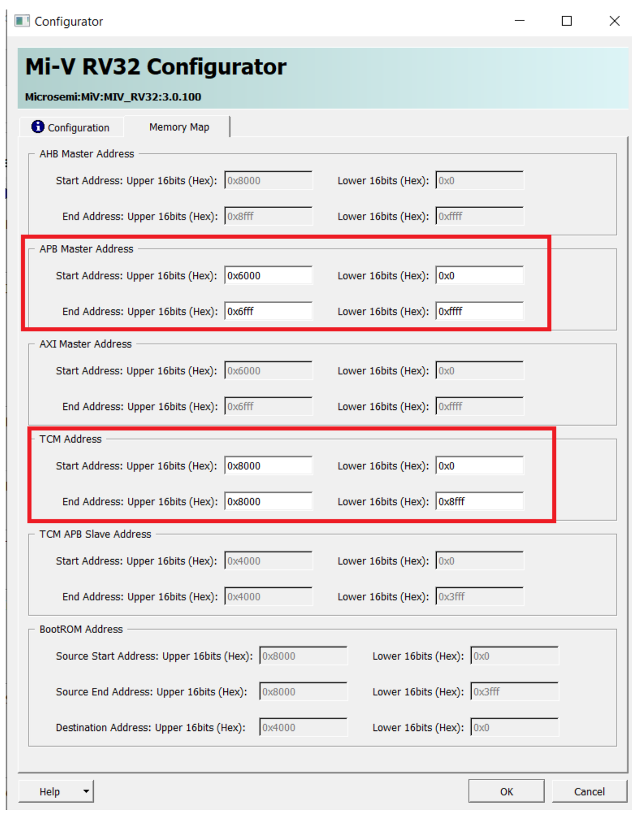


Figure 1-6. Mi-V Configurator—Memory Map Tab

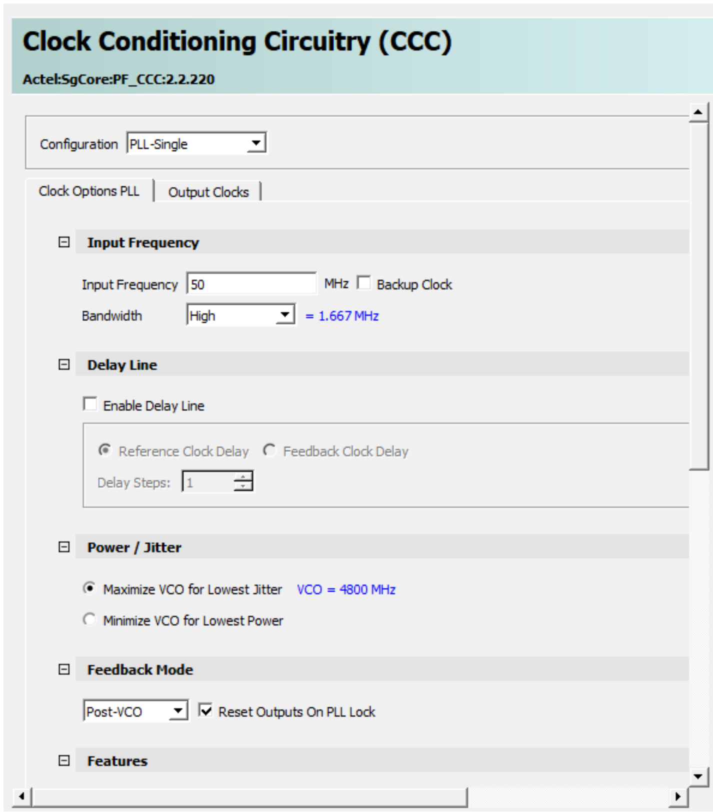


1.3.3.7 PF_CCC_0 (Ask a Question)

PF_CCC_0 (PolarFire Clock Conditioning Circuitry) generates the fabric reference clock that drives the soft processor and the APB peripherals (CoreTSE and CoreSPI). The PF_CCC_0 IP is configured to generate one output fabric clock from an on-board 50 MHz crystal oscillator.

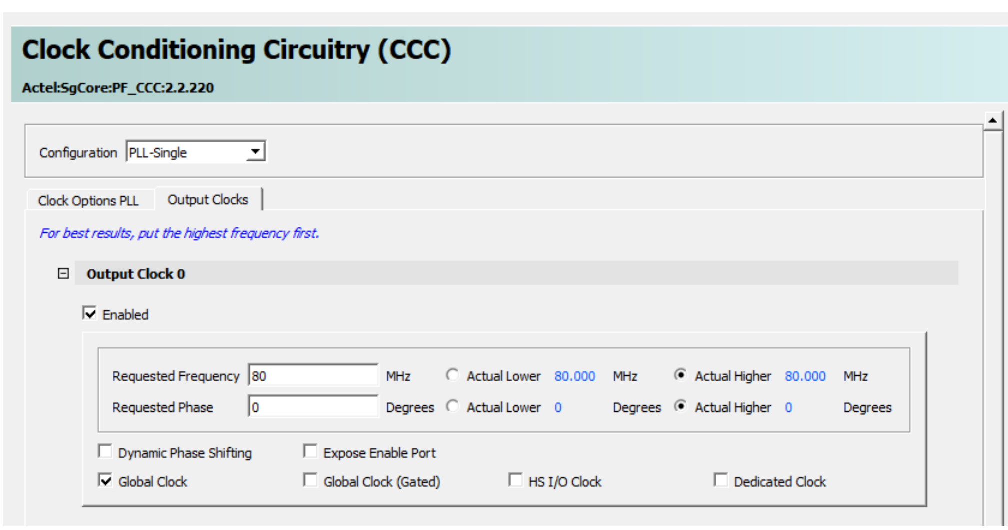
The following figure shows the PF_CCC_0 input clock configuration.

Figure 1-7. PF_CCC_0 Input Clock Configuration



The following figure shows the PF_CCC_0 output clock configuration. This design uses an 80 MHz system clock for configuring the APB peripherals.

Figure 1-8. PF_CCC_0 Output Clock Configuration



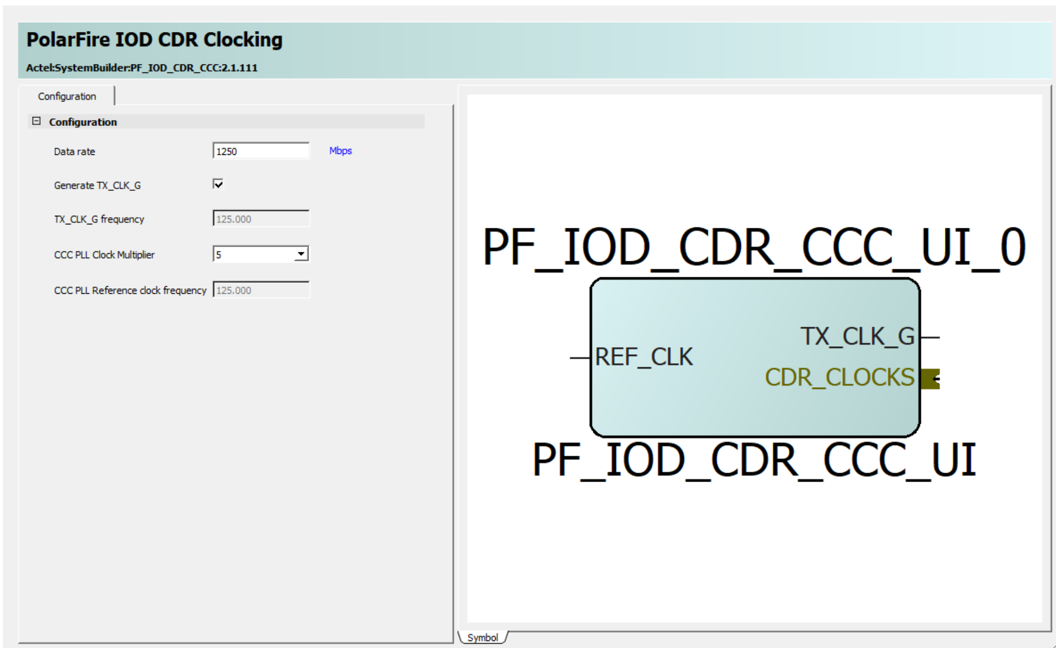
1.3.3.8 PF_IOD_CDR_CCC_C0 (Ask a Question)

The PF_IOD_CDR_CCC IP used for generating high-speed bank clocks for PF_IOD_CDR. This IP is in PLL-DLL cascaded mode to generate high-speed bank clocks of four phases: 0, 90, 180, and 270 from a 125 MHz input. CDR requires four phases of HS_IO_CLK running at half the frequency of the serial data rate. Therefore, the HSIO clock frequency is selected as 625 MHz with four phases.

PF_IOD_CDR_CCC also generates the fabric Tx interface clock (TX_CLK_G) for the CoreTSE block by dividing the bank clock by the ratio of 5. The Delay-Locked Loops (DLL) are needed to control the clock position (delay) with DLL codes when the data is active on the Rx interface (RX_P/RX_N). A glitch-less DLL can adjust the clock delay setting when the data is active.

The following figure shows the PF_IOD_CCC_C0_0 configuration.

Figure 1-9. PF_IOD_CDR_CCC Configuration



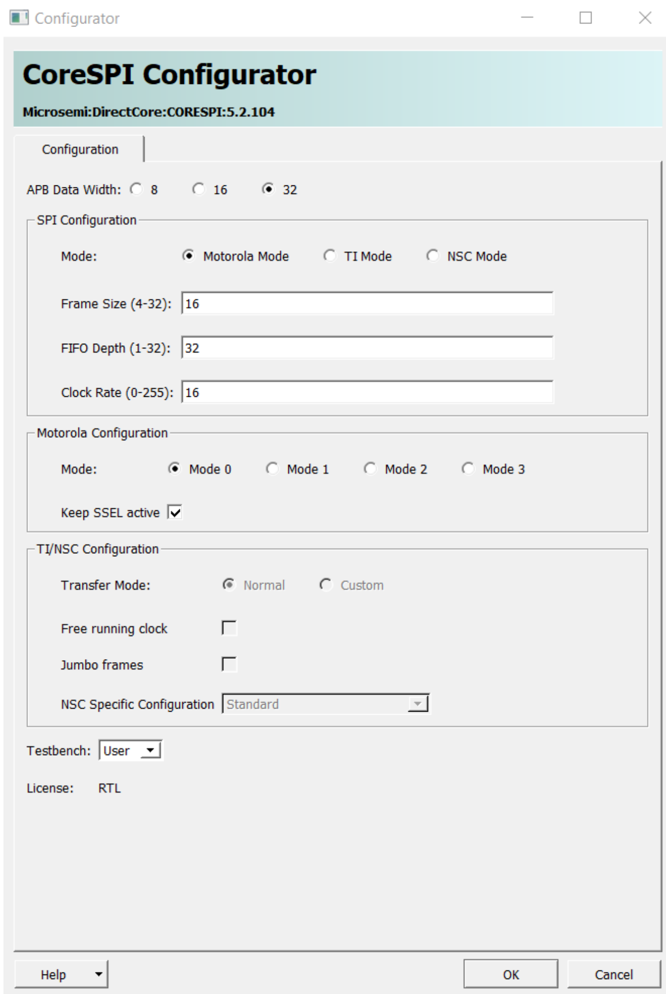
1.3.3.9 CORESPI_0 (Ask a Question)

The CORESPI_0 (CoreSPI) block is a controller IP, which implements the SPI communication. Mi-V configures the ZL30364 clock generation hardware using the CORESPI_0 block. The following points describe the CoreSPI_0 configuration, as shown in Figure 1-10.

- **APB Data Width** is selected as 32 because the design uses 32-bit APB data width
- The default serial protocol mode, Motorola mode, is retained to interface with ZL30364
- Frame size is set to 16 to match the read/write cycles supported by ZL30364
- FIFO depth is set to 32 to store the maximum frames (TX and RX) in FIFO
- Clock rate for the SPI master clock is selected as 16. This is used to generate the SPI clock of 2.35 MHz (SPICLK = PCLK/(2*(clock rate+1) = 80/(2*(7+1)) = 2.35 MHz)
- The **Keep SSEL active** check box is enabled to keep the slave peripheral active between back-to-back data transfers

The following figure shows the CoreSPI configuration.

Figure 1-10. CoreSPI_0 Configurator



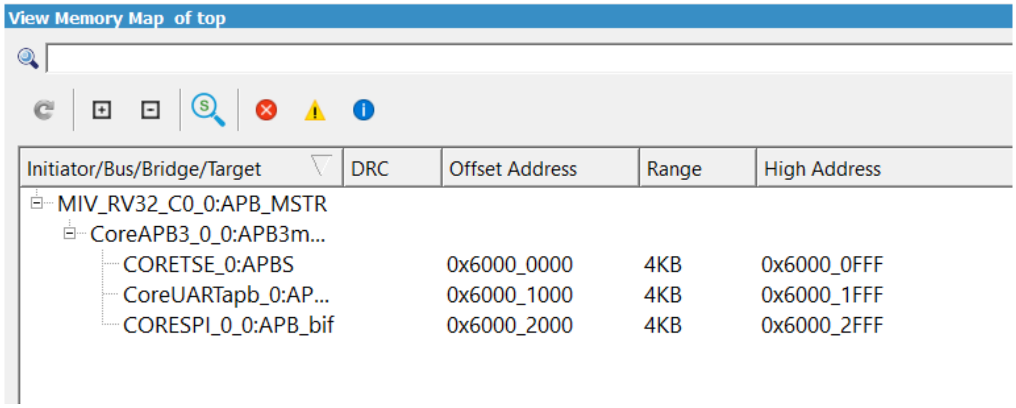
1.3.3.10 CoreUARTapb_0 (Ask a Question)

The CoreUARTapb_0 block is a serial communication controller with a flexible serial data interface. It is used for UART communication between the device and the host PC. This IP retains the default configuration.

1.3.3.11 Design Memory Map (Ask a Question)

The following figure shows the Mi-V processor bus interface memory map.

Figure 1-11. Mi-V Processor Bus Interface Memory Map



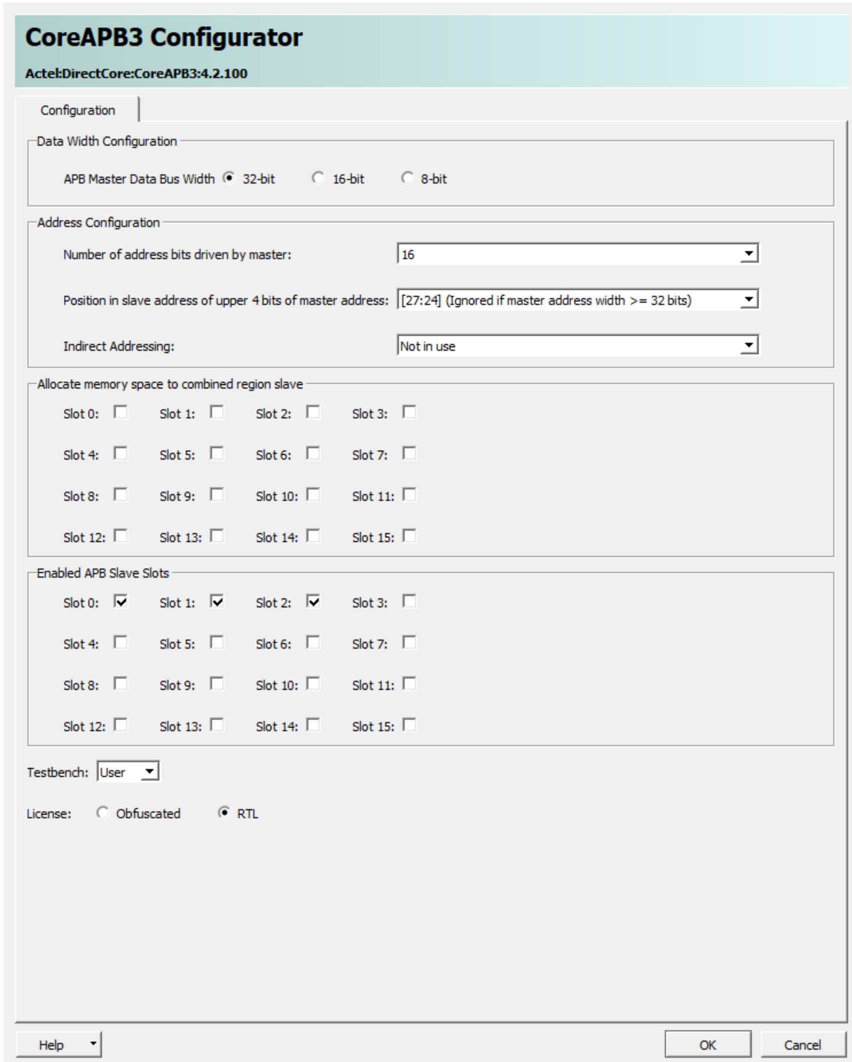
1.3.3.12 CoreAPB3 (Ask a Question)

CoreAPB3 is configured as per the following figure to connect the peripherals CoreTSE, CoreSPI, and CoreUARTapb as slaves.

CoreAPB3 is configured as follows:

- APB Master Data Bus Width: 32-bit
- Number of address bits driven by master: 16. The Mi-V processor addresses slaves using 16-bit addressing, so the final address for these slaves translates to 0x6000_0000, 0x6000_1000, and 0x6000_2000
- Enabled APB Slave Slots: S0, S1, and S2 (for CoreTSE, CoreUARTapb, and CoreSPI, respectively).

Figure 1-12. CoreAPB3 Configuration



1.3.3.13 SSDetect (Ask a Question)

It is an user-defined fabric logic. This block detects the transitions in the incoming data stream. Once the transitions are detected, the CDR is pulled out of the reset state.

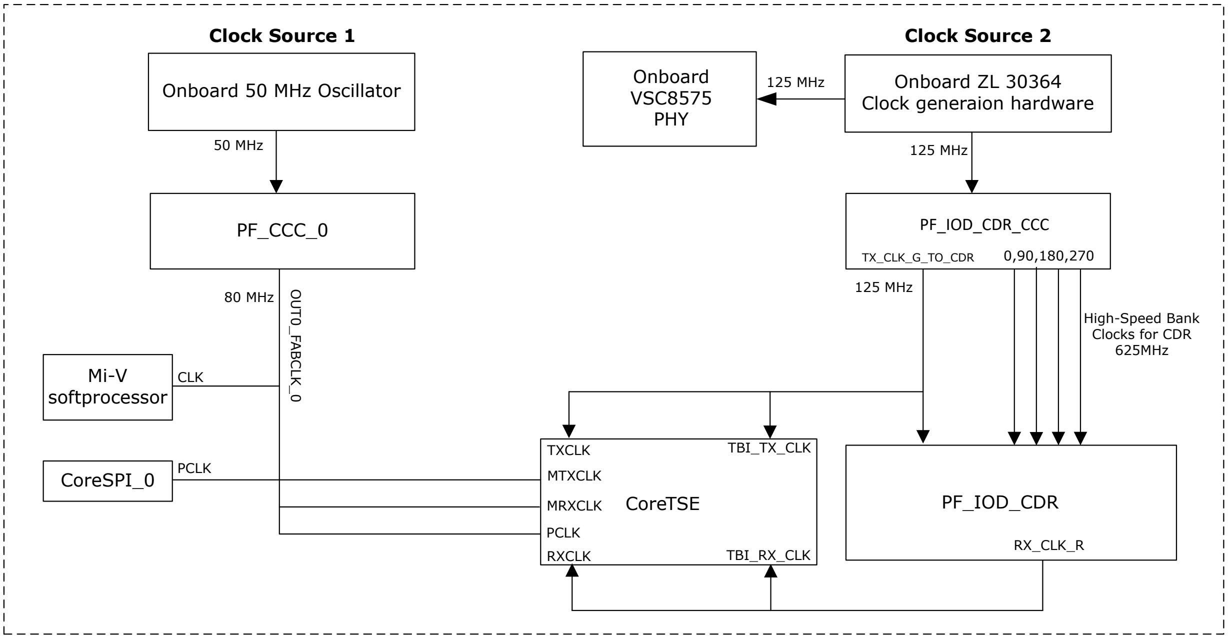
1.4 Clocking Structure (Ask a Question)

In the demo design, there are two clock sources—the on-board 50 MHz oscillator and the on-board ZL30364 clock generation hardware.

- On-board 50 MHz oscillator: This oscillator drives PLL that generates an 80 MHz clock for the Mi-V soft processor and peripherals. In this design, Mi-V processor runs at 80 MHz.
- On-board ZL 30364 clock generation hardware: This hardware generates the reference clocks for VSC PHY, the IOD CDR fabric module, and CoreTSE.

The following figure shows the clocking structure of the demo design.

Figure 1-13. Clocking Structure



2. Libero Design Flow (Ask a Question)

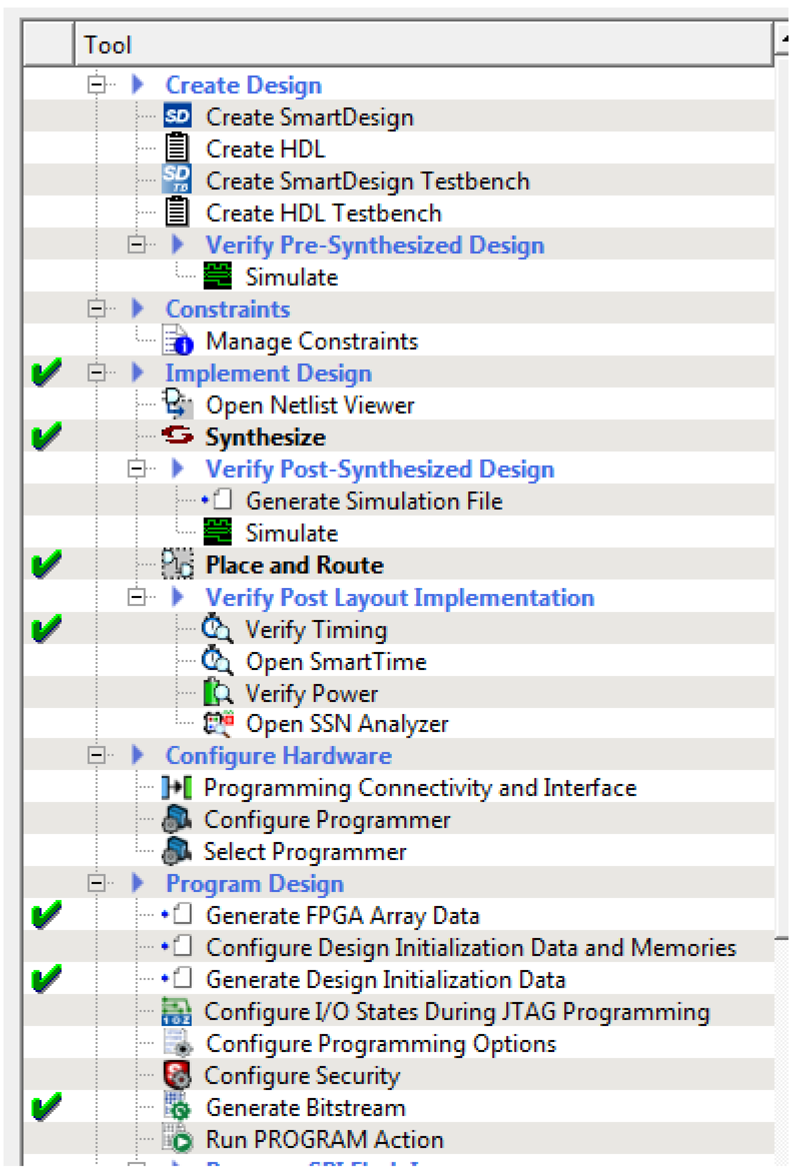
This section describes the Libero design flow for running this demo.

Important:

- To initialize the TCM in PolarFire using the system controller, change the local parameter, l_cfg_hard_tcm0_en, to 1’b1 in the `miv_rv32_opsrv_cfg_pkg.v` file prior to synthesis. See the 2.7 TCM section in the MIV_RV32 v3.0 Handbook from the Libero SoC Catalog.
- To run the Libero design using TCL script, see 5. Appendix 2: Running the TCL Script.

The following figure shows these options in the Design Flow tab.

Figure 2-1. Libero Design Flow Options



2.1 Synthesize (Ask a Question)

To synthesize the design, perform the following the steps:

1. On the **Design Flow** window, double click **Synthesize**. When the synthesis is successful, a green tick mark appears next to **Synthesize**, as shown in Figure 2-1.
2. To view the synthesis report and log files in the **Reports** tab, right click **Synthesize** and select **View Report** . It is recommended to view the `top.srr` and the `top_compile_netlist.log` files for debugging synthesis and compile errors.

2.2 Place and Route (Ask a Question)

The demo project includes the IO PDC file and the floor planner PDC constraint files. The Place and Route process uses these PDC files to place the I/Os and CCC macros.

To place and route the design, perform the following steps:

1. On the **Design Flow** window, double click **Place and Route**. When place and route is successful, a green tick mark appears next to **Place and Route**, as shown in Figure 2-1.
2. To view the place and route report and the log files in the **Reports** tab, right click **Place and Route** and select **View Report**. It is recommended to view the `top_place_and_route_constraint_coverage.xml` file for place and route constraint coverage.

2.2.1 PLL, DLL, and Lane Controller Placement (Ask a Question)

PolarFire FPGA I/O pairs are grouped into lanes. Each I/O bank has multiple lanes. Each lane consists of twelve I/Os (six I/O pairs), a lane controller, and a set of high-speed, low-skew clock resources.

All associated I/Os must be placed in one lane. For example, RX_P and RX_N must be placed in the same lane. For more information, see PolarFire FPGA and PolarFire SoC FPGA User I/O User Guide. The IO Editor shows the placement of the components and I/Os. The PLL of PF_CCC and the PLL, the DLL, and the Lane Controller of PF_IOD_CDR_CCC_C0 are auto placed by Libero SoC.

2.2.2 Resource Utilization (Ask a Question)

The resource utilization report is written to the `top_layout_log.log` file in the **Reports** tab under **iog_cdr_1 Gbps reports** > **Place and Route**. The following table lists the resource utilization of the design after place and route. These values might vary slightly for different Libero runs, settings, and seed values.

Table 2-1. Resource Utilization

Type	Used	Total	Percentage
4LUT	22551	299544	7.53
DFF	12703	299544	4.24
I/O register	0	510	0.00
Logic Elements	24090	299544	8.04
User I/O	21	512	4.10
– Single-ended I/O	17	512	3.32
– Differential I/O pairs	3	256	1.17

2.3 Verify Timing (Ask a Question)

To verify timing, perform the following steps:

1. On the **Design Flow** window, double click **Verify Timing**. When the design successfully meets the timing requirements, a green tick mark appears next to **Verify Timing**, as shown in Figure 2-1.
2. To view the verify timing report and log files in the **Reports** tab, right click **Verify Timing** and select **View Report**.

2.4 Generate FPGA Array Data (Ask a Question)

To generate FPGA array data, perform the following steps:

1. On the **Design Flow** window, double click **Generate FPGA Array Data**.
2. When the FPGA array data is successfully generated, a green tick mark appears next to **Generate FPGA Array Data**, as shown in Figure 2-1.

2.5 Configure Design Initialization Data and Memories (Ask a Question)

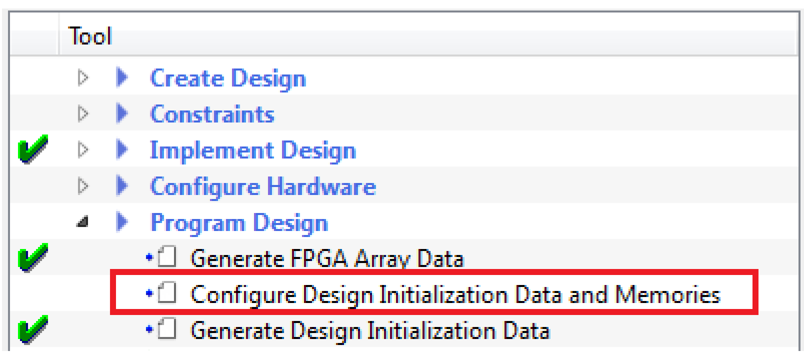
The fabric RAM blocks must be initialized with the user application to configure the PHY and the management registers of CoreTSE. The user application (HEX file) is generated using SoftConsole. This step is used to select the fabric RAM client (HEX file), its storage location (sNVM/µPROM/SPI Flash), and generate the fabric RAM client. The non-volatile memory is programmed with this client and at device power-up, the fabric RAM blocks are initialized with the content from the selected NVM.

The Configure Design Initialization Data and Memories option creates the TCM initialization client. When the PolarFire device powers up, the TCM memory is initialized with the sNVM contents.

To create the TCM initialization client, perform the following steps:

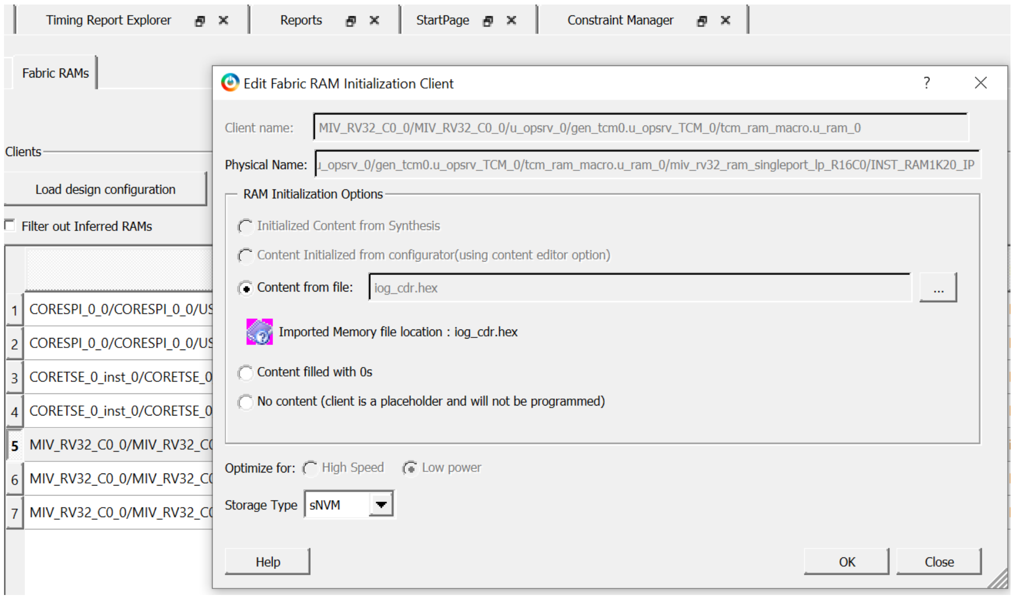
1. On the **Design Flow** window, double click **Configure Design Initialization Data and Memories**, as shown in Figure 2-2.

Figure 2-2. Configure Design Initialization Data and Memories Option



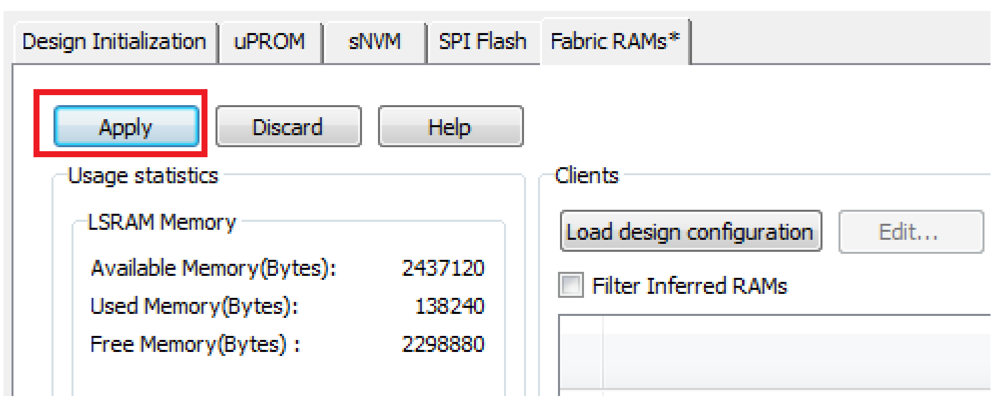
2. In the **Fabric RAMs** tab, configure the `MIV_RV32_C0_0/MIV_RV32_C0_0/u_opsrv_0/gen_tcm0.u_opsrv_TCM_0/tcm_ram_macro.u_ram_0` instance and ensure that the contents are stored in sNVM, and then set the **Storage Type** as **sNVM** as shown in the following figure.

Figure 2-3. Fabric RAMs Tab



3. Import the hex file (`iog_cdr.hex`) from: `mpf_an4623_v2022p3_df\TCL_Scripts\src\src_softconsole`. The `iog_cdr.hex` file is an application file generated using SoftConsole that configures the ZL clock generation hardware, the CoreTSE registers, and the VSC PHY. The application code is initially stored in sNVM. On device power-up, the system controller copies the code to TCM, and the Mi-V processor executes the code from TCM.
4. Click **Apply**.

Figure 2-4. Fabric RAM Tab Apply Option



5. On the **Design Flow** window, double click **Generate Design Initialization Data**. When the initialization client is successfully generated in sNVM, a green tick mark appears next to **Generate Design Initialization Data**, as shown in Figure 2-1.

2.6 Generate Bitstream (Ask a Question)

To generate the bitstream, perform the following steps:

1. On the **Design Flow** window, double click **Generate Bitstream**. When the bitstream is successfully generated, a green tick mark appears next to **Generate Bitstream**, as shown in Figure 2-1.
2. To view the corresponding log file in the **Reports** tab, right click **Generate Bitstream** and select **View Report**.

2.7 Run PROGRAM Action (Ask a Question)

After generating the bitstream, the PolarFire device must be programmed. The programming procedure involves setting up board and invoking the programming command from Libero.

To perform Run PROGRAM Action, follow these steps:

Notes: If you want to program the board using the `.job` file instead, see Programming the Device Using FlashPro, page 26.

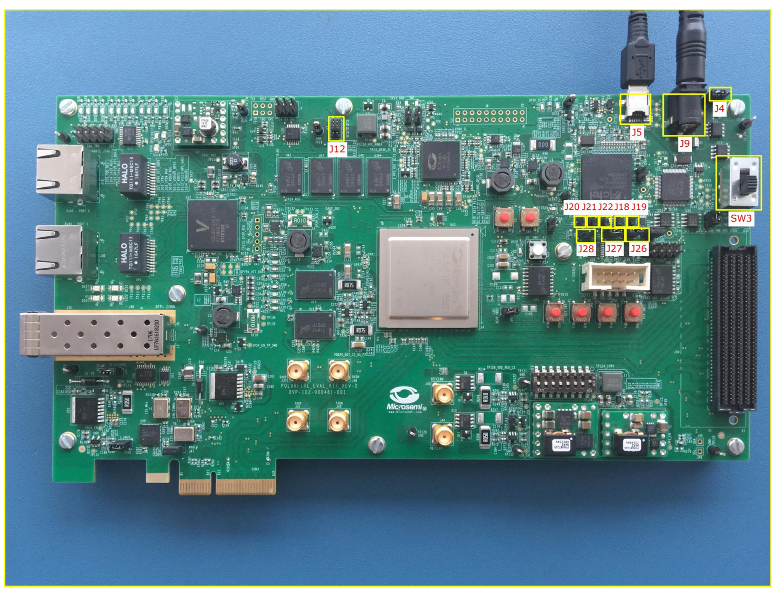
1. Ensure that the jumper settings on the board are listed as in the following table.

Table 2-2. Jumper Settings

Jumper	Setting
J18, J19, J20, J21, and J22	Close pins 2 and 3 for programming through FTDI
J28	Close pins 1 and 2 for programming through the on-board FlashPro5
J4	Close pins 1 and 2 for switching the power manually using SW3
J12	Close pins 3 and 4 for 2.5 V

2. Connect the power supply cable to the **J9** connector on the board.
3. Connect the USB cable from the host PC to **J5** (FTDI port) on the board.
4. Connect the RJ45 cable from the host PC to the **J15** connector (RJ45-PORT 0) on the board. This is required for the Ethernet link after programming.
   The following figure shows the board setup for programming the device.

   Figure 2-5. Board Setup



5. Power up the board using the **SW3** slide switch.
6. On the Design Flow window, double click **Run PROGRAM Action**.
7. When the device is successfully programmed, the LEDs 6, 7, 8, 9, 10, and 11 on the board glow, and a green tick mark appears, as shown in Figure 2-1.
8. To view the corresponding log file in the **Reports** tab, right click **Run PROGRAM Action** and select **View Report**.

The demo is ready to be run. For information about how to run the demo, see 3. Running the Demo.

3. Running the Demo (Ask a Question)

This section describes how to run the 1G loopback demo. The procedure involves transmitting packets from the network card of the host PC to the board and verifying the packets transmitted to and received from the board using Cat Karat.

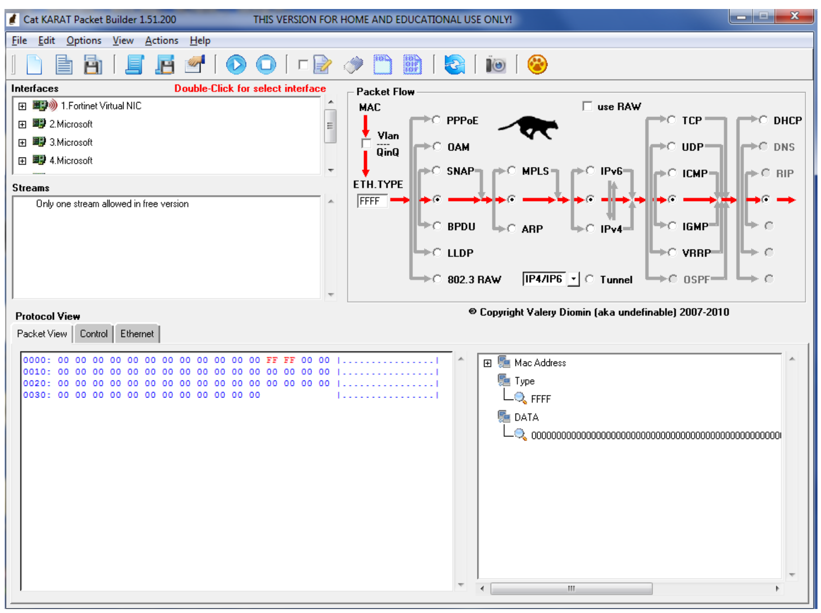
The following procedure assumes that:

- The PolarFire FPGA is programmed with the demo design programming file (`.job`). For more information, see 4. Appendix 1: Programming the Device Using FlashPro Express
- The Cat Karat software is installed on the host PC

To run the demo, perform the following steps:

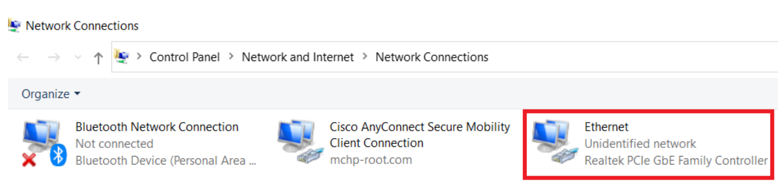
1. Ensure that the RJ45 cable is connected from the host PC to the **J15** connector on the board.
2. Power up the board using the **SW3** slide switch.
3. Confirm that LED 7 is glowing, indicating that the Ethernet PHY link is up and running.
4. Open the Cat Karat software from the Start menu of the host PC. The Cat Karat Packet Builder window opens, see the following figure.

Figure 3-1. Cat Karat Packet Builder Window



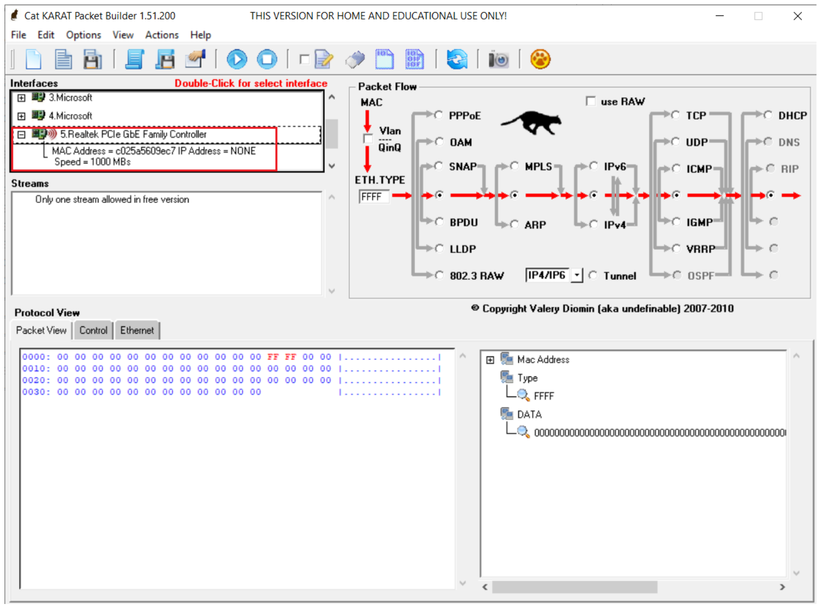
5. From the **Control Panel** of the host PC, note the name of the Ethernet network connection, see the following figure. On a Windows 10 machine, this connection is **Ethernet**.

Figure 3-2. Ethernet Network Connection



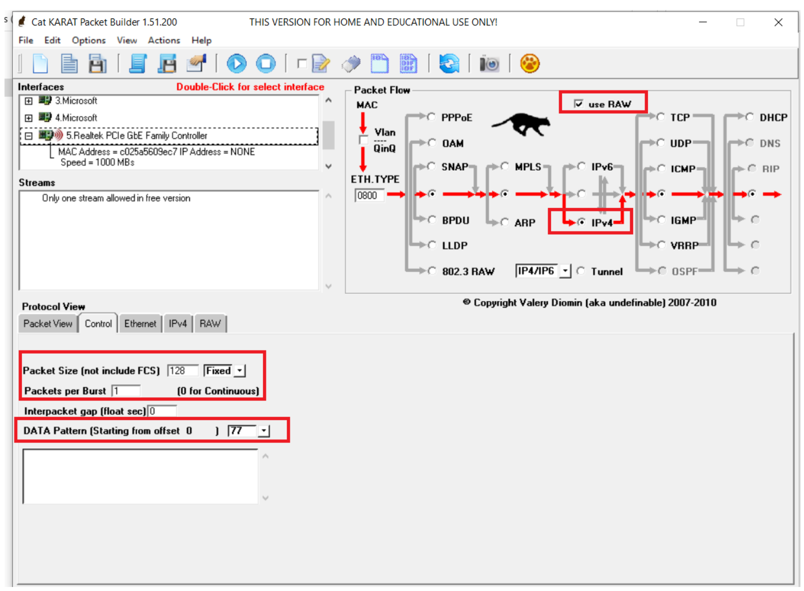
6. Click **Cat Karat Packet Builder** > **Interfaces pane**, and then double click **Ethernet Network connection**, see the following figure.

Figure 3-3. Interface Selection



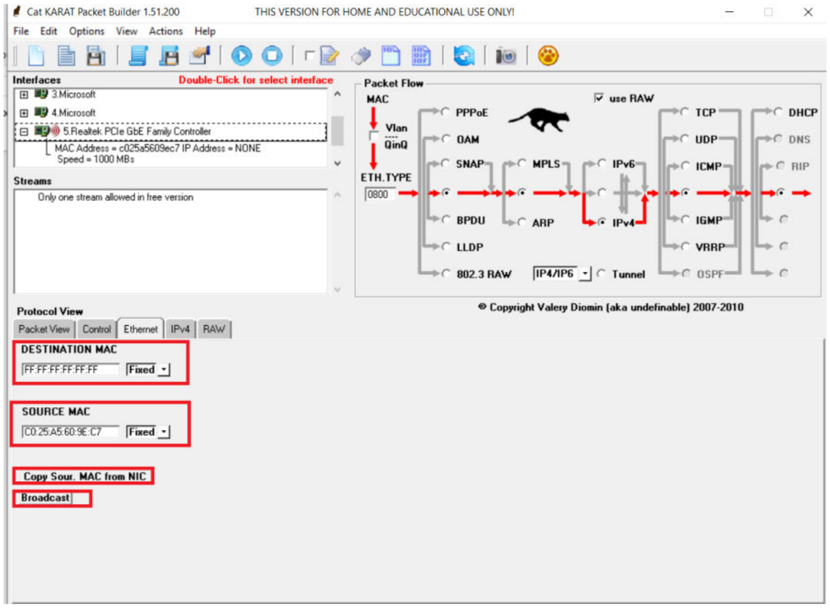
7. In the **Packet Flow** pane, select **use RAW** check box and **IPv4** check box. In the **Control** tab, set **Packets per Burst** to **1** and the **Data Pattern** to **77**, **Packet Size** to **128**, see the following figure.

Figure 3-4. Packet Flow and View Settings



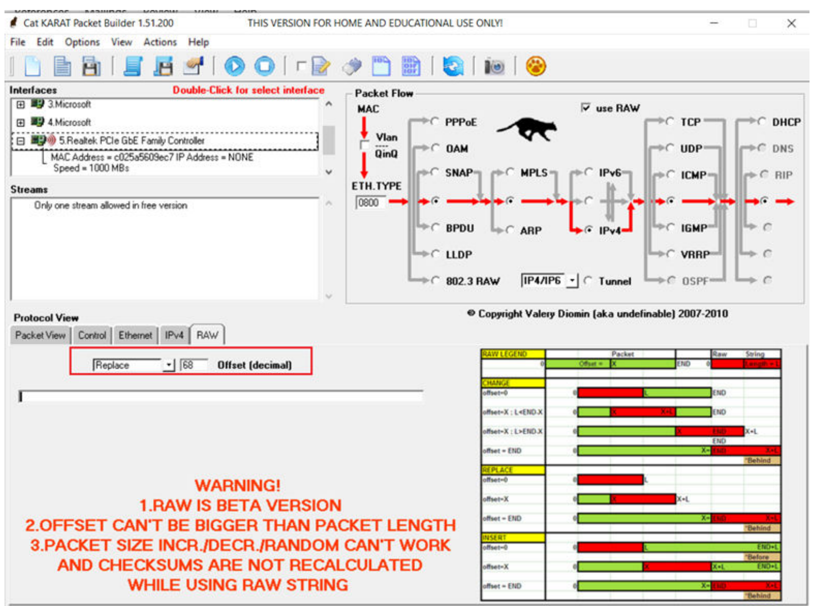
8. In the **Ethernet** tab, click **Copy Source**. **MAC from NIC** for source MAC and click **Broadcast** for Destination MAC, see the following figure.

Figure 3-5. Protocol View—Ethernet Tab



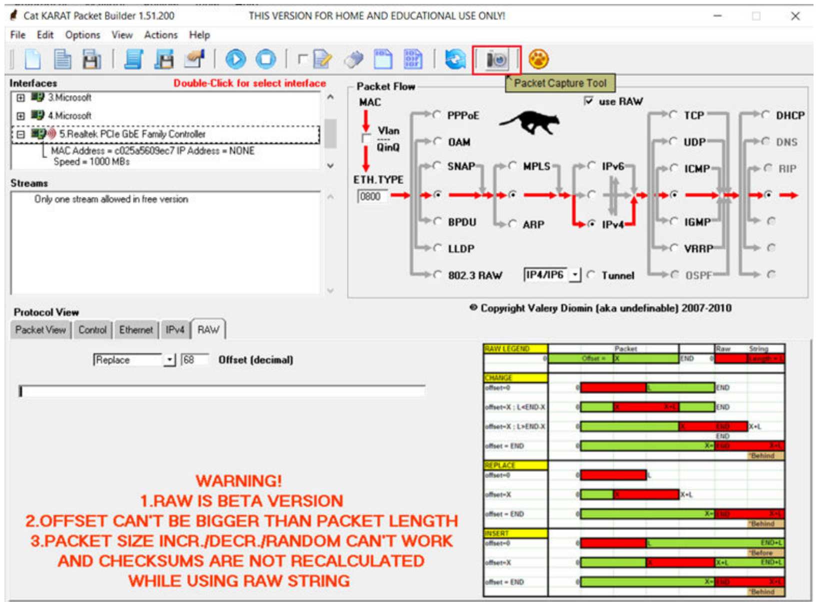
9. In the **IPv4** tab, retain the default settings.
10. In the **RAW** tab, configure **Offset**, see the following figure.

Figure 3-6. Protocol View—Raw Tab



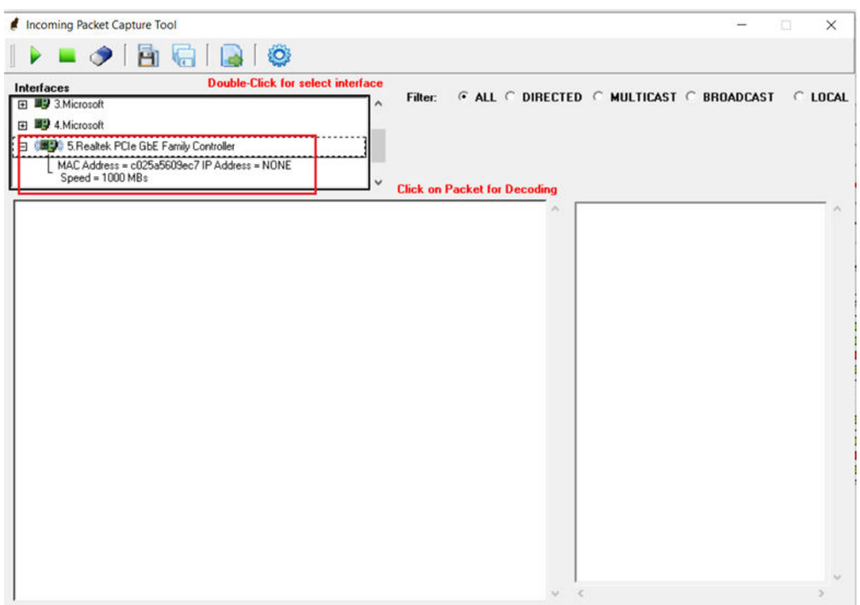
11. Launch **Packet Capture Tool** to monitor the transmitted and received packets, see the following figure.

Figure 3-7. Packet Capture Tool



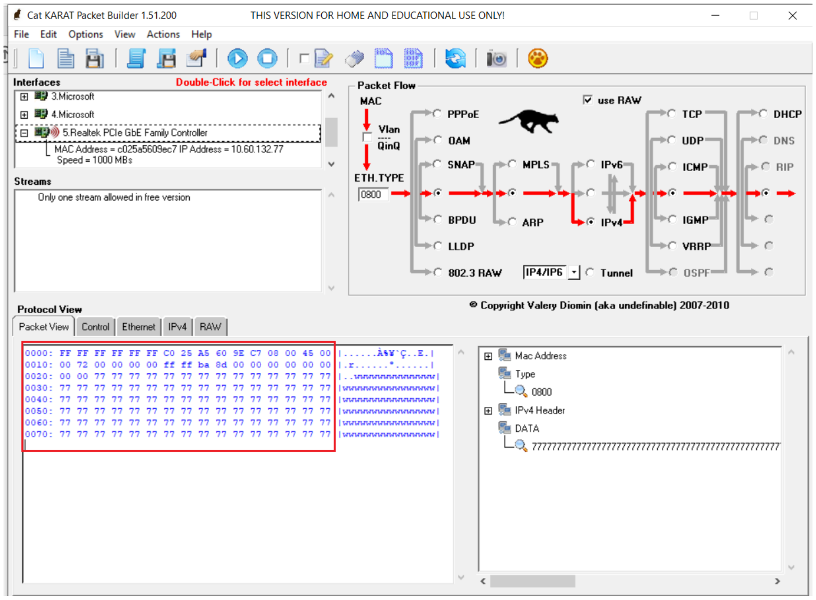
12. Monitor the transmitted and received packets on the **Incoming Packet Capture Tool** window. In **Incoming Packet Capture Tool**, select an interface in the **Interfaces** pane, see the following figure.

Figure 3-8. Incoming Packet Capture Tool—Interfaces Pane



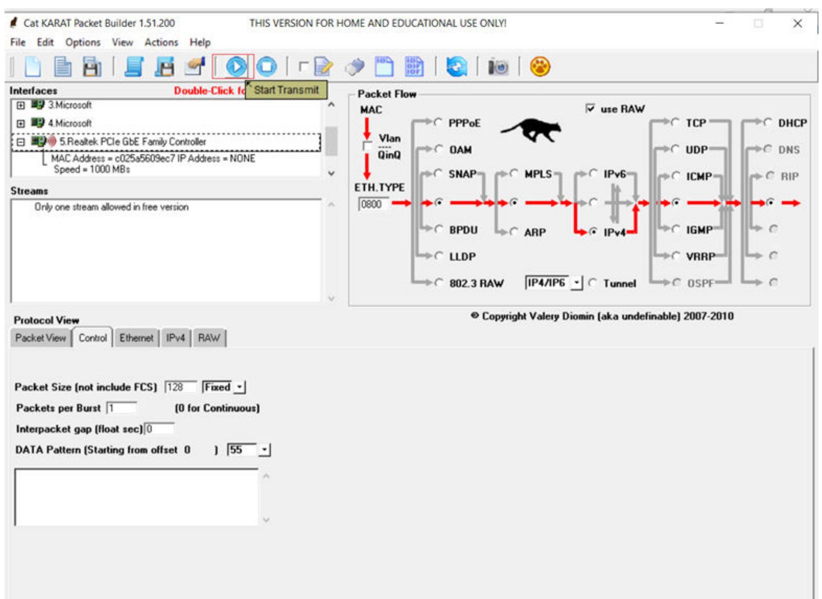
13. Before transmitting, in the **Packet View** tab, check the packet being transmitted, see the following figure.

Figure 3-9. Packet View Tab



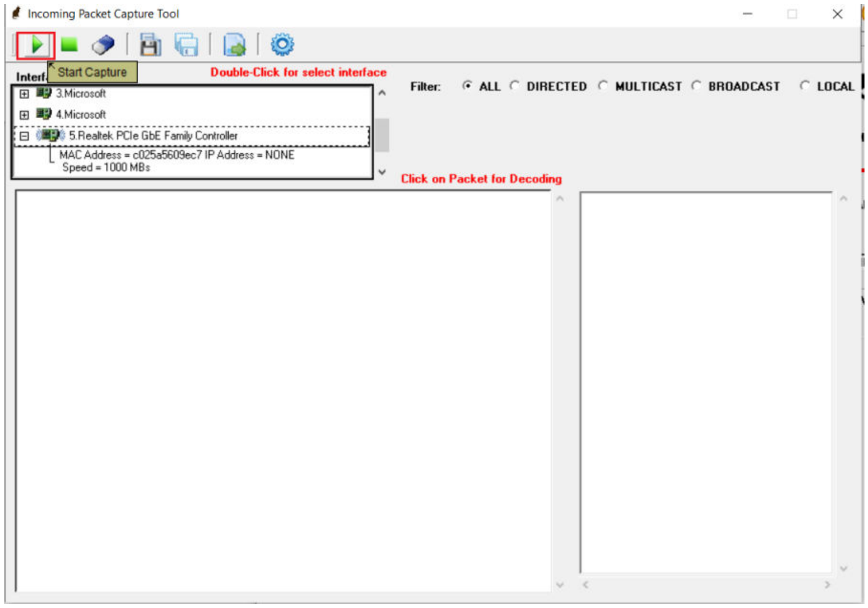
14. In the **Cat Karat** window, click **Start Transmit** (as highlighted in the following figure) to transmit one packet from the host PC to the board.

Figure 3-10. Cat Karat Window—Start Transmit



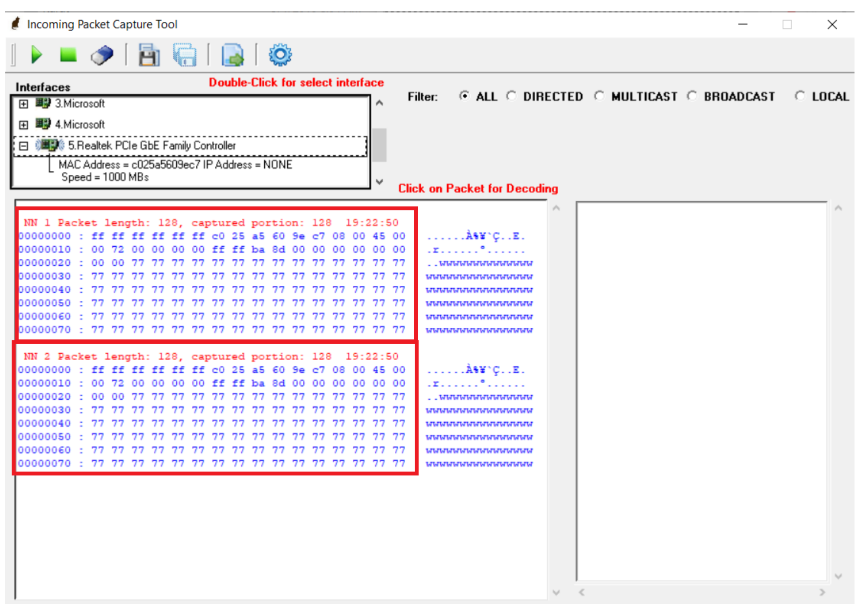
15. Click **Start Capture** (as highlighted in the following figure) to monitor the transmitted and received packets.

Figure 3-11. Incoming Packet Capture Tool—Start Capture



16. After clicking **Start Capture**, you see the transmitted and received packets, as shown in the following figure.
    One packet was transmitted from the host PC to the board. The same packet was looped back at the CoreTSE IP and was sent back to the host PC. All packets transmitted from the host PC network are looped back in the same way.

Figure 3-12. Transmitted and Received Packets



17. Select different burst rates, data patterns, and transmit packets to the board.
18. Power-down the board and close the Cat Karat software.

You have successfully run the demo.

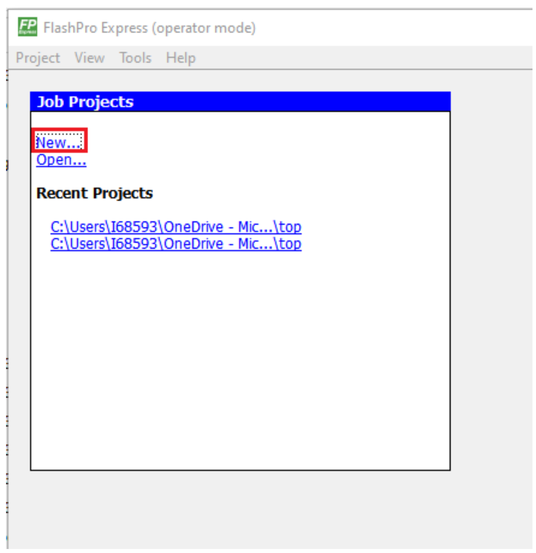
4. Appendix 1: Programming the Device Using FlashPro Express (Ask a Question)

This section describes how to program the PolarFire device with the job file using Flashpro Express. The job file is available at the following design files folder location: `mpf_an4623_v2022p3_df\Programming_Job`

To program the device using FlashPro Express, perform the following steps:

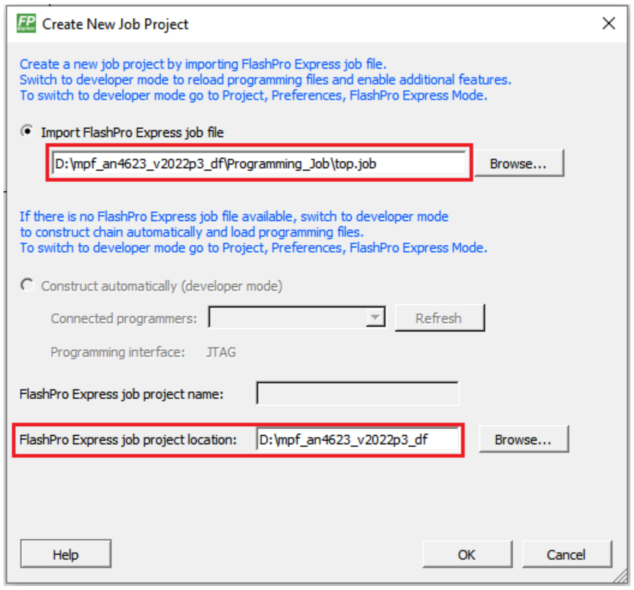
1. Connect the jumpers and set up the PolarFire Evaluation Kit Board as described in steps 1 to 5 of 2.7. Run PROGRAM Action.
2. On the host PC, start the FlashPro Express software from `<$Installation Directory>\Microchip\Designer\binfp`.
3. To create a new job project, on the **Project** menu, select **New** or select **New Job Project from FlashPro Express Job**, as shown in the following figure.

Figure 4-1. FlashPro Express Job Project



4. Enter the following in the **New Job Project from FlashPro Express Job** dialog box:
   - **Programming job file**: Click **Browse**, and navigate to the location where the job file is located and select the file. The default location is: `mpf_an4623_v2022p3_df\Programming_Job`
   - **FlashPro Express job project location**: Click **Browse** and navigate to the location where you want to save the project.

Figure 4-2. New Job Project from FlashPro Express Job



5. Click **OK**. The required programming file is selected and ready to be programmed in the device.
6. The FlashPro Express window appears. Confirm that a programmer number appears in the Programmer field. If it does not, confirm the board connections and click **Refresh/Rescan Programmers**.
7. Click **RUN**. When the device is programmed successfully, a **RUN PASSED** status is displayed. See 3. Running the Demo.
8. Close FlashPro Express, or in the **Project** tab, click **Exit**.

5. Appendix 2: Running the TCL Script (Ask a Question)

TCL scripts are provided in the design files folder under directory TCL_Scripts. If required, the design flow can be reproduced from Design Implementation till generation of job file.

To run the TCL, follow the steps below:

1. Launch the Libero software.
2. Click **Project** > **Execute Script**.
3. Click **Browse,** and then from the downloaded TCL_Scripts directory, select `script.tcl`.
4. Click **Run**.

After successful execution of TCL script, Libero project is created within `TCL_Scripts` directory.

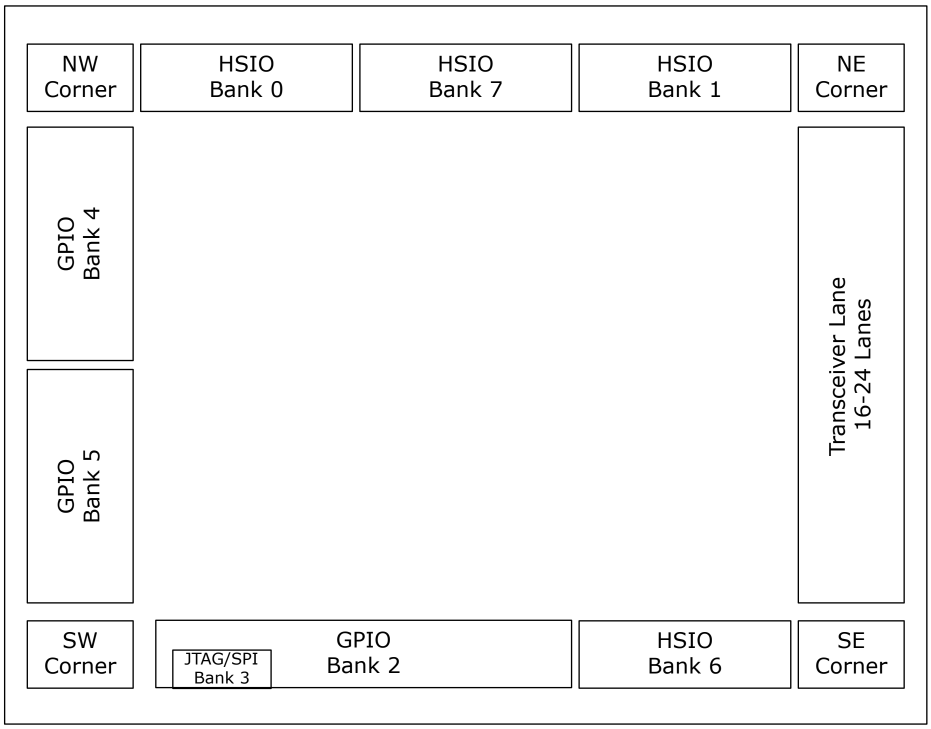
For more information about TCL scripts, refer to `mpf_an4623_v2022p3_df/TCL_Scripts/readme.txt`.

For more information about TCL commands, see Libero® SoC TCL Command Reference Guide. Contact Technical Support for any queries encountered when running the TCL script.

6. Appendix 3: Multi-Lane 1G IOD CDR Design (Ask a Question)

In a multi-lane design, Ethernet traffic from multiple RJ45 cables comes into FPGA through PHY. In such cases, multiple RX and TX ports must be assigned from the PolarFire GPIO Banks to form multiple SGMII links with the PHY. The following figure shows the placement of I/O Banks and PLLs in a PolarFire device (MPF300).

Figure 6-1. I/O Banks and PLL Placement in MPF300



Each Bank has multiple I/O lanes and each I/O lane includes six I/O pairs. The lane controller available in each I/O lane has a clock recovery unit, which is used for the clock recovery of that lane. Therefore, only one SGMII link can be realized from an I/O lane.

For an 8-lane design, eight I/O lanes are used to form eight SGMII links. To enable sharing of the PF_IOD_CDR_CCC, the selection of these I/O lanes must be made in any of the following ways:

- Lanes of the same bank can be selected vertically up to half of the side
- Lanes of the same bank can be selected horizontally up to half of the side
- Lanes from vertical and horizontal banks can be selected

Note: In Libero SoC, when I/O lanes are selected from Bank 5 or 2, or from both and placed, PF_IOD_CDR_CCC selects the SW PLL and is placed in SW. If all I/O lanes are selected from Bank 4, PF_IOD_CDR_CCC selects the NW PLL and is placed in NW.

When the reference clock for all the links is the same:

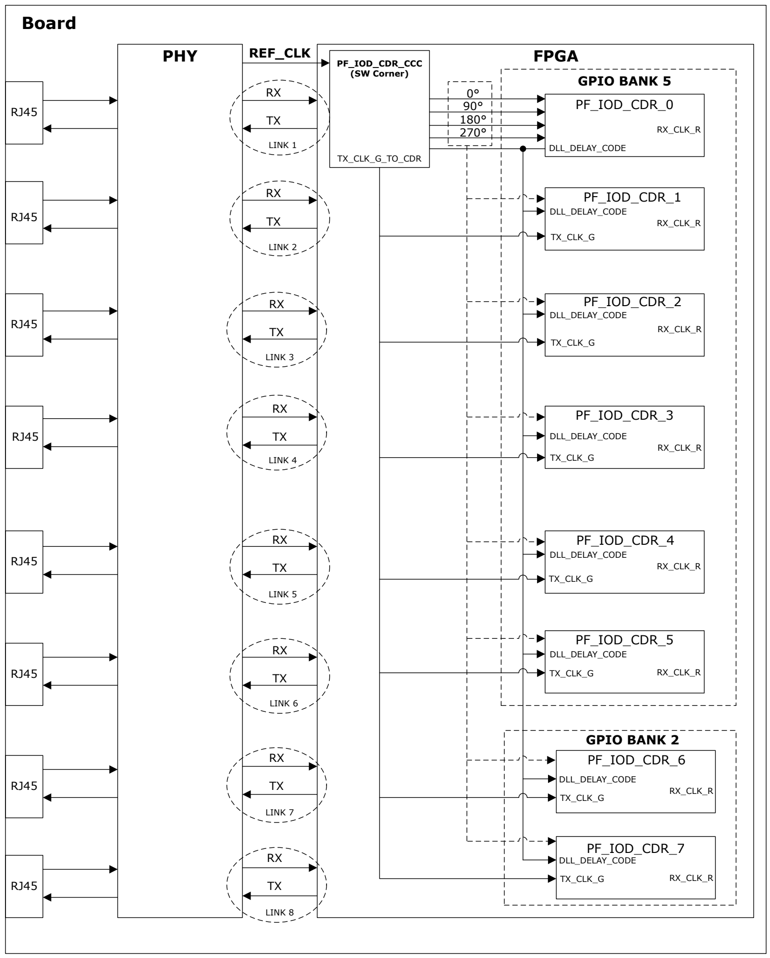
- PF_IOD_CDR_CCC can be shared across all IOD blocks (PF_IOD_CDR) for the HSIO BANK clocks and transmit clock (TX_CLK)
- PF_IOD_CDR_CCC uses an internal lane controller to generate the DLL delay code and share it with all IOD blocks. The DLL delay code is required for phase tuning/adjustment

To conclude, the following IOD resources are used to create an 8-lane design in a PolarFire MPF300 device:

- One PF_IOD_CDR_CCC with a lane controller for DLL delay update
- Eight I/O lanes and lane controllers for clock recovery

The following figure shows the high-level block diagram of an 8-lane design implemented using Libero SoC PolarFire.

Figure 6-2. 8 Lane 1G IOD CDR Design in PolarFire®



As per the preceding figure, eight PF_IOD_CDR instances are instantiated from GPIO Banks 5 and 2 to form eight links. The Clock Conditioning Circuit (CCC), available in the South-West corner, is configured in the PLL-DLL cascaded mode for the clock recovery and DLL delay update.

Apart from eight lane controllers for clock recovery, an additional lane controller from PF_IOD_CDR_CCC is inferred during synthesis for sharing the DLL delay update. This optimizes the utilization of lane controllers in the device.

7. Appendix 4: 1G Ethernet BASE-T and BASE-X Using Transceiver (Ask a Question)

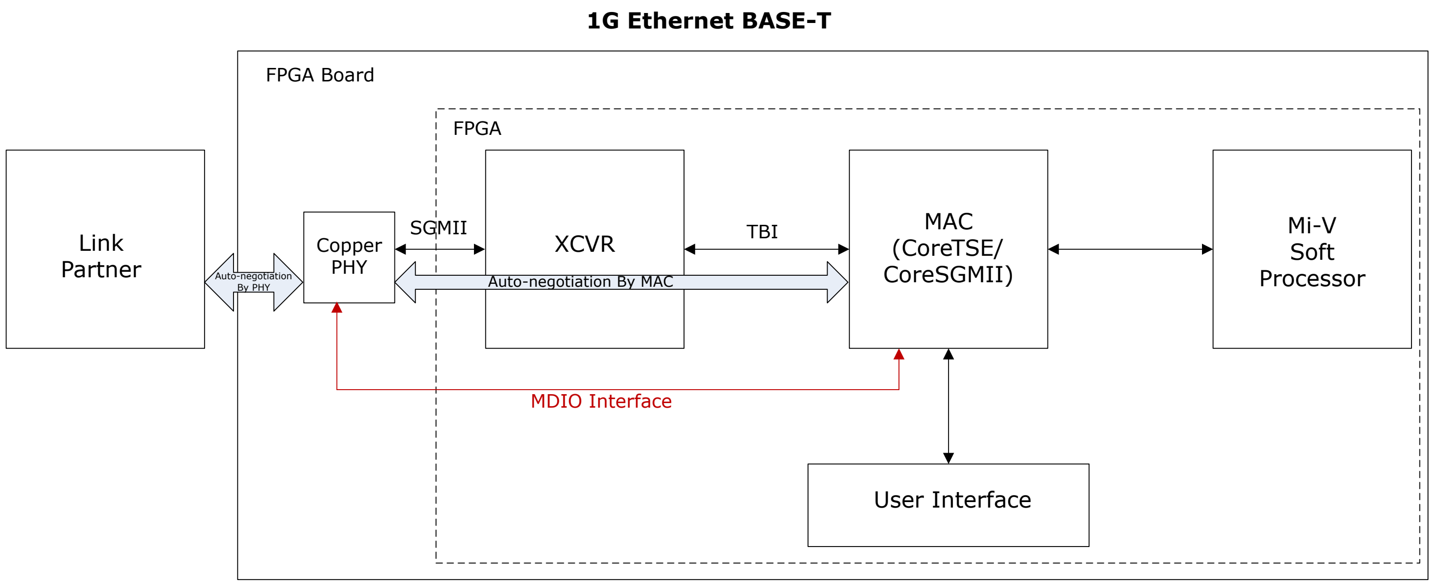
The PolarFire FPGA family includes multiple embedded low-power, performance-optimized transceivers. Each transceiver has both the Physical Medium Attachment (PMA), the protocol Physical Coding Sub-Layer (PCS) logic, and the interfaces to the FPGA fabric. The transceiver has a multi-lane architecture with each lane natively supporting serial data transmission rates from 250 Mbps to 12.7 Gbps. For more information, see PolarFire FPGA and PolarFire SoC FPGA Transceiver User Guide.

This section describes how 1G Ethernet BASE-T and BASE-X designs are implemented in PolarFire FPGAs using the transceivers.

7.1 1G Ethernet BASE-T and BASE-X (Ask a Question)

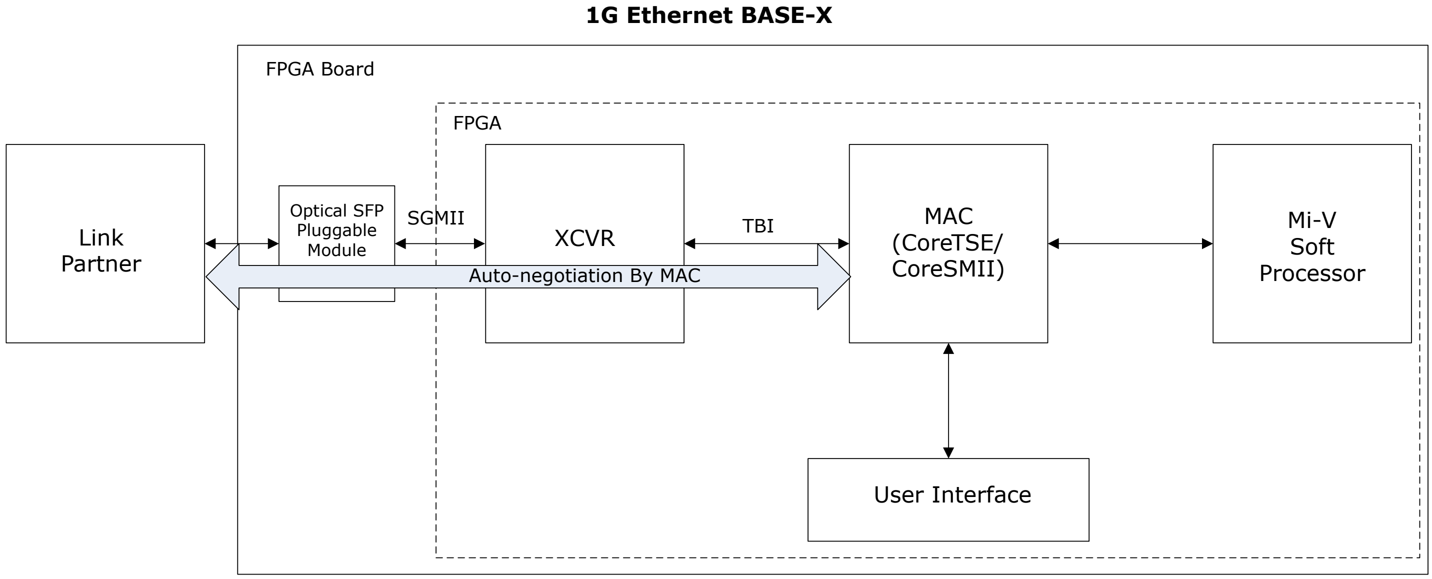
The following figure shows the typical FPGA design for 1G Ethernet BASE-T.

Figure 7-1. 1G BASE-T Design



The following figure shows the typical FPGA design for 1G Ethernet BASE-X.

Figure 7-2. 1G BASE-X Design



The following points summarize the 1G Ethernet BASE-T and BASE-X designs:

- The Mi-V soft processor is used to configure the PHY registers (using MDIO interface), the MAC Configuration, and the Management registers. Users can also implement a fabric logic or any other soft processor to implement these functions.
- The MAC IP is configured in the TBI mode.
- In BASE-T, the management block of the MAC IP auto-negotiates with the onboard PHY as per Clause 28 of the IEEE802.3z standard. The PHY auto-negotiates with the link partner.
- In BASE-X, the management block of the MAC IP auto-negotiates with the link partner as per Clause 37 of the IEEE802.3z standard.
- The Auto-Negotiation (AN) functions are defined in the MAC Management registers 04h to 08h. The bit field formats of these registers are different for BASE-T and BASE-X. For more information about the bit field formats of the AN registers, see *HB0549: CoreTSE v3.1 Handbook* or *HB0627: CoreSGMII v3.2 Handbook* from the Libero SoC Catalog. The following table lists the AN registers.

Table 7-1. AN Registers

Register	Description
04h	AN Advertisement
05h	AN Link Partner Base Page Ability
06h	AN Expansion
07h	AN Next Page Transmit
08h	AN Link Partner Ability Next Page

The following registers are common in BASE-T and BASE-X modes:
  - Control register at address 0x00
  - Status register at address 0x01

Registers 0x04, 0x05, 0x06, 0x07, and 0x08 are based on the configuration.

- XCVR is configured to operate at 1250 Mbps. For more information about XCVR configuration, see 7.2. Transceiver Configuration
- The user data from MAC (CoreTSE non-AHB) is provided on a 32-bit parallel bus

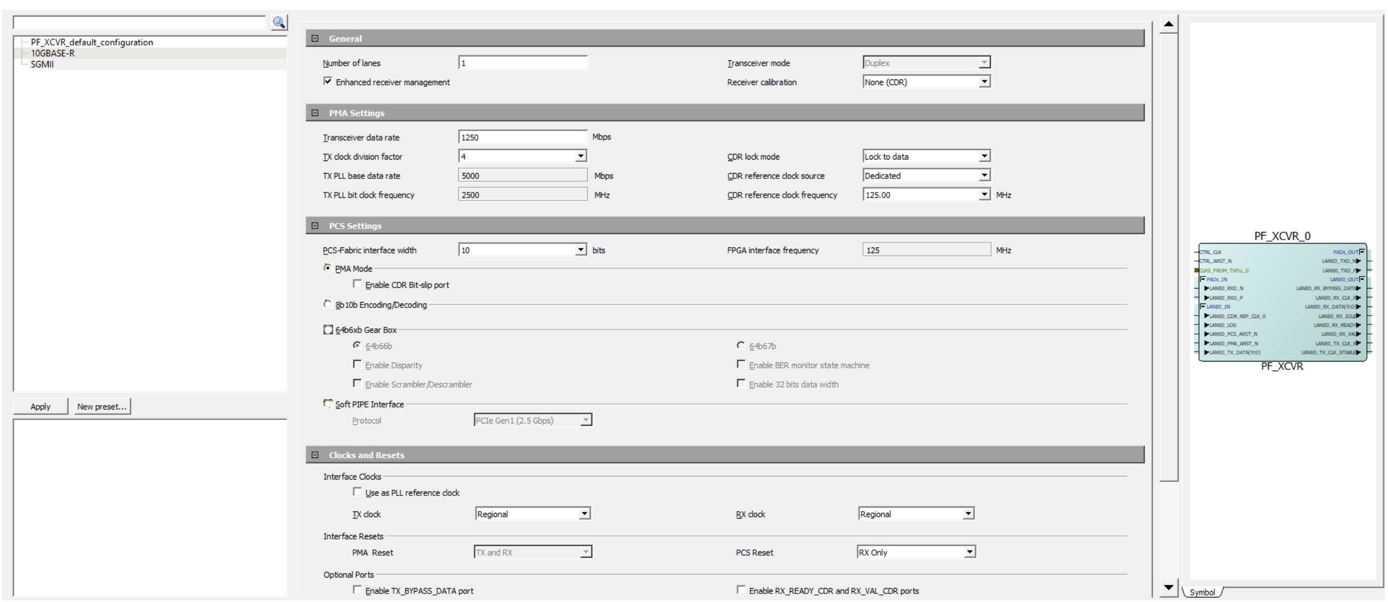
7.2 Transceiver Configuration (Ask a Question)

For 1G Ethernet BASE-T and BASE-X, the transceiver block is configured for 1.25 Gbps data rate. Figure 7-3 shows the configuration of the transceiver block in the Libero SoC design suite. The following table lists the transceiver configuration.

Table 7-2. XCVR Configuration

Parameters	Settings
Number of lanes	1
Data Rate	1250 Mbps
PMA	
TX clock division factor	4
TX PLL base data rate	5000 Mbps
TX PLL bit clock frequency	2500 Mbps
CDR lock mode	lock to data
CDR reference clock source	Dedicated
CDR reference clock frequency	125 MHz
PCS	
PCS-fabric interface width	10 bits
FPGA interface frequency	125 MHz
PMA Mode	Enabled
Clocks and Resets	
TX clock	Regional
RX clock	Regional
PCS Reset	RX Only

Figure 7-3. Transceiver Configuration



7.3 Transceiver Connections (Ask a Question)

This section describes the typical transceiver to CoreTSE connections in BASE-T and BASE-X design.

The following table lists the transceiver input and output port connections.

Table 7-3. XCVR Port Connections

Port Name	Input or Output	Connection Description
CTRL_CLK	Input	40 MHz clock for the enhanced receiver management logic Can be sourced from the on-chip 160 MHz RC oscillator through a clock divider, or it can be connected to the output fabric clock of CCC.
CTRL_ARST_N	—	Input signal to reset ERM Drive this signal from the XCVR_INIT_DONE signal of the PF_INIT_MONITOR component.
CLKS_FROM_TX_PLL	—	XCVR transmit clock sourced from the TX PLL
LANE0_RXD_N LANE0_RXD_P	—	Differential receive input pads for receiving the Ethernet data
LANE0_CDR_REF_CLK	—	125 MHz reference for clock and data recovery
LANE0_PCS_ARST_N	—	Asynchronous active-low reset signal used to reset the PCS module of XCVR lane
LANE0_PMA_ARST_N	—	Asynchronous active-low reset signal used to reset the PMA module of XCVR lane
LANE0_RX_DATA [9:0]	—	The 10-bit RX data from XCVR to CoreTSE:RCG [9:0]
LANE0_TXD_N LANE0_TXD_P	—	Differential transmit output pads
LANE0_RX_CLK_R	—	Recovered regional receive clock from XCVR to the fabric logic and CoreTSE:TBI_RX_CLK
LANE0_TX_DATA [9:0]	—	The 10-bit TX data from CoreTSE:TCG [9:0] to XCVR

For other XCVR ports, see PolarFire FPGA and PolarFire SoC FPGA Transceiver User Guide.

8. Appendix 5: References (Ask a Question)

This section lists the documents that provide more information about the IP cores used in the 1G loopback demo design and about PolarFire 1G Ethernet Solutions in general.

- For more information about PF_IOD_CDR_CCC and PF_IOD_CDR, see PolarFire FPGA and PolarFire SoC FPGA User I/O User Guide
- For more information about CoreTSE, see *HB0549: CoreTSE Handbook* from the Libero SoC Catalog
- For more information about PF_CCC, see PolarFire FPGA and PolarFire SoC FPGA Clocking Resources User Guide
- For more information about PF_SRAM_AXI_AHBL, see PolarFire FPGA and PolarFire SoC FPGA Fabric User Guide
- For more information about CoreAHBLite, see *CoreAHBLite Handbook* from the Libero SoC Catalog
- For information about COREAHBTOAPB3, see *COREAHBTOAPB3 Handbook* from the Libero SoC Catalog
- For more information about CoreAPB3, see *CoreAPB3 Handbook* from the Libero SoC Catalog
- For more information about CoreUARTapb, see *CoreUARTapb Handbook* from the Libero SoC Catalog
- For more information about CoreSPI, see *HB0089: CoreSPI Handbook* from the Libero SoC Catalog
- For more information about PF_INIT_MONITOR, see PolarFire FPGA and PolarFire SoC FPGA Power-Up and Resets User Guide
- For more information about MIV_RV32, see *MIV_RV32 Handbook* from the Libero SoC Catalog
- For general information about PolarFire 1G Ethernet Solutions, see UG0687: PolarFire FPGA 1G Ethernet Solutions User Guide
- For more information about the PolarFire Evaluation board, see UG0747: PolarFire FPGA Evaluation Kit User Guide

9. Revision History (Ask a Question)

Revision	Date	Description
B	05/2023	The following is the list of changes in revision B of the document: • Updated the document for Libero® SoC v2022.3 • Updated Figure 1-2 • Updated Figure 1-3 • Updated Figure 1-4 • Updated Figure 1-7 and Figure 1-8 • Updated Figure 1-9 • Updated Figure 1-12 • Updated the design and `.job` filepath throughout the document
A	07/2022	The following is the list of changes in revision A of the document: • The document was migrated to the Microchip template. • The document number was updated to DS00004623 from 50200799. • Updated the document for Libero® SoC v2022.1
5.0	—	Added 5. Appendix 2: Running the TCL Script.
4.0	—	The following is a summary of the changes made in this revision. • Updated the document for Libero SoC v12.2. • Removed the references to Libero version numbers.
3.0	—	The following is a summary of changes made in this revision. • Updated the document for Libero SoC v12.1. • The design uses a new IP PF_IOD_CDR_CCC. For more information, see 1.3.3.8. PF_IOD_CDR_CCC_C0.
2.0	—	The following is a summary of changes made in this revision. • Updated the document for Libero® SoC v12.0. • Added 6. Appendix 3: Multi-Lane 1G IOD CDR Design. • Added 7. Appendix 4: 1G Ethernet BASE-T and BASE-X Using Transceiver.
1.0	—	This is the first publication of the document.

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