Configuring the ZL30151/ZL30169/ZL30182/ZL3024x/ZL3025x/ ZL3062x/ZL3072x for Optimum RMS Jitter Performance

Introduction

There are two types of devices reflected in this document. There are single channel devices (ZL30151, ZL30169, ZL30250, ZL30251, ZL30252, ZL30253, ZL30622, and ZL30722) and dual channel devices (ZL30182, ZL30244, ZL30245, ZL30255, ZL30623, and ZL30723). Each of the devices can offer up to four modes of operation: Frequency Synthesis (APLL only), Jitter Attenuation (DPLL+APLL), Numerically Controlled Oscillator (NCO), and Spread Spectrum (SS). For purposes of optimizing rms jitter, we are mainly concerned about the first three modes of operation. The ZL30621 and ZL30721 are not covered in this document. Information on how to optimize rms jitter can be found in their respective datasheets.

This document helps in optimizing jitter for a given mode of operation and master clock frequency. Additionally, this document describes how to minimize rms jitter for dual channel devices. Although the GUI of these devices automatically optimizes the device configuration for jitter performance, there is still much that is controlled outside of the GUI.

Jitter Optimization

Choosing an oscillator with low phase noise is necessary in achieving low jitter at the device output (see ZLAN-442 for recommended oscillators). There are also many other factors that affect the output rms jitter. These factors include oscillator type (crystal or XO), oscillator frequency, and mode of operation. These devices do not have a master clock multiplier APLL, but there is an on-chip clock doubler available. Choosing when to use the doubler also plays a role in the optimization of the rms jitter. The following three sections apply to both single and dual channel devices. The last section only applies to dual channel devices.

APLL-Only Mode

The best output rms jitter numbers are in APLL-only mode. In this mode, the XA input is not a master clock input but rather a fourth input reference similar to IC1 through IC3. The lowest acceptable frequency at the input (XA or ICx) is 9.72 MHz for this mode (DPLL+APLL mode goes lower). In general, the higher the input frequency, the lower the output jitter. For applications with output jitter requirements below 0.3 ps rms, an input frequency of 48 MHz or higher is recommended.

In APLL-only mode, the APLL can perform integer multiplication or fractional multiplication. For integer multiplication, the doubler typically is *not* recommended because the doubler generates a large spur that is not filtered by the APLL. In contrast, for APLL fractional multiplication, the doubler *is* recommended because the APLL filters the spur generated by the doubler. The APLL loop bandwidth is automatically optimized by the GUI for integer or fractional multiplication.

DPLL+APLL Mode

In this mode, the master clock required on the XA pin must fall in specific ranges:

- XO, doubler off: 93-130 MHz
- Crystal, doubler on: 46.5-60 MHz

The use of the doubler with an XO is not recommended in this mode.

The best jitter performance for DPLL+APLL mode is achieved with low-cost 93-130 MHz XOs. The on-chip doubler enables use of low frequency fundamental-mode crystals but with approximately 100 fs higher output jitter than when 93-130 MHz XOs are used.

NCO Mode

This mode is similar to the DPLL+APLL mode, except that the DPLL operates open-loop, controlled by software rather than locked to an ICx input clock.

The master clock required on the XA pin must fall in these specific ranges:

- XO, doubler off: 80-130 MHz (wider than DPLL+APLL mode because input sampler is not needed)
- XO, doubler on: 40-65 MHz
- Crystal, doubler on: 40-60 MHz

Dual Channel Devices only

Along with the three modes described above, dual channel devices also have the challenge of using two master clocks. This section describes how to provide an XO and/or crystal to the two channels of a dual channel device with the purpose of minimizing rms jitter.

1. Choosing two different frequencies for the master clock of each channel is recommended. If the frequency of both crystals/XOs is nominally the same, spurs may be present in the phase noise plots of the output signals. Spurs are present because the frequency is not exactly the same, but a few ppb to ppm different thereby causing mixing at the lower frequency offsets of a phase noise plot. Choosing frequencies such as 49.152 MHz and 50 MHz for example will push the spurs further away to negligible offsets such that the rms jitter is not affected.
2. Another option instead of the above is to use only one crystal/XO, but have one of the outputs of the first channel drive the master clock input of the second channel. This method assumes that there is an unused output from the first channel and that the output frequency can be configured to the frequency range of the second channel's master clock input.
3. The last option is to use one XO feeding both channels. This option, from the XO, requires careful routing that runs right across the first channel's XA pin without a stub and then over to the second channel's XA pin and has a 50 Ω shunt termination right at the second channel's XA pin. A 1:2 CMOS fanout buffer could instead be used, but this buffer must have low additive jitter because the output jitter of the ZL30xxx is a function of the master clock (XA) input jitter.

References

Microsemi ZLAN-442, "*Crystals and Oscillators for Next Generation Timing Solutions*", June 2014.

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