



HV7321
Ultrasound TX Pulser
Evaluation Board
User's Guide

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Derek Carlson
VP Development Tools

12-Sep-14
Date

NOTES:

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Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our website (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a “DS” number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is “DSXXXXXXXA”, where “XXXXXXX” is the document number and “A” is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the HV7321 Ultrasound TX Pulser Evaluation Board. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- Recommended Reading
- The Microchip Web Site
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document describes how to use the HV7321 Ultrasound TX Pulser Evaluation Board as a development tool to evaluate the HV7321 4-Channel 5-Level $\pm 80V$ 2.5A Ultrasound Transmit Pulser and the MD1730 8-Channel $\pm 6V$ Low-Noise CW Beamformer ICs. The manual layout is as follows:

- **Chapter 1. “Product Overview”** – Important information about the HV7321 Ultrasound TX Pulser Evaluation Board.
- **Chapter 2. “Installation and Operation”** – This chapter includes a detailed description of each function of the evaluation board and instructions on how to begin using the HV7321 Ultrasound TX Pulser Evaluation Board.
- **Chapter 3. “Software Description”** – This chapter explains the installation steps for installing the MUPB001 (Microchip Ultrasound Platform Board) GUI, provides an in-depth description of the elements of the MUPB001 GUI, and includes a step-by-step guide for generating signals at the HV7321 output.
- **Chapter 4. “PCB Design and Layout Notes”** – This chapter explains important points of PCB design and layout of high voltage ultrasound systems.

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- **Appendix A. “Schematic & Layouts”** – Shows the schematic and PCB layout diagrams for the HV7321 Ultrasound TX Pulser Evaluation Board and for the MUPB001.
- **Appendix B. “Bill of Materials (BOM)”** – Lists the parts used to build the HV7321 Ultrasound TX Pulser Evaluation Board and the MUPB001.
- **Appendix C. “HV7321 Ultrasound TX Pulser Evaluation Board Typical Waveforms”** – Describes the various demonstration waveforms for the HV7321 Ultrasound TX Pulser Evaluation Board.

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	<i>MPLAB® IDE User's Guide</i>
	Emphasized text	...is the <i>only</i> compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	<u><i>File>Save</i></u>
Bold characters	A dialog button	Click OK
	A tab	Click the Power tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	#define START
	Filenames	autoexec.bat
	File paths	c:\mcc18\h
	Keywords	_asm, _endasm, static
	Command-line options	-Opa+, -Opa-
	Bit values	0, 1
	Constants	0xFF, 'A'
Italic Courier New	A variable argument	<i>file.o</i> , where <i>file</i> can be any valid filename
Square brackets []	Optional arguments	mcc18 [options] <i>file</i> [options]
Curly brackets and pipe character: { }	Choice of mutually exclusive arguments; an OR selection	errorlevel {0 1}
Ellipses...	Replaces repeated text	var_name [, var_name...]
	Represents code supplied by user	void main (void) { ... }

RECOMMENDED READING

This user's guide describes how to use HV7321 Ultrasound TX Pulser Evaluation Board. Other useful documents are listed below. The following Microchip documents are available and recommended as supplemental reference resources:

- **HV7321 Data Sheet - “HV7321 - 4-Ch. 5-Level $\pm 80V$ High-Voltage Ultrasound Pulser with T/R Switches” (DS20005639)**
- **MD1730 Data Sheet - “High Speed 8-Channel Ultra-Low Phase Noise Continuous Waveform Transmitter with Beamformer” (DS200005586)**

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- Field Application Engineer (FAE)
- Technical Support

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Technical support is available through the web site at:
<http://www.microchip.com/support>.

DOCUMENT REVISION HISTORY

Revision A (October 2016)

- Initial release of this document.

Revision B (November 2016)

The following is the list of modifications:

- Updated [Appendix B. “Bill of Materials \(BOM\)”](#).
- Minor typographical corrections.

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Chapter 1. Product Overview

1.1 INTRODUCTION

The HV7321 Ultrasound TX Pulser Evaluation Board (ADM00659) works with Microchip Technology Inc.'s Ultrasound Platform Board (ADM00679) to provide a 4-Channel, 5-Level, $\pm 80V$, 2.5A ultrasound transmit pulser demonstration platform including a very low phase noise, 8-Channel $\pm 6V$ CW beamforming waveform generator. The HV7321 Ultrasound TX Pulser Evaluation Board features one HV7321 IC and one MD1730 IC used as a 4-channel CW waveform generator.

1.2 HV7321 IC – DESCRIPTION

The HV7321 is a 4-Channel, 5-Level, $\pm 80V$, 2.5A ultrasound transmit pulser with integrated transmit/receive switches. It is designed for medical ultrasound imaging, non-destructive testing (NDT) and other transducer drive applications.

The output transistors can provide up to $\pm 2.5A$ of current at $\pm 80V$ in Brightness mode (B-mode) and ± 300 mA current in Continuous Wave Doppler mode (CW mode). In CW mode-0 (MODE = PWS = 0), V_{PP1}/V_{NN1} voltage rails are used and the output current is ± 300 mA. This reduces the power dissipation on the chip in CW Mode-0.

The HV7321 also integrates 20Ω T/R and RX damp switches in each channel. 500Ω auto bleeding switches are used for true-zero voltage and minimizing the received noise.

The 220 MHz clock re-timing capability provides low jitter in CWD, PW or B-mode. The clock synchronization realigns the logic input signals to a master clock that reduces various propagation delays caused by FPGA inaccuracies and/or by long PCB traces.

The built-in gate driver floating voltage regulators of the IC provide V_{PP} and V_{NN} high-voltage rails changing interdependently or freely from 0 to $\pm 80V$. Output voltage overshoot clamping diodes clamp to the highest level of the supply pin of V_{PP0} or V_{NN0} respectively. The control inputs ($+2.5/+3.3V$ voltages) are designed to work with FPGA or LVC MOS logic families directly.

The built-in high-voltage CW pulser switches enable the use of external low-voltage CW generators with much better phase CW waveform source.

1.3 MD1730 IC – DESCRIPTION

The MD1730 is an 8-channel low-phase noise CW transmitter with programmable phase delay used for CW beamforming.

The MD1730 is designed for high-end ultrasound imaging systems. In CW Mode-1, the MD1730's 8-channel CW output signals can directly drive two HV7321 external CW inputs (CWIN) through the built-in high-voltage analog switches to drive the probe transducer elements.

The frequency and phase delay of MD1730 outputs can be programmed via a SPI interface. High-speed SPI read/write enables the CW focusing feature.

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In CW mode, dedicated CW signal paths are designed to minimize jitter and phase noise. The CW outputs can have up to $\pm 6V$ voltage swing. Each CW output has a separate programmed phase delay time value. If the CW frequency is set at 5 MHz, the phase delay step size is 6.25 ns, an angular resolution of 11.25° increments when CLK frequency is 160 MHz.

The MD1730 also features two clock output buffers that can drive two HV7321 ICs with single-ended synchronization clock inputs up to 220 MHz.

1.4 HV7321 ULTRASOUND TX PULSER EVALUATION BOARD – FEATURES

- Four channels of HV7321 ultrasound transmitters
- Designed to work with Microchip Ultrasound Platform Board (MUPB001)
- 5-level voltage pulse waveforms outputs
- Dual rails pair of V_{PP0}/V_{NN0} and V_{PP1}/V_{NN1} up to $\pm 80V$ high voltages
- On-board 220 pF/1K dummy load per channel
- $\pm 2.5A$ source and sink current capability
- Built-in active return-to zero (RTZ) MOSFETs
- Built-in high-voltage analog damp switches for “true-zero” RTZ.
- On-board wide band op amp LNA emulation circuits for T/R switch outputs
- Re-timing clock on-board option sources up to 200 MHz frequency
- Fully programmable waveform generation from PC GUI via the MUPB001 board
- Connection-ready for external sync/trigger/clock signals
- On-board 5V-to-2.5V conversion LDO for V_{LL} supply

1.5 HV7321 ULTRASOUND TX PULSER EVALUATION BOARD AND MUPB001 – FUNCTIONAL DESCRIPTION

The HV7321 Ultrasound TX Pulser Evaluation Board can drive transducers as a 5-level and 4-channel transmitter for ultrasound imaging applications and NDT systems. The evaluation board features one HV7321-G 9 x 9 mm 64-lead VQFN packaged integrated circuit and one MD1730 6 x 6 mm 36-lead VQFN packaged integrated circuit.

The board uses two high-speed 20 signal pair carrying capable right-angle backplane connector, which is designed to work with Microchip Ultrasound Platform Board (MUPB001) (ADM00679) as the control signal source.

The MUPB001 has a FPGA, used for demo waveform generation, and a USB-bridge IC that connects the MUPB001 to a PC. By means of a Microsoft® Windows® driver and GUI, the user can generate many optional waveforms and choose several modes to evaluate the ultrasound-imaging transmit-pulser, including the FPGA re-programmable features.

The on-board timing clock management IC allows flexible clock frequency selection. The user can select different clock frequencies using the MUPB001 built-in clock source via GUI, or activate the LVDS output clock oscillator on the HV7321 Ultrasound TX Pulser Evaluation Board by installing 0Ω resistors at the output of the IC oscillator. The LVDS signal is used solely by the MD1730.

These clock frequencies can be further utilized via the on-board clock buffer to drive the single-ended re-timing clock input CLK on the HV7321 if FPGA timing logic inputs are not desired.

The additional buffer on MD1730 can also be used to let the FPGA clock system synchronized with the target evaluation board.

On connectors J5 and J23 there are additional uncommitted pins available to further customize the synchronization or the use of triggers signals. If the HV7321 Ultrasound TX Pulser Evaluation Board is connected to the MUPB001, these signals are all

connected to the FPGA I/O/clock pins. The users can connect the board to their own control signal source or system via the high-speed backplane connectors J5 and J23 (see Figure 1-1).

The HV7321 has built-in T/R switches per channel. Received signals at the output of the T/R switches can be evaluated by using the output (LNAOUT test point on board) of the wide-band transimpedance op-amp. The desired T/R switch output is connected to the op-amp input via jumper. The op-amp has active termination load that emulates the LNA (Low Noise Amplifier) input impedance similar to the one in receiver AFE (Active Front End) Circuit.

There are seven color LEDs on the HV7321 Ultrasound TX Pulser Evaluation Board to indicate the input control signal states.

Jumpers close to SMA connectors are for connecting the on-board dummy R-C load (220 pF//1K) optionally to the transmit (TX) output.

The 220 MHz clock re-timing capability provides low jitter in CWD (Continuous Wave Doppler), PW or B-mode. The clock synchronization realigns the logic input signals to a master clock that reduces various propagation delays caused by FPGA inaccuracies and/or by long PCB traces.

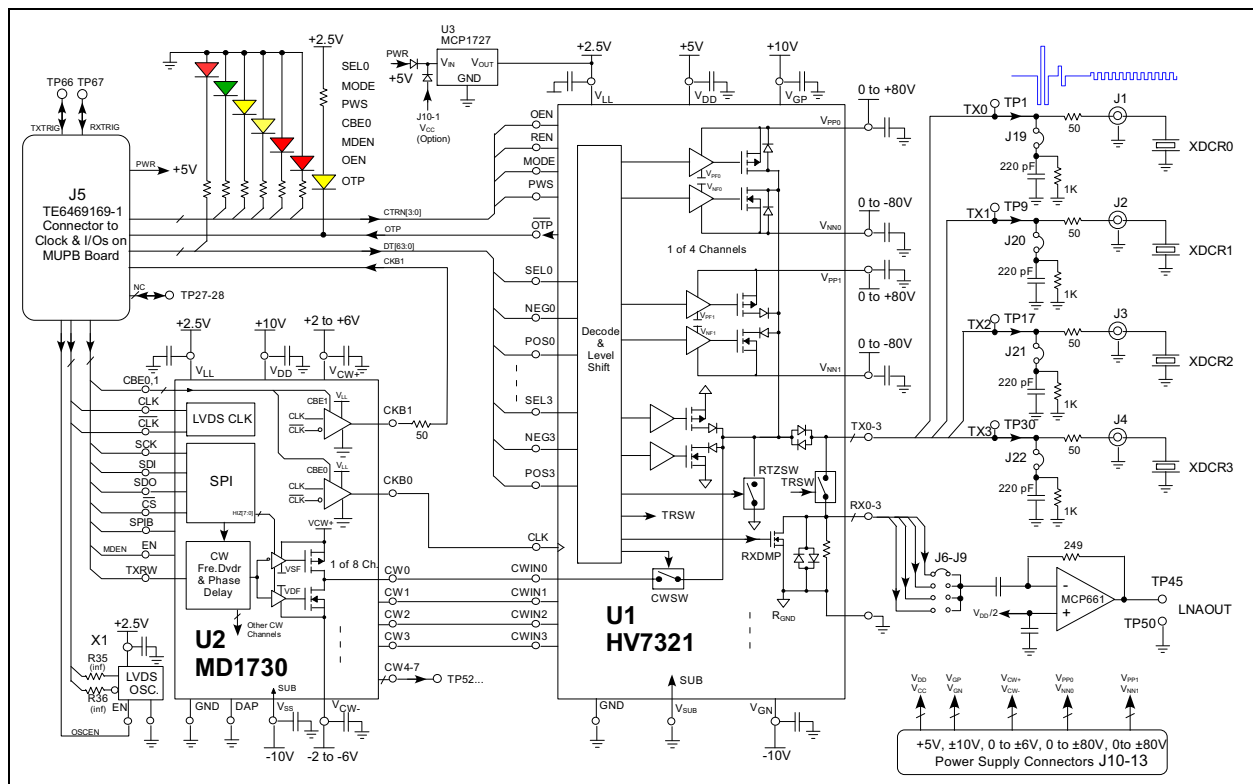


FIGURE 1-1: HV7321 Ultrasound TX Pulser Evaluation Board - Simplified Block Diagram.

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1.6 HV7321 ULTRASOUND TX PULSER EVALUATION BOARD – TECHNICAL SPECIFICATIONS

Parameter	Value
Modes of Operation	B, PW, CW
B-Mode Output Pulses Peak Voltage and Current (SEL = 0)	up to $\pm 80V$ and $\pm 2.5A$ typical
B-Mode Output Pulses Peak Voltage and Current (SEL = 1)	up to $\pm 80V$ and $\pm 2.0A$ typical
CW Output Peak Voltage and Current (MODE = 1)	0 to $\pm 6V$ and ± 800 mA typical. Use CW_{IN0-3} and MD1730
CW Output Peak Voltage and Current (MODE = 0, PWS = 0)	0 to $\pm 6V$ and ± 700 mA typical. Use V_{PP1}/V_{NN1} CW
HV7321 Re-timing Clock Input Frequency	200 MHz max. LVCMOS 2.5V
MD1730 CW Clock Input Frequency	250 MHz max. LVDS/SSTL 2.5/LVCMOS 2.5V
Low-Phase Noise CW Test LVDS Clock Oscillator	Options included
Interface of FPGA Control Signals and USB PC-GUI Software	J5 and J23 Connects to MUPB001 (ADM00679) Interface Board
Logic circuitry 2.5V V_{LL} Voltage Supply LDO Regulator	Built-in, with optional voltage source from MUPB001/J10
TX R-C Test-Load and User Transducer Interface	Built-in, 220 pF//1K per channel with jumper and 50 Ω SMA
On-Board LED Indicator of Signals	SEL0, MODE, PWS, CBE0, MDEN, OEN and OTP
Overtemperature Protection	Overtemperature Protection open-drain output to J5 to MUPB001 included
Floating Gate Driver Voltage Regulators and UVLO	Built-in regulators in HV7321 and MD1730 w/ UVLO
PCB Board Dimensions	127 x 102 mm (5.0 x 4.0 inch)

1.7 DEVICE SUMMARY

The HV7321 Ultrasound TX Pulser Evaluation Board demonstrates the following Microchip products on board:

- HV7321, 4-Channel 5-Level $\pm 80V$ 2.5A Ultrasound Transmit Pulser
- MD1730, 8-Channel, $\pm 6V$ Low-Noise CW Beamformer

The evaluation board also uses the additional IC:

- MCP1727, 1.5A Low-Voltage, Low-Quiescent Current LDO Regulator

1.8 WHAT THE HV7321 ULTRASOUND TX PULSER EVALUATION BOARD KIT INCLUDES

The HV7321 Ultrasound TX Pulser Evaluation Board kit includes:

- HV7321 Ultrasound TX Pulser Evaluation Board (ADM00659)
- Important Information Sheet

Chapter 2. Installation and Operation

2.1 GETTING STARTED

The HV7321 Ultrasound TX Pulser Evaluation Board is fully assembled and tested. For basic waveforms generation the board requires five power supply voltage rails of +5V, $\pm 10V$ and $\pm 80V$. Nine power supply voltage rails are necessary for the full functional demonstration: +5V, $\pm 10V$, 0 to $\pm 6V$, 0 to $\pm 50V$, and 0 to ± 80 . It is strongly recommended that these power supply sources feature adjustable current-limit functions.

2.1.1 Additional Tools Required for Operation

The HV7321 Ultrasound TX Pulser Evaluation Board also requires:

1. an oscilloscope with minimum 500 MHz BW and two high-impedance probes
 - make sure the grounds of the power supply sources are correctly connected to the same ground as the testing oscilloscope ground

In order to demonstrate the HV7321 Ultrasound TX Pulser Evaluation Board waveforms and features, the following additional tools are required:

2. a Microchip Ultrasound Platform Board (MUPB001) (ADM00679)
3. a Microsoft Windows® 7 PC that has the Microchip Ultrasound Platform Board evaluation driver and running the HV7321 Ultrasound TX Pulser Evaluation Board GUI software
 - connect J5 and J23 on the HV7321 Ultrasound TX Pulser Evaluation Board (see [Figure 2-1](#)) to the MUPB001 FPGA control-board
 - connect the MUPB001 FPGA control-board via USB to the Windows-7 PC (see [Figure 2-2](#))

Download the latest ultrasound platform evaluation driver and GUI software from the Microchip website at www.microchip.com.

2.2 SETUP PROCEDURE

To operate the HV7321 Ultrasound TX Pulser Evaluation Board, the following steps must be followed:

1. connect J5 and J23 ([Figure 2-1](#)) to a Microchip Ultrasound Platform Board (MUPB001) (ADM00679) ([Figure 2-2](#)).
2. connect all HV7321 Ultrasound TX Pulser Evaluation Board jumpers on J6, J15, J19, J20, J21 and J22 for the R-C load. See [Figure 2-1](#).
3. connect all power supplies to the voltage supply input connectors J10, J11, J12 and J13 as indicated in [Table 2-1](#) by observing the polarity. See [Figure 2-1](#).

TABLE 2-1: POWER SUPPLY VOLTAGES AND CURRENT-LIMIT SETTINGS

Terminal	Rail Name	Voltage	Average-Current Limit
J10-1	V_{CC}/PWR	+5V	+50 mA
J10-2	V_{DD}	+5V	+20 mA
J10-3	V_{GN}	-10V	-30 mA
J10-4	GND	0V	—

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TABLE 2-1: POWER SUPPLY VOLTAGES AND CURRENT-LIMIT SETTINGS (CONTINUED)

Terminal	Rail Name	Voltage	Average-Current Limit
J10-5	GND	0V	—
J10-6	V _{GP}	+10V	+30 mA
J11-1	V _{CW+}	0 to +6V	+200 mA
J11-2	GND	0V	—
J11-3	V _{CW-}	0 to -6V	-200 mA
J12-1	V _{PP0}	0 to +80V	+5 mA
J12-2	GND	0V	—
J12-3	V _{NN0}	0 to -80V	-5 mA
J13-1	V _{PP1}	0 to V _{PP0}	+5 mA

WARNING

Observe the polarity of each power supply rail and set the voltage and current limit carefully. Note that $\pm 80V$ is the maximum limit for V_{PP0}/V_{NN0}. V_{PP1}/V_{NN1} voltages have to be equal or within V_{PP0}/V_{NN0} voltage range.

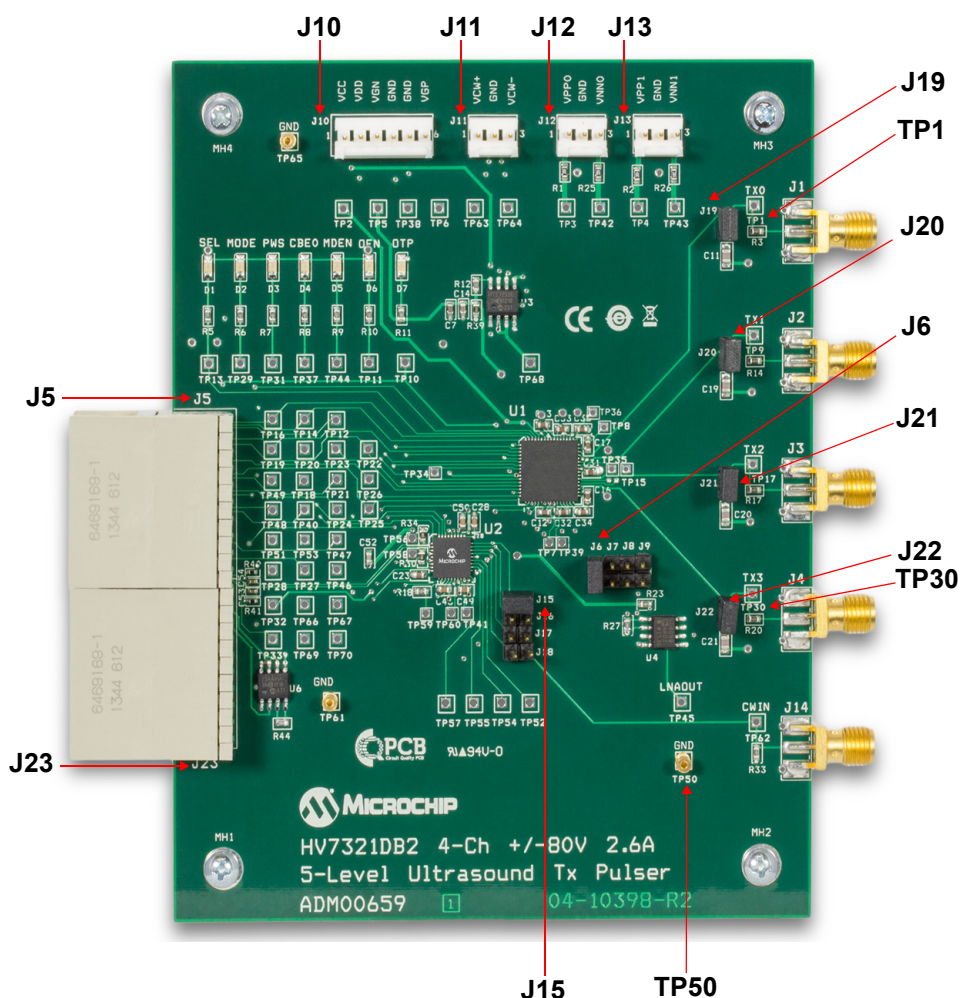


FIGURE 2-1: HV7321 Ultrasound TX Pulser Evaluation Board – Front View.

4. turn on the HV7321 Ultrasound TX Pulser Evaluation Board V_{DD} +5V and the MUPB001 V_{DD} +5V
5. connect the MUPB001 USB cable to the PC (see [Section 2.5](#)). Make sure the MUPB001 software driver is installed correctly and the MUPB001 USB connection to the PC is established.
6. run the MUPB001 GUI software. Check that the LEDs on the HV7321 Ultrasound TX Pulser Evaluation Board are under PC user interface control. Set OEN LED off.
7. turn on $V_{GP}/V_{GN} \pm 10V$, $V_{PP0}/V_{NN0} \pm 25V$ and $V_{PP1}/V_{NN1} \pm 15V$
8. connect the oscilloscope probe ground lead to TP50, apply the probe tip to TP1 or TP30 with the scope trigger source set to the probe and the trigger-level to DC +5V; set the scanning time base to 200 ns per division.
9. enable the TX Pulsed-Echo mode in the GUI to evaluate the waveforms (see [Section 3.4.11](#))
10. if it is necessary to increase the V_{PP}/V_{NN} voltage, adjust the V_{PP0}/V_{NN0} in small increments up to $\pm 80V$ maximum, with the current limiting on

2.2.1 Recommended power-up and power-down sequences

[Table 2-2](#) shows the recommended power-up sequence of the HV7321 Ultrasound TX Pulser Evaluation Board.

Note: Powering the HV7321 Ultrasound TX Pulser Evaluation Board up/down in any arbitrary sequence will not cause any damage to the device. The power up/down sequences in table below are only recommended in order to minimize possible inrush current.

TABLE 2-2: BOARD POWER-UP AND POWER-DOWN SEQUENCES

Step	Power-Up Sequence	Step	Power-Down Sequence
1	V_{LL} on with logic signal low	1	OEN and logic control signal go low
2	V_{DD} , V_{GP} and V_{GN} ON	2	$V_{PP0,1}$ and $V_{NN0,1}$ OFF
3	REN = 1	3	REN = 0
4	$V_{PP0,1}$ and $V_{NN0,1}$ ON	4	V_{DD} , V_{GP} and V_{GN} OFF
5	OEN = 1 and logic control signal active	5	V_{LL} OFF

2.3 INTERFACE CONNECTIONS

[Table 2-3](#) shows the board J5 control interface signals.

TABLE 2-3: J5 CONTROL INTERFACE SIGNALS

Pin #	Name	Test Point	I/O Type	Signal Discretion
J5-A1	PWR	TP68 ⁽¹⁾	+5V Power Input	External +5V power supply via diode D8B to LDO U3 for V_{LL} only
J5-B1	PWR	TP68 ⁽¹⁾	+5V Power Input	
J5-C1	V_{LL} ⁽¹⁾	TP5	2.5V Pull Up	Connected to R39 1K resistor pull-up to +2.5V V_{LL}
J5-D1	OTP	TP10	Open Drain Output	OTP U1-20 HV7321 w/ 200 Ω & LED to +2.5V V_{LL}
J5-A2	NEG0	TP16	LVC MOS-2.5V Input	NEG0 control input pin for U1 HV7321 Channel-0
J5-B2	POS0	TP14	LVC MOS-2.5V Input	POS0 control input pin for U1 HV7321 Channel-0
J5-C2	OEN	TP11	LVC MOS-2.5V Input	Output enable input pin for U1 HV7321
J5-D2	REN	TP12	LVC MOS-2.5V Input	Gate-Regulator enable input pin for HV7321
J5-A3	NEG1	TP19	LVC MOS-2.5V Input	NEG1 control input pin for U1 HV7321 Channel-1

Note 1: Connected indirectly with in-series resistor or capacitor. For more details, refer to [Appendix A. "Schematic & Layouts"](#).

HV7321 Ultrasound TX Pulser Evaluation Board User's Guide

TABLE 2-3: J5 CONTROL INTERFACE SIGNALS (CONTINUED)

Pin #	Name	Test Point	I/O Type	Signal Discretion
J5-B3	POS1	TP20	LVC MOS-2.5V Input	POS1 control input pin for U1 HV7321 Channel-1
J5-C3	NEG2	TP22	LVC MOS-2.5V Input	NEG2 control input pin for U1 HV7321 Channel-2
J5-D3	POS2	TP23	LVC MOS-2.5V Input	POS2 control input pin for U1 HV7321 Channel-2
J5-A4	SEL0	TP13	LVC MOS-2.5V Input	SEL0 control input pin for U1 HV7321 Channel-0
J5-B4	SEL1	TP18	LVC MOS-2.5V Input	SEL1 control input pin for U1 HV7321 Channel-1
J5-C4	NEG3	TP25	LVC MOS-2.5V Input	NEG3 control input pin for U1 HV7321 Channel-3
J5-D4	POS3	TP26	LVC MOS-2.5V Input	POS3 control input pin for U1 HV7321 Channel-3
J5-A5	SEL2	TP21	LVC MOS-2.5V Input	SEL2 control input pin for U1 HV7321 Channel-2
J5-B5	SEL3	TP24	LVC MOS-2.5V Input	SEL3 control input pin for U1 HV7321 Channel-3
J5-C5	MODE	TP29	LVC MOS-2.5V Input	MODE pin of HV7321, if Hi, CWIN[3:0] & MD1730 used
J5-D5	PWS	TP31	LVC MOS-2.5V Input	PWS pin of HV7321, if Lo, use V_{PP1}/V_{NN1} for CW
J5-A6	SCK	TP48	LVC MOS-2.5V Input	SCK pin, SPI interface clock of U2 MD1730
J5-B6	$\overline{CS}$	TP49	LVC MOS-2.5V Input	SCK pin, SPI interface chip-select of U2 MD1730
J5-C6	MDEN	TP44	LVC MOS-2.5V Input	EN pin, chip-enable of U2 MD1730, if Lo, CW[7:0] Hi-Z
J5-D6	SPIB	TP46	LVC MOS-2.5V Input	SPIB SPI broadcasting-mode enable of U2 MD1730
J5-A7	SDI	TP51	LVC MOS-2.5V Input	SDI pin, SPI interface clock of U2 MD1730
J5-B7	SDO	TP53	LVC MOS-2.5V Output	SDO pin, SPI data output from U2 MD1730
J5-C7	CBE0	TP37	LVC MOS-2.5V Input	Clock Buffer-0 enable input pin on U2 MD1730
J5-D7	CBE1	TP40	LVC MOS-2.5V Input	Clock Buffer-1 enable input pin on U2 MD1730
J5-A8	TXTRIG	TP66	LVC MOS-2.5V I/O	FPGA TX launch trigger signal input or output of MUPB
J5-B8	RXTRIG	TP67	LVC MOS-2.5V I/O	FPGA RX mode trigger signal input or output of MUPB
J5-C8	TXRW	TP47	LVC MOS-2.5V Input	CW transmit or SPI read/write control of U2 MD1730
J5-D8	CKB1	TP59 ⁽¹⁾	LVC MOS-2.5V Output	Clock Buffer-1 output from U2 MD1730
J5-A9	NC	NA	LVC MOS-2.5V Input	Not used by the PCB
J5-B9	NC	NA	LVC MOS-2.5V Input	Not used by the PCB
J5-C9	TP27	TP27	LVC MOS-2.5V Input	Connected to TP27 on the PCB
J5-D9	TP28	TP28	LVC MOS-2.5V Input	Connected to TP28 on the PCB
J5-A10	OSCEN	TP32	LVC MOS-2.5V Input	On-board crystal oscillator X1 enable signal
J5-B10	SYNC	TP33	LVC MOS-2.5V Input	Via R31 (INF) to CLK pin of HV7321 as a clock option
J5-C10	CLK_N ⁽¹⁾	TP58 ⁽¹⁾	LVDS / SSTL2.5 Input	LVDS clock input from MUPB001 to U2 MD1730 CLK
J5-D10	CLK_P ⁽¹⁾	TP56 ⁽¹⁾	LVDS / SSTL2.5 Input	LVDS clock input from MUPB001 to U2 MD1730 CLK
J5-xGx	GND	TP50,61,65	Ground / 0V / Return	Ground, 0V reference, shielding or PWR supply return

Note 1: Connected indirectly with in-serial resistor or capacitor. For more details, refer to [Appendix A. "Schematic & Layouts"](#).

2.4 OPERATING THE HV7321 ULTRASOUND TX PULSER EVALUATION BOARD

Refer to [Appendix C. “HV7321 Ultrasound TX Pulser Evaluation Board Typical Waveforms”](#) for HV7321 Ultrasound TX Pulser Evaluation Board typical waveforms and voltages.

2.4.1 B-Mode Multi-Level TX Pulser Operation (PWS = 1, MODE = 0)

In B-Mode multi-level ultrasound transmit pulse generation, the user can select the following options or combinations of options, using a MUPB001 connected to a PC via USB and running the dedicated GUI. These are the options available:

1. ultrasound waveform frequency, fixed frequency 1 to 20 MHz with step of 100 kHz
2. number of half cycles in TX launch burst, from 2 to 16
3. change launch burst Pulse Repetition Frequency (Line Duration) from 5 kHz to 20 kHz, or an interval of 50 to 200 μ s
4. change the half-cycle polarity: positive first only, negative first only, or alternating between positive first and negative first
5. change the V_{PP0}/V_{NN0} and V_{PP1}/V_{NN1} pluses pair order in the launch burst
6. change the pulse(s) damping condition: pulse(s) followed by return-to-zero (RTZ) or not
7. change the receive time (RX-time) T/R switch(es) condition: RTZ, RTZ+, or high Z
8. change the number of levels: 2-level, 3-level or 5-level operation
9. change the duty cycle of pulses: PWM% or Pulse Width with a range of 2 ns to 500 ns according to the frequency of the pulse(s)
10. change the peak voltages of the pulse(s) by changing the V_{PP} and V_{NN} rail supply voltages.

2.4.2 CW Mode-0 Using Voltage of V_{PP1}/V_{NN1} Rails Operation (PWS = 0, MODE = 0, SEL = 1)

Connecting the HV7321 Ultrasound TX Pulser Evaluation Board to a MUPB001 linked to a PC via USB, and running the dedicated MUPB001 GUI allows the user to use the V_{PP1}/V_{NN1} voltage rail with reduced voltages and currents in CW Mode-0. The conditions for this mode of operation are: V_{PP1}/V_{NN1} must be between 0 to ± 6 V, PWS = 0, and MODE = 0. The following options become available:

1. CW Doppler mode waveform frequency, fixed frequency 1 to 7 MHz with step of 100 kHz
2. selection of the CW frequency source: the MUPB001 built-in clock-generator or the low-phase noise crystal-oscillator X1 on the HV7321 Ultrasound TX Pulser Evaluation Board via the MD1730 clock-buffer to re-time synchronize with the FPGA CW waveforms from POS/NEG with SEL = 1
3. changing the CW Doppler mode waveform peak-to-peak voltages by adjusting V_{PP1}/V_{NN1} supply rail voltages.

Note: Normal ranges are within 2 to 6V peak-to-peak at TX3:0 outputs. Higher voltages may overheat the IC(s) and/or components on the PCB, and may even damage them permanently.

2.4.3 Low Phase-Noise CW Beamforming Operation via CWSW and MD1730, Supplied by V_{CW+}/V_{CW-} Rails (PWS = 1, MODE = 1)

In CW Mode-1, the CW Beamforming mode features lower phase-noise by using the built-in high-voltage analog switch in the HV7321. In this mode, the low-voltage CW waveform generator sends the lower phase-noise CW waveforms with a predefined beamforming phase delay.

The CW waveform peak-to-peak voltage swing is defined by the voltage supply rail of V_{CW+}/V_{CW-} on the MD1730. The voltage range of the V_{CW+}/V_{CW-} is 0 to $\pm 6V$, with PWS = 1 and MODE = 1 control conditions. By using a MUPB001 connected to a PC via USB and by running the dedicated GUI, the user has access to these options:

1. CW beamforming (CW Mode-1) waveform frequency, frequency 1 to 8 MHz with step of 100 kHz, generated by programming the CW frequency divider number CWFD[7:0] in the MD1730 SPI register via the MUPB001 PC GUI
2. programming the beamforming phase delay PHDCH[7:0] to define the relative phase delay between channels of the CW waveforms
3. selecting the channel (or channels) set in Doppler receiving mode, by programming the bits of HIZCH in the MD1730 SPI register
4. selection of the CW frequency source: the MUPB001 built-in clock-generator or the low-phase noise crystal-oscillator X1 on the HV7321 Ultrasound TX Pulser Evaluation Board via the MD1730 built-in CW frequency divider
5. changing the CW Doppler mode waveform peak-to-peak voltages by adjusting the V_{CW+}/V_{CW-} supply rail voltages.

Note: Normal ranges are within 2 to 6V peak-to-peak at TX3:0 outputs. Higher voltages may overheat the IC(s) and/or components on the PCB, and may even damage them permanently.

Note: Typical voltages and waveforms are provided in [Appendix C. “HV7321 Ultrasound TX Pulser Evaluation Board Typical Waveforms”](#).

2.5 MICROCHIP ULTRASOUND PLATFORM BOARD (MUPB001)

The MUPB001 is used to generate the control signals for the HV7321 Ultrasound TX Pulser Evaluation Board. It features a flexible ultra-low jitter clock synthesizer and a Spartan-6 XC6SLX9 FPGA.

2.5.1 Connecting the MUPB001 to the PC – Setup Procedure

1. Before connecting the MUPB001 to the PC, make sure that:
 - the latest FPGA code on the platform flash of the MUPB001 FPGA is configured ([Section 3.1](#))
 - the latest GUI is installed and running on the PC (see [Section 3.3](#)).
2. With FPGA code configured and the GUI installed, connect the USB cable between the MUPB001 and the PC. Connect J5 and J23 of the HV7321 Ultrasound TX Pulser Evaluation Board (see [Figure 2-1](#)) to J1 and J2 of the MUPB001 (see [Figure 2-2](#)).
3. Start the GUI. On the bottom left of the status bar a “Not Connected” message is displayed in red (see [Section 3.4.16](#)).
4. Connect the appropriate power supply and turn on the power switch to power up the MUPB. LD1 and DC_IN (LD2) on the MUPB001 should light up green. A “Connected” message should be displayed in green on the bottom left of the status bar GUI (see [Section 3.4.16](#)).

The MUPB001 is now configured and ready to control the HV7321.

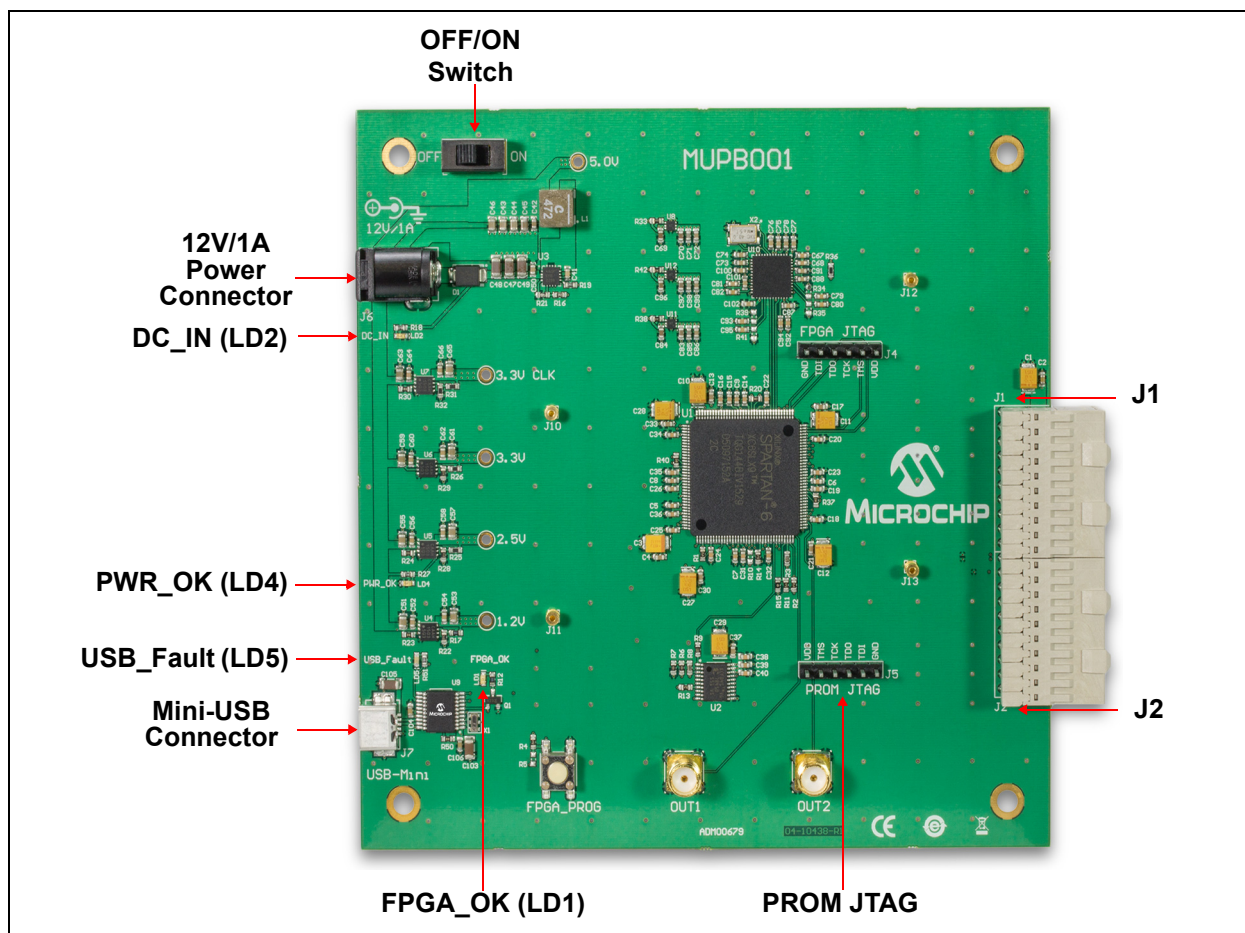


FIGURE 2-2: Microchip Ultrasound Platform Board (MUPB001).

HV7321 Ultrasound TX Pulser Evaluation Board User's Guide

NOTES:

Chapter 3. Software Description

3.1 FPGA CODE CONFIGURATION

Connect the +12V power connector to the Microchip Platform Ultrasound Board (MUPB001) and make sure that the green DC_IN LED is ON, indicating that the power connection is successful.

Turn on the power switch of the MUPB001 and make sure that PWR_OK LED is ON, and that the USB_Fault LED (red) flashes one time. If the USB_Fault LED remains lit, that is an indication that the USB cable is not connected and/or the Windows® operating system did not recognize the USB bridge.

Make sure that the FPGA_OK LED of the MUPB001 is ON. This is an indication that the FPGA code is configured (see [Figure 2-2](#)).

If the FPGA is not configured, or the user wants to modify the FPGA code, it is necessary to configure the FPGA platform flash PROM. The tools needed for FPGA platform flash PROM flash configuration are:

- Xilinx Platform cable USB II: This is a piece of hardware that is sold separately from this evaluation kit. It connects to a PC via USB cable and to the MUPB001 J5 connector via JTAG cables.
- iMPACT tool embedded in Xilinx ISE Project Navigator: Xilinx ISE Project Navigator is the development environment for Xilinx products. It can be downloaded free of charge from the Xilinx web site. iMPACT is the name of the module in Xilinx ISE Project Navigator that provides the configuration of .mcs file to platform flash PROM.
- the .mcs file is the extension of FPGA code files that are synthesized and specifically formatted for Xilinx platform flash PROM configuration.

The code resides in Xilinx platform flash PROM. The platform flash PROM loads the code to FPGA when the system is powered up.

3.2 GETTING STARTED

Download the latest ultrasound platform evaluation driver and GUI software from the Microchip website at <http://www.microchip.com> and install the MUPB001 – HV7321_MD1730 GUI by following the instructions in [Section 3.3](#).

3.3 MUPB001 – HV7321_MD1730 GUI INSTALLATION

The MUPB001 – HV7321_MD1730 GUI software installer can be downloaded from the Microchip web site at <http://www.microchip.com>. Search for the evaluation board on the web site by part number ADM00679. The GUI can be downloaded from the board web page.

1. Open the MUPB001GUI-v.1.0.0-windows-installer.exe. The MUPB001 – HV7321_MD1730 GUI software installer will initiate by launching the **Application Install** dialog box. Click **Next** to start the installation.

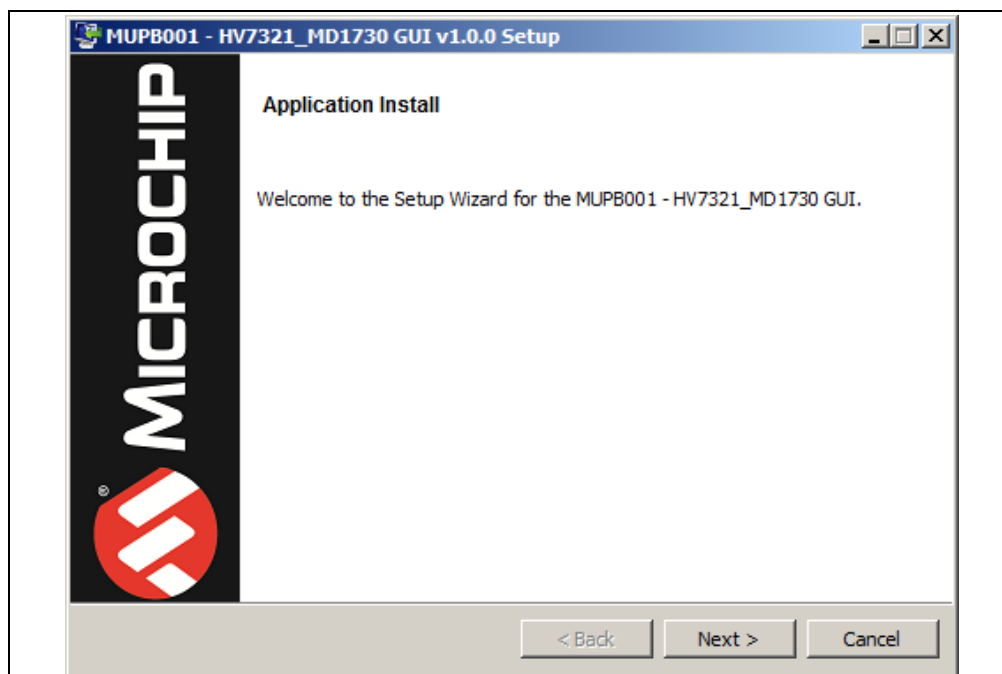


FIGURE 3-1: MUPB001 GUI – Application Install Dialog Box.

2. To proceed with the installation, read the License Agreement and accept by clicking the radio button corresponding to "I accept the agreement", then click **Next**.

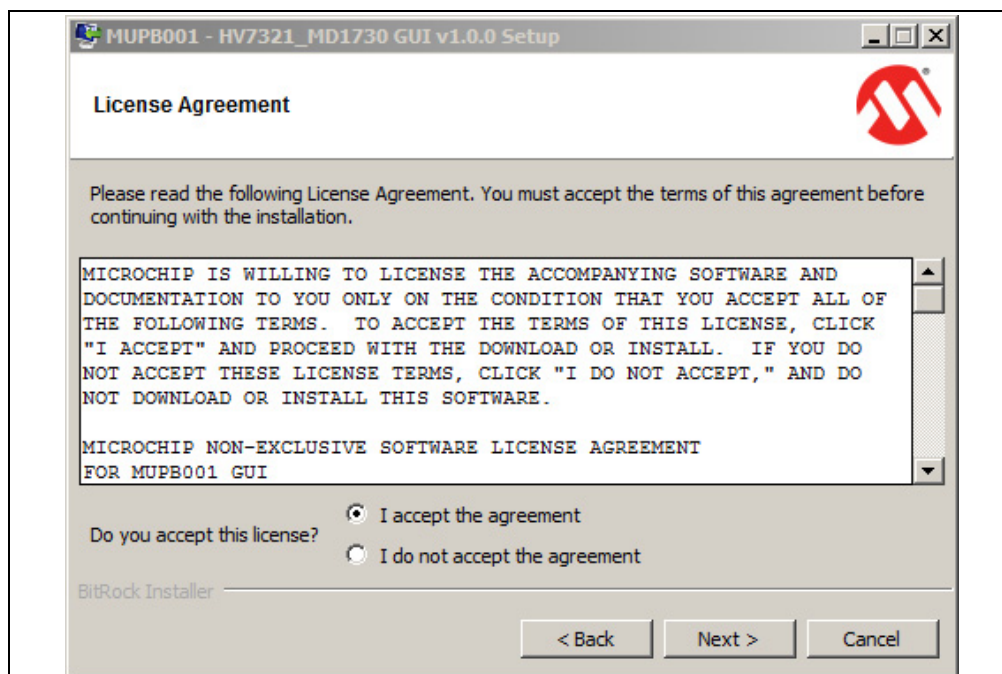


FIGURE 3-2: MUPB001 GUI – License Agreement Dialog Box.

3. On the **Installation Directory** dialog box, browse for the desired location, or click **Next** to install in the default location.

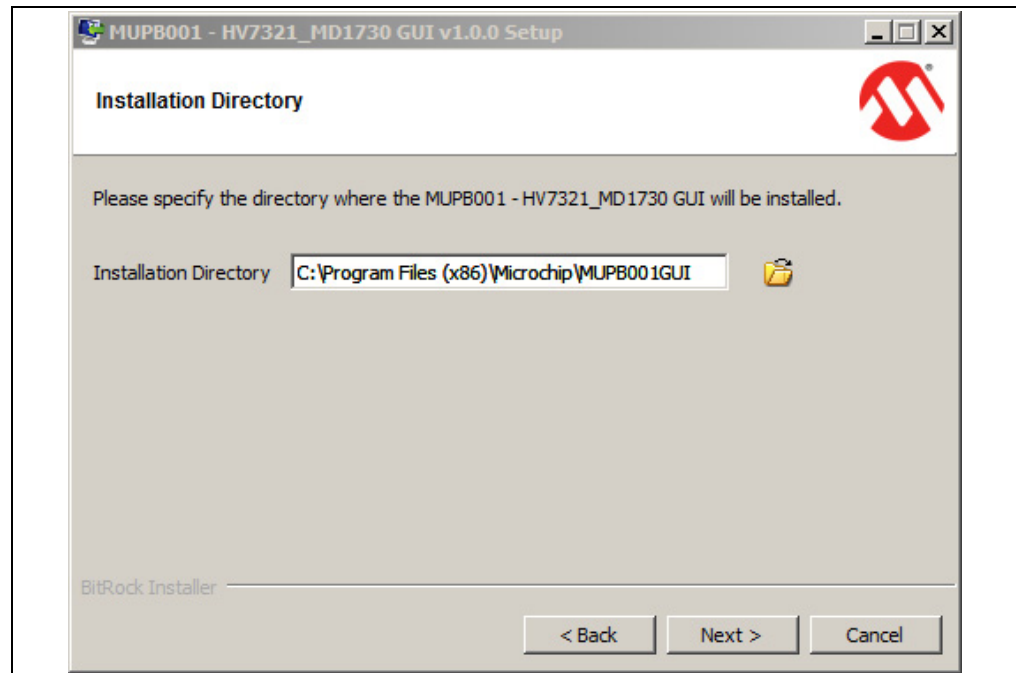


FIGURE 3-3: MUPB001 GUI – Installation Directory Dialog Box.

4. Once the installation path is chosen, the software is ready to install. Click **Next** to proceed.

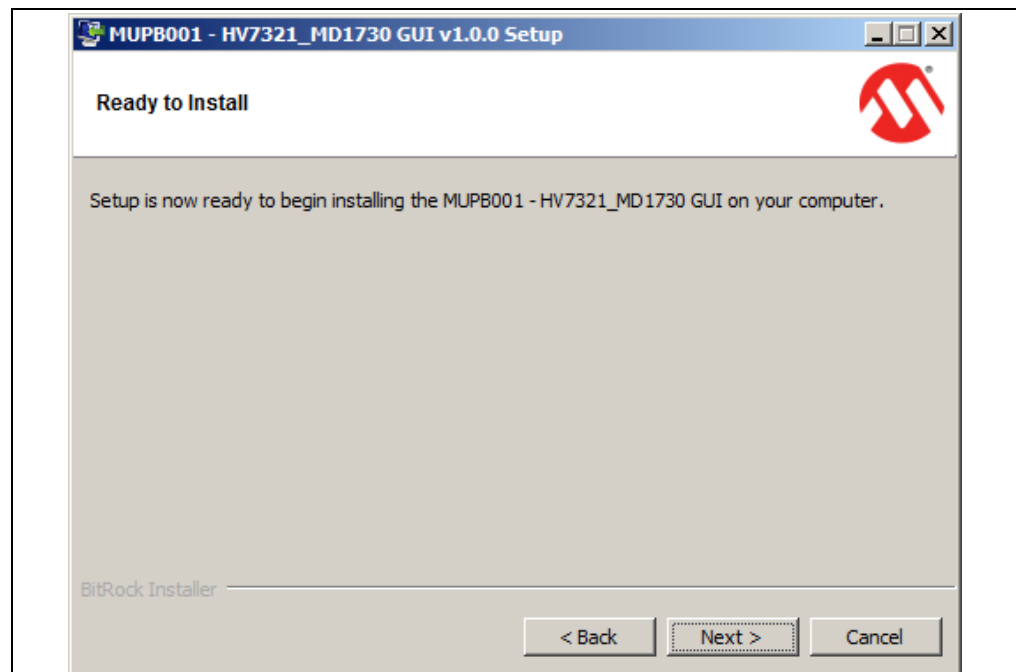


FIGURE 3-4: MUPB001 GUI – Ready-to-Install Dialog Box.

5. The installation status window appears, showing the installation progress. After the installation has completed, click **Next** to continue.

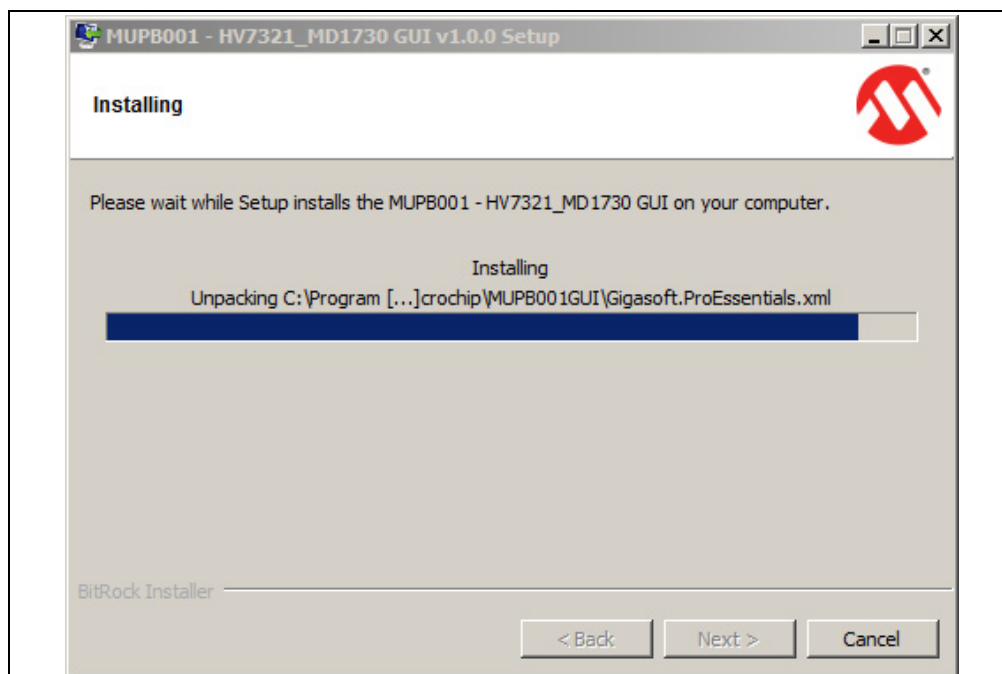


FIGURE 3-5: MUPB001 GUI – Installation Status Window.

6. Once the **Install Complete** dialog box appears, click **Finish** to exit the Installer.

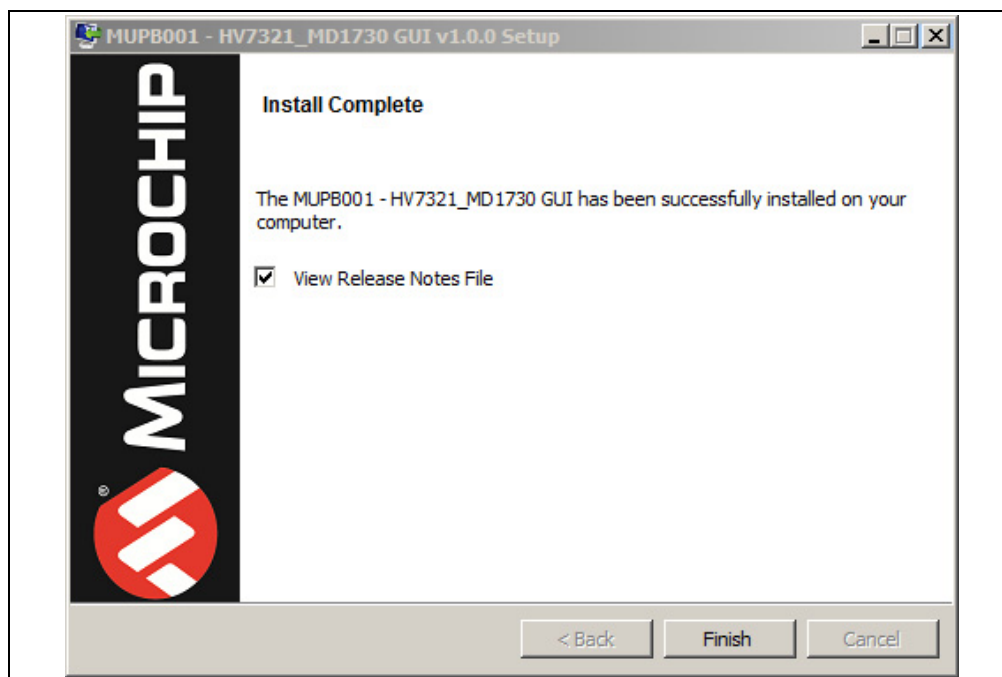


FIGURE 3-6: MUPB001 GUI – Install Complete Dialog Box.

7. Start the software by either going to Windows Start button > All Programs > Microchip > MUPB001 GUI or by clicking the newly-created software icon on the desktop ().

3.4 MUPB – HV7321_MD1730 GUI DESCRIPTION

The elements of the MUPB - HV7321_MD1730 Graphical User Interface are dependent on the selection being made in the **Transmission Mode** list box (3.4.11), labeled with 11 on Figure 3-7.

Transmission Mode “Pulsed-Echo” is selected by default. This section provides a comprehensive overview of the main GUI elements. Some elements are specific to Pulsed-Echo only, while others are shared across transmission modes, i.e., common to the GUI as a whole. The numbered entries in Figure 3-7 (1 through 16) are described in subsections 3.4.1 through 3.4.16.

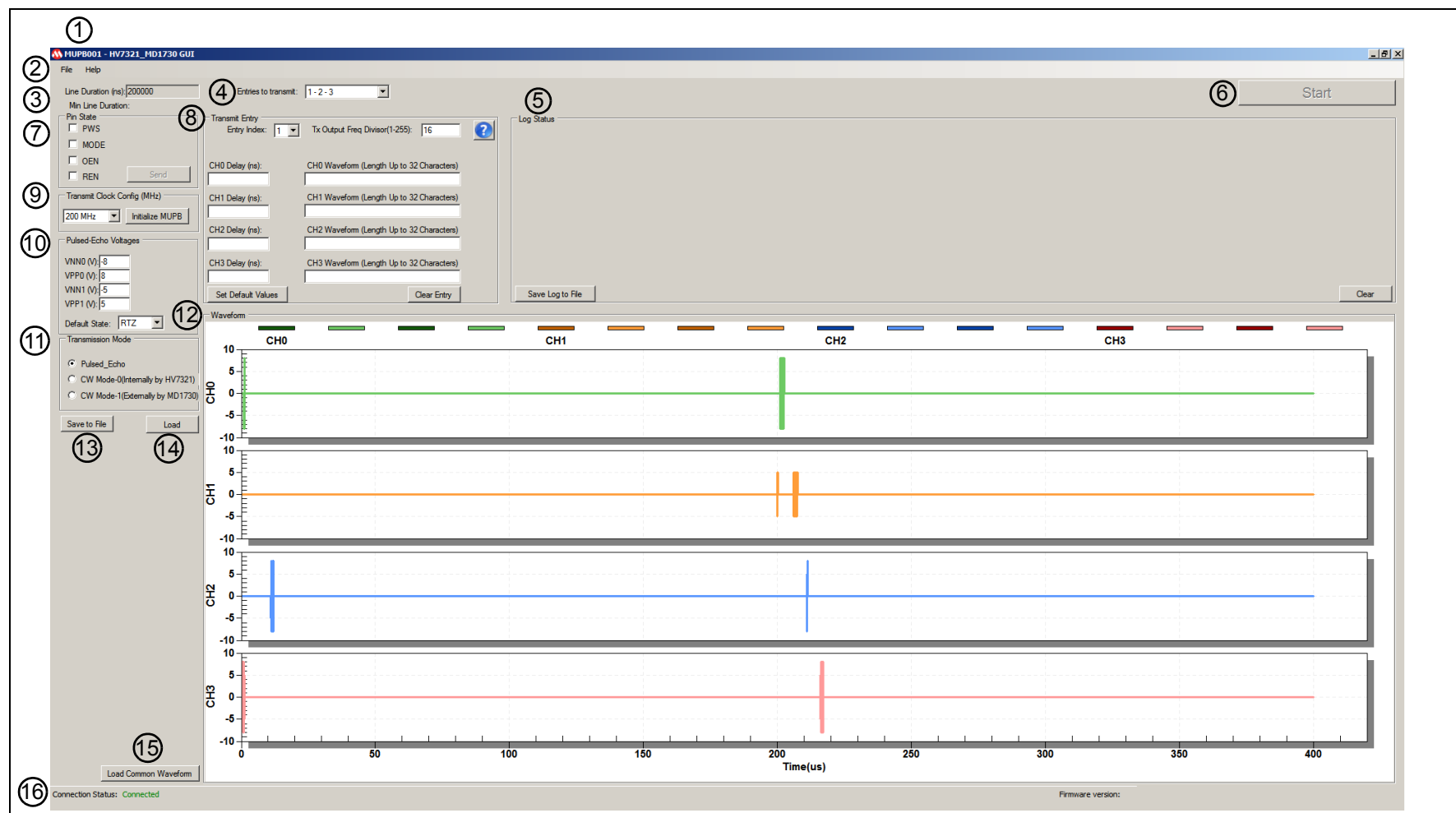


FIGURE 3-7: MUPB001 – HV7321_MD1730 GUI Pulsed-Echo View.

3.4.1 Title Bar

On the MUPB001 – HV7321_MD1730 GUI Ribbon, the Microchip Technology Inc. logo is displayed together with the name of the GUI.

3.4.2 Menu Bar

There are two menus on the Menu bar: **File** and **Help**. Click the **File** menu to open these submenus: **Save Waveform**, **Load Waveform**, **Save Log**, **Refresh**, and **Exit**. Clicking the **Help** menu gives users access to **Show Help**, and **About** submenus.

3.4.3 Line Duration Text Box

The user can set the line duration by entering the required value into the **Line Duration(ns)** text box. The default value is 200000 ns.

3.4.4 Entries to Transmit Drop-Down List Box

One transmission loop makes up one line duration. During one line duration each channel can be set to transmit up to 4 different group of pulses. The options available to the user are **1**, **1 - 2**, **1 - 2 - 3**, and **1 - 2 - 3 - 4**.

3.4.5 Log Status Group Box

The **Log Status** group box is made up of the screen area and the button area.

The **Log Status** screen area shows messages on the status of the initialization of the MUPB001 board transmit frequency and Pulsed-Echo Mode settings. "Initialization Started", "Initialization Completed", "Transmission is started", "Transmission is stopped" are commonly displayed status messages. [Figure 3-8](#) provides an example.

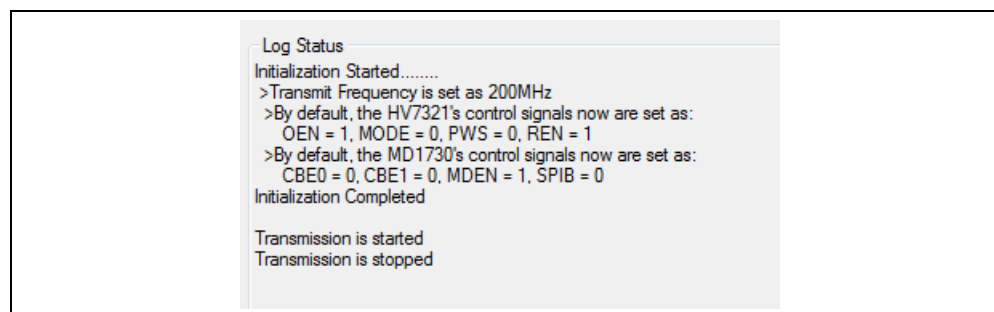


FIGURE 3-8: Log Status Screen Area.

There are two buttons in the **Log Status** button area: **Save Log to File**, and **Clear**.

These buttons allow the user to either save the log in a text file or clear the log screen, respectively.

Clicking the **Save Log to File** button brings up the **Save As** dialog box, which allows the user to navigate to the desired location for the log to be saved, and assign the log a file name.

3.4.6 Start/ Stop Button

The **Start/Stop** button starts and stops the transmission. It becomes available to use once the MUPB001 is connected to the PC via USB, and the connection is recognized by the PC.

3.4.7 Pin State Group Box

The **Pin State** group box is made up of **Pin State** check box and the **Send** button.

The Pin State check box includes the control signals of **PWS**, **MODE**, **OEN**, and **REN**.

PWS must be checked (ON) for Pulsed-Echo mode and unchecked (OFF) for CW Modes. **MODE** has to be selected (ON) for CW Mode-1 and unselected (OFF) for CW Mode-0 and Pulsed-Echo mode.

REN is an abbreviation for “Regulator Enable” and it has to be checked (ON) for turning the internal regulators on. **OEN** refers to “Output Enable” and it has to be selected (ON) for getting the outputs out of High Impedance (high Z) mode.

After checking the desired options, the **Send** button becomes available for sending the settings to the MUPB001.

3.4.8 Transmit Entry Group Box

This group box allows the users to set the parameters for the pulses that are necessary to be transmitted. The **Transmit Entry** group box includes:

- the **Entry Index** drop-down list box:
 - the users can set between 1 and 4 group of pulses for each channel. The default value is 4.
- the **TX Output Freq Divisor (1-255)** text box:
 - the users can adjust the pulse width by entering a value between 1 and 255 in this text box. If **Transmit Clock Config (MHz)** (see [Figure 3-7](#)) is 200 MHz then the clock period is 5 ns. The pulse width is adjusted by dividing the TX Output Freq Divisor to the Transmit Clock Frequency. The default value is 16.
- **4 Channels (0-3) Delay (ns)** text boxes:
 - the relative delay between channels can be defined in these text boxes. The value is expressed in nanoseconds. The default value is 16000 ns.
- **4 Channels (0-3) Waveform (Length Up to 32 Characters)** text boxes:
 - each group of pulses can be made up of up to 32 characters. The building blocks that make up the waveform syntax are presented in [Table 3-1](#).

TABLE 3-1: CHANNEL WAVEFORM SYNTAX

Building Blocks	Definition
0	= VNN0
1	= VPP0
2	= VNN1
3	= VPP1
R	= Return-to-Zero (RTZ)
P	= Receive Mode (RTZ+)
H	= High-Impedance (high Z)

- the **Set Default Values** button:
 - the users can set the entered input values into the **Channels (0-3) Delay (ns)** and **Channels (0-3) Waveform (Length Up to 32 Characters)** text boxes as default values.
- the **Clear Entry** button:
 - this button clears the values entered into the **Channels (0-3) Delay (ns)** and **Channels (0-3) Waveform (Length Up to 32 Characters)** text boxes.
- the **Help** () button:
 - clicking the **Help** button opens the **Information** pop-up window. See [Figure 3-9](#).

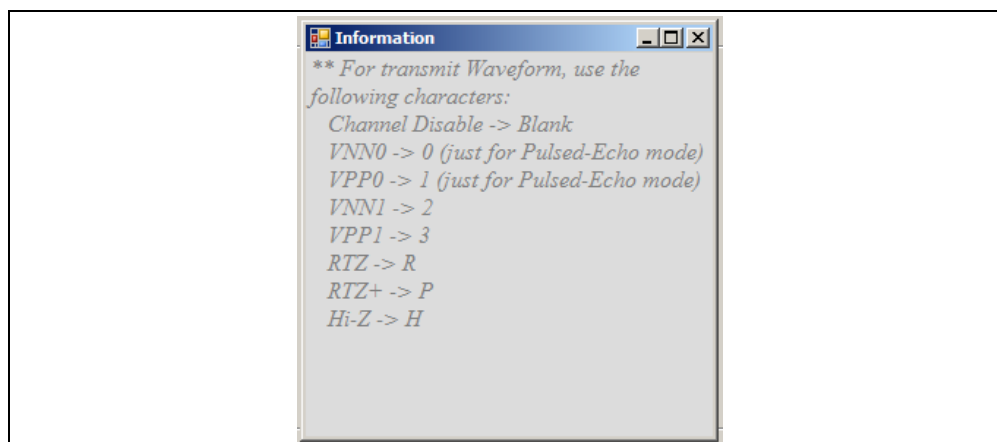


FIGURE 3-9: Information Pop-Up Window.

3.4.9 Transmit Clock Configuration (MHz) Group Box

The **Transmit Clock Configuration (MHz)** group box allows users to set the clock frequency. The **Transmit Clock Configuration (MHz)** group box includes the **Transmit Clock Configuration (MHz)** drop-down list box and the **Initialize MUPB** button. Users can select between **80**, **120**, **160** and **200** MHz clock frequency. The **Initialize MUPB** button is activated once the USB connection between the PC and the MUPB001 is established.

3.4.10 Pulsed-Echo Voltages Group Box

The **Pulsed-Echo Voltages** group box enables users to add numeric values to the voltage values shown on the GUI plot, for labeling purposes.

The **Pulsed-Echo Voltages** group box includes:

- 4 voltage text boxes each corresponding to **VNN0 (V)**, **VPP0 (V)**, **VNN1 (V)**, and **VPP1 (V)**.
- the **Default State** drop-down list box which allows users to select the initial state of the transmission channels. The options available are: **RTZ**, **RTZ+** and **Hi-Z**.

3.4.11 Transmission Mode List Box

The user can select one of the 3 available modes of transmission by checking one option in the **Transmission Mode** list box. The options available are:

- **Pulsed_Echo**: There are 5 voltage levels [**VPP0**, **VPP1**, **Ground** (Return-To-Zero, **RTZ**), **VNN1**, **VNN0**] in addition to High Impedance (**Hi-Z**) and Receive mode (**RTZ+**).
- **CW Mode-0 (Internally by HV7321)**: There are 3 voltage levels [**VPP1**, **Ground** (Return-To-Zero, **RTZ**), **VNN1**] in addition to High Impedance (**Hi-Z**) and Receive mode (**RTZ+**).
- **CW Mode-1 (Externally by MD1730)**: There are 3 voltage levels [**CW+**, **Ground** (Return-To-Zero, **RTZ**), **CW-**] in addition to High Impedance (**Hi-Z**) and Receive mode (**RTZ+**).

3.4.12 Waveform Screen Area

The **Waveform** screen area displays the transmitted waveforms. The signals displayed are not the actual measurements at the HV7321 output but visual representations of what is expected at the output.

The parameters shown in the **Waveform** screen area are dependent on the mode of transmission selected in the **Transmission Mode** list box (see [Section 3.4.11](#)).

3.4.13 The Save to File button

By clicking the **Save to File** button, users can save the currently loaded waveforms and the delay values input in **CH0-3 Delay (ns)** text boxes to a text file.

Clicking this button brings up the **Save As** dialog box that allows the user to navigate to the desired location for the file to be saved, and assign the file a file name.

3.4.14 The Load Button

The **Load** button is used in conjunction with the **Save** button to load the previously saved waveforms and delay values.

Clicking this button activates the **Open** dialog box which allows the user to navigate to the location of the file to be loaded.

3.4.15 The Load Common Waveform Button

The **Load Common Waveform** button allows the user to access a set of 10 predefined waveform profiles (Common Waveform 1 through 10) and load them into the GUI. Only one selection can be active at a time. Depending on the selection being made, the **Channels (0-3) Waveform (Length Up to 32 Characters)** text boxes ([Section 3.4.8](#)) will be updated with a different waveform syntax.

Clicking the **Load Common Waveform** button activates the **Common Waveforms** dialog window. The **Common Waveforms** dialog window is made up of a list box including 10 items, which the users can choose from sequentially.

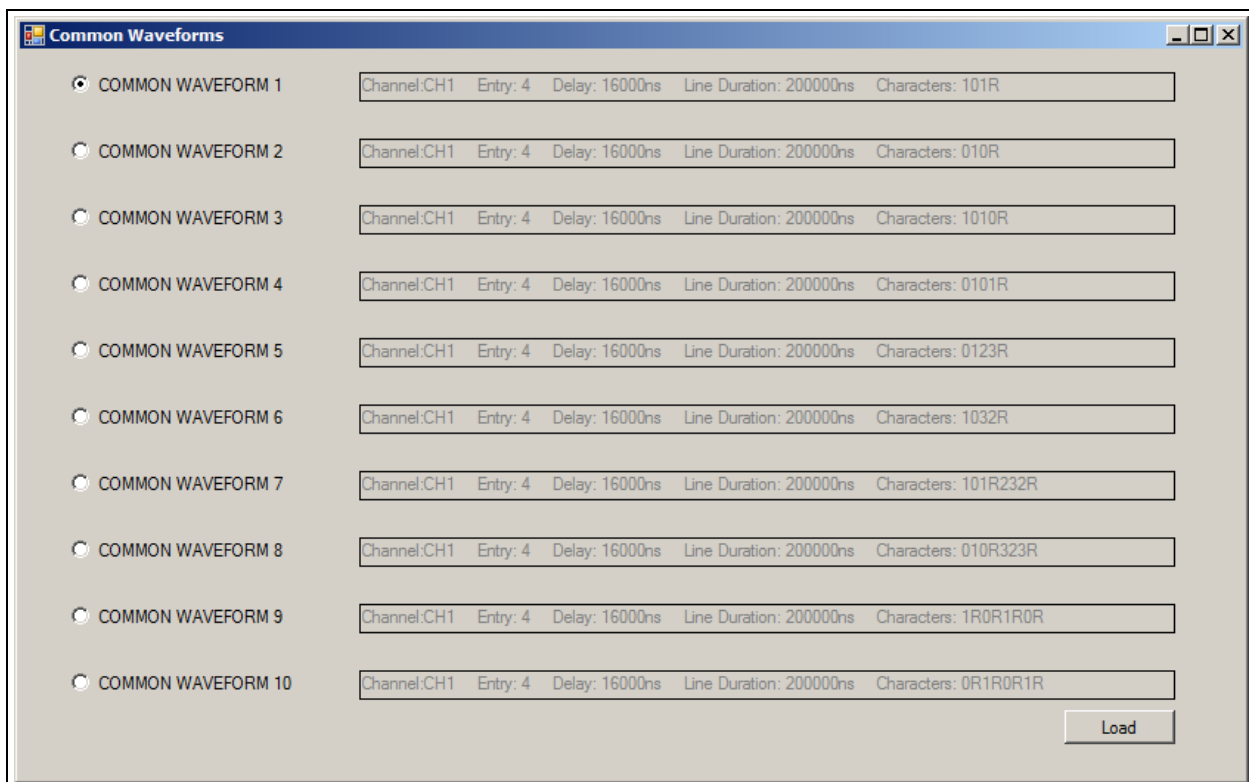


FIGURE 3-10: Common Waveforms Dialog Box.

3.4.16 Connection Status Indicator

The **Connection Status** indicator updates accordingly depending on whether there is a working connection between the PC and the MUBPB001. There are two connection status messages:

- Not Connected (in red): the MUPB001 is not yet powered on or the USB connection is not established.
- Connected (in green): the MUPB001 is powered on and the USB connection is established.

3.5 GUI ELEMENTS SPECIFIC TO CW MODE-0

Selecting **CW Mode-0 (Internally by HV7321)** in the **Transmission Mode** list box (3.4.11) GUI determines a change of the GUI elements displayed, as shown in Figure 3-11. This section provides a short overview of the GUI elements specific to CW Mode-0. The numbered entries in Figure 3-11 (1 through 3) are described in subsections 3.5.1 through 3.5.3.

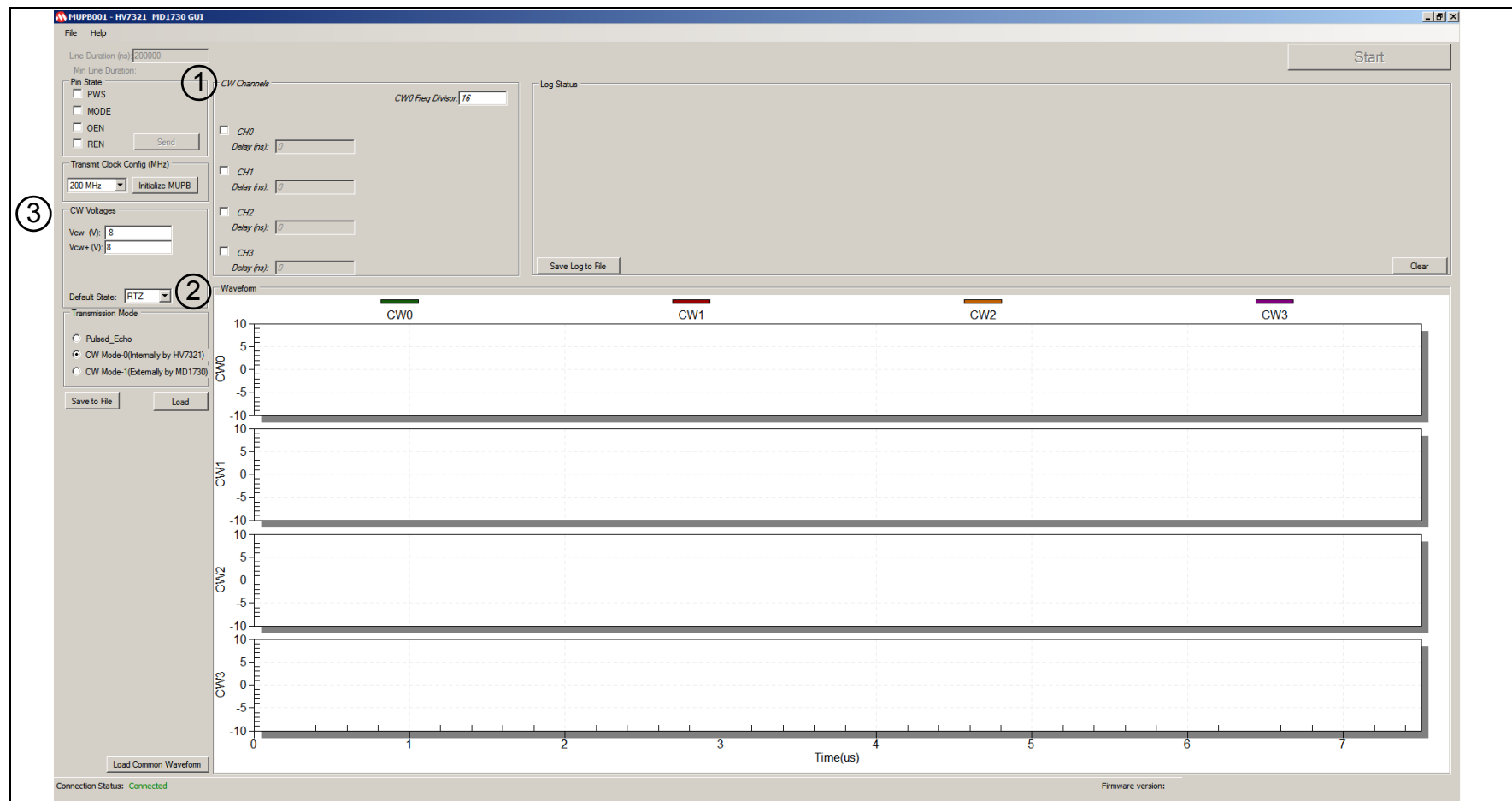


FIGURE 3-11: MUPB001 – HV7321_MD1730 GUI CW Mode-0 View.

3.5.1 CW Channels Group Box

The **CW Channels** group box enables users to set the frequency of the outputs and the relative delays.

The **CW Channels** group box includes the **CW0 Freq Divisor** text box and 4 channel check boxes each corresponding to **CH0**, **CH1**, **CH2**, and **CH3**.

Users can make from 1 to 4 selections at a time. Each channel text box has a **Delay (ns)** text box associated that users can use to set the channel delay value. The **Delay (ns)** text boxes become available once the channel text box is selected.

In **CW0 Freq Divisor** text box users can set the frequency of the CW signal. The CW Frequency is calculated by dividing the to twice the CW0 Freq Divisor:

$$\text{CW Frequency} = (\text{Transmit Clock Config}) / (2 \times \text{CW0 Freq divisor})$$

Selecting the **CH0**, **CH1**, **CH2**, **CH3** check boxes causes the **Waveform screen area** (3.5.2) to be updated with a continuous signal waveform pattern. The waveform patterns are color coded: green for CH0, dark red for CH1, orange for CH2 and purple for CH3.

3.5.2 Waveform Screen Area

The **Waveform Screen Area** shows the active channels as continuous signals. The signals displayed are not the actual measurements at the HV7321 output but visual representations of what is expected at the output.

3.5.3 CW Voltages group box

The **CW Voltages** group box includes:

- 2 voltage text boxes corresponding to **VCW-** and **VCW+**: the values entered in these text boxes will cause the representations of the signals displayed in the **Waveform Screen Area** to change.
- the **Default State** drop-down list box where users can select between **RTZ**, **RTZ+**, and **HI-Z**.

3.6 GUI ELEMENTS SPECIFIC TO CW MODE-1

Selecting **CW Mode-1 (Externally by MD1730)** in the **Transmission Mode** list box (3.4.11) GUI determines a change of the GUI elements displayed, as shown in Figure 3-12. This section provides a short overview of the GUI elements specific to CW Mode-1. The numbered entries in Figure 3-12 (1 through 4) are described in subsections 3.6.1 through 3.6.3.

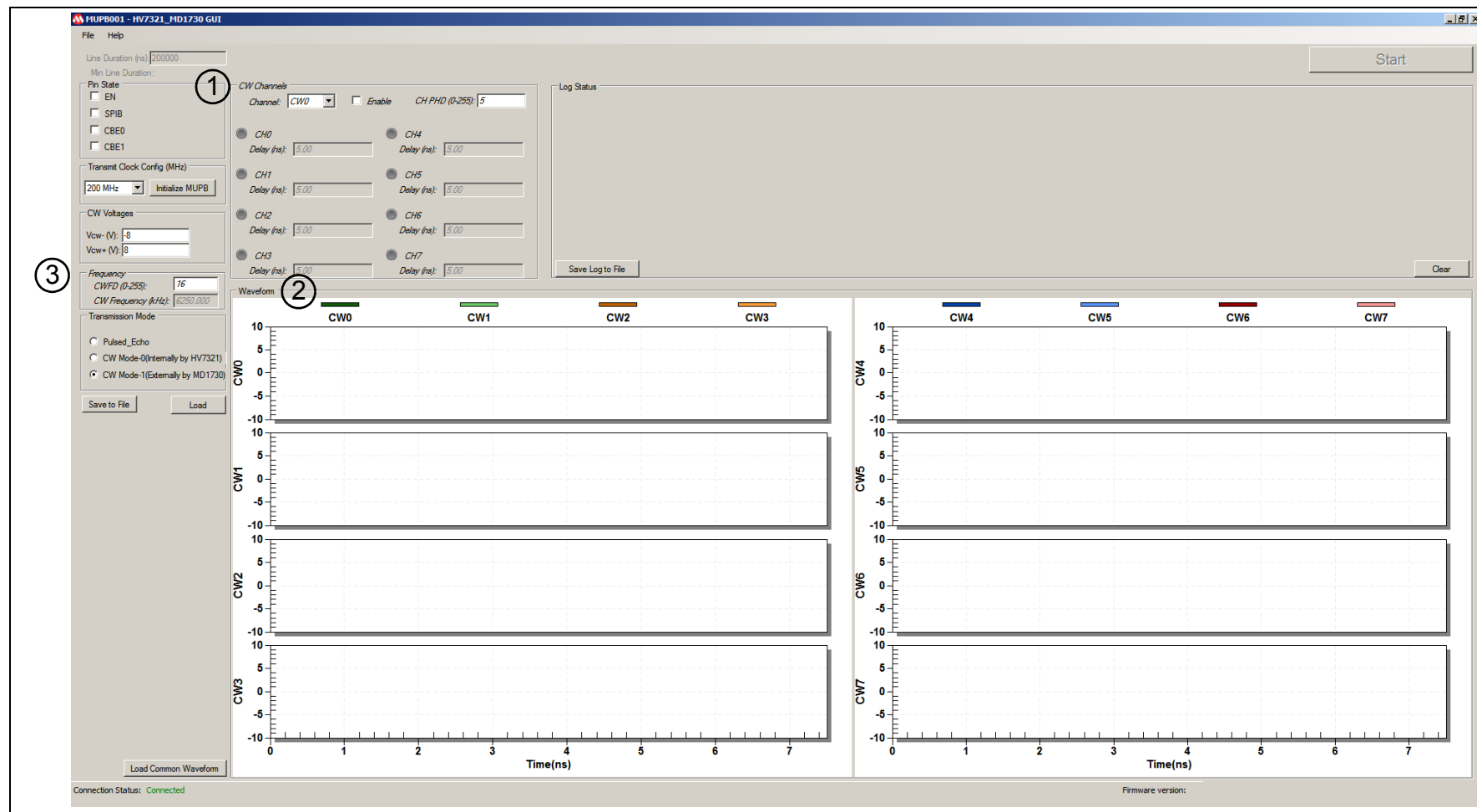


FIGURE 3-12: MUPB001 – HV7321_MD1730 GUI CW Mode-1 View.

3.6.1 CW Channels Group Box

In CW Mode-1, there are 8 transmission channels. The channels are selected and configured in the **CW Channels** group box. The **CW Channels** group box includes:

- the **Channel** drop-down list box in which users can select from 1 to 7 channels sequentially (CW0, CW1, CW2, CW3, CW4, CW5, CW6, CW7). Unlike other cases, the simple selection of the channel does not enable the channel.
- the **Enable** check box: the channels selected in the **Channel** drop-down list box are enabled/disabled by checking/unchecking the **Enable** check box. Enabled channels are marked with a green indicator in the channel enable status screen area.
- the channel enable status screen area is made up of 8 status indicators (gray = disabled, green = enabled), 8 channel labels (**CH0, CH1, CH2, CH3, CH4, CH5, CH6, CH7**), and 8 corresponding **Delay (ns)** text boxes.
- the **CH PHD (0-255)** (Channel Phase Delay Digital Value) text box: users can set the channel phase delay digital value of the CW signal by choosing a value between 0 and 255. The value entered in this text box is used to generate the CH phase delay in nanoseconds. The equivalent delay in nanoseconds will be calculated and displayed in the **Delay (ns)** text boxes corresponding to the channels selected. For the **Delay (ns)** text boxes to be automatically updated with the equivalent channel phase delay digital value, it is necessary to first input a value in the **CH PHD (0-255)** text box and then click outside the text box.

3.6.2 Waveform Screen Area

The **Waveform Screen Area** shows the active channels as continuous signals. The signals displayed are not the actual measurements at the HV7321 output but visual representations of what is expected at the output.

3.6.3 Frequency Group Box

The **Frequency** group box is used to modulate the frequency of the CW.

The **Frequency** group box includes two text boxes:

- the **CWFD (0-255)** (Continuous Wave Frequency Digital Value) text box: the value entered in this text box is used to generate the CW frequency in kHz.
- the **CW Frequency (kHz)** text box: this text box shows the equivalent value in kHz of the value entered in the **CWFD (0-255)** text box. For the **CW Frequency (kHz)** text box to be automatically updated with the equivalent CWFD value, it is necessary to first define the CWFD value and then click outside the text box.

Note: For frequency and delay calculation details, refer to the MD1730 Data Sheet.

3.7 CONFIGURING THE TRANSMISSION OF SIGNALS USING THE GUI

Following is a step-by-step guide for generating Pulsed-Echo signals, CW Mode-0 signals and CW Mode-1 signals at the HV7321 output. After each set of instructions, an oscilloscope screen shot taken at the HV7321 output is presented.

3.7.1 Generating Pulsed-Echo Signals

1. Start the MUPB001 - HV7321_MD1730 GUI.
 - make sure DC-IN LED is ON when the power input is connected to the MUPB001
2. Switch on the MUPB001 to power the board.
 - check that PWR_OK, FPGA_OK LEDs are ON, and the USB_Fault LED is OFF.

- the **Connection Status** indicator (3.4.16) must show “Connected” (in green).
- 3. Set the default state in **Pulsed-Echo Voltages** group box (3.4.10) to RTZ (Ground) by making sure **RTZ** is selected in the **Default State** drop-down list box.
- 4. Set the transmit clock configuration to 200 MHz by making sure **200 MHz** is selected in the **Transmit Clock Config (MHz)** group box. Click the **Initialize MUPB** button to activate the MUPB clock (3.4.9).
- 5. Make sure the default value of 200000 ns is input into the **Line Duration (ns)** text box (3.4.3).
- 6. Check the **Log Status** screen area (3.4.5) and look for the confirmation message that the initialization started and completed with no errors.
- 7. Check that the default transmission mode, Pulsed_Echo, is selected in the **Transmission Mode** list box (3.4.11).
- 8. In the **Pin State** group box, select **PWS**, **OEN** and **REN** by selecting the corresponding check boxes. Leave **MODE** unselected. Click the **Send** button (3.4.7).
- 9. In the **Transmit Entry** group box set the **Entry Index** (entries to transmit) to **1** and the TX Output Freq Divisor to **20** (3.4.8). This sets one group of pulses during the line duration, and a pulse of 100 ns.
- 10. Set the relative delay between channels by entering the following values into the **Channels (0-3) Delay (ns)** text boxes: **30, 60, 90, 120**. Set the waveform length by inputting these values into the **Channels (0-3) Waveform (Length Up to 32 Characters)** text boxes: **1032R, 1010R, 3232R, 0123R**. See Figure 3-13.

The screenshot shows the 'Transmit Entry' configuration window. At the top, 'Entry Index' is set to 1 and 'Tx Output Freq Divisor (2-255)' is set to 20. Below this, there are four rows for channel configuration:

Channel	Delay (ns)	Waveform (Length Up to 32 Characters)
CH0	30	1032R
CH1	60	1010R
CH2	90	3232R
CH3	120	0123R

At the bottom of the window, there are two buttons: 'Set Default Values' and 'Clear Entry'.

FIGURE 3-13: Transmit Entry Group Box Configured for Pulsed-Echo.

- 11. Click the **Start/Stop** button (3.4.6).
- 12. An oscilloscope screenshot of the waveform generated is shown in Figure 3-14.

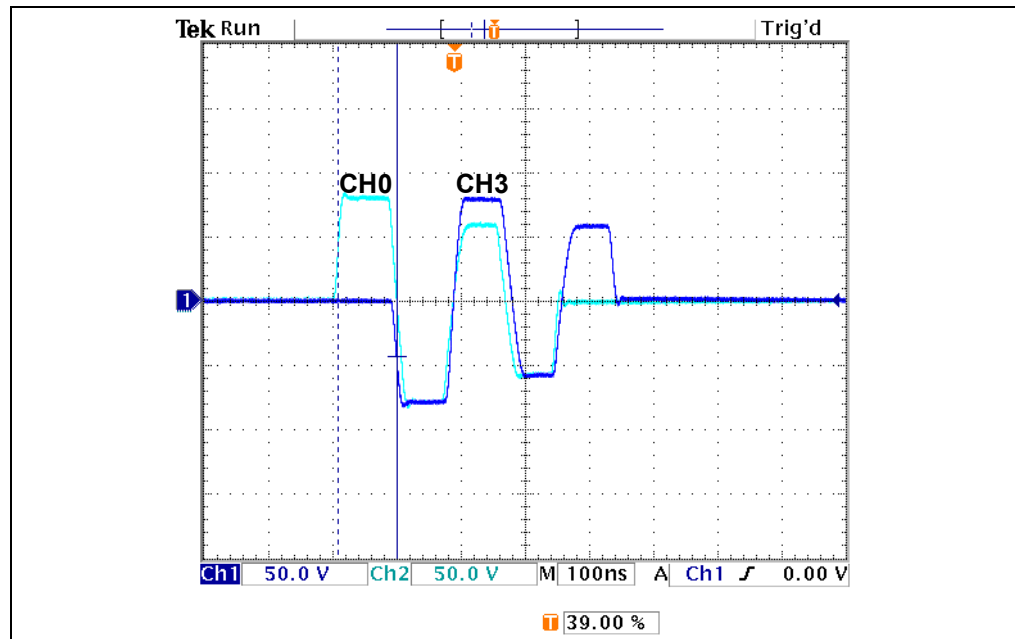


FIGURE 3-14: Pulsed-Echo Output.

3.7.2 Generating CW Mode-0 Signals

1. Start the MUPB001 - HV7321_MD1730 GUI.
 - connect the +12V power connector to MUPB001 board and make sure that the green DC_IN LED is ON indicating that the power connection is successful.
2. Switch on the MUPB001 to power the board.
 - check that PWR_OK, FPGA_OK LEDs are ON, and the USB_Fault LED is OFF.
 - the **Connection Status** indicator (3.4.16) must show “Connected” (in green).
3. Set the default state in **Pulsed-Echo Voltages** group box (3.4.10) to RTZ (Ground) by making sure **RTZ** is selected in the **Default State** drop-down list box.
4. Set the transmit clock configuration to 200 MHz by making sure **200 MHz** is selected in the **Transmit Clock Config (MHz)** group box. Click the **Initialize MUPB** button to activate the MUPB clock (3.4.9).
5. Check the **Log Status** screen area (3.4.5) and look for the confirmation message that the initialization started and completed with no errors.
6. Check that the **CW Mode-0 (Internally by HV7321)** transmission mode is selected in the **Transmission Mode** list box (3.4.11).
7. In the **Pin State** group box, select **OEN** and **REN** by selecting the corresponding check boxes. Leave **PWS** and **MODE** unselected. Click the **Send** button (3.4.7).
 - make sure MDEN and OEN LEDs on HV7321 Ultrasound TX Pulser Evaluation Board are ON.
8. In the **CW Channels** group box (3.5.1), enter 20 in the **CW0 Output Freq Divider**. This sets a CW frequency of 5 MHz. Activate **CH0**, **CH2** and **CH3** by clicking the corresponding check boxes. Set the delay between channels as **CH0 Delay(ns):10, CH2 Delay(ns):20, CH3 Delay(ns):40**.
9. Click the **Start/Stop** button (3.4.6).
10. An oscilloscope screenshot of the waveform generated is shown in Figure 3-15.

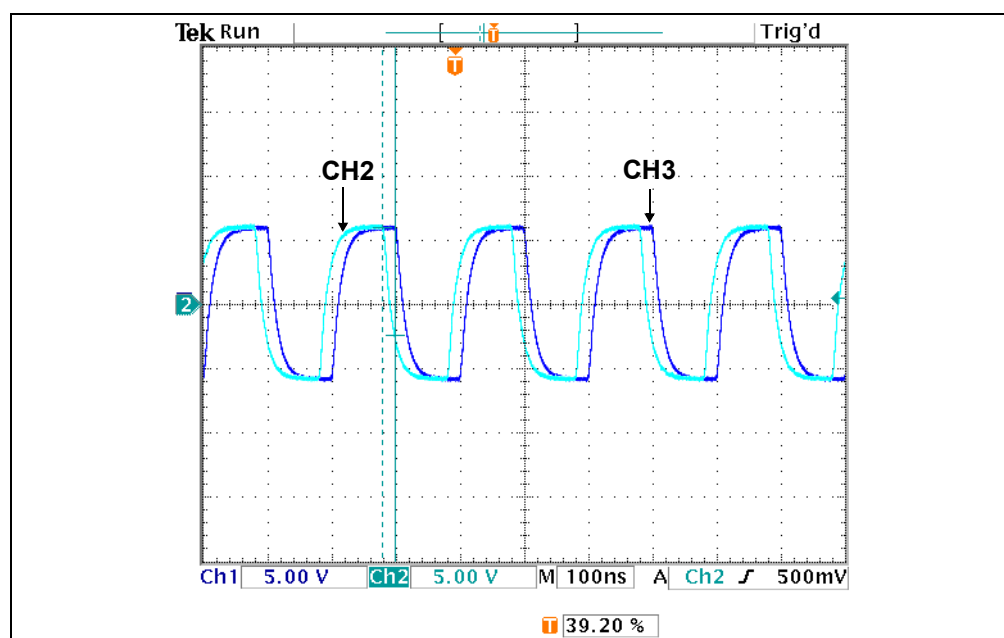


FIGURE 3-15: CW Mode-0 Output.

3.7.3 Generating CW Mode-1 Signals

1. Start the MUPB001 - HV7321_MD1730 GUI.
 - connect the +12V power connector to MUPB001 board and make sure that the green DC_IN LED is ON indicating that the power connection is successful.
2. Switch on the MUPB001 power switch to power the board.
 - check that PWR_OK, FPGA_OK LEDs are ON, and the USB_Fault LED is OFF.
 - the **Connection Status** indicator (3.4.16) must show “Connected” (in green).
3. Set the transmit clock configuration to 200 MHz by making sure **200 MHz** is selected in the **Transmit Clock Config (MHz)** group box. Click the **Initialize MUPB** button to activate the MUPB clock (3.4.9).
4. Check the **Log Status** screen area (3.4.5) and look for the confirmation message that the initialization started and completed with no errors.
5. Check that the **CW Mode-1(Externally by MD1730)** transmission mode is selected in the **Transmission Mode** list box (3.4.11).
6. In the **Pin State** group box, select **EN** and **SPIB** by selecting the corresponding check boxes. Leave **CBE0** and **CBE1** unselected (3.4.7).
 - make sure MODE, MDEN and OEN LEDs on HV7321 Ultrasound TX Pulser Evaluation Board are ON.
7. In the **Frequency, CWFD (0 – 255)** text box (3.6.3) enter **20**. This provides a CW frequency of 5 MHz. Click outside the text box to update the value shown in the **CW Frequency (kHz)** text box to 5000 kHz.
8. Enable **CH0**, **CH2**, and **CH3** in the **CW Channels** group box (3.6.1). Make sure these channel status indicators are green. Set the channel delay as follows:
 - **CH0 Delay(ns):10** by entering **2** in the **CH PHD (0-255)** text box corresponding to CW0
 - **CH2 Delay(ns):20** by entering **4** in the **CH PHD (0-255)** text box corresponding to CW2
 - **CH3 Delay(ns):40** by entering **8** in the **CH PHD (0-255)** text box

corresponding to CW3.

9. Click the **Start/Stop** button (3.4.6).
10. An oscilloscope screenshot of the waveform generated is shown in Figure 3-16.

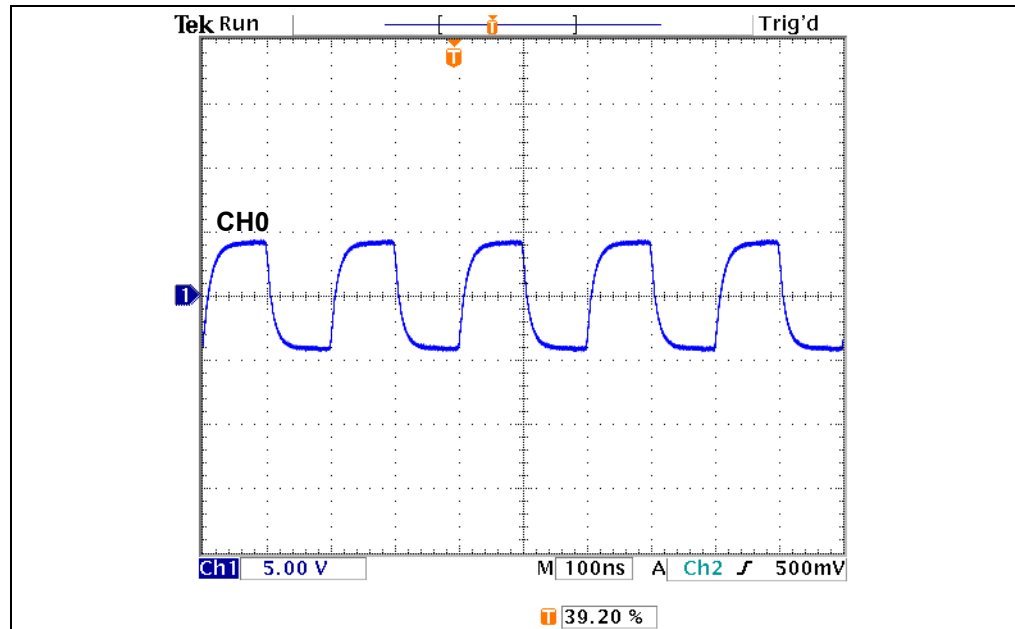


FIGURE 3-16: CW Mode-1 Output ($V_{CW+} = +5V$, $V_{CW-} = -5V$).

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NOTES:

Chapter 4. PCB Design and Layout Notes

4.1 PCB LAYOUT TECHNIQUES FOR HV7321 & MD1730 ULTRASOUND PULSER

The HV7321 is a high-voltage, high-current and high-frequency nanosecond pulse generator integrated circuit. The PCB design and layout are important key development steps to guarantee the success of the design implementation.

4.1.1 High-Voltage, High-Speed Grounding, and Layout Techniques for the HV7321

The large thermal pad at the bottom of the HV7321 device is internally connected to the IC substrate (V_{SUB}). This thermal pad should be connected to 0V or GND externally on the PCB.

The designer needs to pay attention to the connecting traces on the output TX0-3, as these are the high-voltage and high-speed traces. In particular, controlled impedance of 50Ω to the ground plane and more trace spacing needs to be applied in this situation.

High-speed PCB trace design practices that are compatible with about 200 MHz operating speeds are used for the HV7321 Ultrasound TX Pulser Evaluation Board PCB layout. The internal circuitry of the HV7321 can operate at rather high frequencies, with the primary speed limitation being the load capacitance.

Because of the high-speed and high-transient currents that result when driving capacitive loads, the supply-voltage bypass capacitors, and the driver to the FET gate-coupling capacitors should be as close to the pins as possible. The GND pin should have low inductance feed-through via connections that are connected directly to a solid ground plane. Ground plane has to be the second layer of the PCB.

It is advisable to minimize the trace length to the ground plane, and insert a ferrite bead in the power supply lead to the capacitor to prevent resonance in the power supply lines. For applications that are sensitive to jitter and noise, and when using multiple HV7321 ICs, insert an additional ferrite bead between the supply lines of each chip.

To reduce inductance particular attention should be paid to minimizing trace lengths and using sufficient trace width. Surface-mount components are highly recommended. Since the output impedance of the HV7321 high-voltage power stages is very low, in some cases, it is desirable to add a small value resistor in series with the TX3-0 outputs to obtain better waveform integrity at the load terminals after ultrasound probe long cables.

The impedance of the output resistors added to that of the HV7321 power stage output should match the probe cable impedance since at the other end of the transmission line there are normally piezoelectric elements with large parasitic capacitance to ground. However, this reduces the output voltage slew rate at the terminals of a capacitive load.

Attention should be paid to the parasitic coupling from the outputs to the input signal terminals of the HV7321. This feedback may cause oscillations or spurious waveform shapes on the edges of signal transitions. Since the input operates with signals down to 2.5V, even small coupling voltages may cause problems. The use of a solid ground plane and good power and signal layout practices can prevent this problem.

The user should also ensure that the circulating ground return current from a capacitive load cannot react with common inductance to create noise voltages in the input logic circuitry.

4.1.2 High-Frequency Differential Clock, and Low Phase Noise PCB Layout Techniques for the MD1730

The low phase noise feature has to be implemented on three aspects of the design: on the IC, on the signal clock source and on the PCB layout.

Choosing low-ESR and low-ESL decoupling capacitors, and implementing a low-EMI/RFI PCB layout, helps get the best phase noise performance on the MD1730.

The clock input of the MD1730 is designed to take LVDS, LVCMOS 2.5V or SSTL 2.5V differential signals. The suggested clock line traces impedance reference to GND plane is 50Ω, or 100Ω differentially.

In case multiple MD1730s need be used on the same PCB, it is highly recommended to use a differential clock buffer to drive the clock bus. The clock bus should consist of a 50Ω/50Ω coupled differential clock line pair. The 50Ω termination resistor on both lines to GND should be placed next to the last device clock input pin. If the clock source or buffer is powered by a higher than 2.5V V_{CC} , then AC coupling should be used. Refer to Figure 4-1 for details.

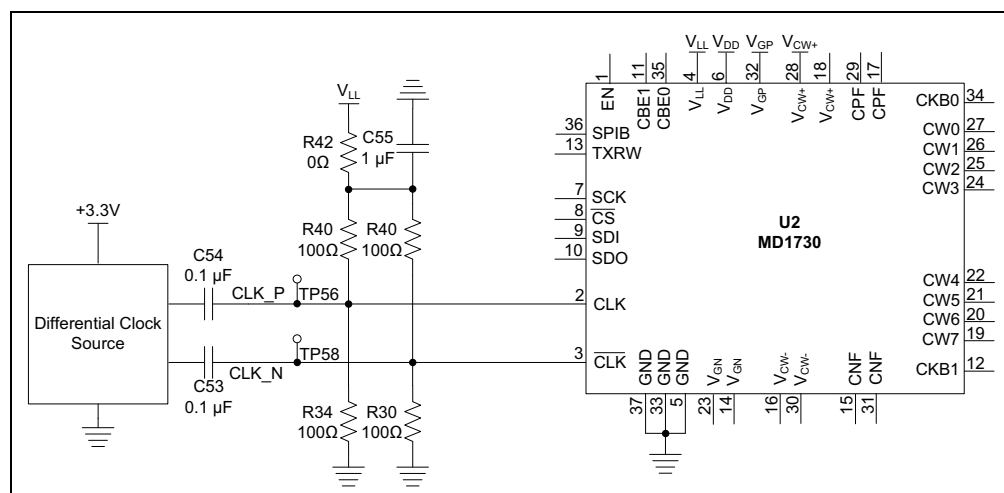


FIGURE 4-1: AC Coupling for MD1730 Differential Clock Inputs.

4.1.3 Selecting the Decoupling Capacitors

The voltage-supply pins (V_{LL} , V_{DD} , V_{GP} , V_{GN} , $V_{PP0/1}$ and $V_{NN0/1}$) can provide fast transient currents of up to 2.0 to 2.8A each. Each supply pin should be connected to a low-impedance bypass capacitor. A surface-mounted ceramic capacitor of 1.0-to-2.2 μF capacitance should be used.

When it comes to capacitor voltage rating, only the capacitors from $V_{PP0/1}$ and $V_{NN0/1}$ pins to GND must be 100V high-voltage type. Low-voltage rating capacitors of 10 to 16V can be used for V_{LL} , V_{DD} , V_{GP} , V_{GN} , C_{POS} , C_{NEG} to GND, $C_{PF0/1}$ to $V_{PP0/1}$, and $C_{NF0/1}$ to $V_{NN0/1}$ respectively.

Additional attention should be paid to what type of ceramic capacitor is selected for these bypass capacitors with regard to the low-impedance, low-voltage and low-temperature coefficient, including the very fast dV/dt of the pulse rising and falling edges. For these purposes it is recommended to use X7R, and X5R capacitors or other more advanced multilayer-ceramic types.

4.1.4 Return-Current Design on PCB Layout

Many EMI problems associated with high-speed circuits occur due to improper design of the return-current path. PCB designers often put a lot of effort into carefully designing traces with the proper length or proper transmission line impedance but neglect the return-current path that completes the current loop. Such EMI problems can usually be avoided if sufficient attention is paid to the return-current path.

The decoupling capacitor should be placed on the PCB as closely as possible to the pin being decoupled. However, the location on the PCB to install the decoupling capacitor is of equal importance. Usually a decoupling capacitor is placed where the high-voltage, high-speed return current ends. In that sense, the placement of the decoupling capacitor will also affect the EMI/RFI performance. The high-peak return current will travel, on the ground plane, from the load back to the decoupling capacitor where the ground via or vias are. The HV7321 pulser output traces on top layer or bottom layer carry high-peak currents, directing the return current to the ground plane, by means of the electromagnetic coupling effect. Therefore, these output traces together with the ground plane form the transmission line that supports a transverse electromagnetic (TEM) wave. In the region where the TEM pulse exists there is a time-varying electric field between the trace and the ground reference plane, the same as in simple micro-strip and strip-line cases. The electric field requires current to be in the two conductors. This current will be in opposite directions in the conductors, and must exist simultaneously with the pulse. The current must flow in both conductors as the pulse moves down the trace. Any discontinuity or break in these current paths, in either the trace or the ground plane, will affect the current, and compromise the signal-integrity or the EMI/RFI performance.

It is very important to keep the low-voltage logic signal traces, the middle-voltage gate driver (such as V_{DD} , V_{GP} , V_{GN} , C_{PF} , C_{NF}), and the high-voltage output stage traces between their decoupling capacitors to the HV7321 respective pin and ground return-current paths all electromagnetically independent of each other and not too close together. These are the challenges of a good PCB layout design while maintaining ground-integrity and keeping the solid ground plane.

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NOTES:

Appendix A. Schematic & Layouts

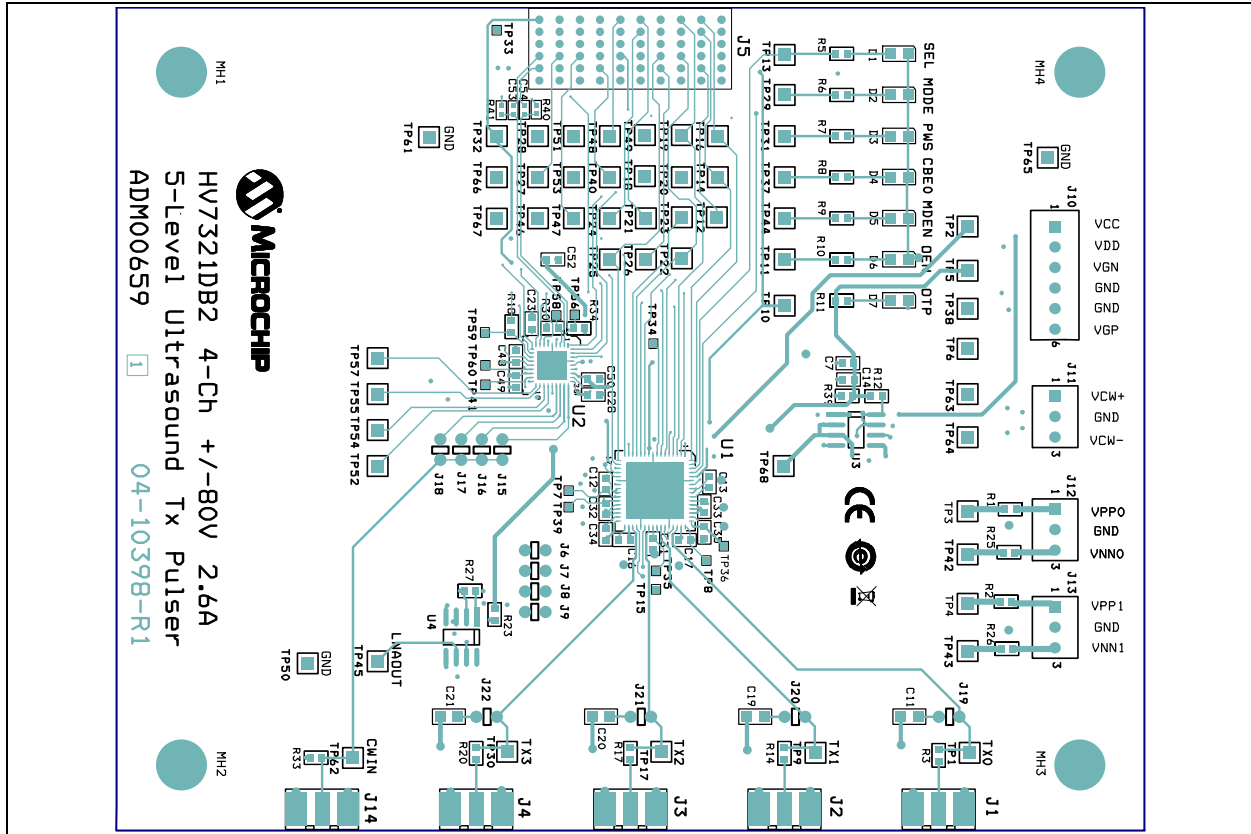
A.1 INTRODUCTION

This appendix contains the following schematics and layouts for the HV7321 Ultrasound TX Pulser Evaluation Board (ADM00659) and for the MUPB001 Microchip Ultrasound Platform Board (ADM00679):

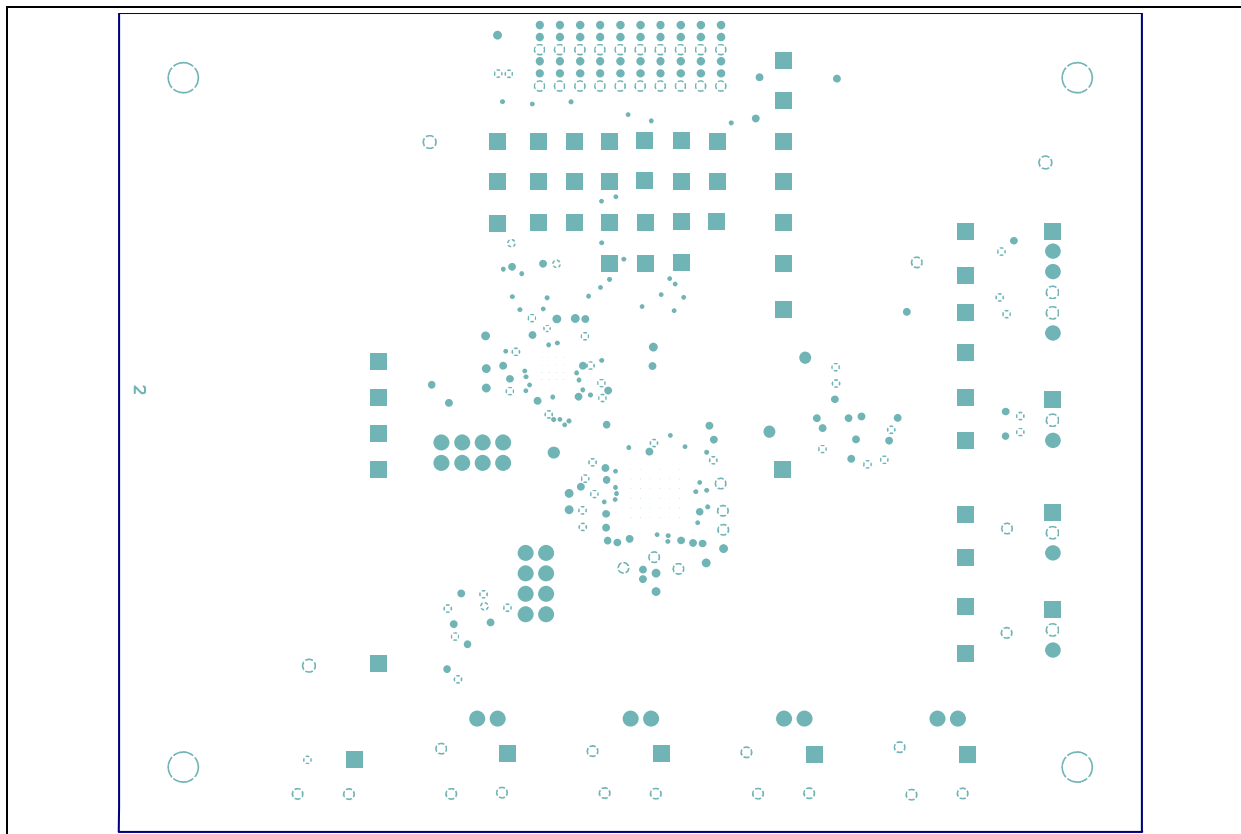
- HV7321 Ultrasound TX Pulser Evaluation Board:
 - ADM00659 – Schematic
 - ADM00659 – Top Copper and Silk
 - ADM00659 – Top Copper
 - ADM00659 – Inner 1 – GND
 - ADM00659 – Inner 2 – PWR
 - ADM00659 – Bottom Copper
 - ADM00659 – Bottom Copper and Silk
- MUPB001 Microchip Ultrasound Platform Board:
 - ADM00679 – Schematic (Connection)
 - ADM00679 – Schematic (Power Supply)
 - ADM00679 – Schematic (USB to SPI)
 - ADM00679 – Schematic (Programmable Clock)
 - ADM00679 – Schematic (FPGA)
 - ADM00679 – Schematic (FPGA Decoupling Capacitors)
 - ADM00679 – Schematic (Connectors)
 - ADM00679 – Top Silk
 - ADM00679 – Top Copper and Silk
 - ADM00679 – Top Copper
 - ADM00679 – Inner 1
 - ADM00679 – Inner 2
 - ADM00679 – Inner 3
 - ADM00679 – Inner 4
 - ADM00679 – Bottom Copper
 - ADM00679 – Bottom Copper and Silk
 - ADM00679 – Bottom Silk

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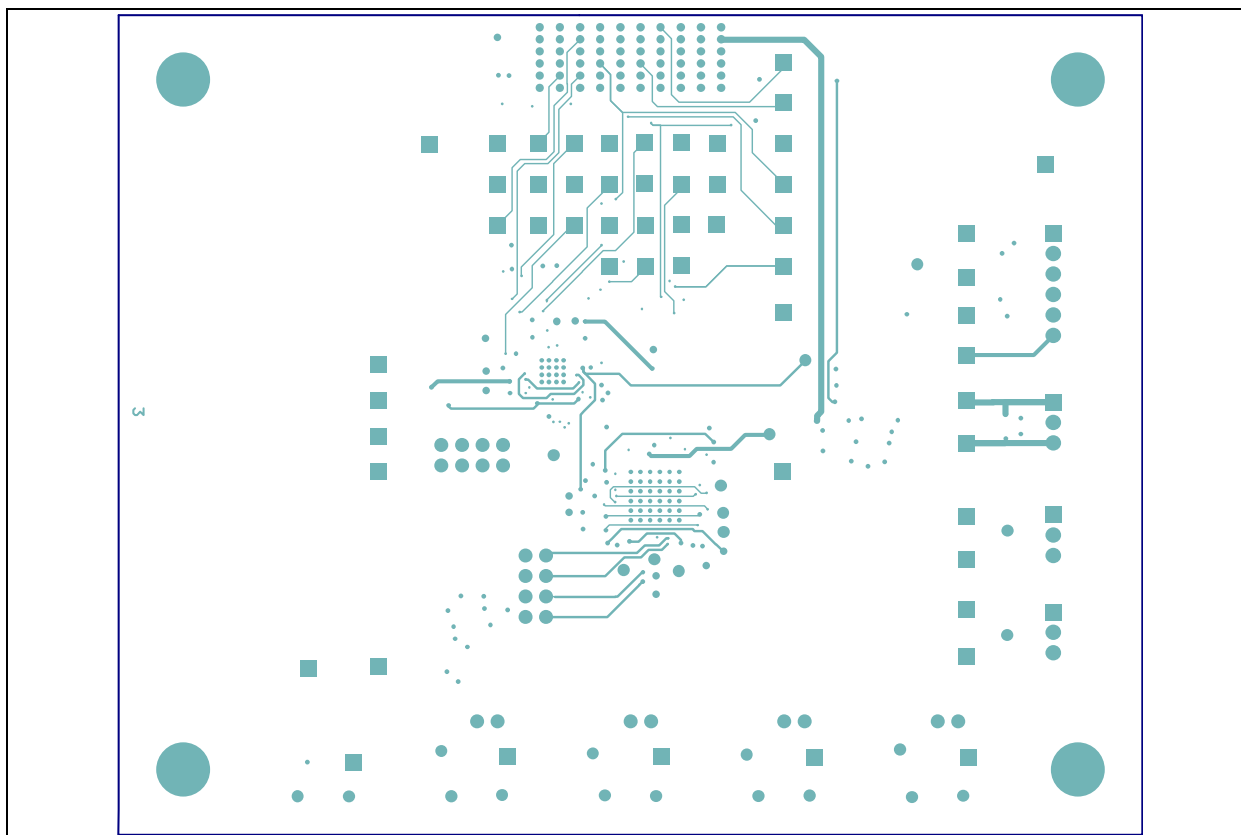
A.3 ADM00659 – TOP COPPER AND SILK



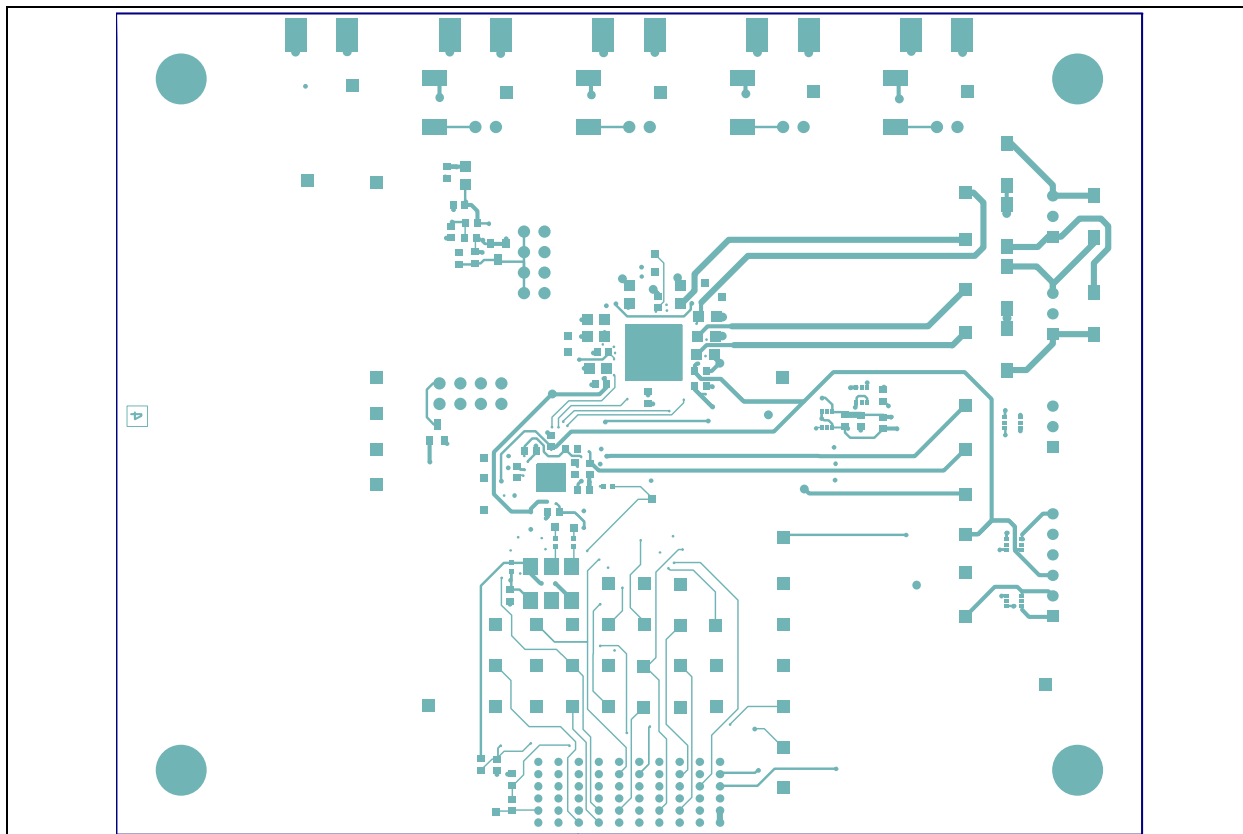
A.5 ADM00659 – INNER 1 – GND



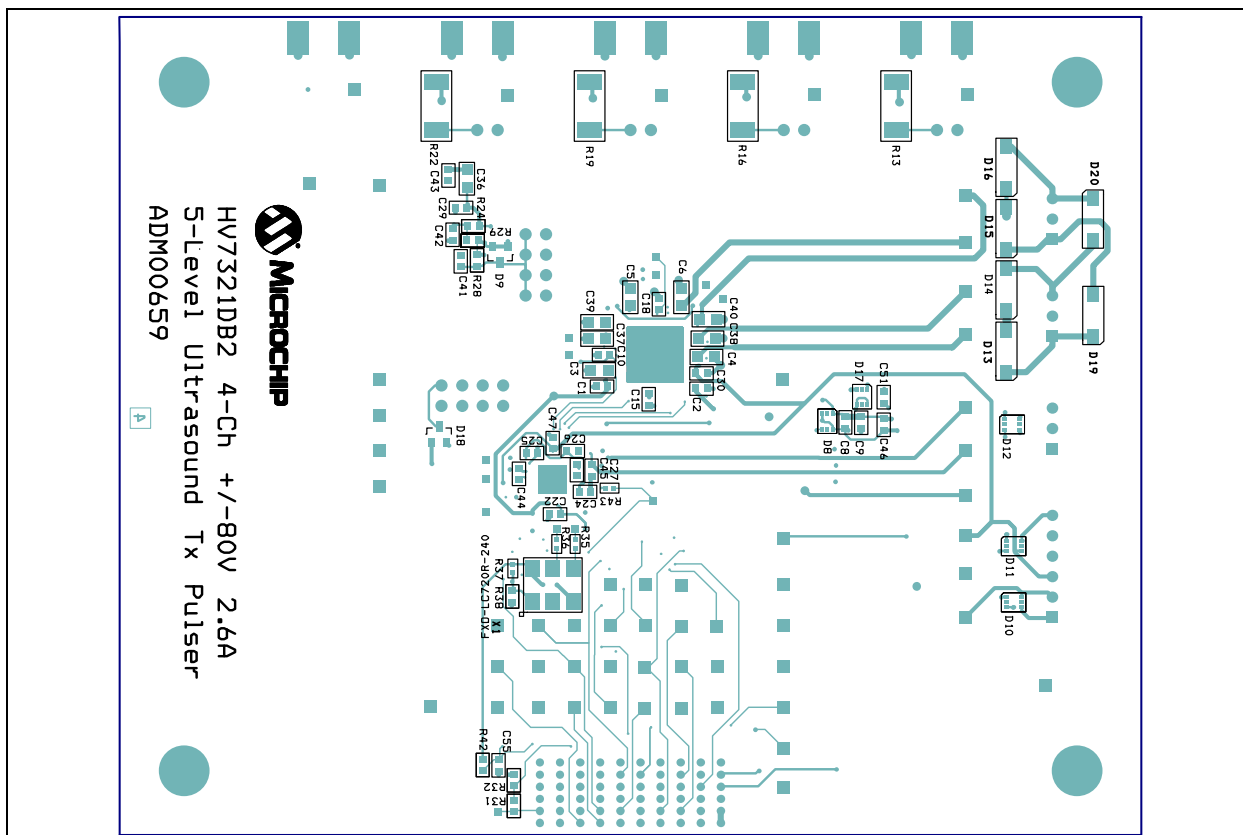
A.6 ADM00659 – INNER 2 – PWR



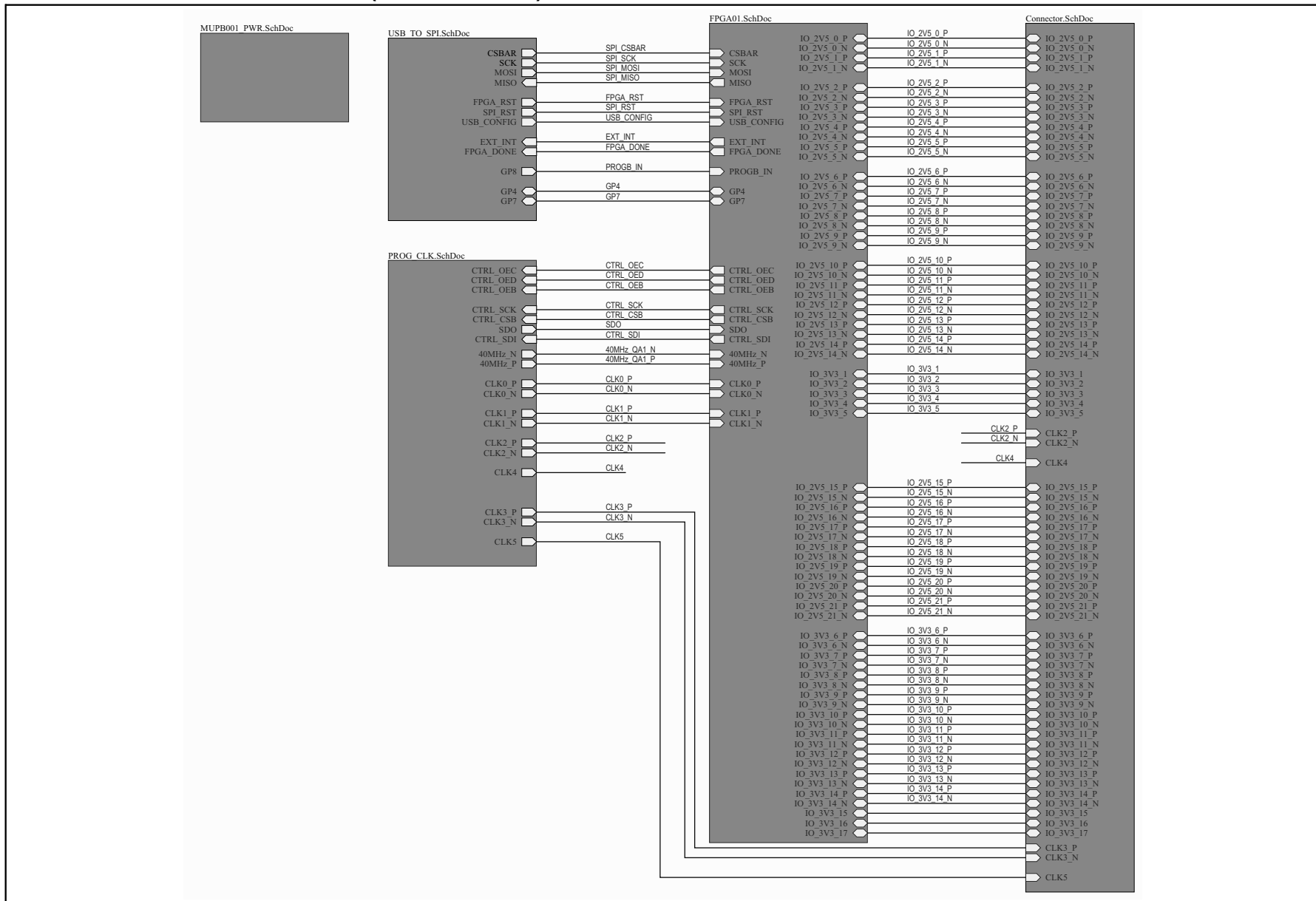
A.7 ADM00659 – BOTTOM COPPER



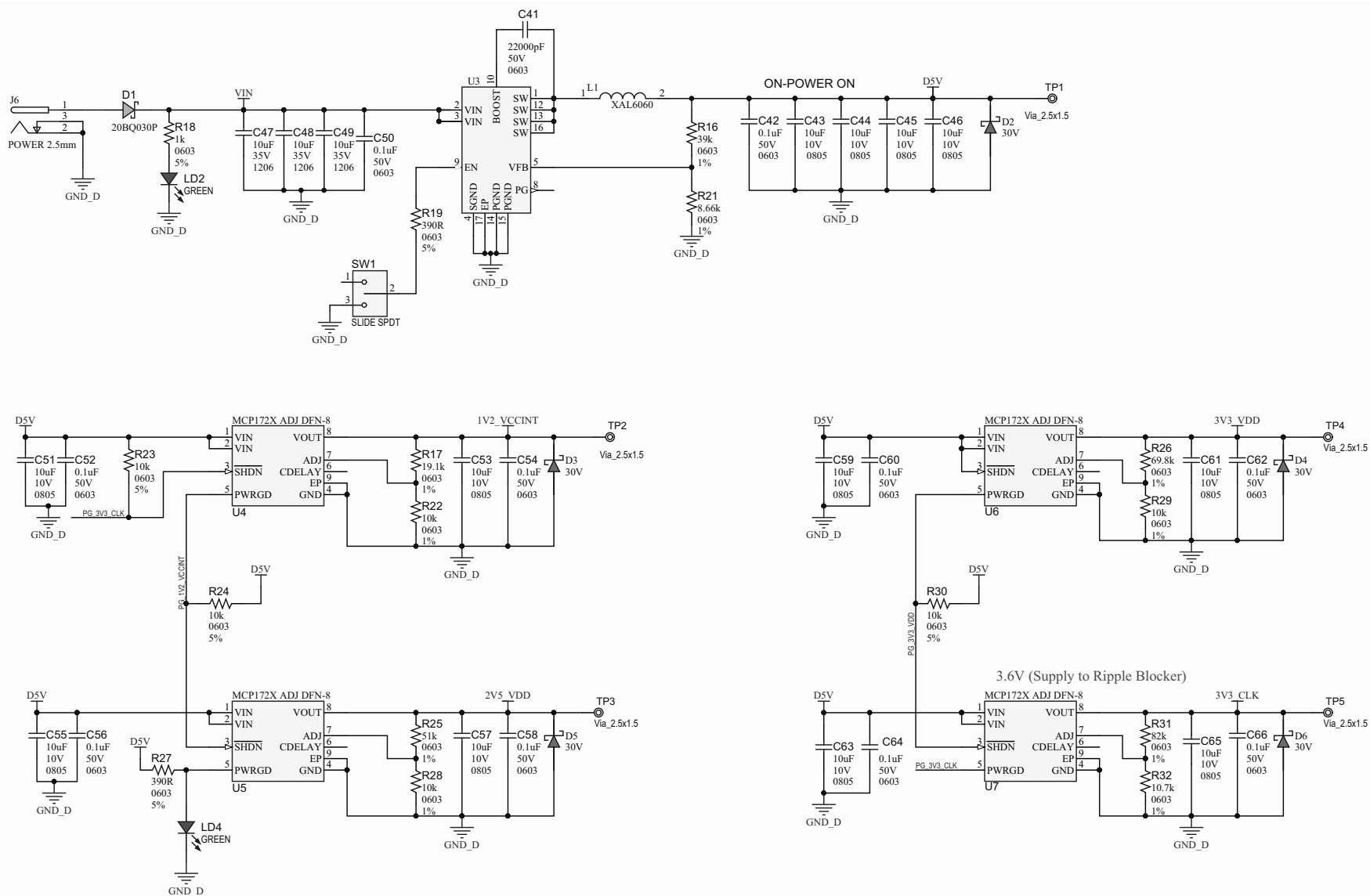
A.8 ADM00659 – BOTTOM COPPER AND SILK



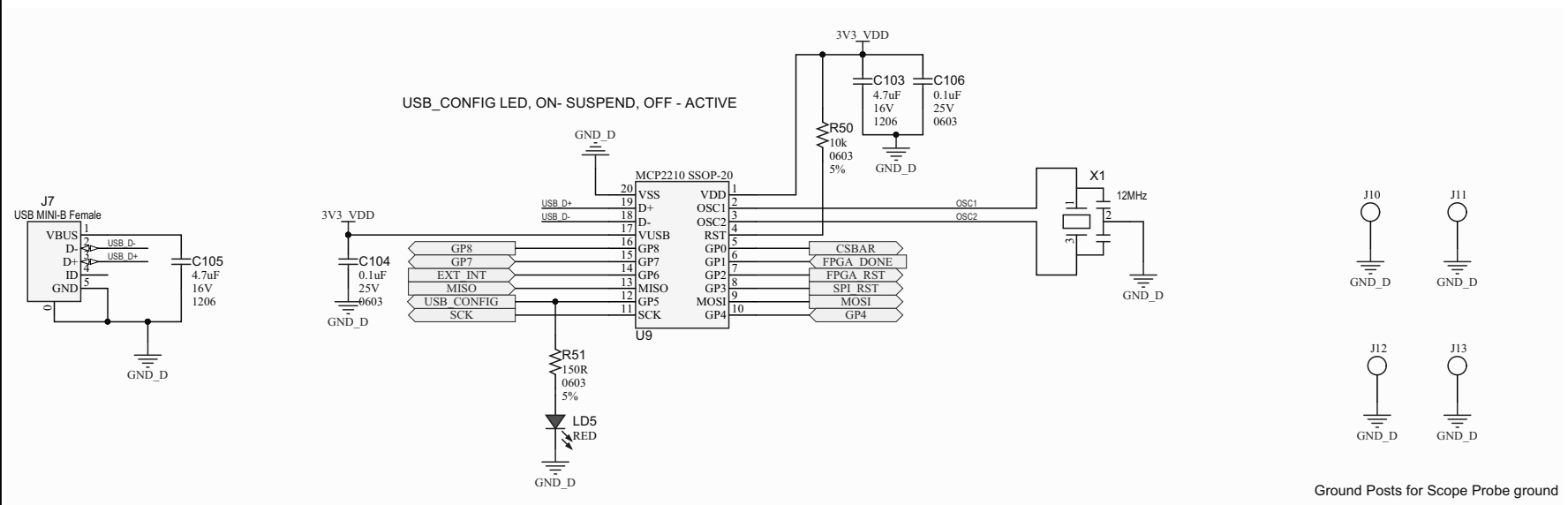
A.9 ADM00679 – SCHEMATIC (CONNECTION)



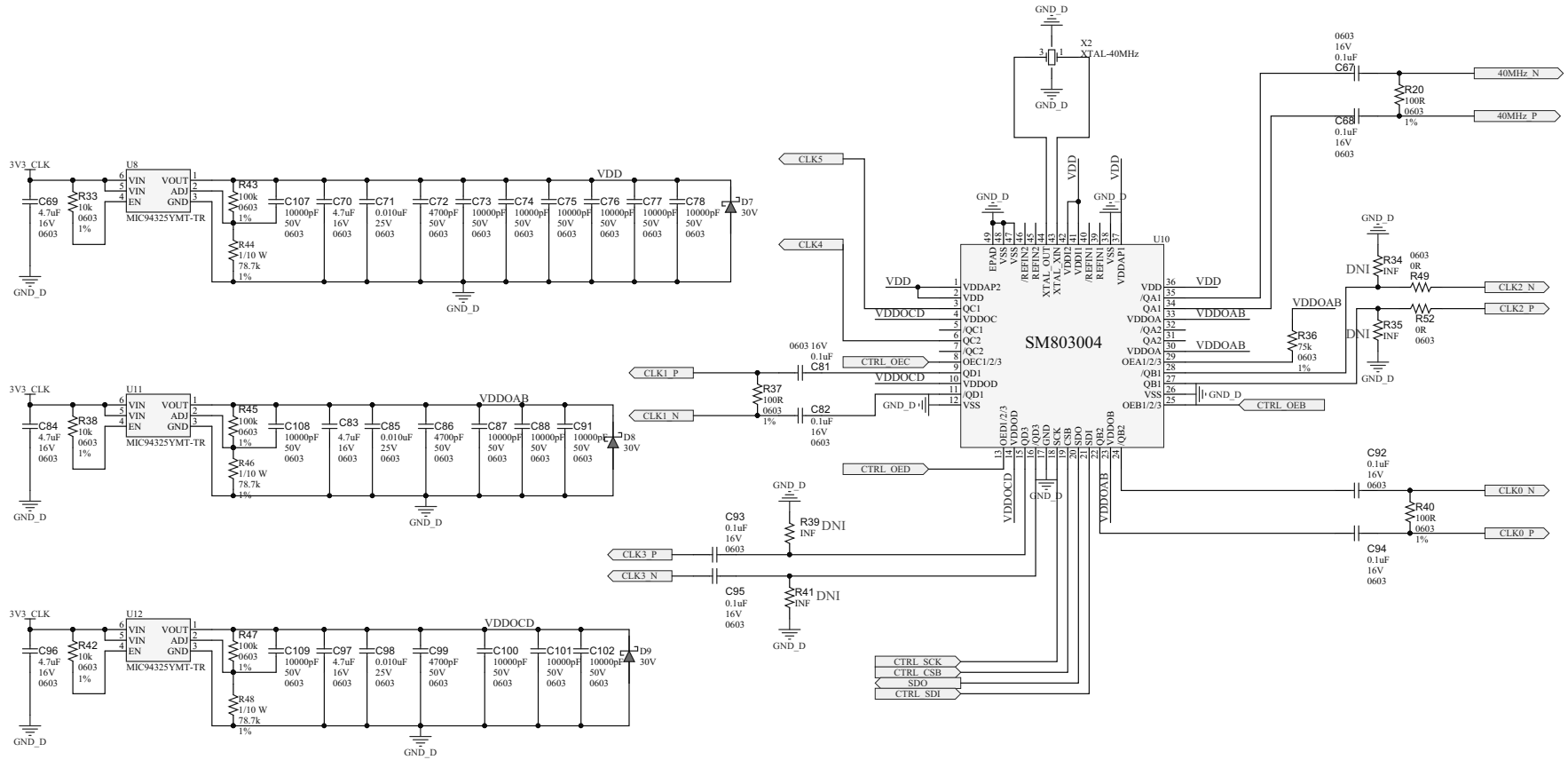
A.10 ADM00679 – SCHEMATIC (POWER SUPPLY)



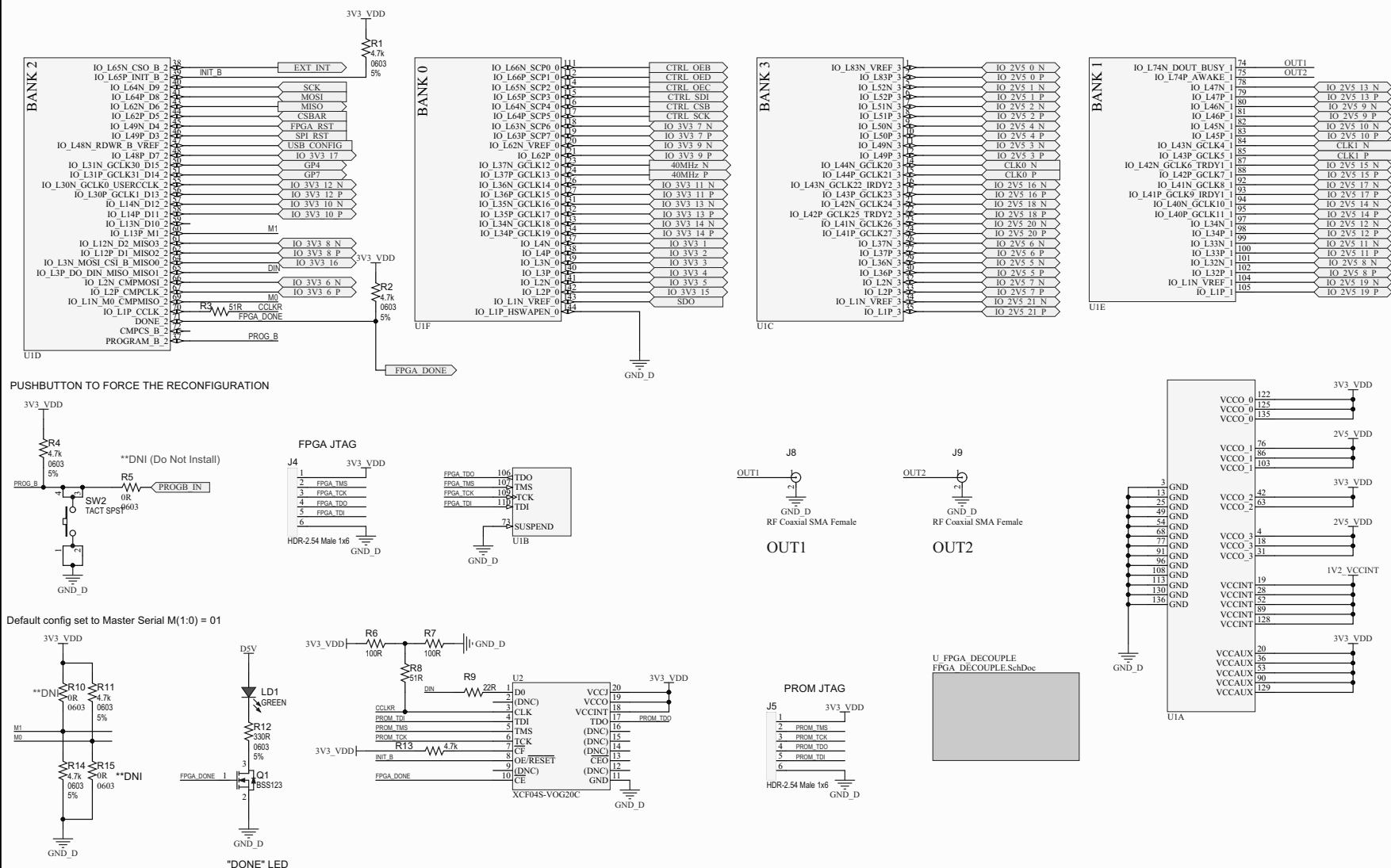
A.11 ADM00679 – SCHEMATIC (USB TO SPI)



A.12 ADM00679 – SCHEMATIC (PROGRAMMABLE CLOCK)

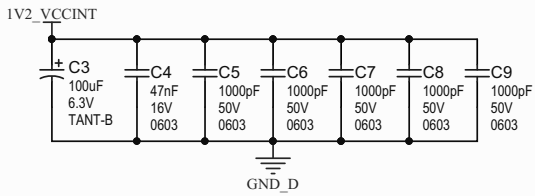


A.13 ADM00679 – SCHEMATIC (FPGA)

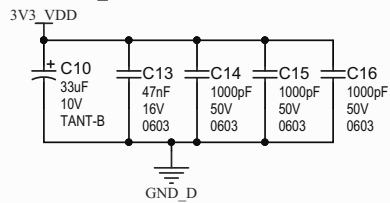


A.14 ADM00679 – SCHEMATIC (FPGA DECOUPLING CAPACITORS)

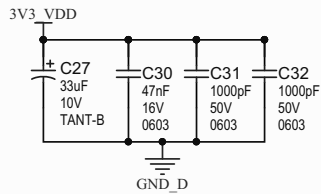
For 1V2_VCCINT



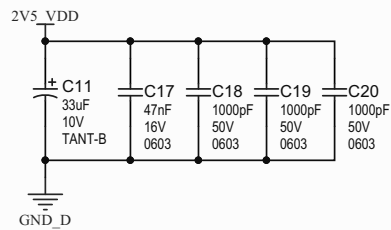
For VCCO_0



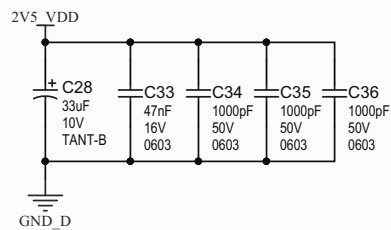
For VCCO_2



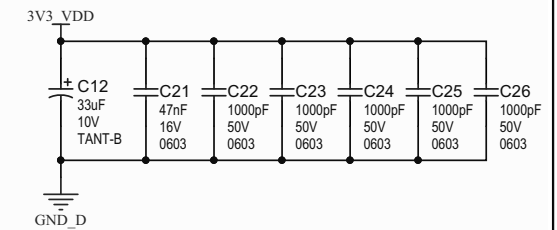
For VCCO_1



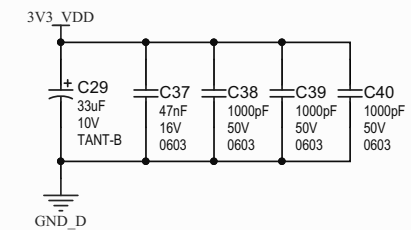
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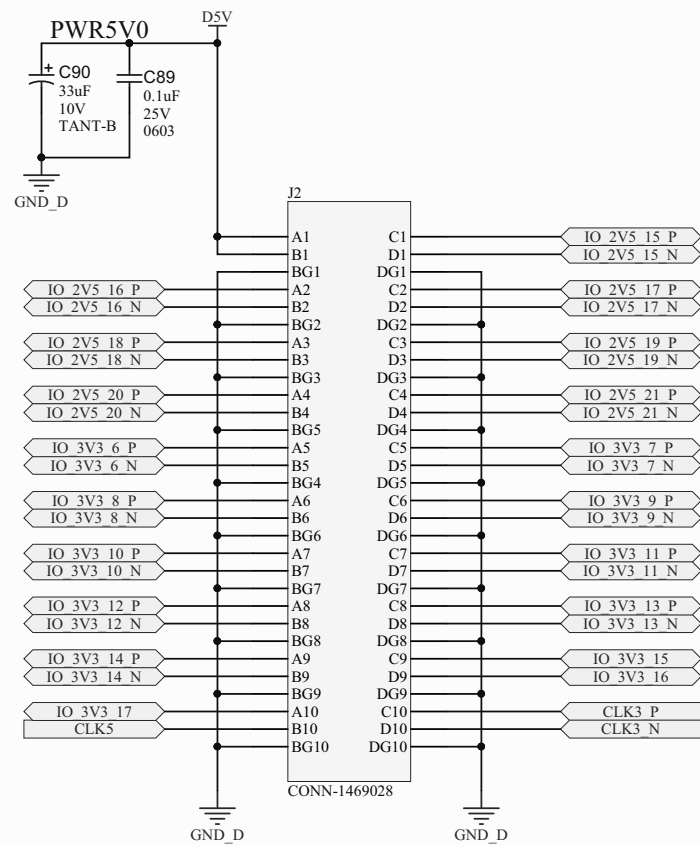
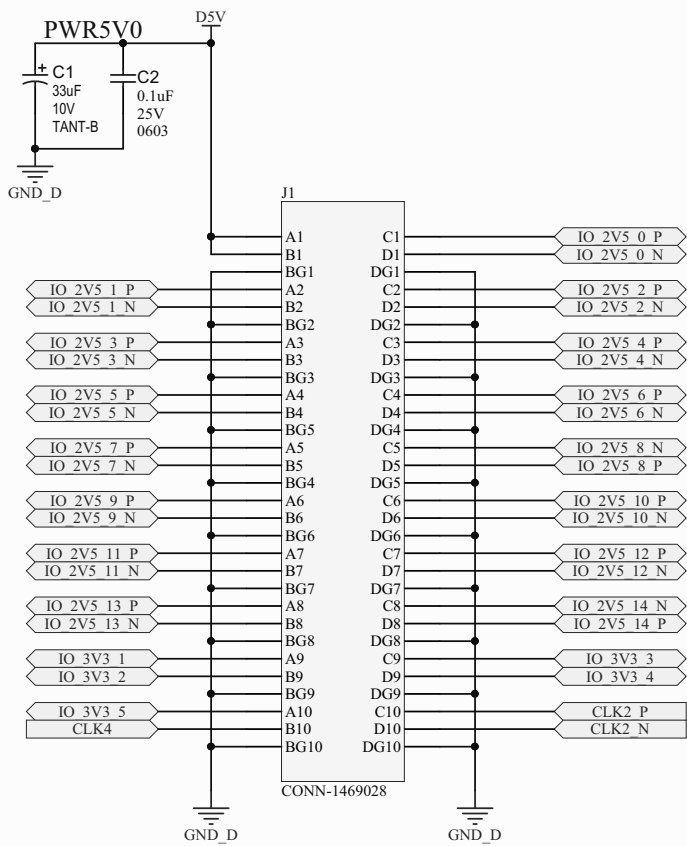
For VCCAUX



For XCF04S

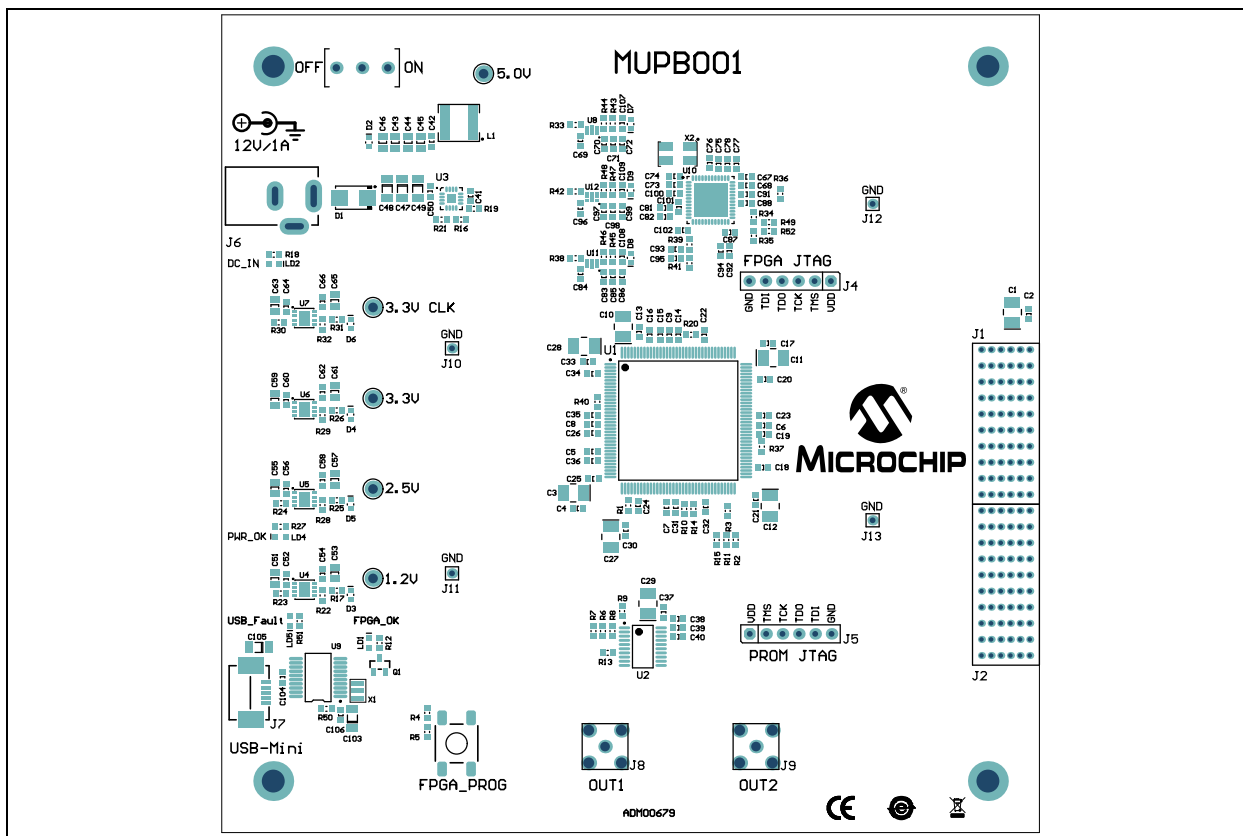


A.15 ADM00679 – SCHEMATIC (CONNECTORS)

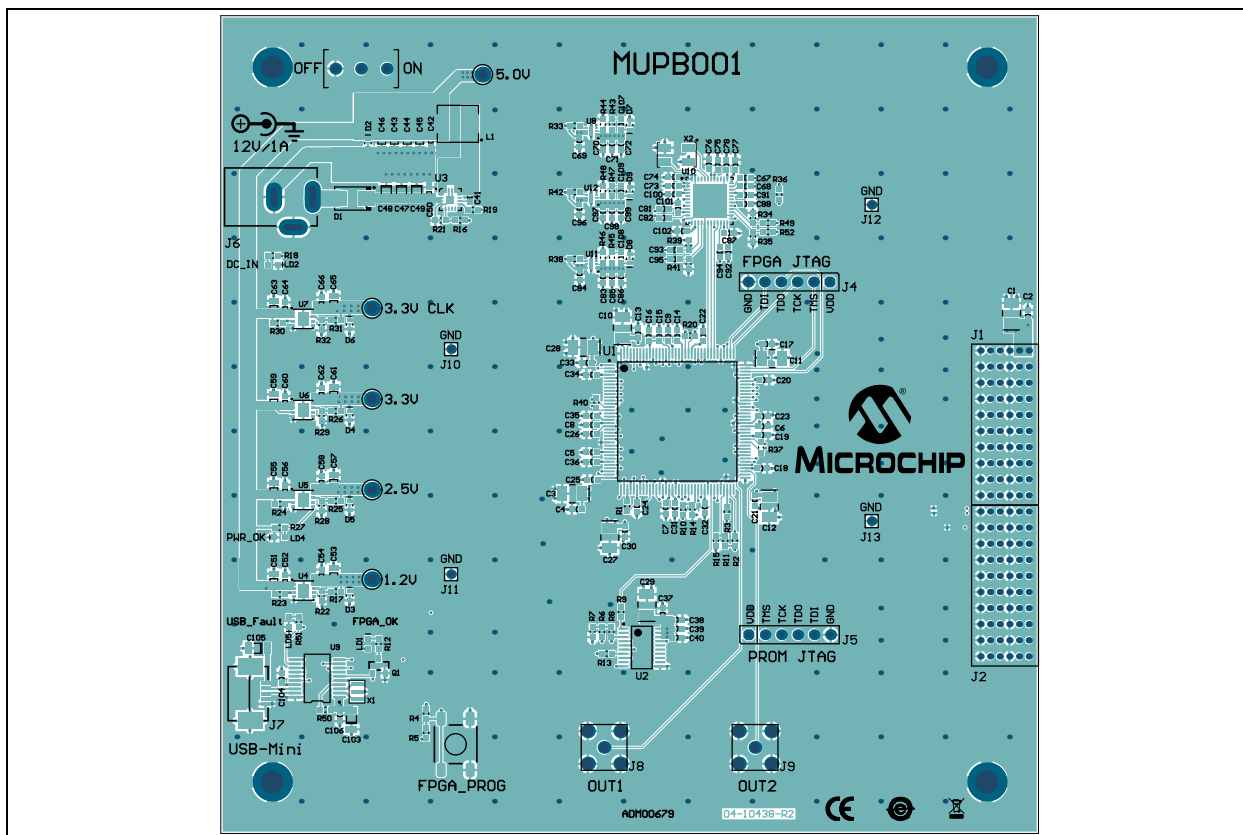


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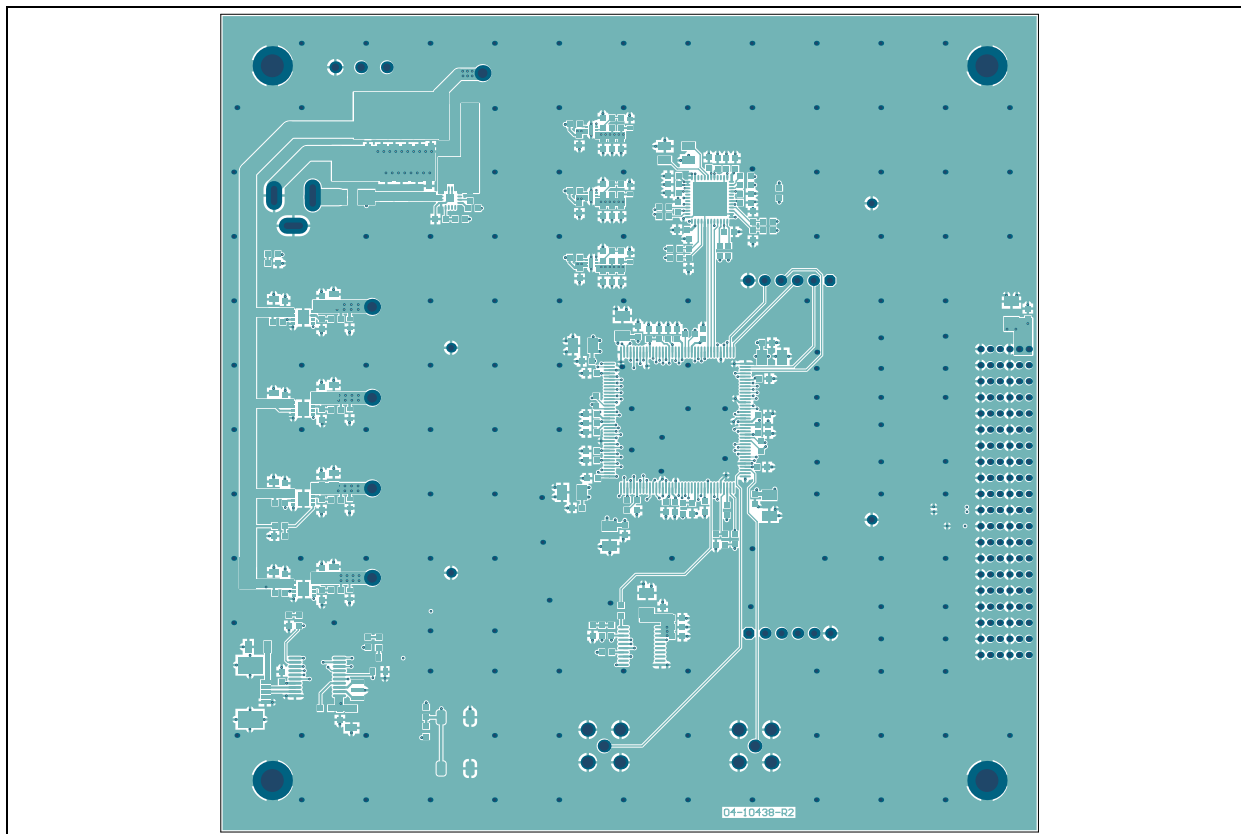
A.16 ADM00679 – TOP SILK



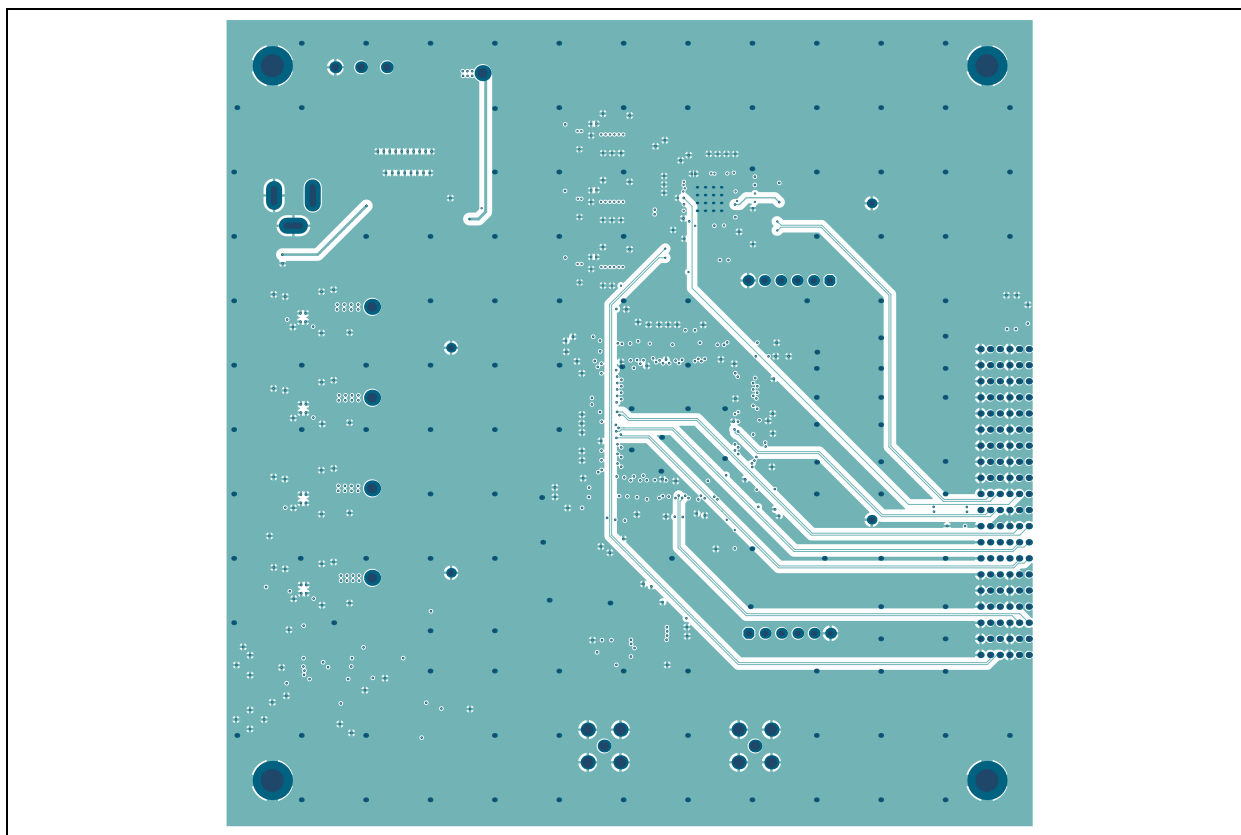
A.17 ADM00679 – TOP COPPER AND SILK



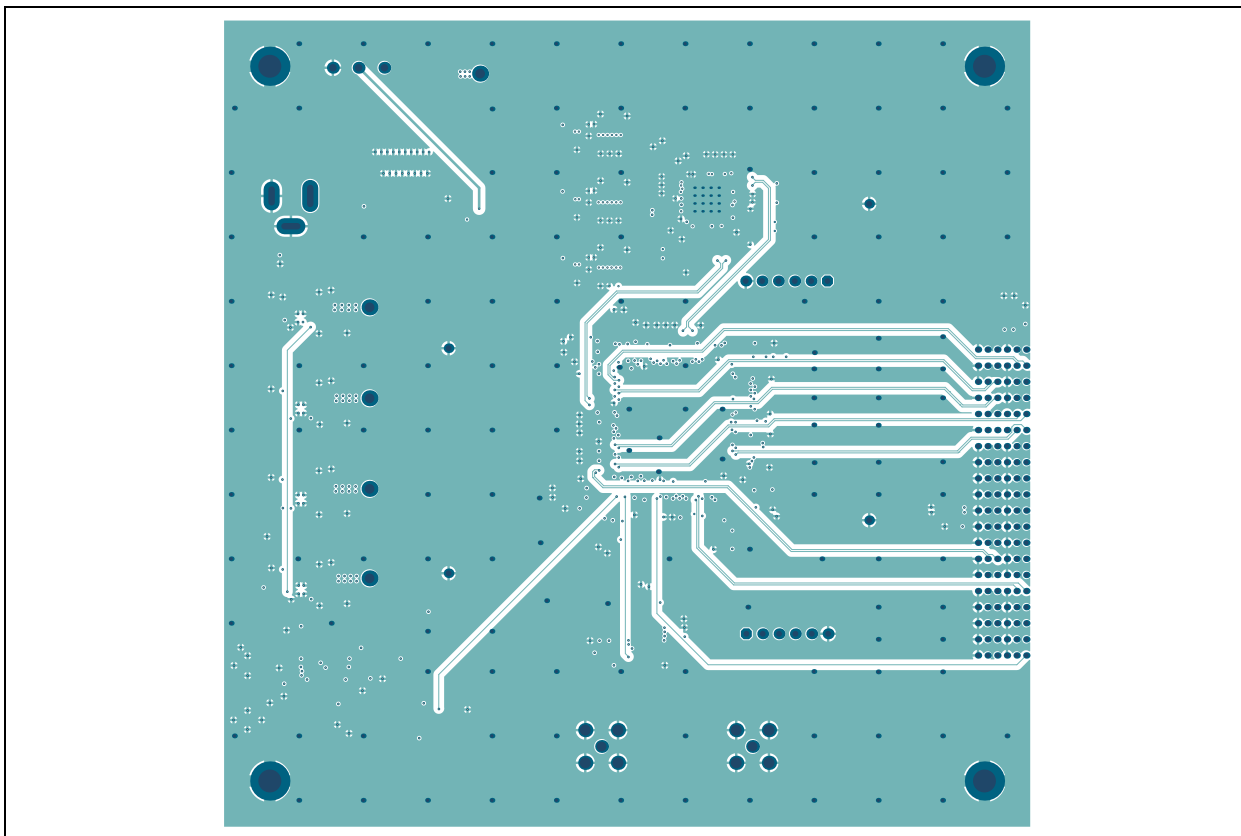
A.18 ADM00679 – TOP COPPER



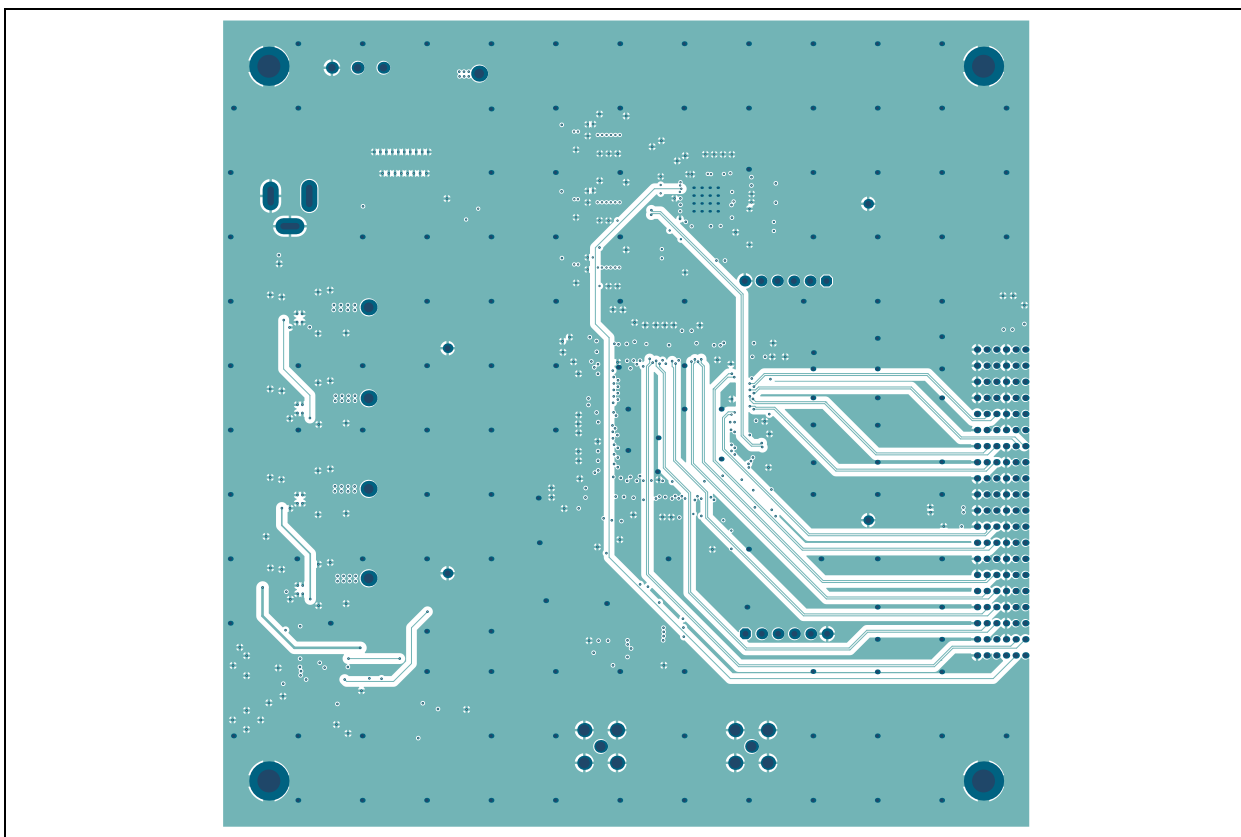
A.19 ADM00679 – INNER 1



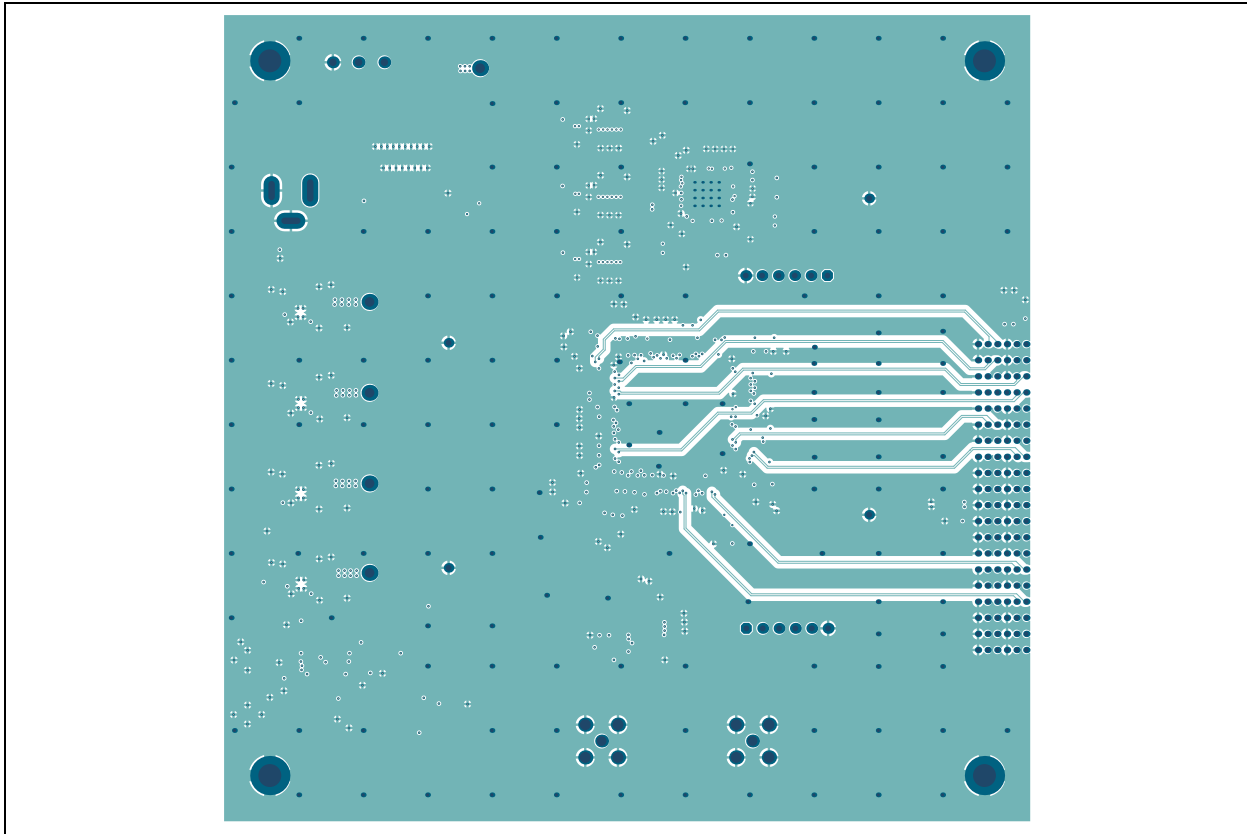
A.20 ADM00679 – INNER 2



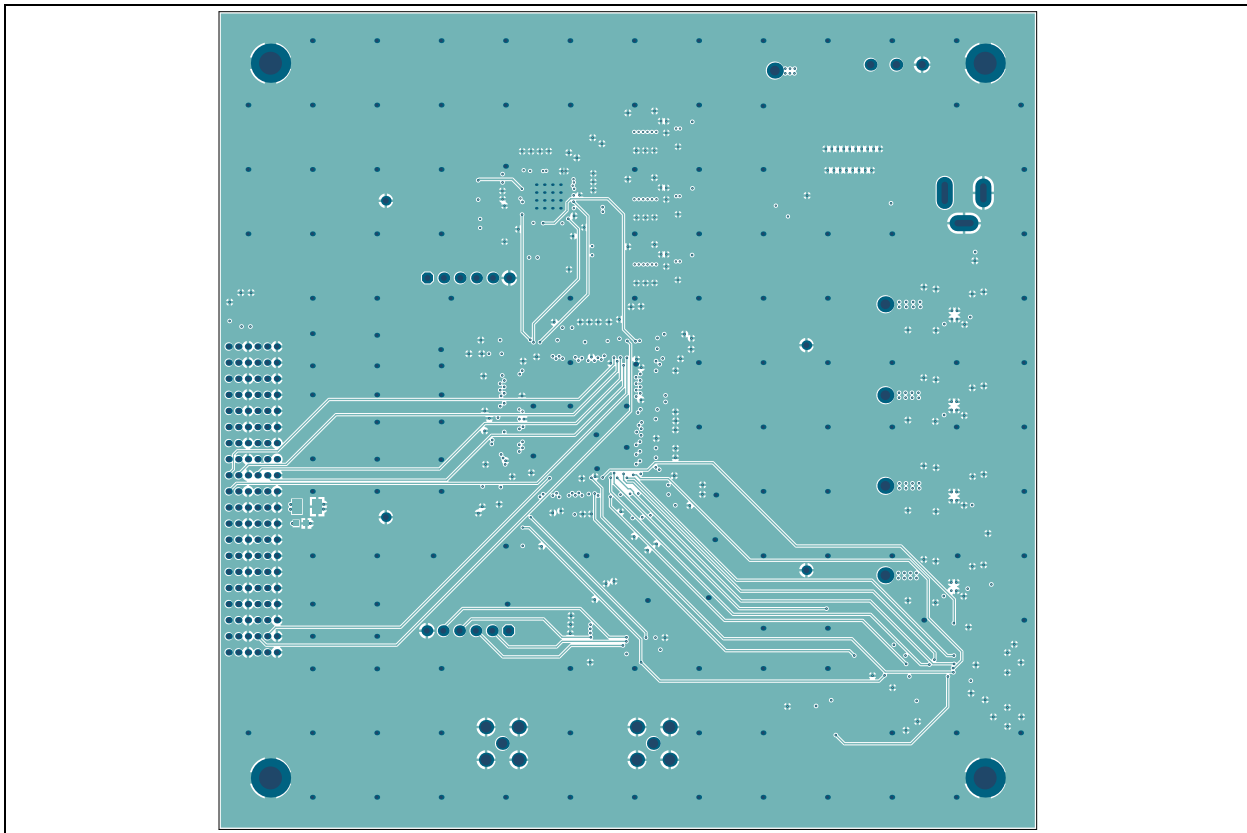
A.21 ADM00679 – INNER 3



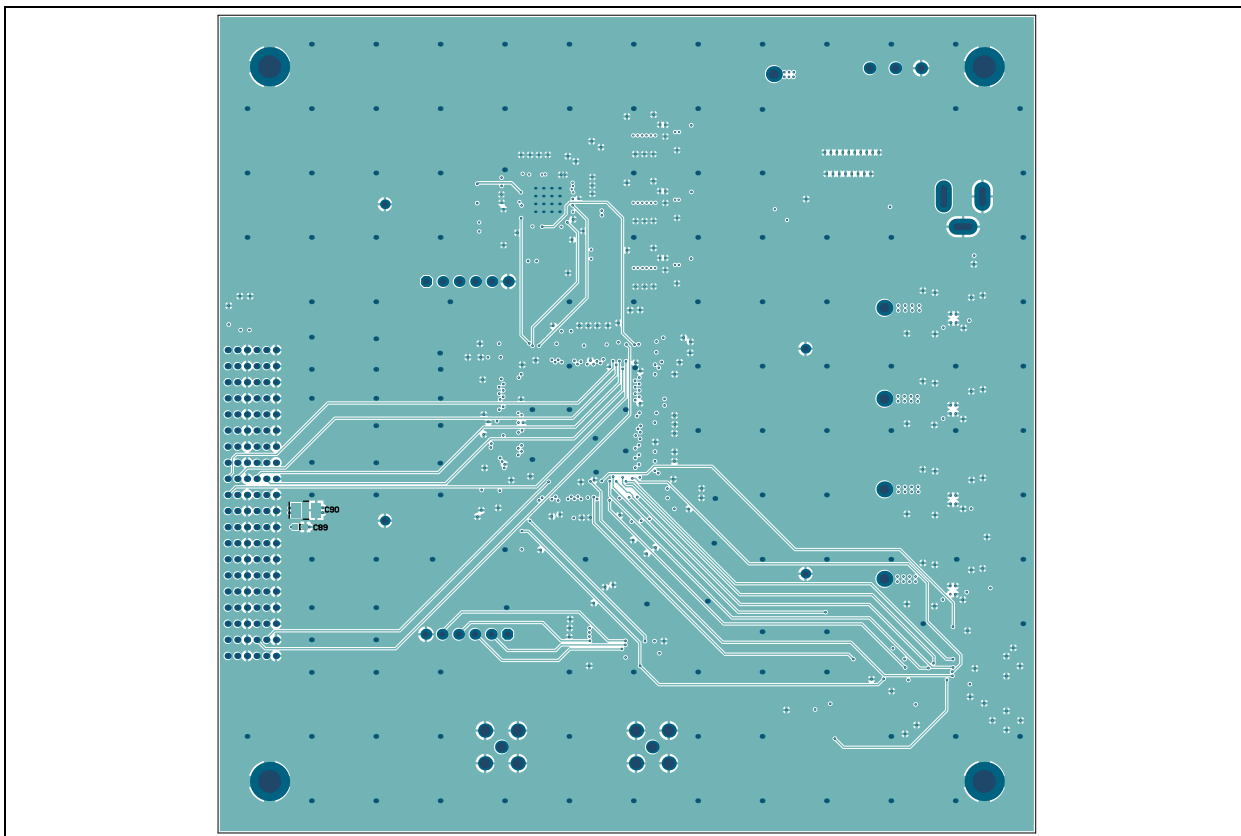
A.22 ADM00679 – INNER 4



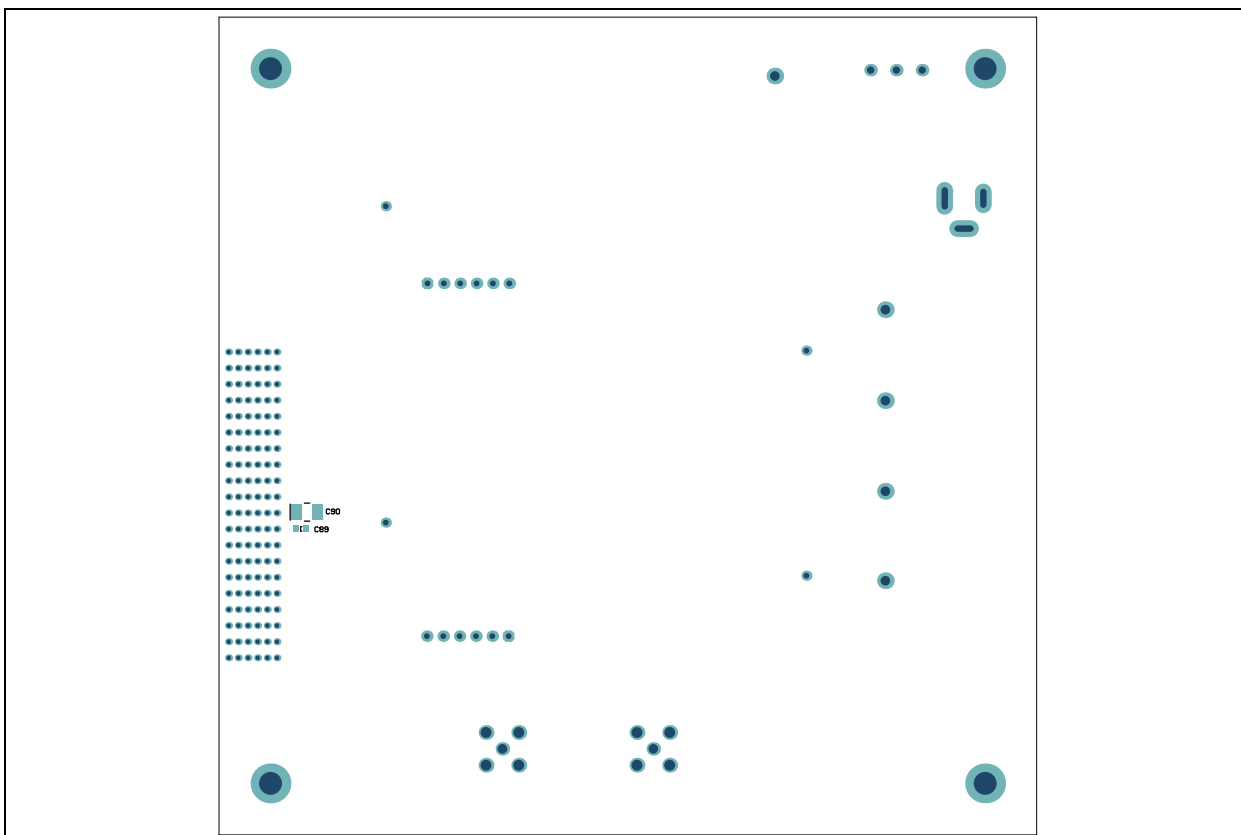
A.23 ADM00679 – BOTTOM COPPER



A.24 ADM00679 – BOTTOM COPPER AND SILK



A.25 ADM00679 – BOTTOM SILK



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NOTES:

Appendix B. Bill of Materials (BOM)

TABLE B-1: HV7321 ULTRASOUND TX PULSER EVALUATION BOARD (ADM00659)
BILL OF MATERIALS (BOM) (Note 1)

Qty.	Reference	Description	Manufacturer	Part Number
28	C1, C2, C8, C9, C12-18, C22, C23, C25, C26, C30-36, C44-46, C55-57	1 μ F 16V Ceramic Capacitor X7R 0603 (1608 Metric) 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	TDK Corporation	C1608X7R1C105M
8	C3-6, C37-40	1 μ F 100V Ceramic Capacitor X7S 0805 (2012 Metric) 0.079" L x 0.049" W (2.00 mm x 1.25 mm)	TDK Corporation	CGA4J3X7S2A105K125AB
2	C7, C29	0.22 μ F 16V Ceramic Capacitor X7R 0603 (1608 Metric) 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	TDK Corporation	C1608X7R1C224K
8	C10, C24, C27, C28, C47-50	2.2 μ F 16V Ceramic Capacitor X5R 0603 (1608 Metric) 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	TDK Corporation	C1608X5R1C225K080AB
4	C11, C19, C20, C21	220 pF 200V Ceramic Capacitor C0G, NP0 0805 (2012 Metric) 0.079" L x 0.049" W (2.00 mm x 1.25 mm)	Panasonic® - ECG	ECJ-2YC2D221J
3	C41, C42, C52	10000 pF 16V Ceramic Capacitor X7R 0603 (1608 Metric) 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	TDK Corporation	C1608X7R1C103K
1	C43	2 pF 50V Ceramic Capacitor C0G, NP0 0603 (1608 Metric) 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	TDK Corporation	CGJ3E2C0G1H020C080AA
1	C51	1000 pF 16V Ceramic Capacitor X7R 0603 (1608 Metric) 0.063" L x 0.032" W (1.60 mm x 0.81 mm)	AVX Corporation	0603YC102KAT2A
3	C53, C54, C112	0.10 μ F 10V Ceramic Capacitor X7R 0402 (1005 Metric) 0.039" L x 0.020" W (1.00 mm x 0.50 mm)	TDK Corporation	C1005X7R1A104K050BB
3	D1, D5, D6	Red LED Indication - Discrete 2V 0805 (2012 Metric)	Lumex® Inc.	SML-LXT0805IW-TR
1	D2	Green LED Indication - Discrete 2V 0805 (2012 Metric)	Lumex Inc.	SML-LXT0805GW-TR
3	D3, D4, D7	Yellow LED Indication - Discrete 2.1V 0805 (2012 Metric)	Lumex Inc.	SML-LXT0805YW-TR
5	D8, D10, D11, D12, D17	Diode Array 2 Independent Schottky 30V 100 mA Surface Mount 6-TSSOP, SC-88, SOT-363	Diodes Incorporated®	BAT54DW-7

Note 1: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

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**TABLE B-1: HV7321 ULTRASOUND TX PULSER EVALUATION BOARD (ADM00659)
BILL OF MATERIALS (BOM) (CONTINUED)(Note 1)**

Qty.	Reference	Description	Manufacturer	Part Number
2	D9, D18	Diode Array 1 Pair Series Connection Standard 70V 215 mA (DC) Surface Mount SC-70, SOT-323	ON Semiconductor®	BAV99WT1G
6	D13-16, D19, D20	Diode Schottky 100V 1A Surface Mount SMA	Diodes Incorporated	B1100-13F
5	J1, J2, J3 J4, J14	SMA Connector Jack, Female Socket 50Ω Board Edge, End Launch Solder	Cinch Connectivity Solutions	142-0711-821
2	J5, J23	CONN HEADER 40POS R/A HM-ZD TIN	TE Connectivity, Ltd.	6469169-1
12	J6-9 J15-22	2 Positions Header, Unshrouded, Breakaway Connector 0.100" (2.54 mm) Through Hole Gold	Molex®	22-28-4023
5	J6 J19-22	2 (1 x 2) Position Shunt Connector Black Open Top 0.100" (2.54 mm) Gold	TE Connectivity, Ltd.	382811-8
1	J10	6 Positions Header, Unshrouded Connector 0.100" (2.54mm) Through Hole Gold	TE Connectivity, Ltd.	3-641213-6
3	J11-J13	3 Positions Header, Unshrouded Connector 0.100" (2.54 mm) Through Hole Gold	TE Connectivity, Ltd.	641213-3
4	MH1-MH4	Hex Standoff Threaded #4-40 Aluminum 0.250" (6.35mm) 1/4"	Keystone Electronics Corp.	1891
4	MH1-MH4	Machine Screw Pan Phillips 4-40	B&F™ Fasteners Supply	NY PMS 440 0025 PH
1	PCB	HV7321 Ultrasound TX Pulser Evaluation Board – Printed Circuit Board	—	04-10398
4	R1, R2 R25, R26	RES SMD 0.1 OHM 5% 1/5W 0603	Panasonic - ECG	ERJ-L03KJ10CV
7	R3, R14 R17, R18 R20, R23 R33	RES SMD 49.9 OHM 1% 1/10W 0603	Panasonic - ECG	ERJ-3EKF49R9V
8	R5-11 R38	RES SMD 200 OHM 5% 1/10W 0603	Panasonic - ECG	ERJ-3GEYJ201V
2	R12 R44	RES SMD 0.0OHM JUMPER 1/10W 0603	Panasonic - ECG	ERJ-3GEY0R00V
4	R13, R16 R19, R22	RES SMD 49.9 OHM 1% 1/10W 0603	Panasonic - ECG	ERJ-3EKF49R9V
2	R24 R29	RES SMD 499 OHM 1% 1/10W 0603	Panasonic - ECG	ERJ-3EKF4990V
1	R27	RES SMD 249 OHM 1% 1/10W 0603	Panasonic - ECG	ERJ-3EKF2490V
3	R28, R32 R39	RES SMD 1K OHM 1% 1/10W 0603	Panasonic - ECG	ERJ-3EKF1001V
2	R30 R34	RES SMD 100 OHM 1% 1/10W 0603	Panasonic - ECG	ERJ-3EKF1000V
7	R31, R35-37	DO NOT POPULATE	—	—

Note 1: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

**TABLE B-1: HV7321 ULTRASOUND TX PULSER EVALUATION BOARD (ADM00659)
BILL OF MATERIALS (BOM) (CONTINUED)(Note 1)**

Qty.	Reference	Description	Manufacturer	Part Number
2	R40, R41	RES SMD 100 OHM 1% 1/10W 0402	Panasonic - ECG	ERJ-2RKF1000X
2	R42, R43	RES SMD 0.00HM JUMPER 1/10W 0402	Panasonic - ECG	ERJ-2GE0R00X
3	TP50, TP61 TP65	PC Pin Terminal Connector Free Hanging (In-Line) Gold 0.030" (0.76mm) Dia.	Mill-Max Mfg. Corporation	3132-0-00-15-00-00-08-0
1	U1	High-Voltage Ultrasound Pulser with T/R Switches	Microchip Technology Inc.	HV7321K6-G
1	U2	Ultra-Low Phase Noise Continuous Waveform Transmitter with Beamformer	Microchip Technology Inc.	MD1730-V/M2
1	U3	Low-Voltage, Low-Quiescent Current LDO Regulator	Microchip Technology Inc.	MCP1727-2502E/SN
1	U4	Rail-to-Rail Output Op Amp	Microchip Technology Inc.	MCP661-E/SN
1	U6	Voltage Feedback Amplifier 1 Circuit 8-SOIC-EP	Analog Devices Inc.	AD8099ARDZ-REEL7
1	X1	200 MHz LVDS XO (Standard) Oscillator Surface Mount 2.5V 34 mA Enable/Disable	Fox Electronics	FXO-LC726R-200

Note 1: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

**TABLE B-2: MUPB001 MICROCHIP ULTRASOUND PLATFORM BOARD (ADM00679)
BILL OF MATERIALS (BOM) (Note 1)**

Qty.	Reference	Description	Manufacturer	Part Number
8	C1 C10-C12 C27-C29 C90	33 μ F Molded Tantalum Capacitors 10V 1411 (3528 Metric) 1.4 Ohm 0.138" L x 0.110" W (3.50 mm x 2.80 mm)	KEMET	T494B336K010AT
4	C2, C89 C104, C106	0.10 μ F 25V Ceramic Capacitor X7R 0603 (1608 Metric) 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	Murata Electronics North America, Inc.	GRM188R71E104KA01D
1	C3	100 μ F Molded Tantalum Capacitors 6.3V 1210 (3528 Metric) 400 mOhm 0.138" L x 0.110" W (3.50 mm x 2.80 mm)	AVX Corporation	TPSB107K006R0400
7	C4, C13 C17, C21 C30, C33 C37	0.047 μ F 16V Ceramic Capacitor X7R 0603 (1608 Metric) 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	Murata Electronics North America, Inc.	GRM188R71C473KA01D
24	C5-C9 C14-C16 C18-C20 C22-C26 C31, C32 C34-C36 C38-C40	1000 pF 50V 10% Ceramic Capacitor X7R MLCC 0603	NIC Components Corp.	NMC0603X7R102K50TRPF

Note 1: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

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**TABLE B-2: MUPB001 MICROCHIP ULTRASOUND PLATFORM BOARD (ADM00679)
BILL OF MATERIALS (BOM) (CONTINUED)(Note 1)**

Qty.	Reference	Description	Manufacturer	Part Number
1	C41	0.022 μ F 50V Ceramic Capacitor X7R 0603 (1608 Metric) 0.063" L x 0.032" W (1.60 mm x 0.81 mm)	AVX Corporation	06035C223JAT2A
10	C42, C50 C52, C54 C56, C58 C60, C62 C64, C66	0.10 μ F 50V Ceramic Capacitor X7R 0603 (1608 Metric) 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	TDK Corporation	C1608X7R1H104M080AA
3	C47-C49	10 μ F 35V Ceramic Capacitor X5R 1206 (3216 Metric) 0.126" L x 0.063" W (3.20 mm x 1.60 mm)	Taiyo Yuden Co., Ltd.	GMK316BJ106KL-T
8	C67, C68 C81, C82 C92-C95	0.10 μ F 16V Ceramic Capacitor X7R 0603 (1608 Metric) 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	Samsung Electro-Mechanics America, Inc.	CL10B104K08NNNC
9	C69, C70 C83, C84 C96, C97 C107-C109	4.7 μ F 16V Ceramic Capacitor X5R 0603 (1608 Metric) 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	TDK Corporation	C1608X5R1C475K080AC
3	C71, C85 C98	10000 pF 25V Ceramic Capacitor X7R 0603 (1608 Metric) 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	Yageo Corporation	CC0603KRX7R8BB103
3	C72, C86 C99	4700 pF 50V Ceramic Capacitor X7R 0603 (1608 Metric) 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	KEMET	C0603C472K5RACTU
12	C73-C78 C87, C88 C91 C100-C102	10000 pF 50V Ceramic Capacitor X7R 0603 (1608 Metric) 0.063" L x 0.032" W (1.60 mm x 0.81 mm)	AVX Corporation	06035C103KAT2A
2	C103, C105	4.7 μ F 16V Ceramic Capacitor X7R 1206 (3216 Metric) 0.126" L x 0.063" W (3.20 mm x 1.60 mm)	KEMET	C1206C475K4RACTU
1	D1	Diode Schottky 30V 2A Surface Mount SMB	Vishay Intertechnology, Inc.	VS-20BQ030TRPBF
8	D2-D9	Diode Schottky 30V 200 mA (DC) Surface Mount SOD-523	Micro Commercial Components	BAT54WX-TP
2	J1 J2	CONN RCPT 40 POS 2 ROW RT ANG T/H	TE Connectivity AMP Connectors	1469028-1
2	J4 J5	6 Positions Header, Unshrouded, Breakaway Connector 0.100" (2.54 mm) Through Hole Tin	Sullins Connector Solutions	PEC06SAAN
1	J6	Power Barrel Connector Jack 2.50 mm ID (0.098"), 5.50 mm OD (0.217") Through Hole, Right Angle	CUI Inc.	PJ-002B
1	J7	USB - mini B USB 2.0 Receptacle Connector 5 Position Surface Mount, Right Angle, Horizontal	Hirose Electric Co., Ltd.	UX60SC-MB-5ST(80)
2	J8 J9	SMA Connector Jack, Female Socket 50 Ω Through Hole Solder	TE Connectivity, Ltd.	5-1814832-1

Note 1: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

**TABLE B-2: MUPB001 MICROCHIP ULTRASOUND PLATFORM BOARD (ADM00679)
BILL OF MATERIALS (BOM) (CONTINUED)(Note 1)**

Qty.	Reference	Description	Manufacturer	Part Number
4	J10-J13	PC Pin Terminal Connector Free Hanging (In-Line) Gold 0.030" (0.76 mm) Dia	Mill-Max Mfg. Corporation	3132-0-00-15-00-00-08-0
1	L1	Fixed Inductors XAL6060 High Current 4.7 μ H 20% 11A	Coilcraft	XAL6060-472MEB
3	LD1, LD2 LD4	Green 568 nm LED Indication - Discrete 2.2V 0603 (1608 Metric)	Kingbright Electronics Co., Ltd.	APT1608SGC
1	LD5	Red 633 nm LED Indication - Discrete 2V 0603 (1608 Metric)	OSRAM Opto Semiconductors GmbH.	LS Q976-NR-1
1	Q1	MOSFET N-CH 100V 170 mA SOT23-3	Diodes Incorporated®	BSS123-7-F
1	PCB	MUPB001 – Printed Circuit Board	—	04-10438
6	R1, R2, R4 R11, R13 R14	RES SMD 4.7K OHM 5% 1/10W 0603	Panasonic - ECG	ERJ-3GEYJ472V
2	R3 R8	RES SMD 51 OHM 5% 1/10W 0603	Panasonic - ECG	ERJ-3GEYJ510V
3	R5, R10 R15	RES TKF 0R 1/10W SMD 0603	NIC Components Corp.	NRC06Z0TRF
6	R5, R10 R34, R35 R39, R41	DO NOT POPULATE	—	—
2	R6 R7	RES SMD 100 OHM 5% 1/10W 0603	Vishay/Dale	CRCW0603100RJNEA
1	R9	RES SMD 22 OHM 5% 1/10W 0603	Panasonic - ECG	ERJ-3GEYJ220V
1	R12	330 Ω $\pm$ 5% 0.063W, 1/16W Temperature Sensitive Specialized Resistor Metal Film 3300 ppm/ $^{\circ}$ C Surface Mount	Panasonic - ECG	ERA-V33J331V
1	R16	RES SMD 39K OHM 1% 1/10W 0603	Panasonic - ECG	ERJ-3EKF3902V
1	R17	RES SMD 19.1K OHM 1% 1/10W 0603	Panasonic - ECG	ERJ-3EKF1912V
1	R18	RES SMD 1K OHM 5% 1/10W 0603	Panasonic - ECG	ERJ-3GEYJ102V
2	R19, R27	RES SMD 390 OHM 5% 1/10W 0603	Panasonic - ECG	ERJ-3GEYJ391V
3	R20, R37 R40	RES SMD 100 OHM 1% 1/10W 0603	Panasonic - ECG	ERJ-3EKF1000V
1	R21	RES SMD 8.66K OHM 1% 1/10W 0603	Yageo Corporation	RC0603FR-078K66L
6	R22, R28 R29, R33 R38, R42	RES SMD 10K OHM 1% 1/8W 0603	Vishay Beyschlag	MCT06030C1002FP500
1	R25	RES SMD 51K OHM 1% 1/10W 0603	Panasonic - ECG	ERJ-3EKF5102V
1	R26	RES SMD 69.8K OHM 1% 1/10W 0603	Panasonic - ECG	ERJ-3EKF6982V

Note 1: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

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**TABLE B-2: MUPB001 MICROCHIP ULTRASOUND PLATFORM BOARD (ADM00679)
BILL OF MATERIALS (BOM) (CONTINUED)(Note 1)**

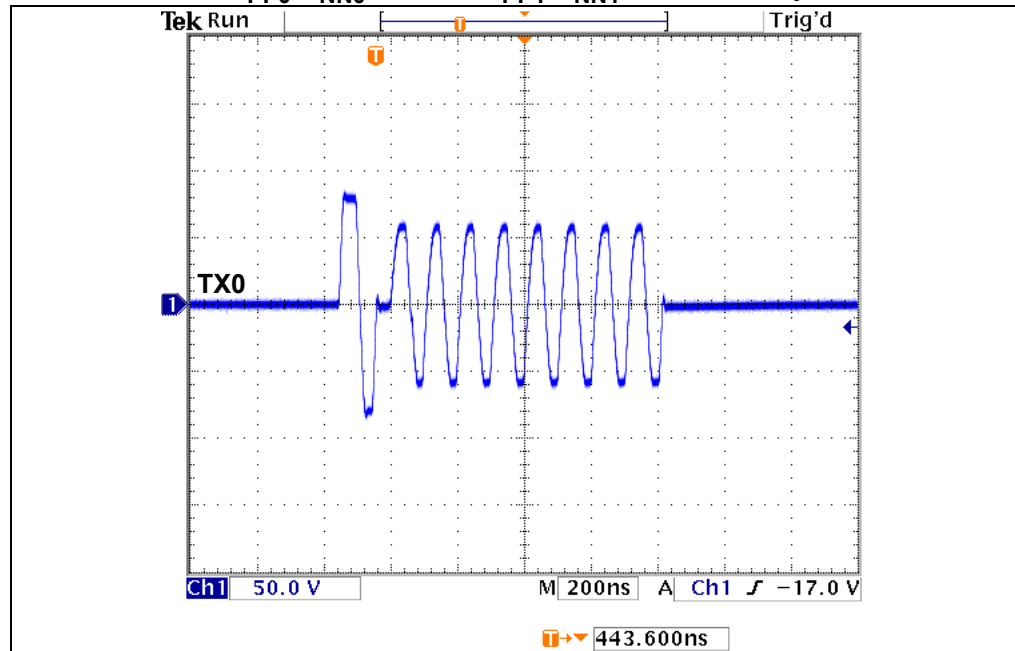
Qty.	Reference	Description	Manufacturer	Part Number
4	R23, R24 R30, R50	RES SMD 10K OHM 5% 1/10W 0603	Panasonic - ECG	ERJ-3GEYJ103V
1	R31	RES SMD 82K OHM 1% 1/10W 0603	Panasonic - ECG	ERJ-3EKF8202V
1	R32	RES SMD 10.7K OHM 1% 1/10W 0603	Panasonic - ECG	ERJ-3EKF1072V
4	R34, R35 R39, R41	RES SMD 150 OHM 1% 1/10W 0603	Stackpole Electronics, Inc.	RMCF0603FT150R
1	R36	RES SMD 75K OHM 1% 1/10W 0603	Panasonic - ECG	ERJ-3EKF7502V
3	R43, R45 R47	RES SMD 100K OHM 1% 1/10W 0603	Panasonic - ECG	ERJ-3EKF1003V
3	R44, R46 R48	RES SMD 78.7K OHM 1% 1/10W 0603	Yageo Corporation	RC0603FR-0778K7L
2	R49 R52	RES SMD 0.0OHM JUMPER 1/10W 0603	Panasonic - ECG	ERJ-3GEY0R00V
1	R51	RES SMD 150 OHM 5% 1/10W 0603	Panasonic - ECG	ERJ-3GEYJ151V
1	SW1	Switch Slide Min. Single Pole Dou- ble Throw On-On PCB Mount 50 Volt DC @ 0.5 Amps Lead 4 mm	Jameco Valuepro	SS-12F56-4
1	SW2	Tactile Switch SPST-NO Top Actu- ated Surface Mount	E-Switch®, Inc.	TL3301NF260QG
1	U1	IC FPGA 102 I/O 144TQFP	Xilinx Inc.	XC6SLX9-2TQG144C
1	U2	IC PROM SRL FOR 4M GATE 20-TSSOP	Xilinx Inc.	XCF04SVOG20C
1	U3	Buck Switching Regulator IC Posi- tive Adjustable 0.9V 1 Output 3A 16-VFQFN Exposed Pad	Microchip Technology Inc.	MCP16323T-ADJE/NG
4	U4-U7	Microchip Analog LDO 0.8V-5V MCP1727T-ADJE/MF DFN-8	Microchip Technology Inc.	MCP1727-ADJE/MF
3	U8, U11 U12	Linear Voltage Regulator IC Positive Adjustable 1 Output 1.2V ~ 3.4V 500 mA 6-TDFN (1.6x1.6)	Microchip Technology Inc.	MIC94325YMT-TR
1	U9	USB Bridge, USB to SPI USB 2.0 SPI Interface 20-SSOP	Microchip Technology Inc.	MCP2210T-I/SS
1	U10	Flexible Ultra-low Jitter Clock Gener- ator	Microchip Technology Inc.	SM803234UMG
1	X1	Resonators 12 MHz 0.1% SMD CSTCE-G	Murata Electronics	CSTCE12M0G15L99-R0
1	X2	40 MHz ±30 ppm Crystal 12 pF 40Ω -20°C ~ +70°C Surface Mount 4-SMD	TXC CORPORATION	7B-40.000MAAE-T

Note 1: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

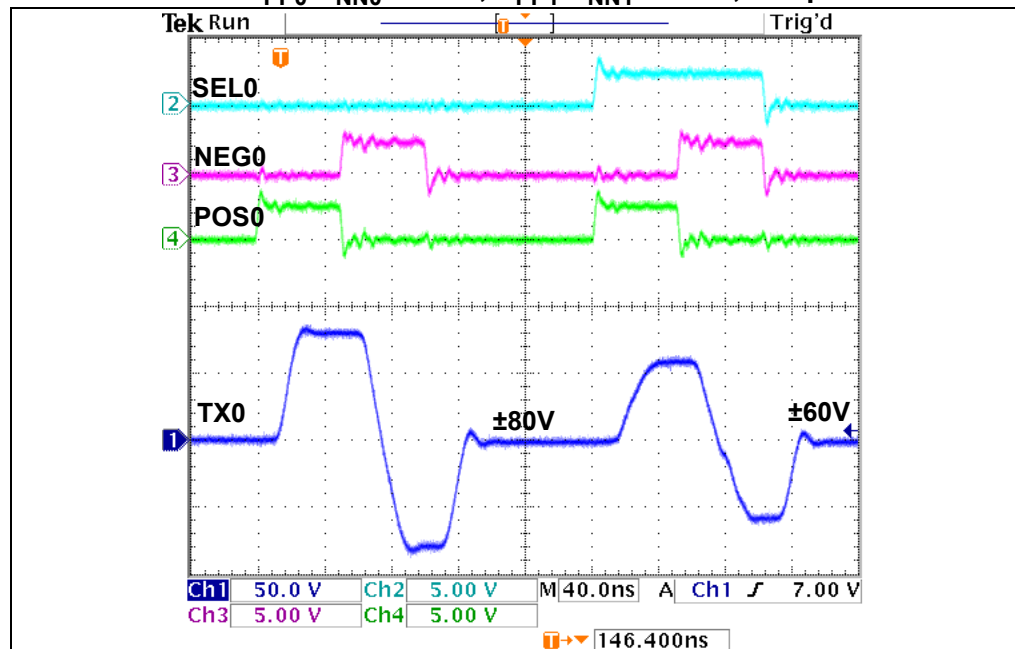
Appendix C. HV7321 Ultrasound TX Pulser Evaluation Board Typical Waveforms

C.1 BOARD TYPICAL WAVEFORMS

C.1.1 5 MHz $V_{PP0}/V_{NN0} = \pm 80V$, $V_{PP1}/V_{NN1} = \pm 60V$, 220 pF//1K Load

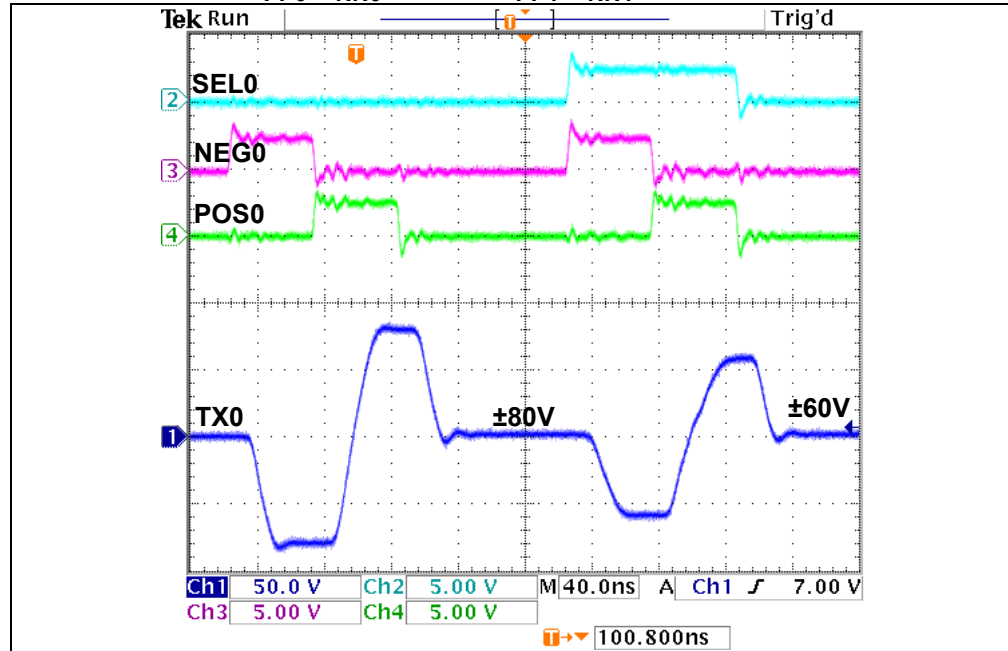


C.1.2 10 MHz $V_{PP0}/V_{NN0} = \pm 80V$, $V_{PP1}/V_{NN1} = \pm 60V$, 220 pF//1K Load

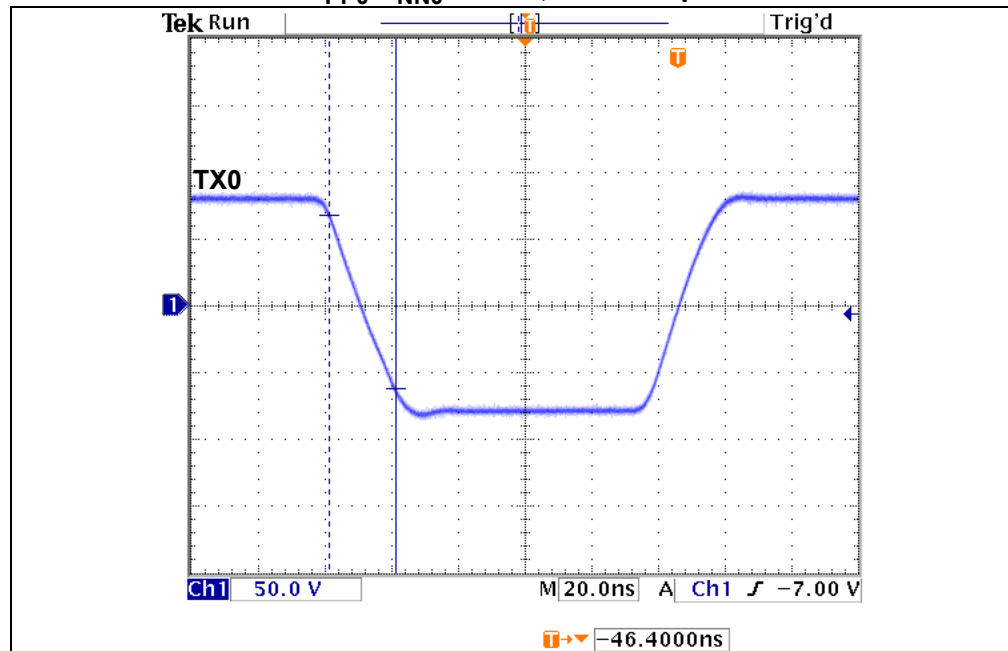


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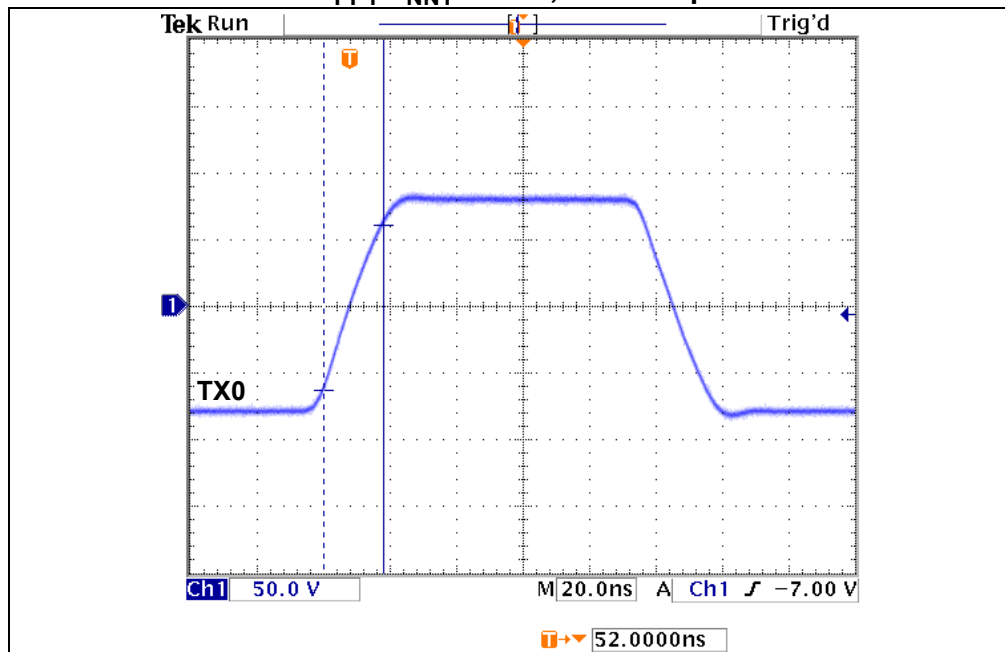
C.1.3 10 MHz $V_{PP0}/V_{NN0} = \pm 80V$, $V_{PP1}/V_{NN1} = \pm 60V$, 220 pF//1K Load



C.1.4 Fall Time of $V_{PP0}/V_{NN0} = \pm 80V$, with 220 pF//1K Load



C.1.5 Rise Time of $V_{PP1}/V_{NN1} = \pm 80V$, with 220 pF//1K Load



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