
Boost Converter Using the PIC16F753 Analog Features

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INTRODUCTION

This technical brief describes a boost power supply based on the PIC16F753, using 100% analog control for output regulation. The implementation has the advantage of not using any processor power, leaving the core free for more complex firmware. Also, the analog loop has a much faster response time to load steps and input voltage changes, making it useful for many applications.

The peripherals needed for the application are:

- One Complementary Output Generator (CWG)
- One Comparator (COMP)
- One Operational Amplifier (OPA)
- One 9-bit Digital-to-Analog Converter (DAC)
- One Fixed Voltage Reference (FVR)
- One Slope Compensation Module (SC)
- One Capture/Compare/PWM Module (CCP)

The peripherals are internally connected through firmware, significantly reducing the number of external pins needed for the implementation.

PERFORMANCE SPECIFICATIONS

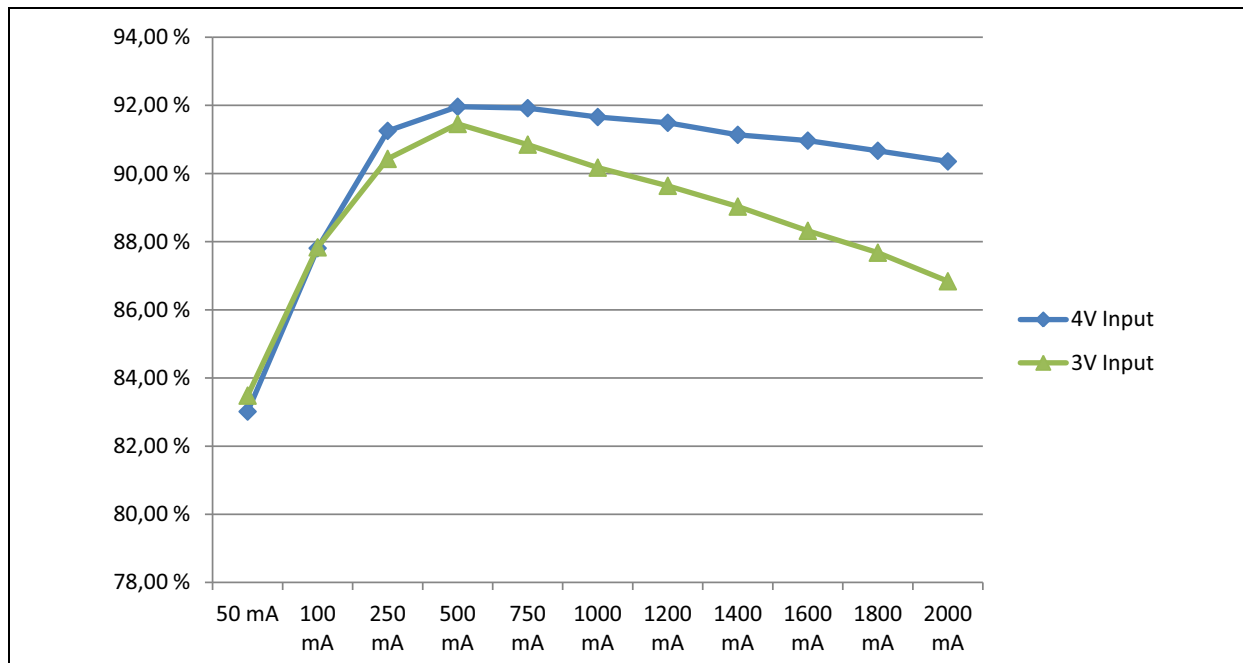
Electrical specifications over operating range:
 $3V \leq V_{DD} \leq 5V$.

TABLE 1: ELECTRICAL SPECIFICATIONS

Input Voltage Range	3-5	Volts DC
Output Voltage	5	Volts DC
Output Current	2	Amperes
Output Power	10	Watts
Code Size	99	Words
Ram Size	0	Bytes
Efficiency	87%	Measured at 2A
Available Code Size	1949	Words
Available RAM Size	128	Bytes

The output voltage is regulated using Peak Current mode control. The output voltage is compared to the reference voltage by the error amplifier (OPA) and the result is fed to the peak current comparator. The internal slope compensation module subtracts a software programmable ramp from the error amplifier output before the peak current comparator. The CCP provides a fixed-frequency, fixed duty cycle control signal and the peak current comparator output is selected as a second (level-based) source for the COG falling edge.

supply.

FIGURE 2: EFFICIENCY

FUNCTIONAL DESCRIPTION

This power supply is a fixed-frequency Peak Current mode converter. The operational amplifier (OPA) is used as an error amplifier (EA) for the output voltage, and a comparator limits the peak inductor current on each switching cycle, based on the EA feedback. The voltage reference for the EA is generated by the DAC and can be changed on-the-fly in firmware. The CCP peripheral generates a fixed frequency, fixed duty cycle control signal for the COG. The peak current comparator is used to close the loop through by selecting it as a second falling edge event source (limits duty cycle on each switching pulse based on EA feedback).

After the peripherals are configured and connected together, the control loop runs by itself, requiring 0% processor time.

Peak current control schemes require slope compensation for duty cycles over 50% to prevent oscillation. For lower duty cycles, slope compensation will also help stabilize the control loop, if the current shunt is small. The internal slope compensation module subtracts a software programmable ramp from the error amplifier output before the peak current comparator.

For the boost topology, the inductor current is equal to the input current. The peak inductor current is measured directly on a resistor placed between the transistor source and the ground.

Output current limiting is not integrated into the control loop, thus a second comparator should be used for this purpose and selected as an auto-shutdown source for the COG. The error amplifier output is the inductor peak current limit, so keeping this value low by a resistor divider helps with inrush current problems and catastrophic short-circuit conditions. Of course, the downside of this approach is that the system gain is reduced and that it will respond slower to transients. The OPA output pin is the same as the slope compensation module input pin, so the two peripherals can be used together without any additional external connectivity. If a resistor divider is used to limit OPA output voltage, it must be routed externally to the FVR buffer input pin.

Input voltage is connected to the microcontroller using a small diode and is bootstrapped to the output. Thus, when the output voltage rises, it will power the microcontroller and MOSFET driver. This is more efficient because a higher V_{GS} will improve $R_{DS(ON)}$ and the interval below 4.5V is problematic for most power transistors. This also makes the FVR the only stable reference available, and the circuit requires a few changes to ensure that the loop reference voltage is always independent from the supply or output voltage. Since the control loop reference voltage is derived from the DAC, this peripheral needs to have a stable reference, too. The FVR of 1.2V is selected as the DAC reference, thus fulfilling all the mentioned requirements.

It is important to mention that the boost topology has a clear DC path from the power source to the output, through the inductor and rectifier diode, even if the switching transistor is blocked. The current limiting loop can only prevent overcurrent until the switching frequency becomes zero. From this point on, catastrophic short-circuit events can occur without an additional protection switch. A second transistor can be placed on the output low side to cut off the load in case of a short circuit.

For comparator-based short-circuit protection, the reference must be stable over the whole voltage operating range. Since the output current shunt voltage is usually too small to use with the 1.2V FVR directly, it needs to be routed outside through the FVR buffer and then through a resistive divider to obtain the desired reference voltage for the comparator. Since the FVR buffer is used this way, the OPA output must be used directly with the SC, without the additional divider. This solution uses 0% processor time but also uses more pins and peripherals. For ADC-based short-circuit protection, the current shunt voltage and the FVR are read in firmware. The FVR voltage is necessary to calculate V_{DD} (when $<5V$), which in this case is the ADC reference voltage. While this second solution does not use the extra comparator, I/O pins and external resistors, it will need some program space and processor time.

The component values shown in this document are to be treated only as a starting point. They need to be tuned for each design. The converter must be compensated for a specific load and the stability must be verified across the entire range of operating conditions.

Compared to a solution using a specialized PWM controller chip, performance is similar, but a PIC[®] microcontroller-based solution adds invaluable flexibility. Also, the analog control loop runs by itself, so the microcontroller core is 100% free to run user algorithms, measure power supply parameters or transmit relevant information.

APPLICATIONS

The analog control loop makes the power supply fast enough for dynamic loads and input voltage changes.

For current-controlled loads like LEDs or thermoelectric cells, the voltage feedback can be replaced by average current feedback. The power supply can be also used for applications which require both voltage and current control like CC/CV battery chargers. The PIC16F753 DAC has nine bits of resolution, which translate into a minimum voltage step of 50 mV with a 1/5 output divider.

MCU PERIPHERAL CONFIGURATION DRAWING

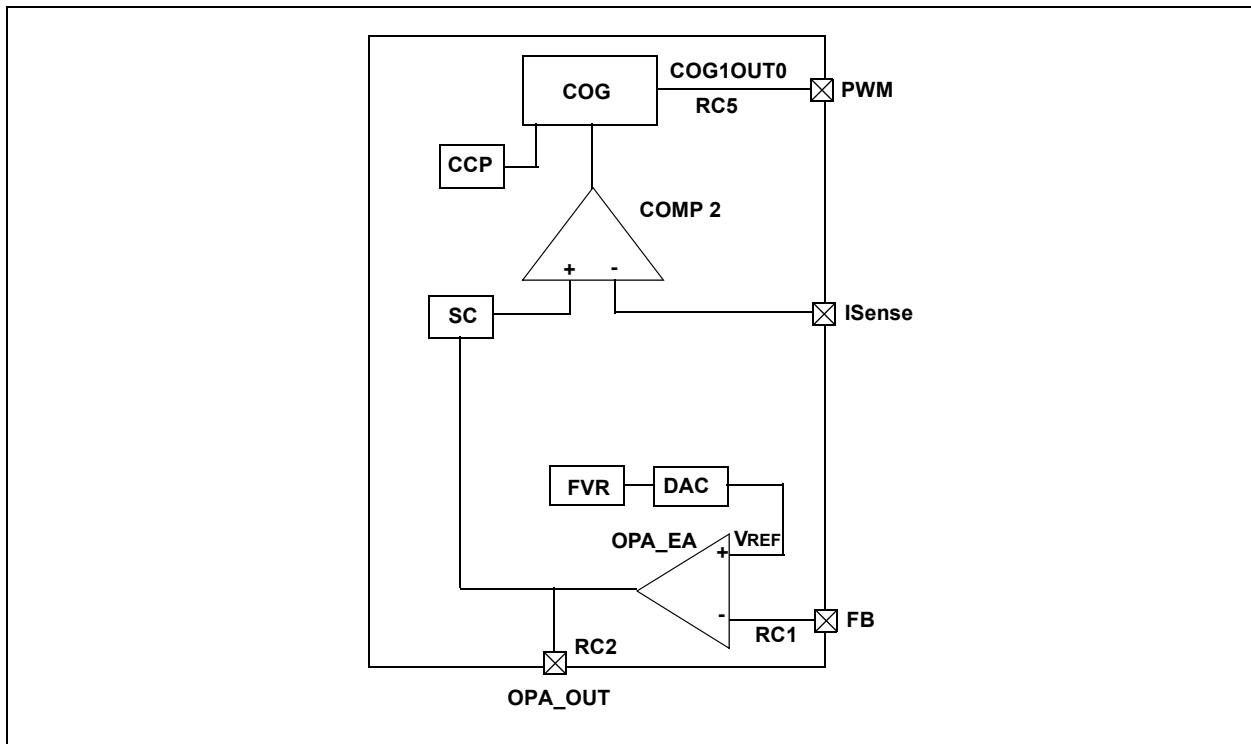
The application needs one OPA, one comparator and one DAC. The DAC output can be internally routed to the OPA, so this feature saves one pin. The CCP module generates a fixed-frequency, fixed duty cycle signal for the COG. Depending on the user option to limit the OPA output, the resistor divider needs to be externally connected to the FVR buffer input. If not using the resistor divider, only one pin is used instead of two. In this case, the OPA output, which is the same as the SC input, is configured as an analog pin and should not be used for other purposes.

The input-only digital pin, $\overline{\text{MCLR}}$, can be used for a button or a similar functionality. During run-time, the programming data I/O pin (PGD) are free for user-specific functionality.

TABLE 2: PIC16F753 PERIPHERAL CONFIGURATION

Pin No.	Name	Function
1	VDD	Supply voltage
14	VSS	Ground connection
10	RC0	Analog input (COMP) – peak current sensing
9	RC1	Analog input (OPA) – output voltage feedback
8	RC2	Analog output (OPA) – error amplifier output
12	RA1/PGC/ FVRIN	Analog input FVR buffer input for peak current limit from error amplifier/ Programming clock
13	PGD	Programming data
5	COG1OUT0/ RC5	Transistor control signal (PWM)

FIGURE 3: PERIPHERAL CONFIGURATION



PLOTS OF KEY PARAMETERS

Table 3 contains some characteristics of the charger obtained with an input of 3V and an output of 5V. The switching frequency is 250 kHz.

TABLE 3: POWER SUPPLY CHARACTERISTICS

Output Current (mA)	Duty Cycle (%)	Efficiency (%)
0	skipping	N/A
50	26.3	83.5
100	37.2	87.8
250	43.2	90.4

TABLE 3: POWER SUPPLY CHARACTERISTICS

Output Current (mA)	Duty Cycle (%)	Efficiency (%)
500	43.9	91.4
750	44.6	90.8
1000	45.3	90.1
1200	45.7	89.6
1400	46.4	89.0
1600	46.9	88.3
1800	47.4	87.6
2000	48.2	86.8

Note 1: Efficiency is calculated including power loss on current shunt.

FIGURE 4: DUTY CYCLE vs. LOAD CURRENT

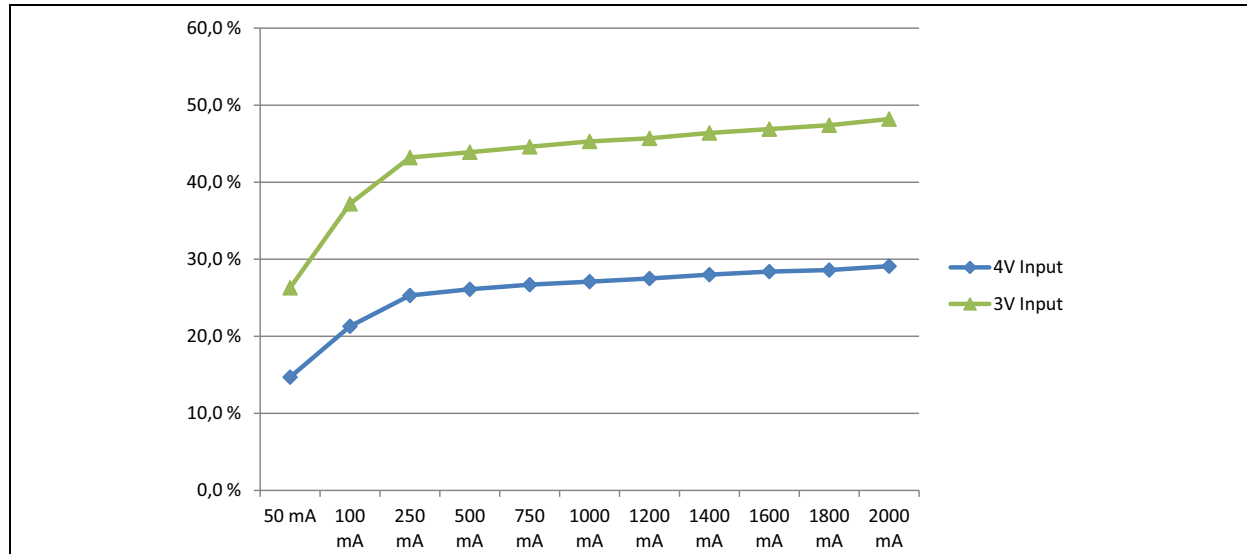


Figure 4 shows the converter operating frequency for 3V and 4V input at different output currents. Once the inductor current becomes continuous, the duty cycle changes very little, only to compensate for component power losses. The power loss becomes very easy to see on the efficiency graph (see Figure 2).

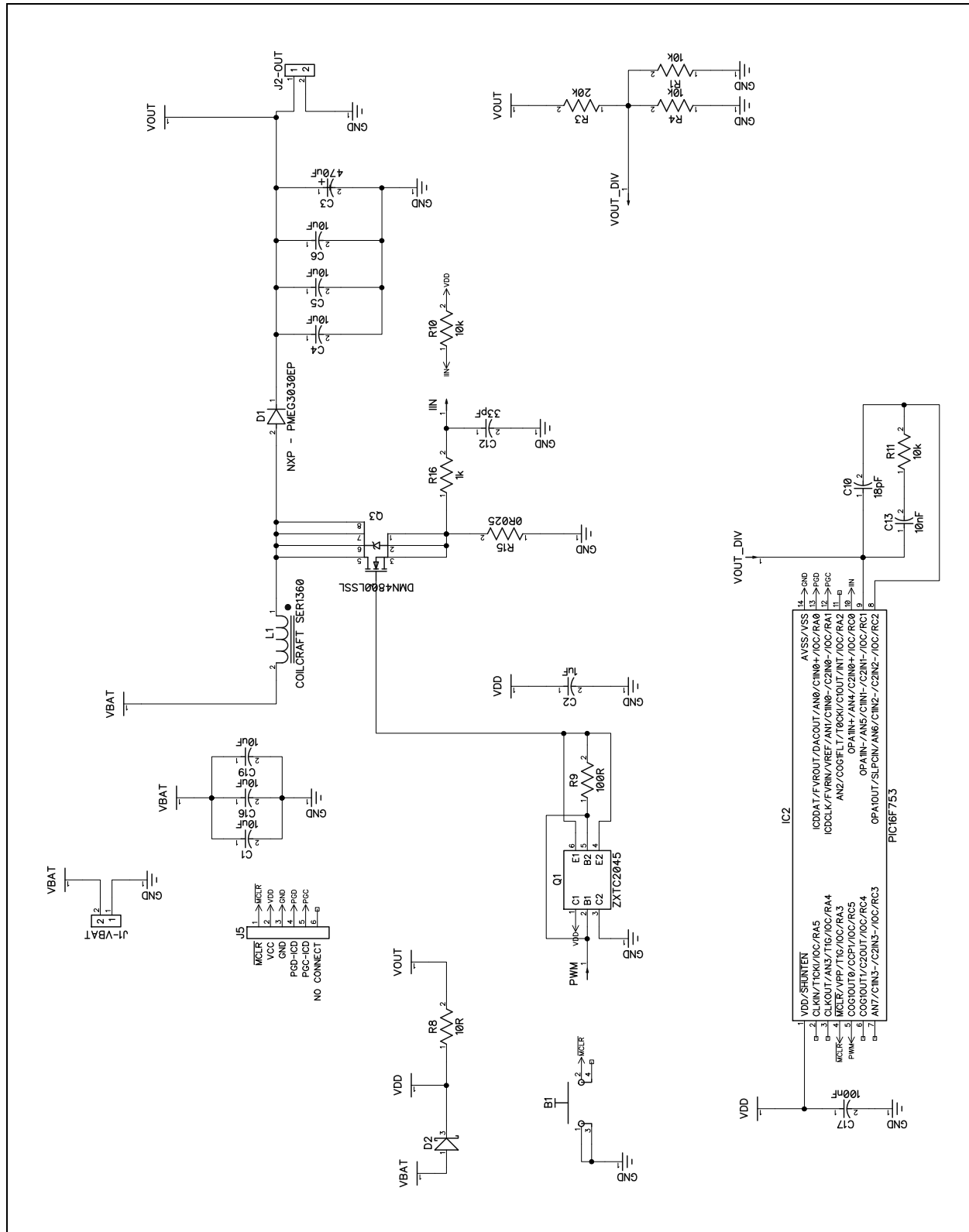
GLOSSARY

TABLE 4: ACRONYMS

PWM	Pulse-Width Modulation
ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
COG	Complementary Output Generator
FVR	Fixed Voltage Reference
OPA	Operational Amplifier
EA	Error Amplifier
SC(M)	Slope Compensation (Module)
CCP	Capture Compare PWM

APPENDIX A:

FIGURE A-1: SCHEMATIC



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