KSZ9131RNX

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip KSZ9131RNX. These checklist items should be followed when utilizing the KSZ9131RNX in a new design. A summary of these items is provided in Section 9.0, "Hardware Checklist Summary," on page 13. Detailed information on these subjects can be found in the corresponding sections:

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The KSZ9131RNX implementor should have the following documents on hand:

- *KSZ9131RNX Gigabit Ethernet Transceiver with RGMII Support Data Sheet*
- *KSZ9131RNX Silicon Errata and Data Sheet Clarification*
- KSZ9131RNX Reference Design Schematic

2.2 Pin Check

- Check the pinout of the part against the data sheet. Ensure all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Ground

- The ground pins, **GND**, should be connected to the solid ground plane on the board.
- It is recommended that all ground connections be tied together to the same ground plane. Separate ground planes are not recommended.

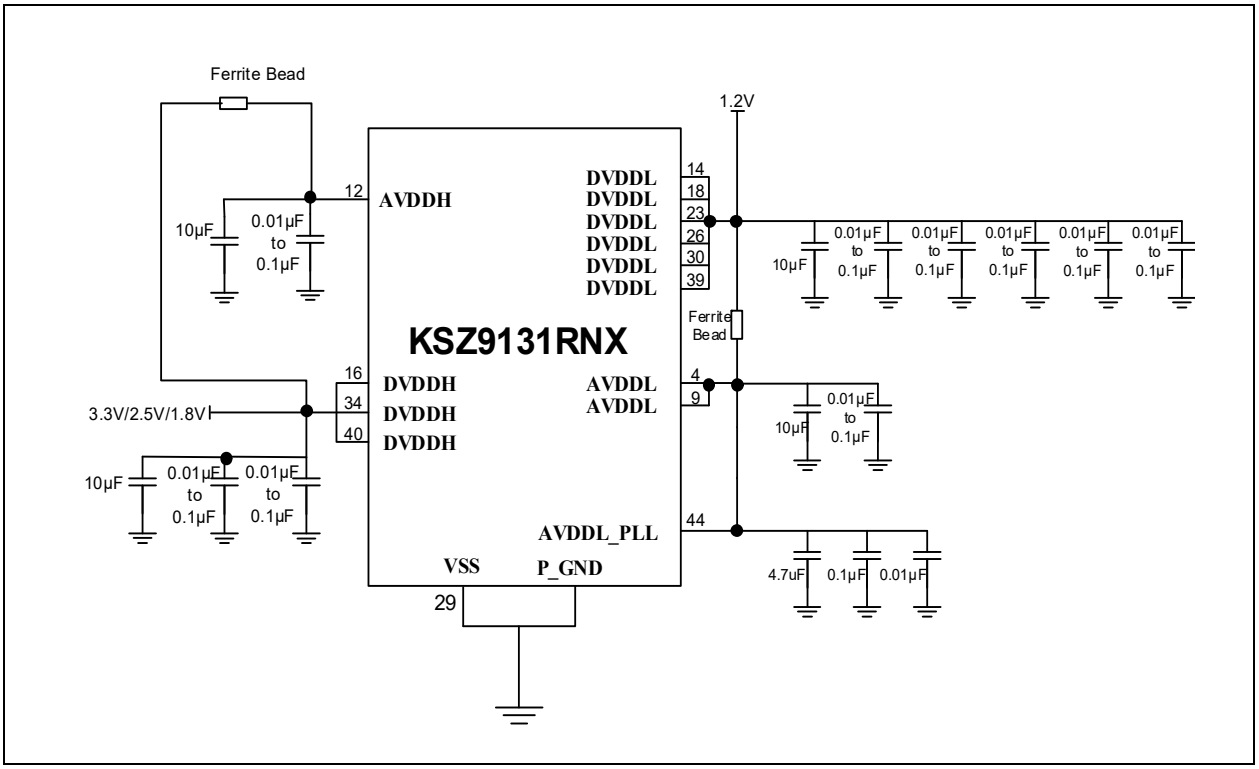
3.0 POWER

- The analog supply (**AVDDH**) is located on pins 1 and 12, and requires a connection to **VDDA** (created from +3.3V through a ferrite bead). Bulk capacitance should be placed on each side of the ferrite bead. Generally, a 100Ω to 220Ω (at 100 MHz) ferrite bead is used. Each **AVDDH** pin should include 0.1 µF and 10 µF capacitors to decouple the device. The capacitor size should be SMD_0603 or smaller.
- The **AVDDL** (pins 4 and 9) is the analog core voltage supply. It should be connected to a +1.2V supply (created from +1.2V through a ferrite bead). Bulk capacitance should be placed on each side of the ferrite bead. Generally, a 100Ω to 220Ω (at 100 MHz) ferrite bead is used. Each **AVDDL** pin should include 0.1 µF and 22 µF capacitors to decouple the device. The capacitor size should be SMD_0603 or smaller.
- The **DVDDH** (pins 16, 34 and 40) is the variable supply voltage for the I/O pads. It should be connected to the +3.3V, 2.5V, or 1.8V supply. A bulk capacitor is needed close to the source to prevent any droop in the supply when the part starts. Decoupling capacitors need to be placed as close to the part as possible to reduce high-frequency noise being injected through EMI interference.

- The **DVDDL** (pins 14, 18, 23, 26, 30 and 39) is the digital core voltage supply. It should be connected to the +1.2V supply. A bulk capacitor must be placed close to the source to prevent any droop in supply when the part starts. Decoupling capacitors must be placed as close to the part as possible to reduce high-frequency noise being injected through EMI interference.
- **AVDDL_PLL** (pin 44) supplies power to the KSZ9131RNX PLL. Decouple with a 4.7 µF to 10 µF capacitor, a 0.1 µF capacitor, and a 0.01 µF capacitor to ground. After that, connect them to the +1.2V power trace or plane through a ferrite bead.

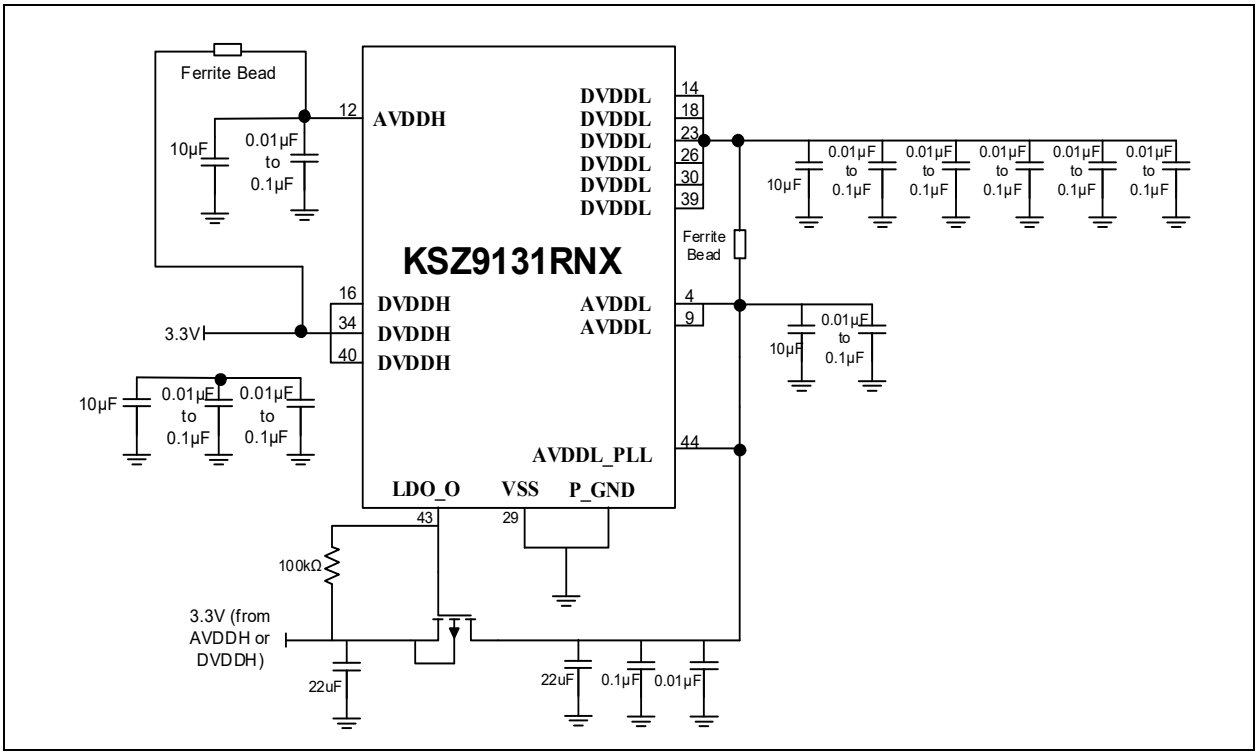
Power and ground connections without LDO are shown in Figure 3-1 without using the LDO. The power and ground connections with the LDO (using an external MOSFET) are shown in Figure 3-2

FIGURE 3-1: POWER AND GROUND CONNECTIONS WITHOUT LDO



Caution: This +1.2V supply is for internal logic only. **Do not** power other circuits or devices with this supply.

FIGURE 3-2: POWER AND GROUND CONNECTIONS WITH LDO



Caution: This +1.2V supply is for internal logic only. **Do not** power other circuits or devices with this supply.

Note: If in-rush current is of concern, the 22 µF capacitor on the 3.3V end (Source) of the P-channel MOSFET can be reduced to 10 µF to 12 µF.

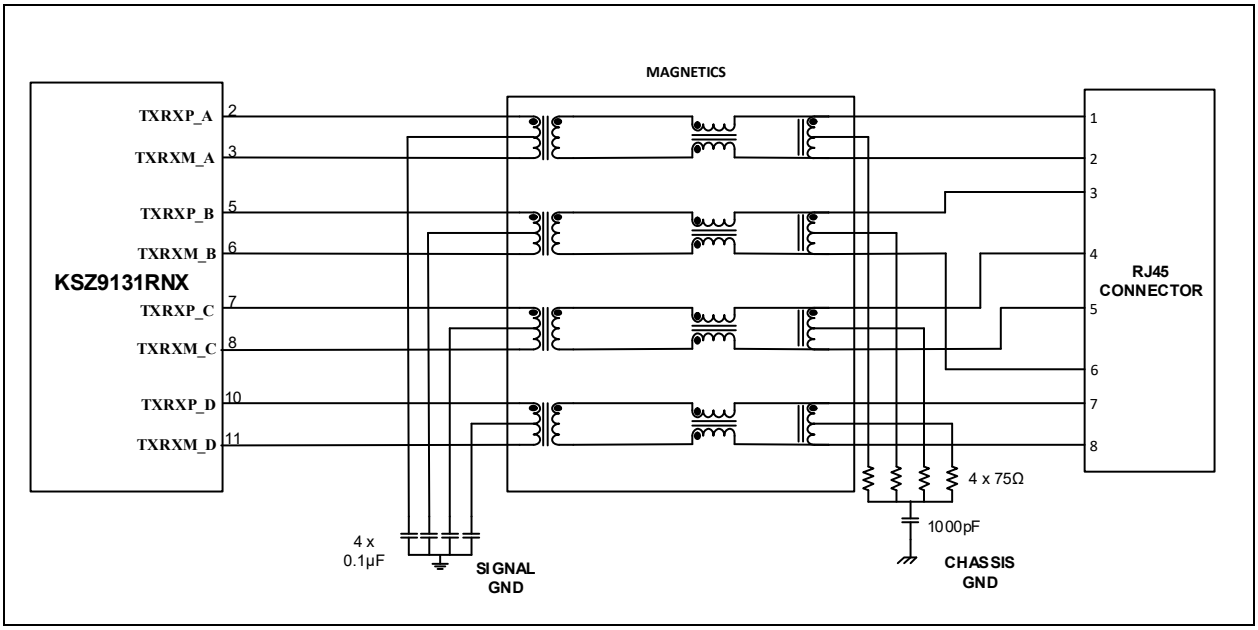
4.0 ETHERNET SIGNALS

4.1 10/100/1000 MBPS Interface Connection

- **TXRXP_A** (pin 2): This pin is the transmit/receive positive connection from pair A of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXRXM_A** (pin 3): This pin is the transmit/receive negative connection from pair A of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXRXP_B** (pin 5): This pin is the transmit/receive positive connection from pair B of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXRXM_B** (pin 6): This pin is the transmit/receive negative connection from pair B of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXRXP_C** (pin 7): This pin is the transmit/receive positive connection from pair C of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXRXM_C** (pin 8): This pin is the transmit/receive negative connection from pair C of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXRXP_D** (pin 10): This pin is the transmit/receive positive connection from pair D of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXRXM_D** (pin 11): This pin is the transmit/receive negative connection from pair D of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.

For 10/100/1000 Mbps channel connections details, refer to Figure 4-1.

FIGURE 4-1: 10/100/1000MBPS CHANNEL CONNECTIONS



4.2 10/100/1000 Magnetics Connection

- The center tap connection on the KSZ9131RNX side for Pair A channel only connects a 0.1 µF capacitor to GND and no bias is needed.
- The center tap connection on the KSZ9131RNX side for Pair B channel only connects a 0.1 µF capacitor to GND and no bias is needed.
- The center tap connection on the KSZ9131RNX side for Pair C channel only connects a 0.1 µF capacitor to GND and no bias is needed.
- The center tap connection on the KSZ9131RNX side for Pair D channel only connects a 0.1 µF capacitor to GND and no bias is needed.
- The center taps of the magnetics for all pairs should not be connected together without this 0.1 µF to ground. The reason is the Common-mode voltage can be different between pairs, especially for 10/100 operation. (Pairs A and B are active, while pairs C and D are inactive.)
- The center tap connection for each pair (A, B, C, and D) on the cable side (RJ45 side) should be terminated with a 75Ω resistor through a common 1000-pF, 2-KV capacitor to chassis ground.
- Only one 1000-pF, 2-KV capacitor to chassis ground is required. It is shared by Pair A, Pair B, Pair C, and Pair D center taps.
- The RJ45 shield should connect to chassis ground. This includes RJ45 connectors with or without integrated magnetics. See Section 8.2 for guidance on how chassis ground should be created from digital/signal ground.

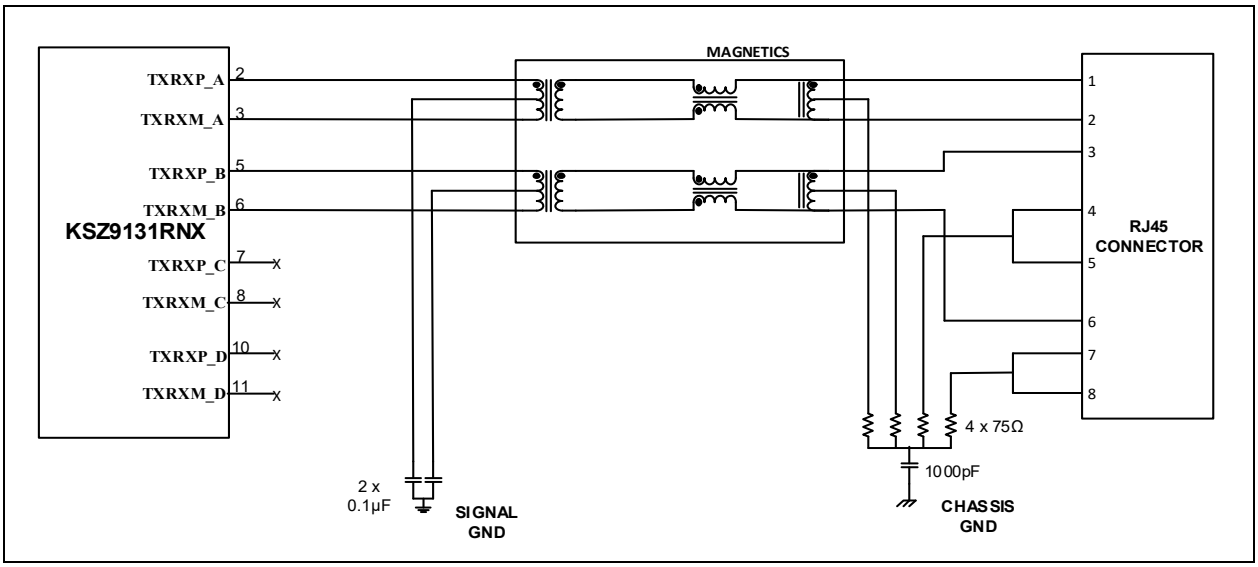
4.3 10/100 MBPS Interface Connection

- For designs needing only a 10/100 connection, the 1000 Mbps capability must be removed. The following steps remove the 1000 Mbps advertisement for Auto-Negotiation:
  1. Set Port Register 0x00, Bit [6] = '0' to remove 1000 Mbps speed.
  2. Set Port Register 0x09, Bits [9:8] = '00' to remove Auto-Negotiation advertisements for 1000 Mbps.
  3. Write a '1' to Register 0x00, Bit [9], a self-clearing bit, to force a restart of Auto-Negotiation.
- **TXRXP_A** (pin 2): This pin is the transmit/receive positive connection from pair A of the internal PHY. This pin connects to the 10/100 magnetics. No external terminator and bias are needed.
- **TXRXM_A** (pin 3): This pin is the transmit/receive negative connection from pair A of the internal PHY. This pin connects to the 10/100 magnetics. No external terminator and bias are needed.
- **TXRXP_B** (pin 5): This pin is the transmit/receive positive connection from pair B of the internal PHY. This pin connects to the 10/100 magnetics. No external terminator and bias are needed.

- **TXRXM_B** (pin 6): This pin is the transmit/receive negative connection from pair B of the internal PHY. This pin connects to the 10/100 magnetics. No external terminator and bias are needed.
- **TXRXP_C** (pin 7): This pin can be left as NC (No Connect)
- **TXRXM_C** (pin 8): This pin can be left as NC (No Connect)
- **TXRXP_D** (pin 10): This pin can be left as NC (No Connect)
- **TXRXM_D** (pin 11): This pin can be left as NC (No Connect).

For 10/100 Mbps channel connections details, refer to Figure 4-2.

FIGURE 4-2: 10/100 MBPS CHANNEL CONNECTIONS



4.4 10/100 Magnetics Connection

- The center tap connection on the KSZ9131RNX side for Pair A (Transmit Channel) only connects a 0.1 µF capacitor to GND and no bias is needed.
- The center tap connection on the KSZ9131RNX side for Pair B (Receive Channel) only connects a 0.1 µF capacitor to GND and no bias is needed.
- The center taps of the magnetics of the transmit and receive channels should not be connected together. The reason is the Common-mode voltage can be different between pairs.
- The center tap connection on the KSZ9131RNX side for the receive channel is connected to the transmit channel center tap on the magnetics.
- The center tap connection on the cable side (RJ45 side) for Pair A should be terminated with a 75Ω resistor through a 1000-pF, 2-KV capacitor to chassis ground.
- The center tap connection on the cable side (RJ45 side) for Pair B should be terminated with a 75Ω resistor through a 1000-pF, 2-KV capacitor to chassis ground.
- Only one 1000-pF, 2-KV capacitor to chassis ground is required. It is shared by both Pair A and Pair B center taps.
- MDI Connections:
  - Pin 1 of the RJ45 is **TX**+ and should trace through the magnetics to TXRXP_A (pin 2) of the KSZ9131RNX.
  - Pin 2 of the RJ45 is **TX**– and should trace through the magnetics to TXRXM_A (pin 3) of the KSZ9131RNX.
  - Pin 3 of the RJ45 is **RX**+ and should trace through the magnetics to TXRXP_B (pin 5) of the KSZ9131RNX.
  - Pin 6 of the RJ45 is **RX**– and should trace through the magnetics to TXRXM_B (pin 6) of the KSZ9131RNX.
- MDIX Connections:
  - Pin 3 of the RJ45 is **TX**+ and should trace through the magnetics to TXRXP_B (pin 6) of the KSZ9131RNX.
  - Pin 6 of the RJ45 is **TX**– and should trace through the magnetics to TXRXM_B (pin 5) of the KSZ9131RNX.
  - Pin 1 of the RJ45 is **RX**+ and should trace through the magnetics to TXRXP_A (pin 2) of the KSZ9131RNX.

  - Pin 2 of the RJ45 is **RX**– and should trace through the magnetics to TXRXP_A (pin 3) of the KSZ9131RNX.
- When using the KSZ9131RNX device in the Auto MDIX mode of operation, an Auto MDIX style magnetics module (that is, the one where the two channels are identical) is required.

4.5 10/100 MBPS RJ45 Connection

- Pins 4 and 5 of the RJ45 connector interface to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000-pF, 2-KV capacitor. There are two methods of accomplishing this:
  - Pins 4 and 5 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω resistor to the 1000-pF, 2-KV capacitor.
  - For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel perform like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω resistor causes the entire circuit to function as a 75Ω resistor. So, by shorting pins 4 and 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000-pF, 2-KV capacitor to chassis ground, an equivalent circuit is created.
- Pins 7 and 8 of the RJ45 connector interface to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000-pF, 2-KV capacitor. There are two methods of accomplishing this:
  - Pins 7 and 8 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω resistor to the 1000-pF, 2-KV capacitor.
  - For a lower component count, the resistors can be combined. The two 49.9-Ω resistors in parallel perform like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω resistor causes the entire circuit to function as a 75Ω resistor. So, by shorting pins 7 and 8 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000-pF, 2-KV capacitor to chassis ground, an equivalent circuit is created.
- The RJ45 shield should be attached directly to chassis ground. This includes RJ45 connectors with or without integrated magnetics. See Section 8.2 for guidance on how chassis ground should be created from digital/signal ground.

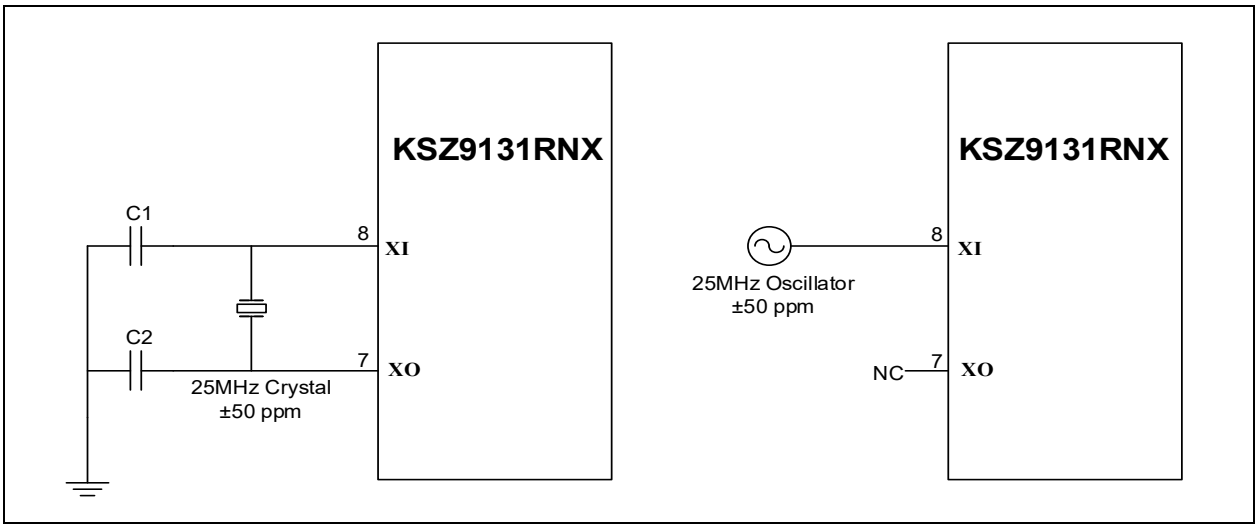
5.0 CLOCK CIRCUIT

5.1 Crystal and External Oscillator/Clock Connections for MII Mode

- A 25.000-mhz (±50ppm) crystal should be used to provide the clock source. For the complete crystal specifications and tolerances, refer to the *KSZ9131RNX Data Sheet*.
- **XI** (pin 8) is the clock circuit input for the KSZ9131RNX device. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- **XO** (pin 7) is the clock circuit output for the KSZ9131RNX device. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- Since every system design is unique, the capacitor values are system dependent, based on the CL spec of the crystal and the stray capacitance value. The PCB design, crystal, and layout all contribute to the characteristics of this circuit.

- Alternately, a 25.000-MHz, 3.3-V clock oscillator may be used to provide the clock source for the KSZ9131RNX. When using a single-ended clock source, XO (pin 7) should be left floating as a No Connect (NC). See Figure 5-1.

FIGURE 5-1: CRYSTAL AND OSCILLATOR CONNECTIONS



6.0 DIGITAL INTERFACES

6.1 RGMII™ Interface

- The KSZ9131RNX complies with the RGMII™ v2.0 specification, which delays the RX_CLK from the RXD, RX_DV lines. Please see the *KSZ9131RNX Data Sheet* for details.
- For the KSZ9131RNX RXD to RX_CLK delay, the MAC must be either compliant with RGMII v2.0 (accept RXD to RXCLK delay of at least 1.2 ns) or set the delay on the RX_CLK line to comply with the RGMII v2.0 specification. If the MAC is either not compliant with RGMII v2.0 or cannot set the delay on RX_CLK, a combination of trace delay and provided KSZ9131RNX pad skew settings can help meet the timing. Suggestion is to design at least 0.3 ns of delay (4.5 cm/1.8 inches longer PCB trace on RX_CLK than longest RXD, RX_DV/RX_CTL PCB trace) to provide margin to use the KSZ9131RNX pad skew registers to align for sufficient delay. When using either an external RGMII MAC interface, comply with the proper connections for the 14 signals specified in Table 6-1, which also includes two management pins (MDC and MDIO).

TABLE 6-1: RGMII™ CONNECTIONS

From:	Connects to:
KSZ9131RNX	**RMII™ MAC Device**
RXD0 (pin 32)	RXD<0>
RXD1 (pin 31)	RXD<1>
RXD2 (pin 28)	RXD<2>
RXD3 (pin 27)	RXD<3>
RX_DV/RX_CTL (pin 33)	RX_DV
RX_CLK (pin 35)	RX_CLK
TXD0 (pin 19	TXD<0>
TXD1 (pin 20	TXD<1>
TXD2 (pin 21	TXD<2>
TXD3 (pin 22)	TXD3
TXEN (pin 25)	TX_EN
GTX_CLK (pin 24)	GTX_CLK
MDIO (pin 37)	MDIO
MDC (pin 36)	MDC

- Provisions should be made for series terminations for all outputs on the RGMII interface. Series resistors enable the designer to closely match the output driver impedance of the KSZ9131RNX and the PCB trace impedance to minimize ringing on the signals. Exact resistor values are application-dependent and must be analyzed in-system. A suggested starting point for the value of these series resistors is 33Ω.

6.2 RGMII™ Series Source Termination

TABLE 6-2: RGMII™ SERIES SOURCE TERMINATIONS

Signal	RGMII™ Mode
RXD0	33Ω
RXD1	33Ω
RXD2	33Ω
RXD3	33Ω
RX_DV/RX_CTL	33Ω
RX_CLK	33Ω
TXD0	33Ω
TXD1	33Ω
TXD2	33Ω
TXD3	33Ω
TX_EN	33Ω
GTX_CLK	33Ω

6.3 Required External Pull-ups

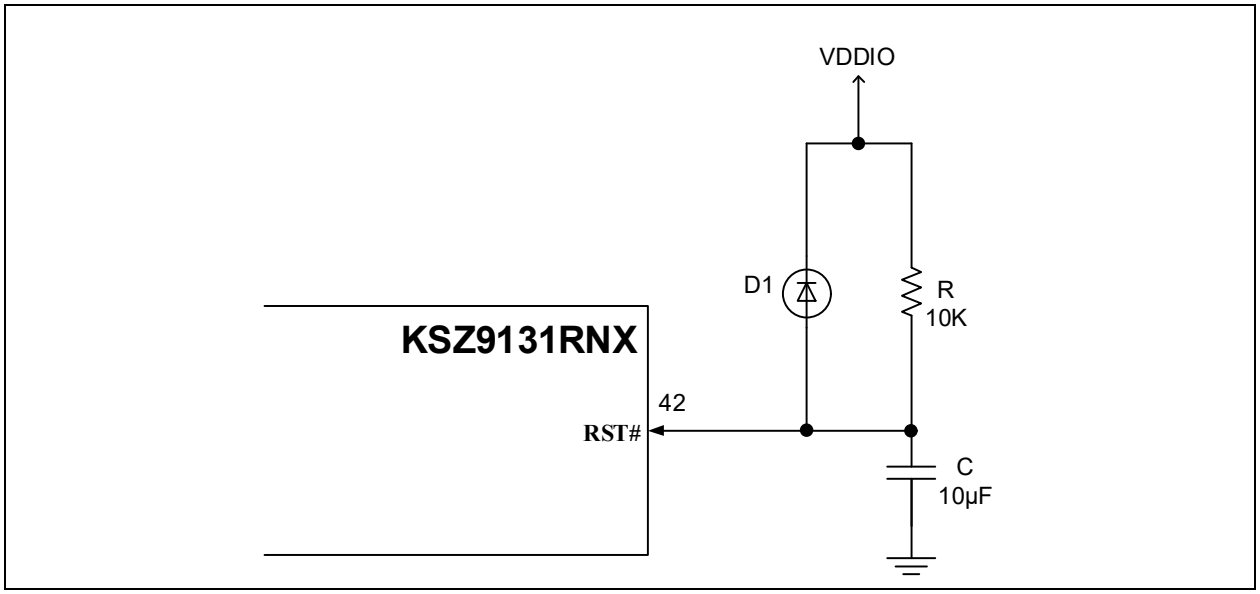
- When using the KSZ9131RNX MDC/MDIO management pins, a pull-up resistor of 1 kΩ on the **MDIO** signal (pin 37) is required.
- If used, the **INTRP** (pin 38) requires a 4.7 kΩ external pull-up resistor since this output is an open drain. If the **INTRP** pin is not used, then this pin can float.

7.0 STARTUP

7.1 Reset Circuit

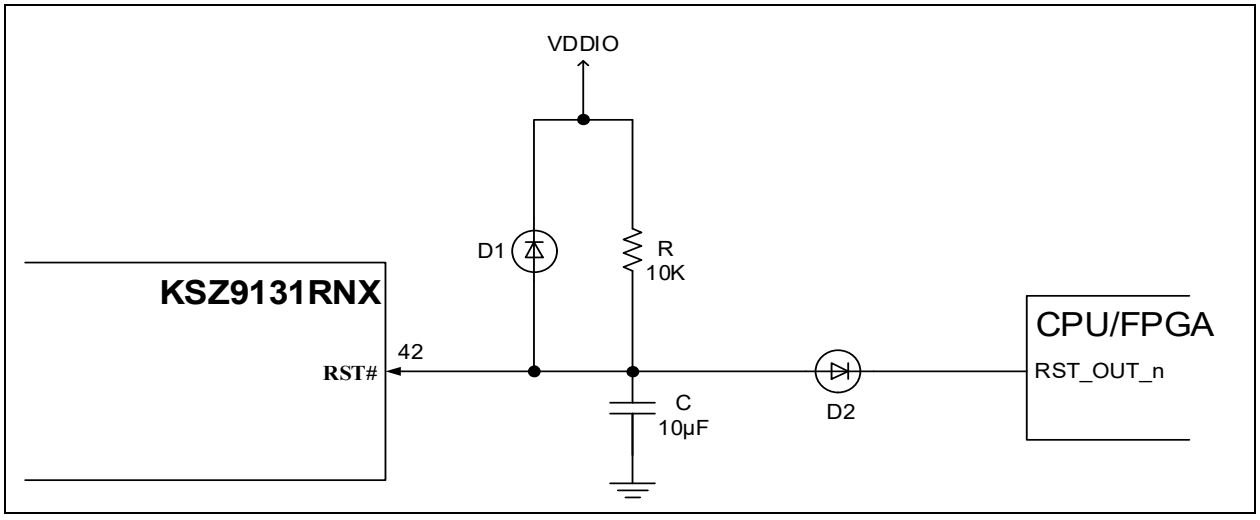
- **RST#** (pin 42) is an active-low reset input. This signal resets all logic and registers within the KSZ9131RNX. A hardware reset (**RST#** assertion) is required following power-up. Please refer to the latest copy of the *KSZ9131RNX Data Sheet* for reset timing requirements. Figure 7-1 shows a recommended reset circuit for powering up the KSZ9131RNX when reset is triggered by the power supply.

FIGURE 7-1: RESET TRIGGERED BY POWER SUPPLY



- Figure 7-2 details the recommended reset circuit for applications where reset is driven by an external CPU or FPGA. The reset out pin (RST_OUT_n) from the CPU/FPGA provides the warm reset after power-up. If the Ethernet device and CPU/FPGA use the same VDDIO voltage, D2 can be removed and both reset pins can be directly connected.

FIGURE 7-2: RESET CIRCUIT INTERFACE WITH CPU/FPGA RESET OUTPUT



7.2 Configuration Mode Pins (Strapping Options)

- The Configuration mode pins of the KSZ9131RNX (**MODE[3:0]**) control the default configuration of the 10/100 PHY. Speed, duplex, auto-negotiation, and power-down functionality can be configured through these pins. The value of these three pins are latched upon power-up and reset. In some systems, the MAC receive input pins may drive high during power-up or reset and consequently cause the PHY strap-in pins on the RGMII™ signals to be latched high. In this case, it is recommended to add 1 kΩ pull-downs on these PHY strap-in pins to ensure the PHY does not strap in to an incorrect mode configuration or is not configured with an incorrect PHY address. Refer to the *KSZ9131RNX Data Sheet* for complete details for the operation of these pins.

7.3 LED Pins

- The KSZ9131RNX provides two LED signals. These indicators display speed, link, and activity information about the current state of the PHY. The LED pins drive low to light up the LED indicators, which should have their anode ends tied to 3.3V and their cathode ends tied through a series resistor (typically 220Ω to 470Ω). Refer to the *KSZ9131RNX Data Sheet* for further details on how to connect each pin for correct operation.
- The LED functionality signal pins are shared with the following pin strapping functions:
  - LED2 is shared with **PHYAD1** on pin 15 for KSZ9131RNX.
  - LED1 is shared with **PHYAD0** and **PME_N1** on pin 17 for KSZ9131RNX.

Note 1: For 1.8V VDDIO, LED indication support is not recommended due to the low voltage. Without the LED indicator, the **PHYAD1** and **PHYAD0/PME_N1** strapping pins are functional with a 4.7 kΩ pull-up to 1.8V VDDIO (or be floated) for a value of '1', and with a 1.0 kΩ pull-down to ground for a value of '0'.

2: If using RJ45 jacks with integrated LEDs and 1.8V VDDIO, a level shifting is required from LED 3.3V to 1.8V. In this case, a bipolar transistor or a level shifting device can be used.

8.0 MISCELLANEOUS

8.1 REXT Resistor

- The **REXT** pin on the KSZ9131RNX must connect to ground through a 6.04 kΩ resistor with a tolerance of 1.0%. This is used to set up critical bias currents for the embedded 10/100/1000 Ethernet physical device.

8.2 Other Considerations

- Incorporate a large SMD footprint (SMD_1210) to connect the chassis ground to the digital ground. This allows some flexibility at EMI testing for different grounding options. Leaving the footprint open allows the two grounds to remain separate. Shorting them together with a 0 ohm resistor connects them. For best performance, short them together with a cap or a ferrite bead.
- Be sure to incorporate enough bulk capacitors (4.7 µF to 22 µF) for each power plane.

9.0 HARDWARE CHECKLIST SUMMARY

TABLE 9-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet.		
	Section 2.3, "Ground"	Verify if the grounds are tied together.		
Section 3.0, "Power"	Section 3.0, "Power"	Ensure that **VDDA_3.3** and **VDDIO** are within the range 3.135V to 3.465V, and a 22 µF capacitor is on each pin.		
		VDD_1.2 requires two 0.1 µF capacitors.		
		For LDO designs, check the capacitance on both the drain and source of FET have at least 22 µF.		
		For LDO designs, make sure the 100 kΩ resistor is in place (see Figure 3-2) to prevent in-rush current.		
Section 4.0, "Ethernet Signals"	Section 4.1, "10/100/1000 MBPS Interface Connection"	Verify if each pair's positive and negative connections move to the following: Pair A – Pair 1 of the magnetics Pair B – Pair 2 of the magnetics Pair C – Pair 3 of the magnetics Pair D – Pair 4 of the magnetics		
	Section 4.2, "10/100/1000 Magnetics Connection"	Verify if each of the Pair A, Pair B, Pair C, and Pair D center taps moves from a 0.1 µF capacitor to digital/signal GND. There cannot be a shorting of the connections to a common point before these capacitors.		
		Verify on magnetics if each cable side center-tap moves through a 75Ω resistor.		
		Verify if the center taps of all pairs move to a common point through a 1000 pF, 2-kV capacitor to chassis GND.		
	Section 4.3, "10/100 MBPS Interface Connection" (10/100 only)	Verify if each pair's positive and negative connections move to the following: Pair A – Pair 1 of the magnetics Pair B – Pair 2 of the magnetics Pair C – No Connect (NC) Pair D – No Connect (NC)		
	Section 4.4, "10/100 Magnetics Connection" (10/100 only)	Verify if each of Pair A and Pair B center taps move from a 0.1 µF capacitor to digital/signal GND. There cannot be a shorting of the connections to a common point before these capacitors.		
		Verify on magnetics if each cable side center-tap goes through a 75Ω resistor terminated with RJ45 pins 4/5 and RJ45 pins 7/8 through a 1000 pF, 2-kV capacitor.		
	Section 4.5, "10/100 MBPS RJ45 Connection" (10/100 only)	Verify if pins 4/5 and 7/8 of the RJ45 connect to CAT-5 cable and are terminated to chassis ground through a 1000-pF, 2-kV capacitor.		

TABLE 9-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 5.0, "Clock Circuit"	Section 5.1, "Crystal and External Oscillator/Clock Connections for MII Mode"	Verify the use of 25 MHz ±50 ppm crystal or 25 MHz ±50 ppm clock source.		
Section 6.0, "Digital Interfaces"	Section 6.1, "RGMII™ Interface"	Confirm proper RMII™ signals between MAC and PHY interface based on Table 6-2.		
	Section 6.2, "RGMII™ Series Source Termination" and Section 6.3, "Required External Pull-ups"	Confirm proper RMII signals between MAC and PHY interface with correct termination resistors (33Ω) and external pull-up for MDIO signal.		
Section 7.0, "Startup"	Section 7.1, "Reset Circuit"	Confirm proper reset circuit design: standalone reset or external CPU/FPGA reset.		
	Section 7.2, "Configuration Mode Pins (Strapping Options)"	Confirm mode settings and PHYAD (PHY Address) settings.		
		In systems where the MAC receive input pins are driven high after reset, it is recommended to add 1 kΩ pull-downs on the PHY strap pins.		
	Section 7.3, "LED Pins"	If used, confirm proper connections, taking into consideration shared functionality on select LED pins.		
Section 8.0, "Miscellaneous"	Section 8.1, "REXT Resistor"	Confirm proper REXT resistor (6.04 kΩ, 1.0%).		
	Section 8.2, "Other Considerations"	Incorporate a large SMD footprint (SMD_1210) to connect the chassis ground to the chip ground instead of the digital ground.		
		Incorporate sufficient power plane bulk capacitors (4.7 µF to 22 µF).		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003370A (02-05-2020)	Initial release	

THE MICROCHIP WEBSITE

Microchip provides online support via our WWW site at www.microchip.com. This website is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the website contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip website at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the website at: http://microchip.com/support

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

ISBN:978-1-5224-5576-9

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

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