Interfacing Timing Devices to Switchtec™ Devices

Introduction

The PM85xx family of Switchtec™ PCIe switch devices require a number of PCIe reference clocks to operate. This application note shows the biasing and termination networks needed to connect various families of Microsemi timing products to the PM85xx devices. It also shows methods for power supply sequencing that will satisfy the requirements of the Switchtec devices and the timing devices.

ZL30251 Clock Multiplier and Frequency Synthesizer Family

The ZL30251 is a 3-output clock multiplier and frequency synthesizer device which can be used to provide 100 MHz reference clocks to the PM85xx devices. This section shows how the device should be connected to the PM85xx device reference clock input, and shows the power supply sequencing options for the devices.

The following devices have the same output drivers as the ZL30251, and can be connected to the PM85xx reference inputs in the same way as the ZL30251 outputs: ZL30151, ZL3025x, ZL30169, ZL30244, ZL30245, ZL30255, ZL30182, ZL3062x, ZL3072x

Interconnection

The ZL30251 output drivers can be configured as CML or HSTL.

When configured for CML, the drivers have 50Ω internal pull-ups to VDD. The driver should be set to 800mV. Since the Voh voltage of the CML driver is greater than the maximum voltage allowed by the PM85xx receiver, the interface must be AC coupled. The differential signal should be terminated in a 100Ω resistor as shown in Figure1. Because of the double termination (50Ω in the ZL30251 and 100Ω at the end of the transmission line), the signal swing at the receiver will be attenuated by half. If the driver is set to 800mV, the swing at the receiver will be 400mV, meeting the Vid_min of the receiver with margin.

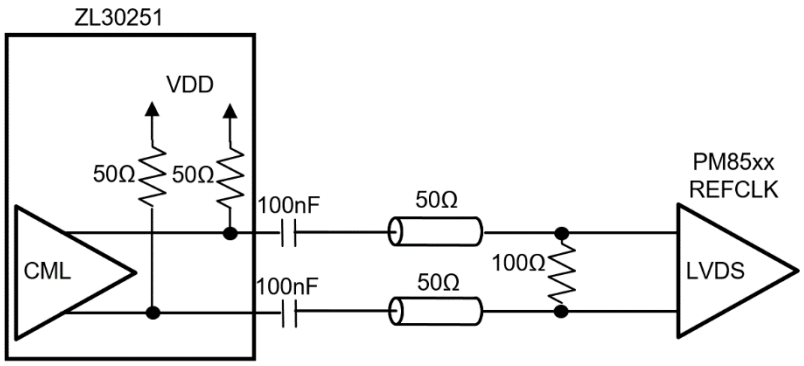

Figure 1 **AC-Coupled Termination for ZL30251 with CML Drivers**

If DC coupling is required, the ZL30251 output should be configured for HSTL. In this mode, the VDDO for the driver should be connected to 1.8V, so that the swing of the reference clock is below the 2.0V maximum of the receiver.

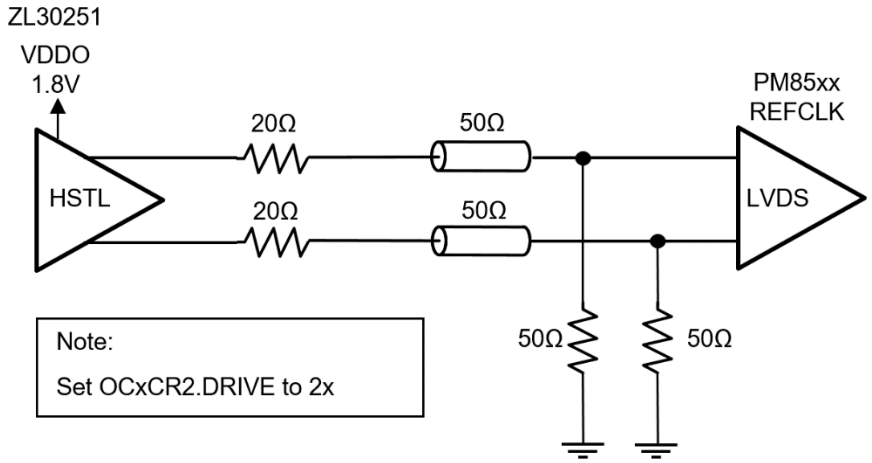

Figure 2 **DC-Coupled Termination for ZL30251 with HSTL Drivers**

It is also possible to connect VDDO to 1.5V, use 30Ω series resistors, and set OCxCR2.DRIVE to 4x.

Power Sequencing for the ZL30251 Family

Note that the ZL30251 requires that the 3.3V rail be powered on before or at the same time as the 1.8V rail. The PM85xx requires the opposite sequence. Please see section Power Sequencing Suggestions for Devices Requiring Opposite Sequence for suggestions on managing the sequencing requirements.

ZL30267 10-Output Clock Multiplier and Frequency Synthesizer Family

The ZL30267 is a 10-output clock multiplier and frequency synthesizer device which can be used to provide 100 MHz reference clocks to the PM85xx devices. This section shows how the device should be connected to the PM85xx device reference clock input, and shows the power supply sequencing options for the devices.

The following devices have the same output drivers as the ZL30267, and can be connected to the PM85xx reference inputs in the same way as the ZL30267 outputs: ZL3026x and ZL40250, ZL40251, ZL40252, ZL40253.

Interconnection

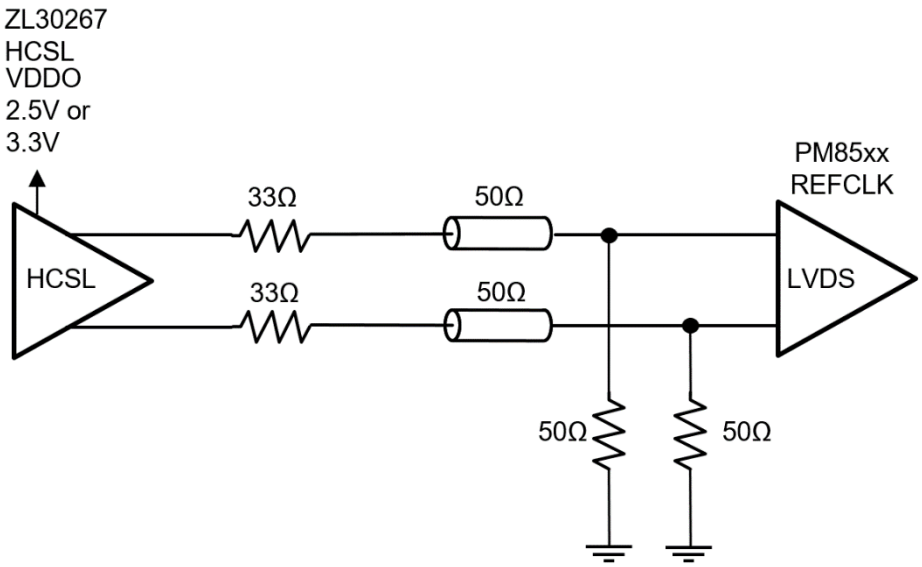

Figure 3 **DC-coupled Termination for ZL30267 with HCSL outputs**

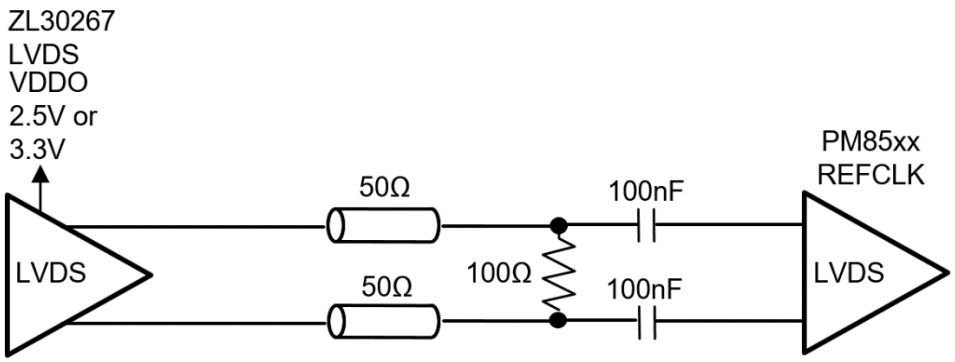

Figure 4 **AC-coupled Termination for ZL30267 with LVDS or Programmable Diff outputs**

Note that if Programmable Diff outputs are selected, V_{OD} should be set to 400 mV. The setting for V_{CM} doesn't matter since the circuit is AC coupled.

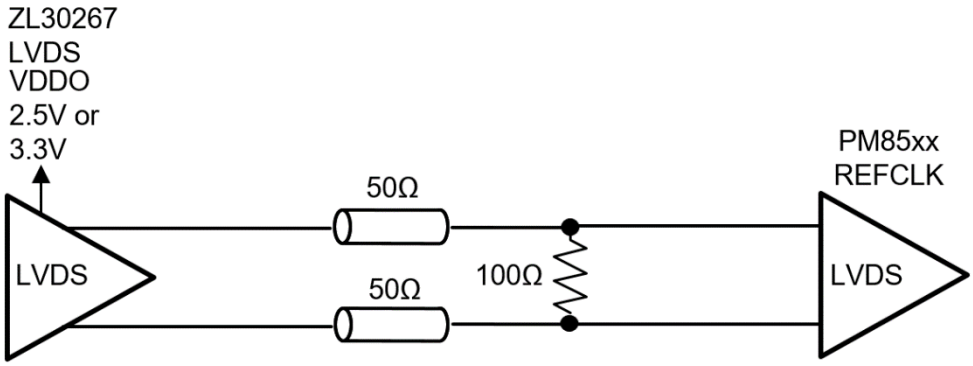

Figure 5 **DC-coupled Termination for ZL30267 with LVDS or Programmable Diff Outputs**

Note that if Programmable Diff outputs are selected, V_{CM} should be set to 1.2V, and V_{OD} should be set to 400 mV.

Power Sequencing for the ZL30267 Family

Note that the ZL30267 requires that the 3.3V rail be powered on before or at the same time as the 1.8V rail. The PM85xx requires the opposite sequence. Please see section Power Sequencing Suggestions for Devices Requiring Opposite Sequence for suggestions on managing the sequencing requirements

ZL40230 10-Output Clock Buffer Family

The ZL40230 is a 10-output clock buffer device which can be used to provide 100 MHz reference clocks to the PM85xx devices. This section shows how the device should be connected to the PM85xx device reference clock input, and shows the power supply sequencing options for the devices.

The following devices have the same output drivers as the ZL40230, and can be connected to the PM85xx reference inputs in the same way as the ZL40230 outputs: ZL40231,ZL40234, and ZL40235.

There are several options for interconnection, as shown in the following section.

Interconnection

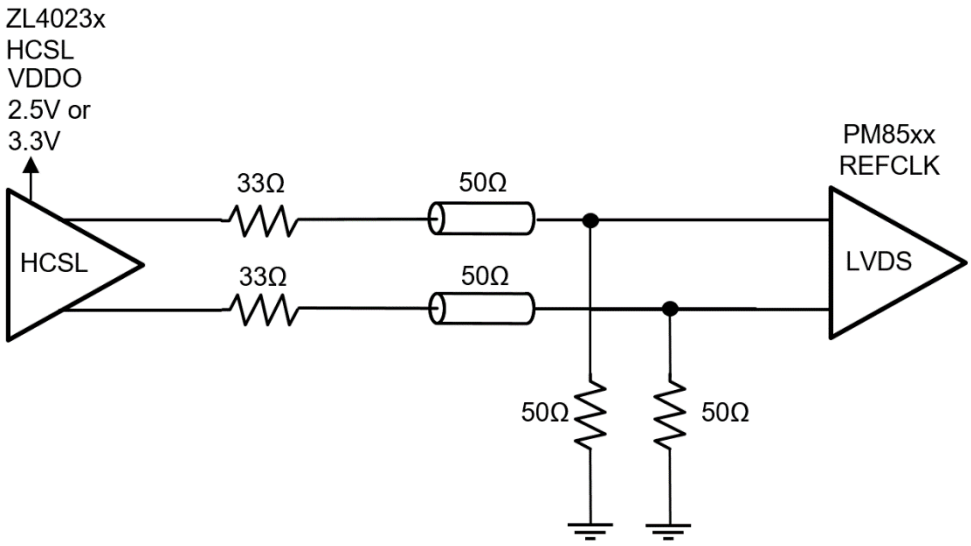

Figure 6 **DC-coupled Termination for ZL4023x with HCSL outputs**

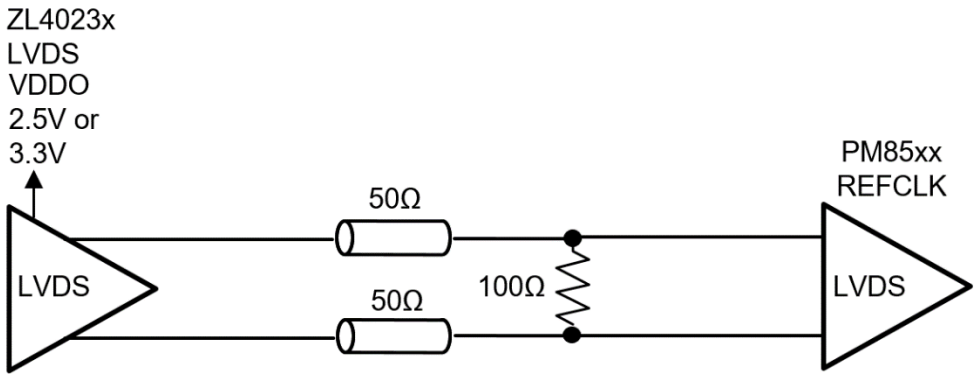

Figure 7 **DC-coupled Termination for ZL4023x with LVDS outputs**

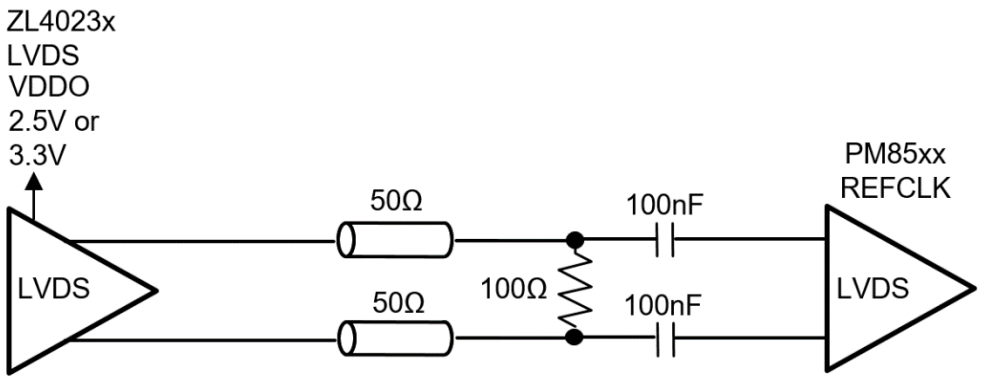

Figure 8 **AC-coupled Termination for ZL4023x with LVDS outputs**

Power Sequencing for the ZL40230 Family.

The ZL40230 family of devices does not have a requirement on power supply sequencing, so no special provisions are required. The PM855x power sequencing should be followed – 1.8V should be provided before 3.3V.

Power Sequencing Suggestions for Devices Requiring Opposite Sequence

The ZL30251 family and the ZL30267 family required the 3.3V supply to be applied before or at the same time as the 1.8V supply. The PM85xx family requires the opposite sequence – that is 1.8V should be applied before 3.3V. This can cause difficulties in designing a power circuit that satisfies all the device families.

One way to meet this objective is to power the 3.3V rail for the ZL30xxx devices from the same regulator that powers the 3.3V rail of the PM85xx. Then the 1.8V rail for the ZL30xxx can be supplied from a dedicated 1.8V regulator powered from the 3.3V rail. The 1.8V rail for the PM855x must be supplied by some other means, and it must be provided prior to the 3.3V rail being supplied.

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