VSC8572/VSC8574
Application Note
VSC8572/VSC8574 Transition Design Guide

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Revision 2.0 was the second release of this document published in September 2012. In this revision, the API Software section was updated to address previous errata considerations.

1.2 Revision 1.0

Revision 1.0 was the first release of this document. It was published in July 2012.

2 Introduction

This document highlights considerations when transitioning through one of the following device changes.

1. VSC8572 (revision C) to VSC8572-01 (revision D)
2. VSC8572-03 (revision C) to VSC8572-04 (revision D)
3. VSC8574 (revision C) to VSC8574-01 (revision D)
4. VSC8574-03 (revision C) to VSC8574-04 (revision D)

3 Package, Pinout, and Marking Changes

Revision D uses the same package as revision C. There are no pinout changes moving from revision C to revision D.

Revision D uses copper bond wires instead of gold bond wires. As part of the copperwire implementation, the mold compound changed.

A solid white square mark, used to identify screening to specific ATE test criteria, is no longer printed on revision D devices.

4 Design Recommendations

4.1 API Software

Vitesse requires using API revision 4.03 or greater for Revision D. Revision 4.03 is the first API revision to include:

- Initialization scripts required by the new revision containing:
  - Optimal settings for link performance in 100Base-TX and 1000Base-TEEE modes. This was a revision C erratum.
  - Optimal settings for 10Base-Te signal performance. This was a revision C erratum.
- Ability to disable the “New SPI Mode” software workaround on the old revision for the “truncated timestamp output” erratum. This erratum is fixed in revision D silicon. Any customer using the recommended software workaround for the old revision can continue to do so in the new revision. However, Vitesse recommends disabling the “New SPI Mode” and utilizing the SPI bus as described in the revision D datasheet.

See the appropriate revision C errata document on the web for more information on the above errata.

4.2 Device ID Changes

The device revision number, in IEEE802.3 register 3 bits 3:0, has been changed to “0010” in revision D. In addition, the device version, bits 31-28, in the JTAG user-code device identification register has been changed to “0010”.

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