VSC8501/VSC8502

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip VSC8501/VSC8502 product family. It is meant to help customers achieve first-pass design success.

Note: The VSC8501 and VSC8502 use the same 136-pin Advanced Quad Flat No-Lead (aQFN) package. The VSC8501 has one port while the VSC8502 has two ports. Pin comparison is shown in Table 2-1.

These checklist items should be followed when utilizing the VSC8501/VSC8502 in a new design. A summary of these items is provided in Section 11.0, "Hardware Checklist Summary". Detailed information on these subjects can be found in the corresponding sections:

- Section 2.0, "General Considerations"
- Section 3.0, "Power"
- Section 4.0, "Thermal Considerations"
- Section 5.0, "Media Interface"
- Section 6.0, "Clock Circuit"
- Section 7.0, "MAC Interface"
- Section 8.0, "RGMII Interface Clock Considerations"
- Section 9.0, "Serial Management Interface (SMI)"
- Section 10.0, "Miscellaneous"

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The VSC8501/VSC8502 implementor should have the following documents on hand:

- *VSC8501-03 Data Sheet* or *VSC8502-03 Data Sheet*
- *Advanced Quad Flat No-Lead (aQFN) Package Surface Mount Assembly Guidelines - ENT-AN1232*
- *VSC8502RD(-VR) Reference Design Board Files - VPPD-03820* (This provides the schematics for external regulator power setup. Ignore the internal regulator design.)
- ENT-AN0098 Application Note Magnetics Guide

These documents can be found at www.microchip.com/VSC8501 and www.microchip.com/VSC8502.

2.2 Design Considerations

- For the VSC8501, refer to the “Design Considerations” section of the *VSC8501 Data Sheet*.
- For the VSC8502, refer to the “Design Considerations” section of the *VSC8502 Data Sheet*.

2.3 Pin Check

- Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.
- Table 2-1 provides a list of the pins that differ between these two devices:

TABLE 2-1: VSC8501 AND VSC8502 PIN COMPARISON

Pin Number	VSC8501 Pin Name	VSC8502 Pin Name
A4	FASTLINK_FAIL/PHYADD0	FASTLINK_FAIL
A5	RESERVED_36	LED2_PHY1
A6	RESERVED_31	RXD5_1
A7	RESERVED_30	RXD4_1
A9	RESERVED_20	TX_CLK_1
A10	RESERVED_16	TXD0_1
A11	RESERVED_15	TXD1_1
A12	RESERVED_12	TXD4_1
A13	RESERVED_9	TXD7_1
A26	PHYADD1	RCVRDCLK1/PHYADD1
A30	RESERVED_7	P1_D3N
A31	RESERVED_6	P1_D3P
B5	RESERVED_37	LED3_PHY1
B6	RESERVED_33	RXD7_1
B7	RESERVED_28	RXD2_1
B8	RESERVED_25	RX_DV_1/RX_CTL_1
B9	RESERVED_24	RX_ER_1
B10	RESERVED_17	TX_EN_1/TX_CTL_1
B11	RESERVED_22	CRS_1
B12	RESERVED_11	TXD5_1
B13	RESERVED_10	TXD6_1
B28	RESERVED_3	P1_D1N
B29	RESERVED_2	P1_D1P
C2	RESERVED_35	LED1_PHY1
C4	RESERVED_26	RXD0_1
C5	RESERVED_21	COL_1
C6	RESERVED_19	GTX_CLK_1/TXC_1
C7	RESERVED_23	RX_CLK_1
C8	RESERVED_13	TXD3_1
C10	RESERVED_8	MDINT_1
C23	RESERVED_5	P1_D2N
C24	RESERVED_4	P1_D2P
C25	RESERVED_1	P1_D0N
C26	RESERVED_0	P1_D0P
D8	RESERVED_29	RXD3_1
D9	RESERVED_27	RXD1_1
D11	RESERVED_18	TX_ER_1
D12	RESERVED_14	TXD2_1
E6	RESERVED_34	LED0_PHY1
E8	RESERVED_32	RXD6_1

2.4 Ground Considerations

This section shows the ground considerations for VSC8501/VSC8502. Section 4.0, "Thermal Considerations" also explains the importance of grounds for thermal dissipation.

2.4.1 EXPOSED GROUND PAD

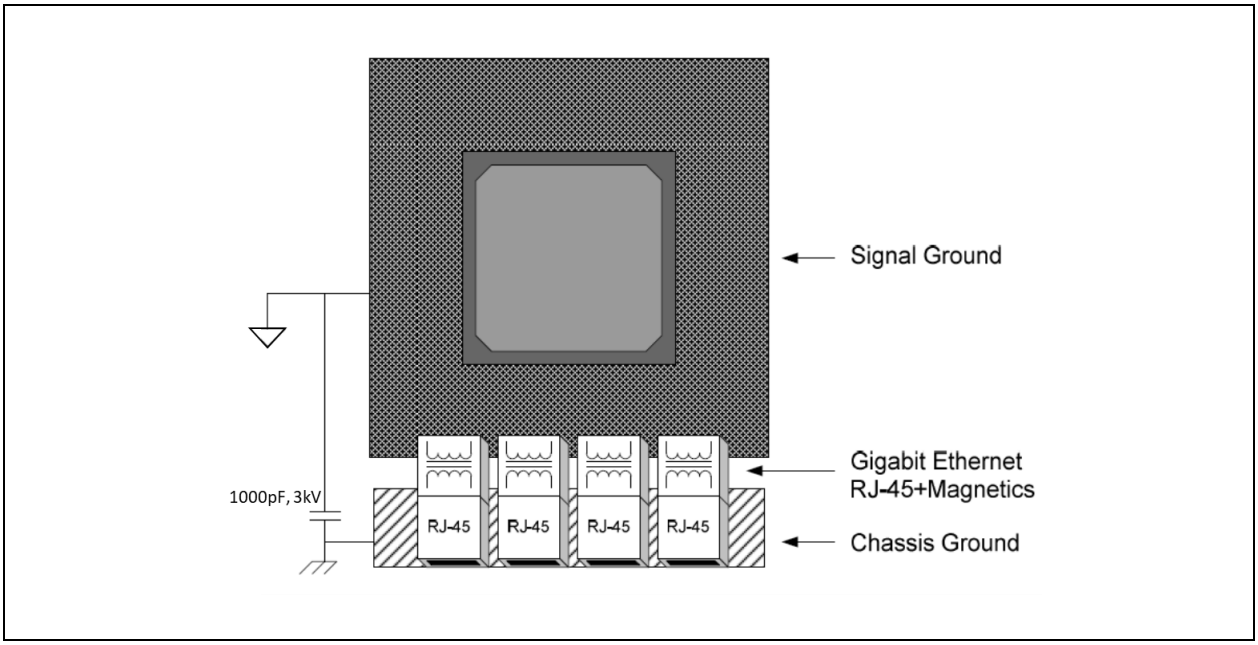
The VSC8501/VSC8502 has an Advanced Quad Flat No-Lead (aQFN) 136-pin package. The package has an exposed pad at the bottom of the device. The exposed pad provides a path for electrical grounding as well as a heat transfer point to the PCB and is sometimes referred to as the “thermal paddle”. (See Section 4.0, "Thermal Considerations".) The pad provides a very low inductive to the ground plane, which is ideal for high-speed applications. The pad is soldered directly to the land pattern of the PCB. The size of the land pattern can be larger than the exposed pad of the device; however, the solder mask must not be larger than the exposed pad. Additional exposed pad PCB design guidelines can be found in Section 4.0, "Thermal Considerations".

Note: These exposed pad recommendations are guidelines based on generic design practices applicable to most customer applications. It is also important to consider repair and rework issues of the assembled product. Check with the PCB manufacturer and assembly house of the end product using this device to determine if additional design rules must be met. Specifically, the reader is encouraged to seek application notes directly from the packaging vendor on the best practice design with the package type. For example, per ASE guidelines, stencil openings are recommended to be 20% of exposed paddle area, in 2x2 array.

2.4.2 GROUND ISOLATION

To isolate the board from ESD events and to prevent a Common-mode noise ground path, a separate chassis ground region should be allocated. This separate chassis ground, as shown in Figure 2-1, should be electrically connected to the external chassis and to the shield ground of the RJ-45 connectors.

FIGURE 2-1: GROUND PLANE LAYOUT



3.0 POWER

3.1 Power Supply and Ground Pins

The VSC8501/VSC8502 family does not provide on-chip regulators. Table 3-1 lists the power supply pins and associated functional pins. All power supply pins must be connected to their respective voltage input, even if certain functions are not used for a specific application. No power supply sequencing is required. However, clock and power must be stable before releasing NRESET from ground.

TABLE 3-1: POWER SUPPLY AND GROUND PINS

Name	Pin	Description
VDD1	D6, D7, D18, D20	1.0V digital core power supply
VDD1A	D26, D28, D30, D32	1.0V analog power requiring additional PCB power supply filtering
VDD25A	D27, D29, D31	2.5V analog power requiring additional PCB power supply filtering
VDDIO	D5, D21, D22	2.5V or 3.3V general I/O power supply
VDDMAC0	C12, E10, E11	2.5V or 3.3V RGMII/GMII/MII MAC power supply for PHY0
VDDMAC1	C3, C9, D10	2.5V or 3.3V RGMII/GMII/MII MAC power supply for PHY1
VDDMDIO	D13	1.2V, 2.5V or 3.3V power for SMI pins
RESERVED	E2, E16	Reserved signal, connect to device V_{SS}
VSS_CASE	Exposed pad, E7	Common device ground

Note: The **VDDMAC1** pins shall be connected to the same external supply rail as VDDMAC0. It is a required supply input on the VSC8501 single PHY port device. It is also a required supply input even if PHY1 is unused on the VSC8501/VSC8502 dual PHY device.

3.2 Defeatured Internal Regulator Pins

The **RESERVED** pins listed in Table 3-2 should be left unconnected, and the Regulator Enable (REG_EN_*) pins should be grounded.

TABLE 3-2: REGULATOR PINS

Name	Pin	Type	I/O Domain	Description
RESERVED	D24	A	VDDREG_33	Reserved signal, leave unconnected
RESERVED	B1	A	VDDREG_33	Reserved signal, leave unconnected
RESERVED	E15	A	VDDREG_33	Reserved signal, leave unconnected
RESERVED	E3	A	VDDREG_33	Reserved signal, leave unconnected
RESERVED	D25	A	VDDREG_33	Reserved signal, leave unconnected
RESERVED	D1	A	VDDREG_33	Reserved signal, leave unconnected
REG_EN_10	C18	A	VDDREG_33	Connect to device V_{SS}
REG_EN_25	D2	A	VDDREG_33	Connect to device V_{SS}
RESERVED	E17	A	VDDREG_33	Reserved signal, leave unconnected
RESERVED	E1	A	VDDREG_33	Reserved signal, leave unconnected

Note 1: This pin shall be connected to the same external supply rail as VDDMAC0. It is a required supply input for the single-port as well as the dual-port device.

3.3 Power Supply Planes

- The VSC8501/VSC8502 requires a minimum of two power rails, 1.0 and 2.5V. The filtered analog 1.0V and 2.5V supplies should not be shorted to any other digital supply at the package or PCB level. Refer to the data sheet for other power-supply options.
- The most important PCB design and layout considerations are as follows:
  - Ensure that the return plane is adjacent to the power plane (without a signal layer in between).
  - Ensure that a single plane is used for voltage reference with splits for individual voltage rails within that plane.

Try to maximize the area of each power split on the power plane based on corresponding via coordinates for each rail to maximize coupling between each voltage rail and the return plane.

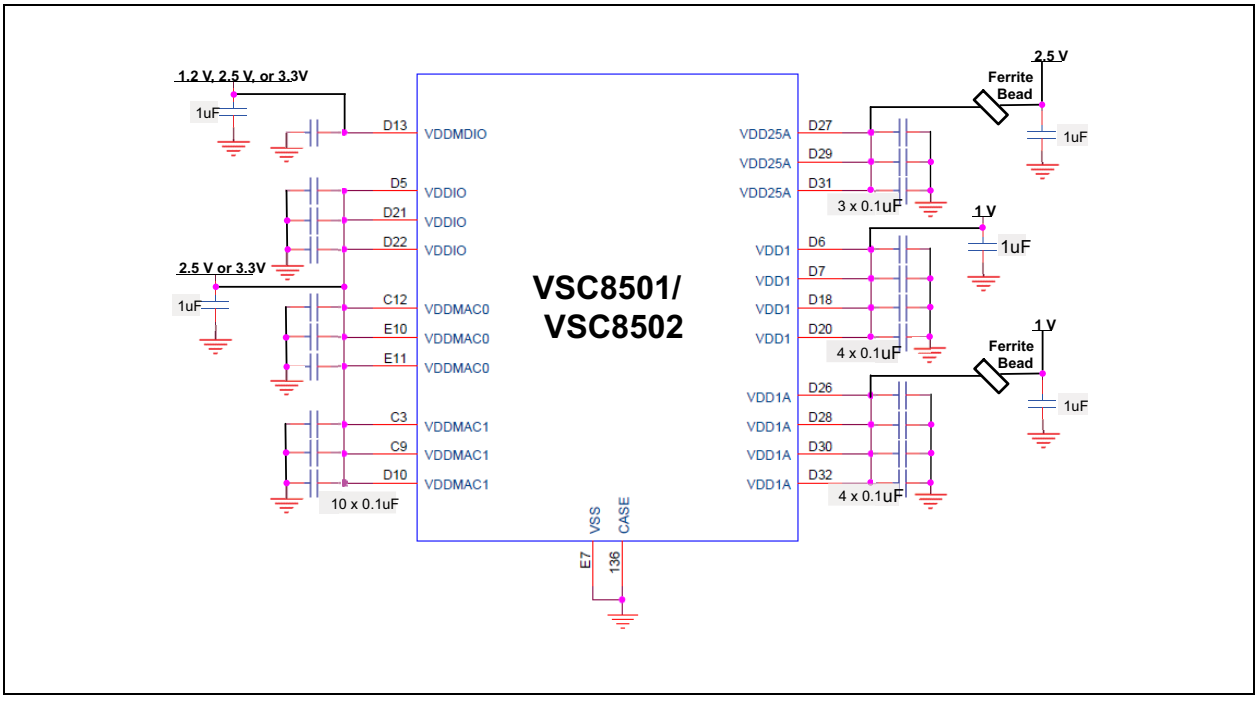
- Minimize resistive drop while efficiently conducting away heat from the device using one-ounce copper cladding.

- Four-layer PCBs with only one designated power plane must adhere to proper design techniques to prevent random system events, such as CRC errors. Each power supply requires the lowest resistive drop possible to power pins of the device with correctly positioned local decoupling. For more information, see Section 3.5, "Decoupling Capacitors".
- Ferrite beads should be used over a series inductor filter whenever possible, particularly for high-density or high-power devices.

3.4 Power Circuit Connection and Analog Power Plane Filtering

- The analog power supplies are VDD25A and VDD1A.
- A ferrite bead should be used to isolate each analog supply from the rest of the board. The bead should be placed in series between the bulk decoupling capacitors and local decoupling capacitors.
- Because all PCB designs yield unique noise coupling behavior, not all ferrite beads or decoupling capacitors may be needed for every design. It is recommended that system designers provide an option to replace the ferrite beads with 0Ω resistors once a thorough evaluation of system performance is completed.
- Ferrite beads are *not* recommended on digital supplies VDD1A and VDD25A.

FIGURE 3-1: POWER SUPPLY CONNECTIONS AND LOCAL FILTERING



3.5 Decoupling Capacitors

- Bulk decoupling capacitors should be tantalum electrolytic and can be placed at any convenient position on the board. Make sure that bulk capacitors (4.7 µF to 22 µF) are incorporated in each power rail of power supply.
- Local decoupling capacitors should be X5R or X7R ceramic and placed as close as possible to the VSC8501/VSC8502's power pins for each power pin. Assuming that the VSC8501/VSC8502 is on the top side of a PCB board, the best location for local decoupling capacitors is on the bottom/underside of the PCB board directly under the device.

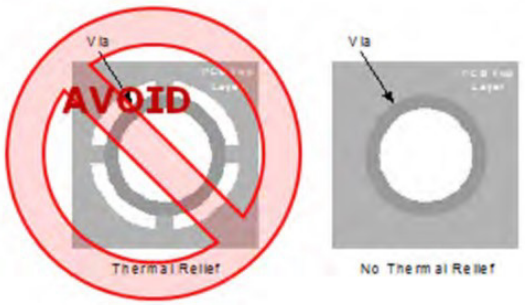
3.6 Current Requirements

- Consult the relevant data sheet for maximum current requirements.

4.0 THERMAL CONSIDERATIONS

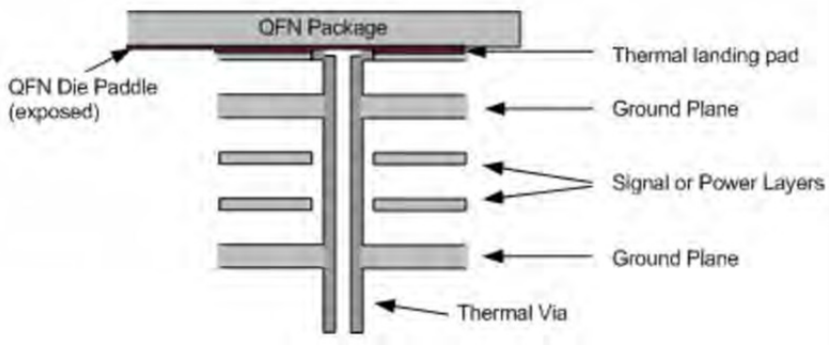
- For proper cooling, maximize the number of via connections to the ground plane for efficient thermal dissipation. Furthermore, additional ground planes enhance thermal dissipation and signal integrity performance. For the multi-row QFN package, because the die-attach (or thermal) paddle is exposed and directly conducts heat away from the die, thermal vias should be drilled within the landing boundary, opposite the exposed paddle. The VSC8502 PCB reference design package includes an example of appropriate thermal connections for this device.
- When connecting the thermal vias to ground planes, it is advisable to avoid thermal-relief connection traces as shown on the left-hand side of Figure 4-1 as these are designed to prevent the flow of heat through the PCB. Instead, the thermal vias should have a solid connection to the traces and planes on each layer as shown on the right-hand side of Figure 4-1.

FIGURE 4-1: THERMAL VIAS



- To dissipate heat below the package, the PCB thermal vias should connect to the solid ground planes within the board (minimum 1-oz. cladding is recommended). Refer to Figure 4-2 for a simplistic profile of a thermal via within the PCB's thermal land area below the multi-row QFN paddle; package I/O pins and their corresponding pads are not shown. Also, steps should be taken to prevent solder wicking by the thermal vias. To avoid solder wicked by the thermal via during the soldering process, it is recommended that the vias be fully copper plated. If copper plating does not plug the vias, thermal vias can be tented with solder mask on the top layer. The solder mask should be larger than the diameter of the via.

FIGURE 4-2: THERMAL GROUND PLANE CONNECTION



5.0 MEDIA INTERFACE

5.1 PHY → Magnetics

Note: For VSC8501, "*Pn*" represents Port 0 (P0). For VSC8502, "*Pn*" represents Port 0 (P0) and Port 1 (P1).

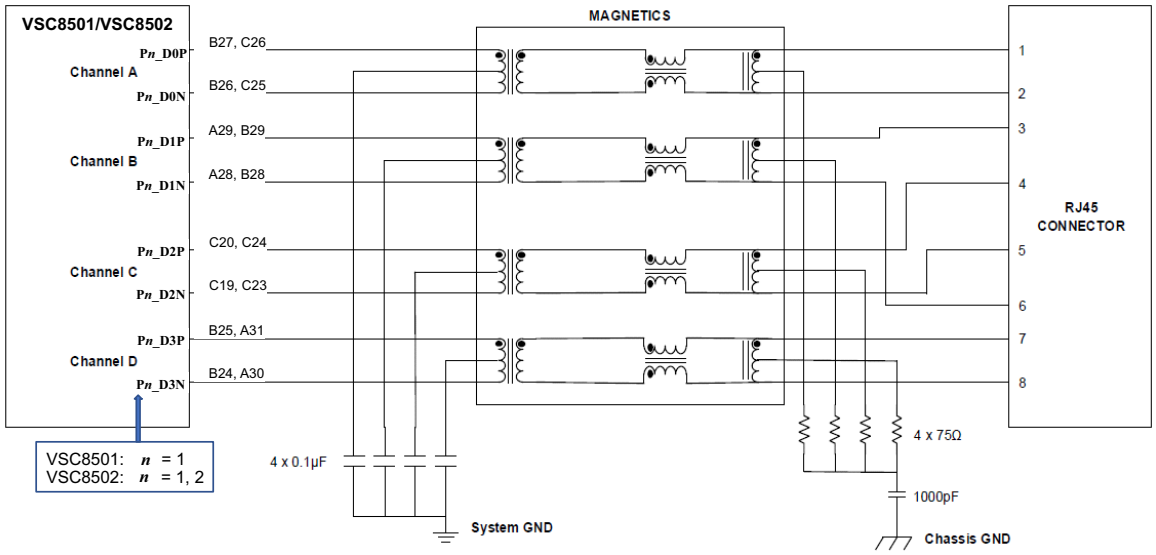
- ***Pn*_D0N** (B26, C25): This pin is the transmit/receive (TX/RX) negative connection from Pair A of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- ***Pn*_D0P** (B27, C26): This pin is the TX/RX positive connection from Pair A of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- ***Pn*_D1N** (A28, B28): This pin is the TX/RX negative connection from Pair B of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- ***Pn*_D1P** (A29, B29): This pin is the TX/RX positive connection from Pair B of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- ***Pn*_D2N** (C19, C23): This pin is the TX/RX negative connection from Pair C of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- ***Pn*_D2P** (C20, C24): This pin is the TX/RX positive connection from Pair C of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- ***Pn*_D3N** (B24, A30): This pin is the TX/RX negative connection from Pair D of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- ***Pn*_D3P** (B25, A31): This pin is the TX/RX positive connection from Pair D of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.

For 10/100/1000 Mbps channel connection details, refer to Figure 5-1.

5.2 Magnetics → RJ-45

- The center tap connection on the VSC8501/VSC8502 side for Pair A channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center tap connection on the VSC8501/VSC8502 side for Pair B channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center tap connection on the VSC8501/VSC8502 side for Pair C channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center tap connection on the VSC8501/VSC8502 side for Pair D channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center taps from all four pairs of the magnetic should not be connected together. The reason is the Common-mode voltage can be different between pairs, especially for 10/100 operation. (Pairs A and B are active, while Pairs C and D are inactive.)
- The center tap connection for each pair (A, B, C and D) on the cable side (RJ-45 side) should be terminated with a 75Ω resistor through a common 1000 pF, 2 kV capacitor to chassis ground.
- Only one 1000 pF, 2 kV capacitor to chassis ground is required. It is shared by Pair A, Pair B, Pair C and Pair D center taps.
- The RJ-45 shield should connect to chassis ground. This includes RJ-45 connectors with or without integrated magnetics. (See Section 5.4, "Other Considerations" for guidance on how chassis ground should be created from system ground.)
- For the magnetics selection, refer to magnetics suggested guidelines (ENT-AN0098 Application Note Magnetics Guide on the device product page) for reference.

FIGURE 5-1: CHANNEL CONNECTIONS



5.3 Layout Considerations

The **TXVPx_n** and **TXVNx_n** pins interface to the external CAT5 cable and are organized in four differential pairs (x = A, B, C, D) for each PHY port. When routing these pairs on a PCB, the characteristics must match either of the following:

- Route each trace single-ended with a characteristic impedance of 50Ω referenced to ground.
- Route each positive and negative trace on each port as differential pairs with 100Ω characteristic differential impedance.

5.4 Other Considerations

Incorporate an SMD ferrite bead footprint to connect the chassis ground to the system ground. This allows some flexibility at EMI testing for different grounding options if leaving the footprint open keeps the two grounds separated. For best performance, short the grounds together with a ferrite bead or a capacitor. Users are required to place the capacitor/ferrite bead far away from the VSC8501/VSC8502 device in PCB layout placement for better ESD.

6.0 CLOCK CIRCUIT

6.1 Clock Inputs

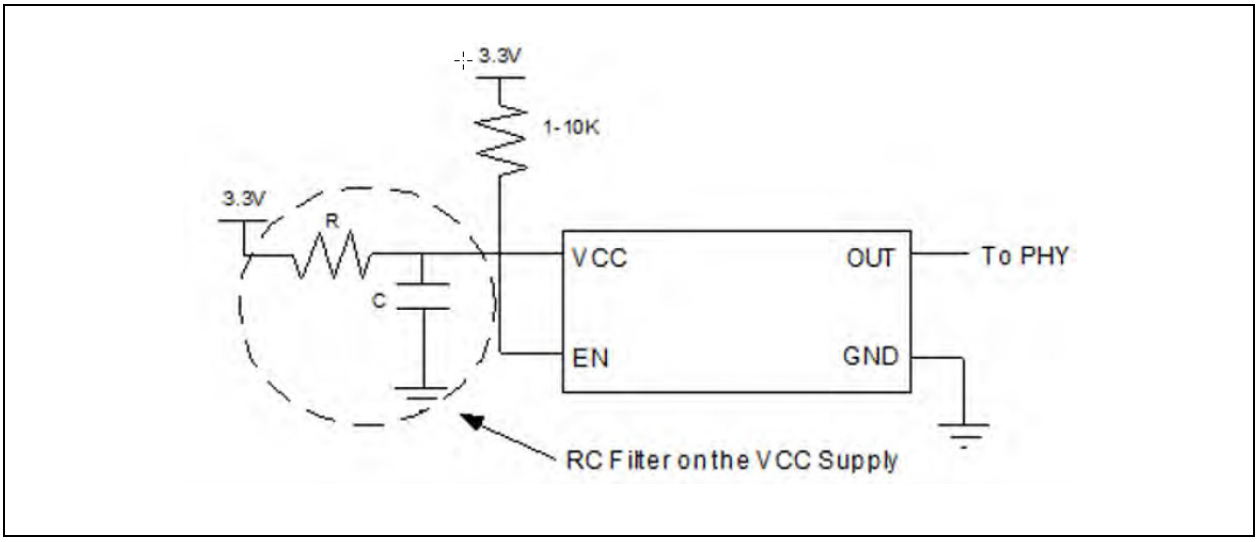
The device reference clock supports a single-ended, CMOS logic-level drive clock signal with either a 25 MHz or a 125 MHz frequency.

The **REFCLK_SEL** pin configures the reference clock frequency (defaults to 25 MHz with an on-chip pull-up resistor) that is expected as input on the **REFCLK** input pin. Refer to the data sheet for additional details.

6.2 Clock Power Supply Filtering

If using a 25 MHz or a 125 MHz 4-pin oscillator with a **VCC** pin, it is recommended that an RC filter be implemented to avoid power-supply switching noise coupling into the PHY. The filter should be set to filter out the frequency of the supply's switching regulation frequency. The OUT signal should be tied to **REFCLK**.

FIGURE 6-1: CLOCK POWER SUPPLY FILTERING



Thus, for a supply with a switching frequency of 350 kHz, use an R value of 2.2Ω and a C value of 11 µF.

7.0 MAC INTERFACE

The VSC8501/VSC8502 supports MII, GMII and RGMII MAC interfaces.

The device pins dedicated to the MAC-PHY interface is shown in Table 7-1.

TABLE 7-1: MAC INTERFACE PINS

Pin Name	Pin Number	Type	I/O Domain		PHY		Description
			VDDMAC0	VDDMAC1	VSC8501	VSC8502	
COL_0	E9	O	√	—	√	√	GMII/MII collision output for PHY0
CRS_0	C15	O	√	—	√	√	GMII/MII carrier sense output for PHY0
GTX_CLK_0/TXC_0	B16	I, PD	√	—	√	√	GMII/RGMII transmit clock input for PHY0
RX_CLK_0	D16	O	√	—	√	√	GMII/MII receive clock output for PHY0
RX_DV_0/RX_CTL_0	D15	O	√	—	√	√	GMII/MII receive data valid output/ RGMII receive control output for PHY0
RX_ER_0	C14	O	√	—	√	√	GMII/MII receive data error output for PHY0
RXD[0:3]_0	A19, B15, A18, D14	O	√	—	√	√	RGMII/GMII/MII data output for PHY0
RXD[4:7]_0 (Note 1)	C13, A17, A16, B14	O	√	—	√	√	GMII data output for PHY0
TX_CLK_0 (Note 2)	D17	O	√	—	√	√	MII transmit clock output for PHY0
TX_EN_0/TX_CTL_0	C16	I, PD	√	—	√	√	GMII/MII transmit data enable input/ RGMII transmit data control input for PHY0
TX_ER_0	A21	I, PD	√	—	√	√	GMII/MII transmit data error input for PHY0
TXD[0:3]_0	A22, B17, D19, A23	I, PD	√	—	√	√	RGMII/GMII/MII data input for PHY0
TXD[4:7]_0	B18, B19, E12, A24	I, PD	√	—	√	√	GMII data input for PHY0
COL_1	C5	O	—	√	—	√	GMII/MII collision output for PHY1
CRS_1	B11	O	—	√	—	√	GMII/MII carrier sense output for PHY1
GTX_CLK_1/TXC_1	C6	I, PD	—	√	—	√	GMII/RGMII transmit clock input for PHY1
RX_CLK_1	C7	O	—	√	—	√	GMII/MII receive clock output for PHY1
RX_DV_1/RX_CTL_1	B8	O	—	√	—	√	GMII/MII receive data valid output/ RGMII receive control output for PHY1

Note 1: When operating a PHY port in 1000 Mbps mode with the RGMII MAC interface, ingress data is driven on the **RXD[4:7]** output pins of the corresponding port. The **RXD[4:7]** pins should be ignored in that case because they are not specified for the RGMII interface.

2: When operating a PHY port in 1000 Mbps mode with the GMII MAC interface, the **TX_CLK** pin for the corresponding port will drive the TX_CLK output. TX_CLK should be ignored because it is not used in 1000 Mbps mode.

TABLE 7-1: MAC INTERFACE PINS (CONTINUED)

Pin Name	Pin Number	Type	I/O Domain		PHY		Description
			VDDMAC0	VDDMAC1	VSC8501	VSC8502	
RX_ER_1	B9	O	—	√	—	√	GMII/MII receive data error output for PHY1
RXD[0:3]_1	C4, D9, B7, D8	O	—	√	—	√	RGMII/GMII/MII data output for PHY1
RXD[4:7]_1 (Note 1)	A7, A6, E8, B6	O	—	√	—	√	GMII data output for PHY1
TX_CLK_1 (Note 2)	A9	O	—	√	—	√	MII transmit clock output for PHY1
TX_EN_1/TX_CTL_1	B10	I, PD	—	√	—	√	GMII/MII transmit data enable input/ RGMII transmit data control input for PHY1
TX_ER_1	D11	I, PD	—	√	—	√	GMII/MII transmit data error input for PHY1
TXD[0:3]_1	A10, A11, D12, C8	I, PD	—	√	—	√	RGMII/GMII/MII data input for PHY1
TXD[4:7]_1	A12, B12, B13, A13	I, PD	—	√	—	√	GMII data input for PHY1

Note 1: When operating a PHY port in 1000 Mbps mode with the RGMII MAC interface, ingress data is driven on the **RXD[4:7]** output pins of the corresponding port. The **RXD[4:7]** pins should be ignored in that case because they are not specified for the RGMII interface.

2: When operating a PHY port in 1000 Mbps mode with the GMII MAC interface, the **TX_CLK** pin for the corresponding port will drive the TX_CLK output. TX_CLK should be ignored because it is not used in 1000 Mbps mode.

7.1 Design Details

The guidelines in this section apply to all interfaces. With the high-speed nature of these interfaces, careful attention must be paid to the PCB layout to maintain adequate signal integrity. The MAC output pins have been designed with fast rise and fall times to allow for 125 MHz operation. To adequately accommodate these signals on a PCB, it is recommended that the traces be designed as either microstrip or stripline transmission lines with a characteristic impedance of 50Ω. It is also important that an unbroken plane exist below and/or above these signals.

The characteristic impedance of each MAC receive interface PCB trace must total 50Ω. For the VSC8501/VSC8502 MAC receive interface, each pin has a nominal output impedance of 11Ω, thus an external 39Ω series resistor is required for each signal of the MAC receive interface.

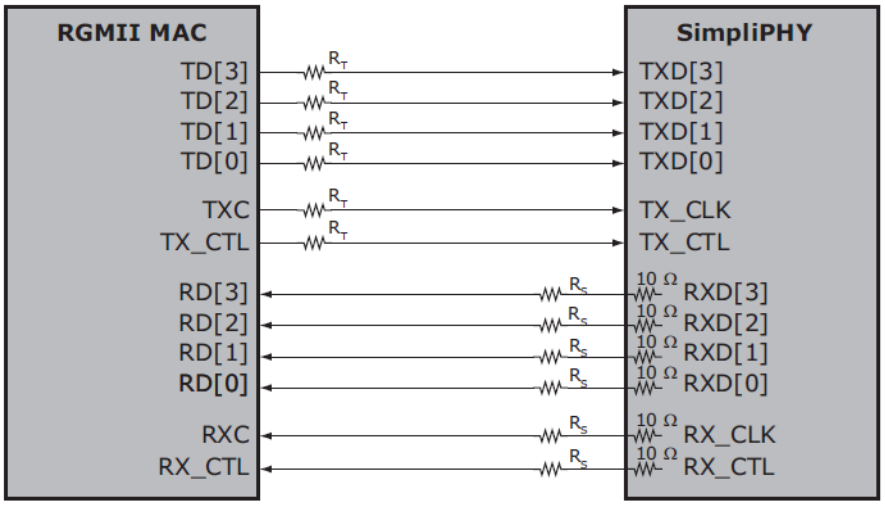
For the VSC8501/VSC8502 MAC transmit interface, careful attention must be paid to the output impedance of the pins on the MAC or switch device. If that impedance is less than 50Ω, additional series termination resistors are required. These resistors should be placed as close as possible to the MAC or switch device.

For MII and GMII routing, each port should be independently matched in length to within 120 mils (approximately 3 mm). It is not necessary to match the lengths of the TX traces to RX traces. The TX traces can be of a different length in respect to the RX trace lengths.

7.2 RGMII MAC Interface

The VSC8501/VSC8502 device supports RGMII versions 1.3 and 2.0 (2.5V). The RGMII interface supports all three speeds (10 Mbps, 100 Mbps and 1000 Mbps) and is used as an interface to an RGMII-compatible MAC.

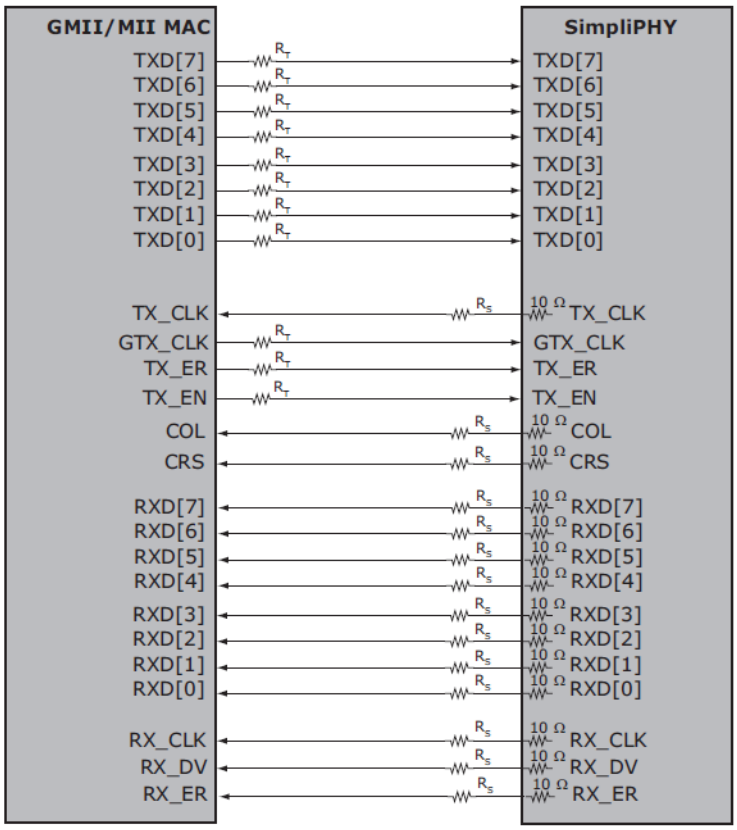
FIGURE 7-1: RGMII MAC INTERFACE



7.3 GMII/MII Interface

The GMII/MII interface supports all three speeds (10 Mbps, 100 Mbps and 1000 Mbps) and is used as an interface to a GMII/MII-compatible MAC.

FIGURE 7-2: GMII/MII MAC INTERFACE



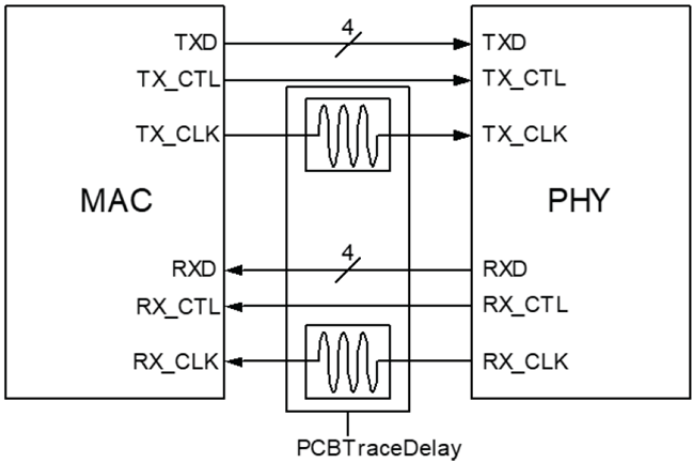
8.0 RGMII INTERFACE CLOCK CONSIDERATIONS

Proper operation of the RGMII bus requires careful control of the timing relationship between clock and data signals. The RGMII specification requires that the signal clock be delayed by a half-bit time (2 ns) at the receiving end of the data path. This clock delay can be added externally (extended clock trace length), or by using internal delays built into the VSC8501/VSC8502.

8.1 External Delay Compensation

A delay of 1.5 ns to 2.0 ns can be added to the TX_CLK[0:1] and RX_CLK[0:1] signals by routing them through a long PCB “trombone” trace delay. Figure 8-1 shows the delay-line routing for a single port (that is, the port suffixes are omitted from signal names in the following figures).

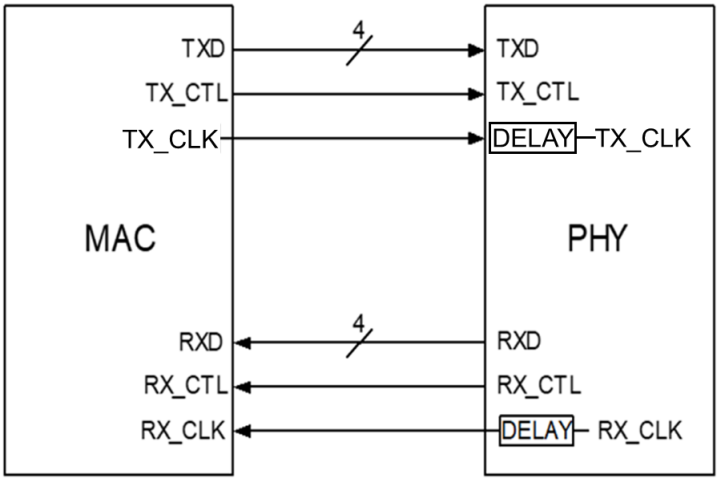
FIGURE 8-1: RGMII EXTERNAL DELAY COMPENSATION



8.2 Internal Delay Compensation

The VSC8501/VSC8502 supports RGMII V2.0 specifications. The RGMII interface needs to meet Ingress Internal Delay (RGMII-IID) and Egress Internal Delay (RGMII-EID) specifications. In most cases, setting the VSC8501/VSC8502 RGMII-ID is required based on other end RGMII-ID to meet the RGMII V2.0 specifications. RX_CLK delay is set using field 20E2.6:4, and TX_CLK delay is set using field 20E2.2:0.

FIGURE 8-2: RGMII INTERNAL DELAY COMPENSATION



9.0 SERIAL MANAGEMENT INTERFACE (SMI)

9.1 MDIO Management Interface

The MDIO management interface consists of a bidirectional data path (MDIO) and a clock reference (MDC). The maximum data rate of the MDIO interface is 2.5 Mbps.

TABLE 9-1: MDIO MANAGEMENT PINS

Name	Pin	Type	I/O Domain	Description
MDC	C11	I	LVTTL	Management data clock. A 0 MHz to 12.5 MHz reference input is used to clock serial MDIO data into and out of the PHY.
MDIO	R5	I/O	LVTTLOD	MDIO data receive and transmit
MDINT	A14	O, OD	VDDMIO	Management interrupt signal (VSC8501)
MDINT_0 MDINT_1	A14 C10	O, OD	VDDMIO	Management interrupt signals (VSC8502)

Note 1: A pull-up resistor (~2 kΩ, to the VDDMDIO domain) is required on MDIO. Depending on the master device, a pull-up may also be needed on MDC.

2: Management Interrupt signals are open-drain (OD) and require an external pull-up resistor. If unused, it may be left unconnected, without a resistor.

9.2 SMI Interrupt

- For the VSC8501, the SMI includes an interrupt signal, MDINT, for signaling the station manager when certain events occur on the device.
- For the VSC8502, the SMI includes two output interrupt signals, MDINT_0 and MDINT_1, for signaling the station manager when certain events occur on the device.

10.0 MISCELLANEOUS

10.1 PHY Configuration Pins

The following table lists the PHY configuration pins.

TABLE 10-1: PHY CONFIGURATION PINS

Name	Pin	Type	I/O Domain	Description
CLK_SQUELCH_IN	A2	I, PD	VDDIO	Input control to squelch recovered clock
COMA_MODE	B22	I/O, PU	VDDIO	When this pin is asserted high, all PHYs are held in a powered down state. When deasserted low, all PHYs are powered up and resume normal operation. This signal is also used to synchronize the operation of multiple chips on the same PCB to provide visual synchronization for LEDs driven by separate chips. (Note 1)
FASTLINK_FAIL	A4	O	VDDIO	Fast link failure indication signal
NRESET	E14	I, PD	VDDIO	Device reset. Active low input that powers down the device and sets all register bits to their default state.
RCVRDCLK1/PHYADD1	A26	I/O, PD	VDDIO	Clock output, can be enabled or disabled. Output a clock based on the selected active media with programmable frequency. This pin is not active when NRESET is asserted. When disabled, the pin is held low. Also functions as device SMI address bit 1 that is latched when NRESET is deasserted. (Note 2)
RCVRDCLK2/PHYADD2	B23	I/O, PD	VDDIO	Clock output, can be enabled or disabled. Output a clock based on the selected active media with programmable frequency. This pin is not active when NRESET is asserted. When disabled, the pin is held low. Also functions as device SMI address bit 2 that is latched when NRESET is deasserted. (Note 2)
PHYADD3	D23	I, PD	VDDIO	Device SMI address bits 3 (Note 2)
PHYADD4	C17	I, PD	VDDIO	Device SMI address bits 4 (Note 2)
REFCLK	B3	I	VDDIO	Reference clock
REFCLK_SEL	E4	I, PU	VDDIO	Reference clock frequency select signal

Note 1: For more information, see Section 3.15.1 “Initialization” of the data sheet. For information about a typical bring-up example, see Section 3.15 “Configuration” of the data sheet.

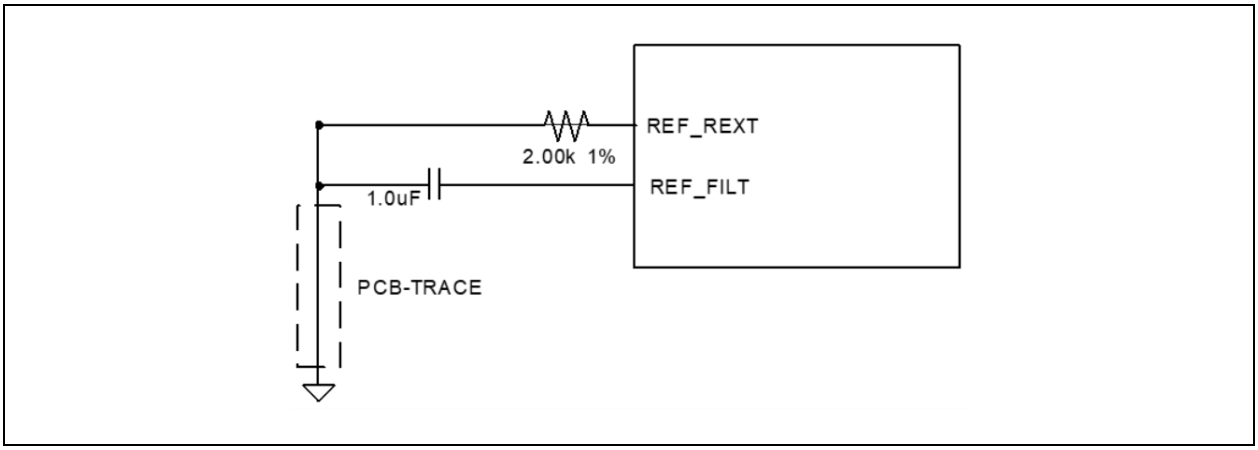
2: When pulled high to 3.3V VDDIO, the pull-up must be composed of a 2.4 kΩ from VDDIO to PHYADD, and 10 kΩ from PHYADD to VSS.

10.2 REF_FILT/REF_REXT Pins

- For proper operation, the VSC8501/VSC8502 must generate an on-chip band gap reference voltage at the **REF_FILT** pin. For this, the following components are required for each VSC8501/VSC8502 in the system:
  - 2.0 kΩ resistor, 1% tolerance, minimum 1/16 watt
  - 1 µF capacitor, 10% tolerance, NPO, X7R, or X5R ceramic materials are all acceptable
- For best performance, special considerations for the ground connection of the voltage reference circuit are necessary to prevent bus drops that would cause inaccuracy of the reference voltage. The ground rather than being connected individually to a common ground plane. This PCB signal trace should then be connected to a ground plane at a single point. In addition, the reference capacitor and resistor should be placed as close as possible to

the VSC8501/VSC8502. See Figure 10-1.

FIGURE 10-1: VOLTAGE REFERENCE SCHEMATIC



10.3 LED Support

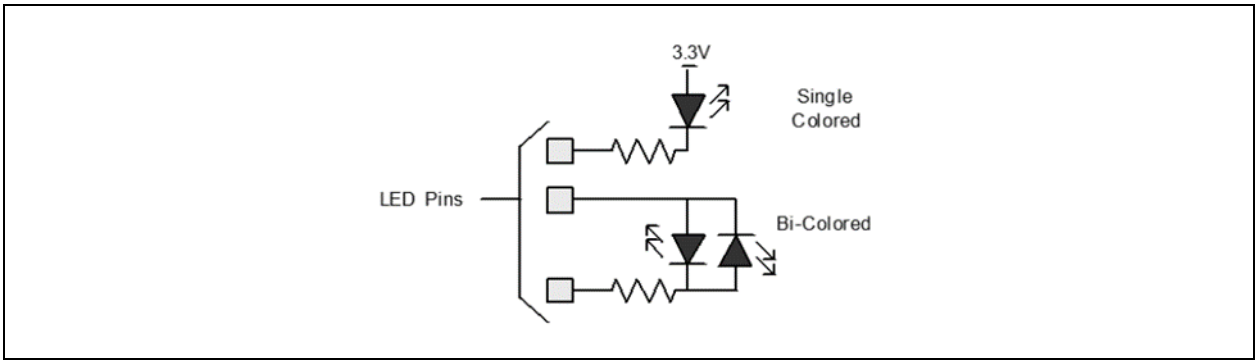
- The LED interface supports the following configuration: direct drive, basic serial LED mode and enhanced serial LED mode. Each LED pin can be configured to display different status information that can be selected by setting the LED mode in register 29. In addition to the LED modes in register 29, there are also additional LED modes that are enabled on the **LED0** pin whenever the corresponding register 19E1, bits 15 to 12 are set to 1. (See the corresponding VSC8501/VSC8502 data sheet for information on specific LED settings).

TABLE 10-2: LED PINS

Name	Pin	Type	Description
LED[0:3]_PHY0	E13, B21, A25, B20	O	LED direct-drive outputs, VSC8501 and VSC8502. A serial LED stream can also be implemented.
LED[0:3]_PHY1	E6, C2, A5, B5	O	LED direct-drive outputs, VSC8502 only. A serial LED stream can also be implemented.

- Each VSC8501/VSC8502 PHY port can support up to four single-colored LEDs and two bicolored LEDs. Each LED pin sinks current when an indication is present and deasserts when inactive. By design, each LED pin can also drive current when not active. This is very useful in the case for bicolored LEDs. Each LED pin in the VSC8501/VSC8502 can be designated to indicate any of the possible LED status signals thereby further simplifying the overall design.

FIGURE 10-2: LED CONFIGURATION



10.4 Reset

- The VSC8501/VSC8502 must be reset at power-up.

TABLE 10-3: RESET PIN

Pin Name	Pin	Type	I/O Domain	Description
NRESET	E14	I, PD	VDDIO	Device reset. Active low input that powers down the device and sets all register bits to their default state.

- Once all input power supplies (1.0V, 2.5V and if applicable 3.3V) are stable, the JTAG reset can be deasserted 100 nanoseconds after REFCLK is stable. Hardware (**NRESET**) reset should not be deasserted until at least 100 nanoseconds after deasserting JTAG reset.

  Note: Since the values of the **REFCLK_SEL** pin is latched on the rising edge of the **NRESET** pin, it is required that the 2.5V power supply is stable before the rising edge of NRESET. The **NRESET** should never be tied directly to logic high on the PCB because the VSC8501/VSC8502 will behave unpredictably if done. If the design cannot control the **NRESET** pin, then a small RC circuit must be added to this signal to provide the necessary delay.

- The following events occur in the following order when the VSC8501/VSC8502 is brought out of reset (this is triggered by a low-to-high transition of the **NRESET** pin):

1. Values for the **REFCLK_SEL** pins are latched asynchronously immediately out of reset.
2. Approximately 100 milliseconds after deassert of NRESET, the analog reference voltages and current stabilize. This is seen on the **REF_REXT** and **REF_FILT** pins.
3. Once a stable analog reference is established, the internal PLL will require 110 microseconds to lock. The PLL provides the device with its internal clocks.
4. With a locked PLL, the analog-to-digital converter (ADC) blocks require 4.9 milliseconds to calibrate.
5. Once the ADC is calibrated, the device is in normal operation and its **MDC** and **MDIO** pins are operational.
6. Follow the configuration steps shown in Section 3.15 “Configuration” of the data sheet.

10.5 JTAG

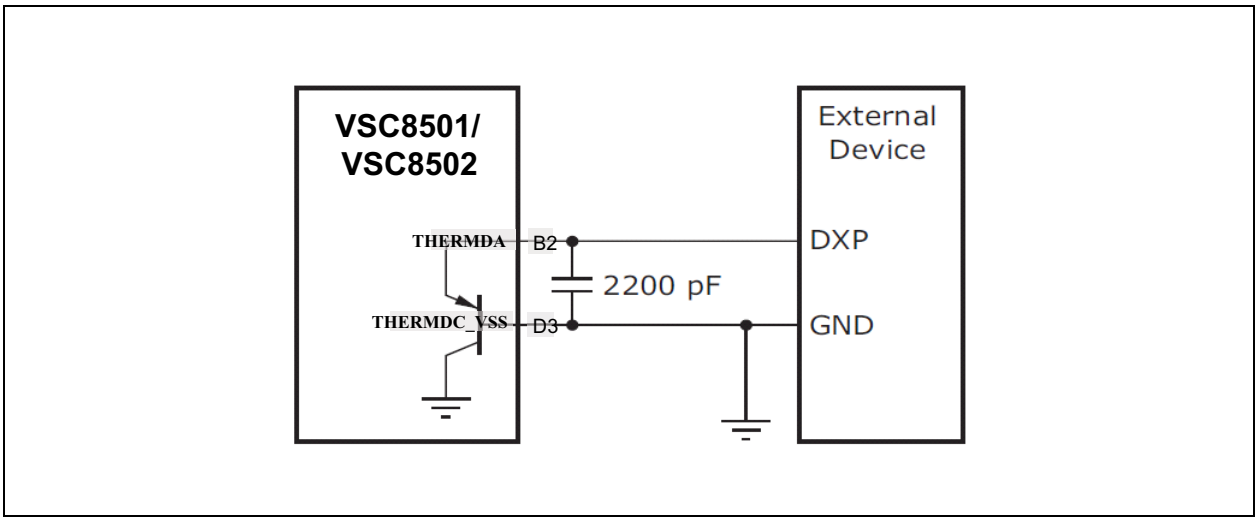
TABLE 10-4: JTAG PIN

Pin Name	Pin	Type	I/O Domain	Description
JTAG_CLK	B4	I, PU	VDDIO	JTAG clock
JTAG_DI	A3	I, PU	VDDIO	JTAG test serial data input
JTAG_DO	C1	O	VDDIO	JTAG test serial data output
JTAG_TMS	E5	I, PU	VDDIO	JTAG test mode select
JTAG_TRST	D4	I, PU	VDDIO	JTAG reset **Note:** When JTAG is not in use, this pin must be tied to ground with a pull-down resistor.

10.6 Thermal Diode

Note: The VSC8501/VSC8502 family does not support operation of the thermal diode under reverse bias.

FIGURE 10-3: THERMAL DIODE



10.7 No Connect Pins

TABLE 10-5: NO CONNECT PIN

Pin Name	Pin	Type	Description
NC_[1:4]	A1, A8, A20, A27	NC	No Connect

11.0 HARDWARE CHECKLIST SUMMARY

TABLE 11-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents are on hand.		
	Section 2.2, "Design Considerations"	Data sheet design considerations are understood.		
	Section 2.3, "Pin Check"	Design pins match the data sheet.		
	Section 2.4, "Ground Considerations"	All ground pins connect to a single ground. Solid ground planes should be used.		
Section 3.0, "Power"	Section 3.1, "Power Supply and Ground Pins"	Design is compliant with Table 3-1.		
	Section 3.2, "Defeatured Internal Regulator Pins"	Design is compliant with Table 3-2.		
	Section 3.3, "Power Supply Planes"	When creating a PCB layout, refer to this section for power supply planes design.		
	Section 3.4, "Power Circuit Connection and Analog Power Plane Filtering"	Make sure that the analog planes are filtered with ferrite beads, while digital planes are not. Examine possible resistive voltage drop in distribution.		
	Section 3.5, "Decoupling Capacitors"	Ensure that there is one decoupling capacitor near each power pin and at least a 1 µF bulk capacitor per rail. See Figure 3-1.		
	Section 3.6, "Current Requirements"	Ensure that the power rails can supply adequate current as specified in the data sheet.		
Section 4.0, "Thermal Considerations"	Section 4.0, "Thermal Considerations"	Use dedicated thermal vias. Do not use ground vias for thermal relief.		
Section 5.0, "Media Interface"	Section 5.1, "PHY → Magnetics"	Verify all PHY to Magnetics analog signals as shown in Figure 5-1.		
	Section 5.2, "Magnetics → RJ-45"	Verify all Magnetics to RJ45 analog signals as shown in Figure 5-1.		
	Section 5.3, "Layout Considerations"	Verify trace impedance for each signal.		
	Section 5.4, "Other Considerations"	Add SMD ferrite bead footprint to connect chassis ground to system ground.		
Section 6.0, "Clock Circuit"	Section 6.1, "Clock Inputs"	Verify **REF_SEL** configuration pin setup matches clock signal frequency.		
	Section 6.2, "Clock Power Supply Filtering"	Implement RC filter to avoid power supply switching noise coupling in to PHY.		
Section 7.0, "MAC Interface"	Section 7.1, "Design Details"	Follow design recommendation for impedance and trace length.		
	Section 7.2, "RGMII MAC Interface"	Verify pin-to-pin connections and input/output connections follow Figure 7-1.		
	Section 7.3, "GMII/MII Interface"	Verify pin-to-pin connections and input/output connections follow Figure 7-2.		
Section 8.0, "RGMII Interface Clock Considerations"	Section 8.0, "RGMII Interface Clock Considerations"	Verify RGMII timing between clock and data using external “trombone” traces or using MAC and PHY built-in delays.		
Section 9.0, "Serial Management Interface (SMI)"	Section 9.0, "Serial Management Interface (SMI)"	Follow Table 9-1. Verify MDINT signals are correctly routed to host device.		

TABLE 11-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 10.0, "Miscellaneous"	Section 10.1, "PHY Configuration Pins"	Verify that pin configuration (pull-up/pull-down) provides the correct POR setup when NRESET is brought high.		
	Section 10.2, "REF_FILT/REF_REXT Pins"	Follow the recommended design presented in this section.		
	Section 10.3, "LED Support"	Follow the recommended design presented in this section.		
	Section 10.4, "Reset"	Verify the timing specified in this section. Follow the configuration setup outlined in Section 3.15 of the data sheet.		
	Section 10.5, "JTAG"	JTAG_TRST should be tied to ground with pull-down resistor when not in use.		
	Section 10.6, "Thermal Diode"	Follow the schematic shown in Figure 10-3.		
	Section 10.7, "No Connect Pins"	Refer to this section for “No Connect” pins.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00005018A (05-25-23)	Initial release	

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