



SCH322x Serial Ports IRQ Sharing Issue in Windows with Installing ACPI 5.0

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INTRODUCTION

This document provides BIOS engineers a quick reference to port System BIOS in support of the SCH322x Serial ports IRQ Sharing issue in Windows 8.1 and Windows10 with installing the ACPI 5.0.

References

The following documents should be referenced when using this white paper. See your Microchip representative for availability.

- SCH322x Product Brief
- SCH3223 Data Sheet Rev. A (11-12-15)
- AN1975 - SCH3227/SCH3226/SCH3224/SCH3222 System BIOS Porting Guide, Rev. A (06-25-15)
- AN1976 - SCH3223 System BIOS Porting Guide, Rev. A (07-07-15)
- ACPI Specification, Rev. 5.0a, (11-13-13)

ISSUE DESCRIPTION

Serial ports IRQ Sharing are inactive on Windows 8.1/Windows 10 with installing the ACPI revision 5.0 in FACP table. Using the same system BIOS to support for serial ports IRQ Sharing are active on Windows 7 or on Windows 8.

DEVICE

SCH322x

PLATFORM

Intel Shark Bay-M (Grays Reef) platform or Intel next generation Desktop or Mobile platform.

SYSTEM BIOS

UEFI BIOS and must install the ACPI Revision 5.0 in the FACP table.

DEVICE FUNCTION INITIALIZATION

- Initializing both Serial port1 and Serial port2 to share an IRQ 14.

Note 1: Refer to Section 5.1, “Runtime Register Block - Logical Device A Flow Chart and Description” in AN1975 - SCH3227/SCH3226/SCH3224/SCH3222 System BIOS Porting Guide, Rev. A (06-25-15) to initialize the SCH322x Runtime Registers for Serial port2.

2: SioDSRegisterWrite Macro (Logical Device Number, Offset register, Register value).

```
SioLDRRegisterWrite (0x4, 0x60, 0x03);// Set COM1 Base I/O Address = 03F8h.  
SioLDRRegisterWrite (0x4, 0x61, 0xF8);//  
SioLDRRegisterWrite (0x4, 0xF0, 0x80);// COM1 and COM2 shared IRQ  
SioLDRRegisterWrite (0x4, 0x70, 0x0E); // IRQ 14  
SioLDRRegisterWrite (0x4, 0x30, 0x01);// Active  
SioLDRRegisterWrite (0x5, 0x60, 0x02);// Set COM2 Base I/O Address = 02F8h.  
SioLDRRegisterWrite (0x5, 0x61, 0xF8);  
SioLDRRegisterWrite (0x5, 0xF0, 0x00); // COM2  
SioLDRRegisterWrite (0x5, 0x70, 0x0E); // IRQ 14  
SioLDRRegisterWrite (0x5, 0x30, 0x01);// Active
```

IN SYSTEM BIOS ASL CODES

To support for the SCH322x Serial ports IRQ sharing, the IRQ Descriptor must be set up to “Edge, Active Low, Shared” or “Level, Active Low, Shared” for both Serial ports then booting into the Windows 7/8/8.1, both Serial ports resource are no conflicts in the Windows\Device Manager.

If set up the IRQ Descriptor to “Edge, Active High, Shared” or “Level, Active High, Shared” for both Serial ports then booting into the Windows 7/8/8.1/10, both Serial ports resource are conflicts with yellow bangs in the Windows\Device Manager.

IRQ TYPE DEFAULT DEFINITIONS

In the ACPI Specification

The Interrupt Information is defined in the ACPI Spec. V.3.0 or V.5.0 below, The ACPI Spec. defined the IRQ type default setting is supported for “edge, active high, non-shared” for UART IRQ Information in Note below.

Offset	Field Name
Byte 3	<p>IRQ Information. Each bit, when set, indicates this device is capable of driving a certain type of interrupt. (Optional—if not included then assume edge sensitive, high true interrupts.) These bits can be used both for reporting and setting IRQ resources.</p> <p>Note: This descriptor is meant for describing interrupts that are connected to PIC-compatible interrupt controllers, which can only be programmed for Active-High-Edge-Triggered or Active-Low-Level-Triggered interrupts. Any other combination is invalid. The Extended Interrupt Descriptor can be used to describe other combinations.</p> <p>Bit[7:6] <i>Reserved</i> (must be 0)</p> <p>Bit[5] Wake Capability, _WKC 0x0 = Not Wake Capable: This interrupt is not capable of waking the system. 0x1 = Wake Capable: This interrupt is capable of waking the system from a low-power idle state or a system sleep state.</p> <p>Bit[4] Interrupt Sharing, _SHR 0x0 = Exclusive: This interrupt is not shared with other devices. 0x1 = Shared: This interrupt is shared with other devices.</p> <p>Bit[3] Interrupt Polarity, _LL 0 Active-High – This interrupt is sampled when the signal is high, or true 1 Active-Low – This interrupt is sampled when the signal is low, or false.</p> <p>Bit[2:1] <i>Ignored</i></p> <p>Bit[0] Interrupt Mode, _HE 0 Level-Triggered – Interrupt is triggered in response to signal in a low state. 1 Edge-Triggered – Interrupt is triggered in response to a change in signal state from low to high.</p>

Note: *Low true, level sensitive interrupts may be electrically shared, but the process of how this might work is beyond the scope of this specification.*

Note: *If byte 3 is not included, High true, edge sensitive, non-shareable is assumed.*

In the SCH3223 Data Sheet

The SCH3223 UART IRQ default to “edge high” (ISA compatible), as follows:

Table 22-6: LOGICAL DEVICE REGISTERS

Logical Device Register	Address	Description
Interrupt Select Defaults: 0x70 = 0x00 or 0x06 on VCC POR, VTR POR, PCI RESET and SOFT RESET 0x72 = 0x00, on VCC POR, VTR POR, PCI RESET and SOFT RESET	(0x70, 0x72)	Only register 0x70 is implemented for each logical device. Refer to Interrupt Configuration Register description. Unused register (0x72) will ignore writes and return zero when read. Interrupts default to edge high (ISA compatible).

WORKAROUND FOR THIS ISSUE

SCH322x does not have the registers to initialize the interrupt polarity. We provide two suggestions to do the system BIOS workaround for this issue, as follows:

Note: BIOS engineers may select Suggestion 1 or Suggestion 2 to fix this issue, both suggestions cannot be used together.

Suggestion 1:

Install ACPI Revision 4.0 in the FACP table to support the Serial ports IRQ sharing issue.

Suggestion 2:

Modify the Serial port ASL codes to fix this issue, such as: both COM1 and COM2 devices share an interrupt - IRQ14. Below are the details.

In _STA method:

Report the Serial port device is present and enabled to OS. To fix a bug that cold booting into the Windows and uninstalling the Serial port device in Device Manager and rebooting into the Windows, the system will reboot twice.

```
Method(_STA)
{
    Return(0x0F)
}
```

In _CRS method:

To set the ACPI IRQ information Byte 3 to 0x19, refer to Table 6-163, "IRQ Descriptor Definition" of the ACPI Specification, Rev. 5.0a, as follows:

Bit[4]: Interrupt Sharing, _SHR = 1 // Shared

Bit[3]: Interrupt Polarity, _LL = 1 // Active-Low

Bit[0]: Interrupt Mode, _HE = 1 // Edge-Triggered

The IRQ information of _CRS is set to *IRQ(Edge, ActiveLow, Shared) {0x0E}*.

In _PRS method:

To set the IRQ information to *IRQ(Edge, ActiveHigh, Shared) {0x0E}*.

Note: There is a limitation for Suggestion 2 that it's only supported one Serial port resource in _PRS, such as:

```
Name(_PRS, ResourceTemplate() {
    StartDependentFn(0, 0) {
        IO(Decode16, 0x3F8, 0x3F8, 0x08, 0x08)
        IRQ(Edge, ActiveHigh, Shared) {0x0E}
    }
    EndDependentFn()
}
```

For the Windows behavior, we cannot support user to dynamically update the Serial ports resources in the Windows\Device Manager, otherwise, the workaround will fail.

APPENDIX A: WHITE PAPER REVISION HISTORY

TABLE A-1:

Revision	Section/Figure/Entry	Correction
DS00002131A (03-23-16)		Document Release

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