# AN1785

# ESD and EOS Causes, Differences and Prevention

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## INTRODUCTION

In many microcontroller-based applications, the microcontroller is subjected to various types of electromagnetic noise. Electrical noises may cause undesirable behavior on the application. Two of these types of noise events are referred to as Electrostatic Discharge (ESD) and Electrical Overstress (EOS). This application note discusses these two types of events, what causes them and how to minimize the impact of them on the application.

## WHAT IS ESD?

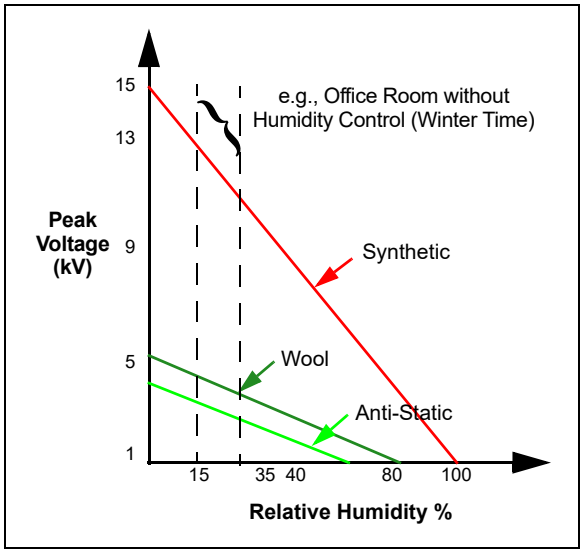
The Electrostatic Discharge (ESD) is the most common phenomena of Electromagnetic Compatability (EMC). The word *electrostatic* indicates static electricity accumulated by specific materials that come into contact with one another, such as rubbing your feet on a wool carpet. The electric spark that is sometimes experienced when touching metal, or a car, is the phenomenon of Electrostatic Discharge. The amount of electric discharge depends upon the material and environment, including humidity.

ESD not only happens when a human comes in contact with a statically-charged material. Machines and furniture, such as lab tables, can also accumulate static electricity, and discharge when electrical components come in contact with them.

Specification IEC 61000-4-6 defines the static electricity accumulated by humans and machines. The models are called the “Human Body Model (HBM)” and “Machine Model (MM)”.

Figure 1 below shows the ESD voltages as defined by the IEC standards.

**FIGURE 1: ESD VOLTAGES**




As described in Figure 1, the accumulated static electricity depends on the relative humidity of the environment. When the humidity is lower, the accumulated static electricity is higher. Table 1 describes typical voltages with very common materials used in daily life with respect to the relative humidity.

**TABLE 1: COMMON STATIC VOLTAGES**

| Static Voltages as a Function of Relative Humidity (RH) | 20% RH (kV) | 80% RH (kV) |
|---|---|---|
| Walking across a vinyl floor | 12 | 0.25 |
| Walking across a synthetic carpet | 35 | 1.5 |
| Arising from a foam cushion | 18 | 1.5 |
| Picking up a polyethylene bag | 20 | 0.6 |
| Sliding a styrene box on a carpet | 18 | 1.5 |
| Removing mylar tape from a PC board | 12 | 1.5 |
| Shrinkable film on a PC board | 16 | 3.0 |
| Triggering a vacuum solder remover | 8 | 1.0 |
| Aerosol circuit freeze spray | 15 | 5.0 |

ESD testing is done at various levels in a product cycle, such as at the component level (for example, Microchip's MCU), at the board level (such as control board) and at the end equipment level (such as a washing machine). Microchip publishes the "*Corporate Quality Handbook*" (DS00169) that explains its corporate component-level testing methodology. The handbook is available from the Microchip web site at https://www.microchip.com/quality.

After the chip is assembled on a PCB, a system designer will test the application for ESD sensitivity at the PCB level. Typically, at this level, the connectors and the cables have a conducted discharge applied to them.

An end equipment manufacturer, such as an appliance manufacturer, will test the end equipment for ESD sensitivity based on the first point of contact. The first point of contact is defined as the point of contact for the end user or assembly equipment. For example, on a refrigerator, the point of contact is the door handle or dispenser keys; on a washing machine, it could be the keys of a display or control knobs. An example of an ESD immunity testing specification for PCBs and end products can be found in the international standard, IEC-61000-4-2.

In general, to minimize the effects of ESD on PCBs and end products, the design should shunt the ESD energy to ground in the most effective way possible.

## WHAT IS EOS?

In a semiconductor environment, Electrical Overstress (EOS) is a term used to describe the phenomenon that may occur when an electronic device is subjected to a current or voltage that is beyond the specification limits of the device. The Electrical Overstress may result in thermal damage to the entire device or a portion of the device. The thermal damage is the result of the excessive heat generated during the EOS event. When a device is subjected to high voltage or current, resistive heating in the connections within the device generates excessive temperatures. Typically, the excessive heat is localized around the area where the electrical stress is exerted. This results in damage to the device, and most of the time, this damage is visible to the naked eye.

EOS can be the result of a single non-recurring event or the result of ongoing periodic, or non-periodic events. An EOS event can be a momentary event, lasting only milliseconds, or can last as long as the conditions persist. After the EOS energy is dissipated, the device may be permanently damaged and may become non-functional or partially functional.

### Possible Causes of EOS

The following is a list of issues that can cause EOS:

1. Power supply voltage surge beyond the absolute maximum voltage range.
2. Switching circuits on the board may cause high-voltage spikes internal to the board, propagated to other devices on the board.
3. External connections, such as capacitive charge on an external cable, antenna pick-up of external switching noise and inductive loads can create voltage spikes.
4. Excessive noise on the ground plane caused by poor grounding.
5. I/O switching creating voltage overshoots or undershoots.
6. Electromagnetic Interference (EMI) due to poor shielding in an electrically noisy environment.
7. Improper power-up sequences can apply unintended voltage levels or polarities to the device.
8. ESD events that cause damage, or weaken the device, making it more susceptible to future EOS events.
9. Latch-up events may result in EOS damage if the current is high or if it persists for an extended period of time.

## ESD VERSUS EOS

The primary difference between ESD and EOS events is their time duration. ESD events are generally between 500V and 8000V, and last for less than 300 ns. During an ESD event, the peak current can reach many amps of current, but because the event is so short, a well designed ESD protection circuit can shunt this energy to ground which causes no damage. While voltage and current levels can be similar, an EOS event has a much longer duration, typically from 1 ms to many minutes.

Electrical failure in an application may show one or more of the following symptoms:

1. Excess supply current
2. Low resistance between the supply voltage and ground
3. Shorted input or output pins to either the supply voltage, or ground
4. Open connections to one or multiple pins – I/O, supply voltage or ground
5. Functional failure due to internal damage to the device
6. Unexpected device Resets
7. Device latch-up

The difference between the observed symptoms of EOS and ESD are often not clear, and in some cases, a wrong diagnosis can lead to an ineffective solution. The following section contains some guidelines that may help identify an EOS failure versus an ESD failure, along with photos and diagrams that illustrate the typical damage seen for each type of failure.

The goal of the **"Characteristics of an ESD Failure"** section is to help in understanding the differences, so proper feedback can be provided to achieve timely solutions to the failures.

## CHARACTERISTICS OF AN ESD FAILURE

| | |
|---|---|
| **Note:** | The following pictures are taken from actual failure analysis reports to illustrate various examples of ESD and EOS failures. |

An ESD failure is identified by the following damage conditions:

- Small focused area of failures
- Typically focused around an I/O pad and associated circuitry
- Characterized by melt filaments between junctions of transistors, causing a short
- Can be very small and difficult to find
- Only a single device is damaged
- Only one type of damage mode

**FIGURE 2: DAMAGE TO ESD CLAMP BETWEEN I/O AND Vss – I/O PIN UNDER MAGNIFICATION**

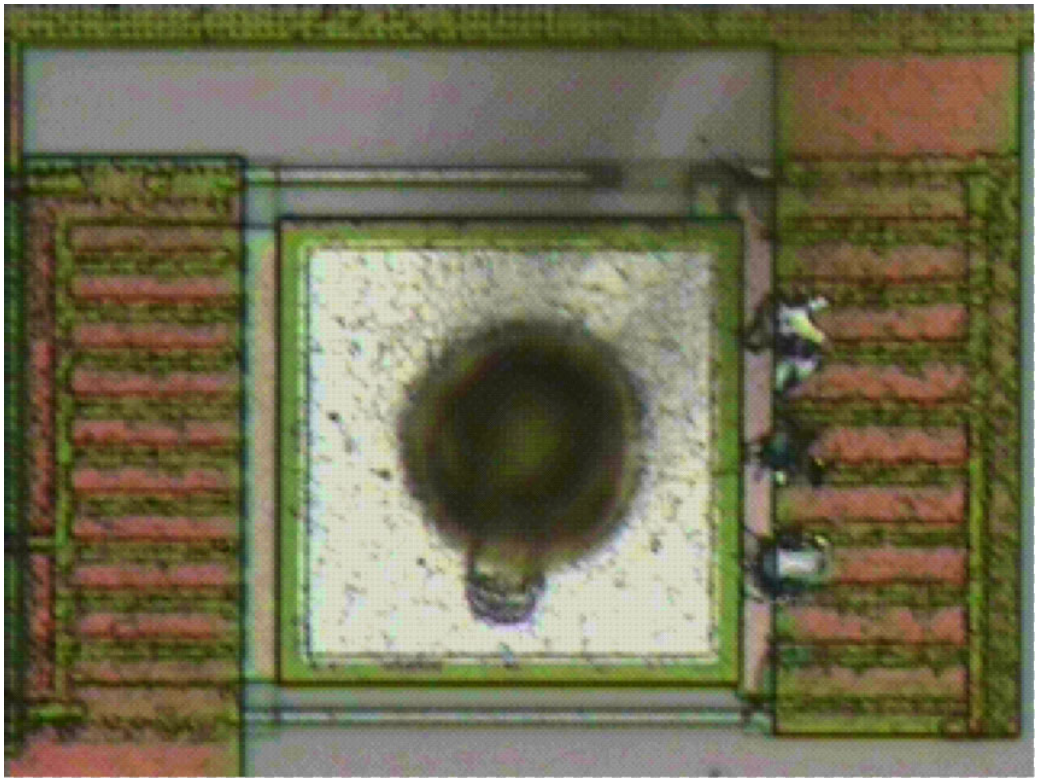


Figure 3 shows ESD damage to gate oxide, indicative of a charged device ESD failure, an input without any protection or where there is no secondary protection.

**FIGURE 3: ESD DAMAGE TO GATE OXIDE – IMAGE OF A DEPROCESSED CHIP LAYER**

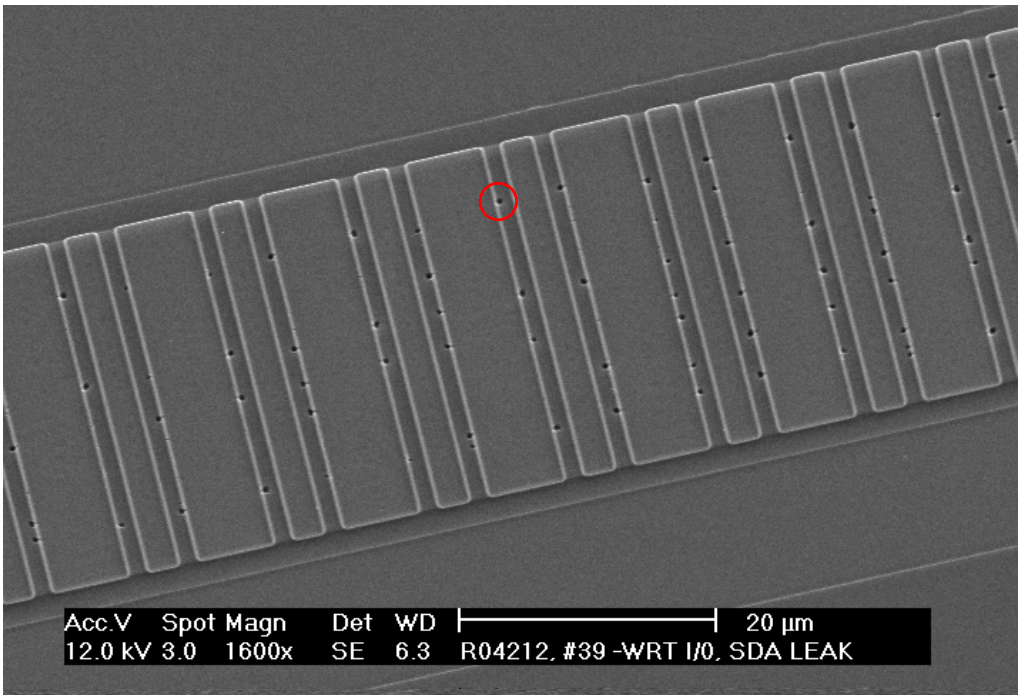


**FIGURE 4: ESD DAMAGE TO METAL INTERCONNECTS**

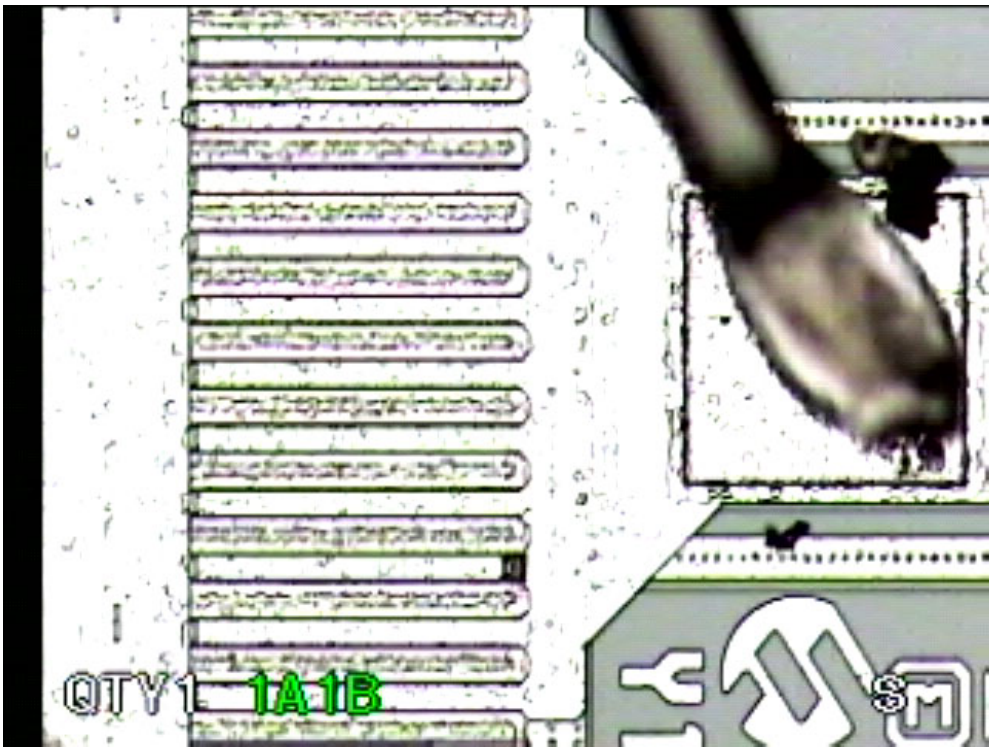



**FIGURE 5: ESD DAMAGE TO SILICON JUNCTION**

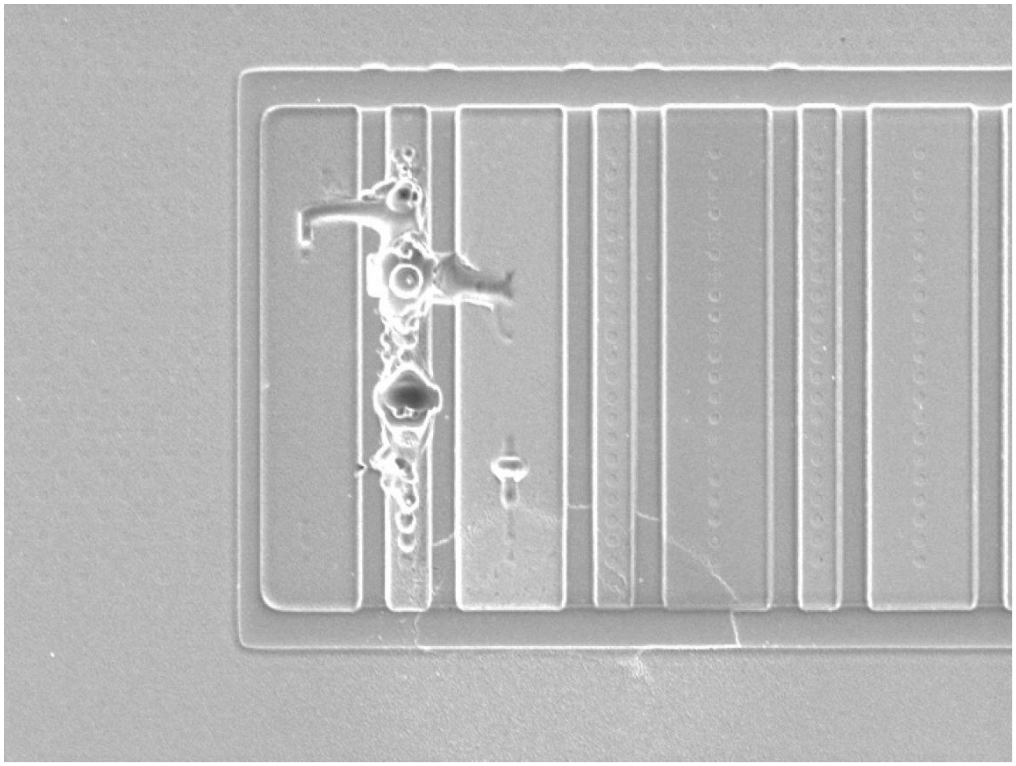
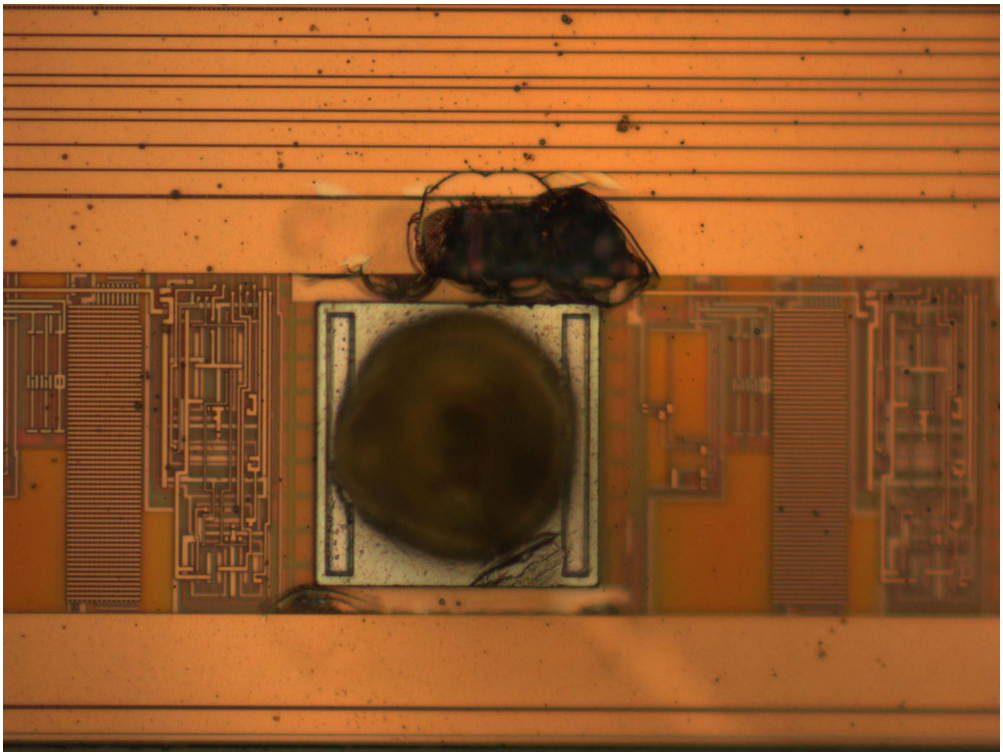


Figure 6 shows ESD damage that is so severe it almost resembles EOS. This could be a condition where an EOS event further damaged the circuit which was already weakened by ESD.

**FIGURE 6: SEVERE ESD DAMAGE**



## CHARACTERISTICS OF AN EOS FAILURE

An EOS failure is identified by the following damage conditions:

- Large areas of damage are seen
- Characterized by a large amount of melted metal
- Can be localized to an I/O pad or internal to the die in the case of an EOS event on a supply pin
- Damage can encompass many devices
- Can have many different simultaneous damage types

Other causes of EOS are:

- Output currents which exceed device maximums (short circuits or low-impedance loads)
- I/O pins which spike above $V_{DD}$ or below $V_{SS}$
- $V_{DD}$ which exceeds the $V_{DD}$ maximum specification

EOS is a long-term event and is usually caused by user or test errors (e.g., the part may have been put in the socket backwards). The most common cause of EOS is overvoltage on either the I/O pin or the supply pin.

### Visual Damage Due to EOS

When failure analysis is done on a device, typically, EOS damage can be seen as visual damage on the device using only an optical microscope. This damage is the result of the high temperature experienced during the EOS event.

External damage to the package may also be seen as a result of EOS stress and is characterized by:

1. Cracked package
2. Visible bulge in mold compound
3. Physical hole in mold compound
4. Burnt/discolored mold compound

The sample may be damaged more than listed above, but a careful analysis, by removing the capsulating material from the part, may show the following internal damage due to excessive temperature:

1. Package/die delamination from excessive heat
2. Melted or burnt metal layers
3. Carbonized mold compound
4. Discoloration to metal lines
5. Melted or vaporized bond wires

### Examples of EOS Failure

The following figures illustrate the different examples of EOS failure.

**FIGURE 7: MOLD COMPOUND CARBONIZATION DUE TO EOS EXCESSIVE HEAT**

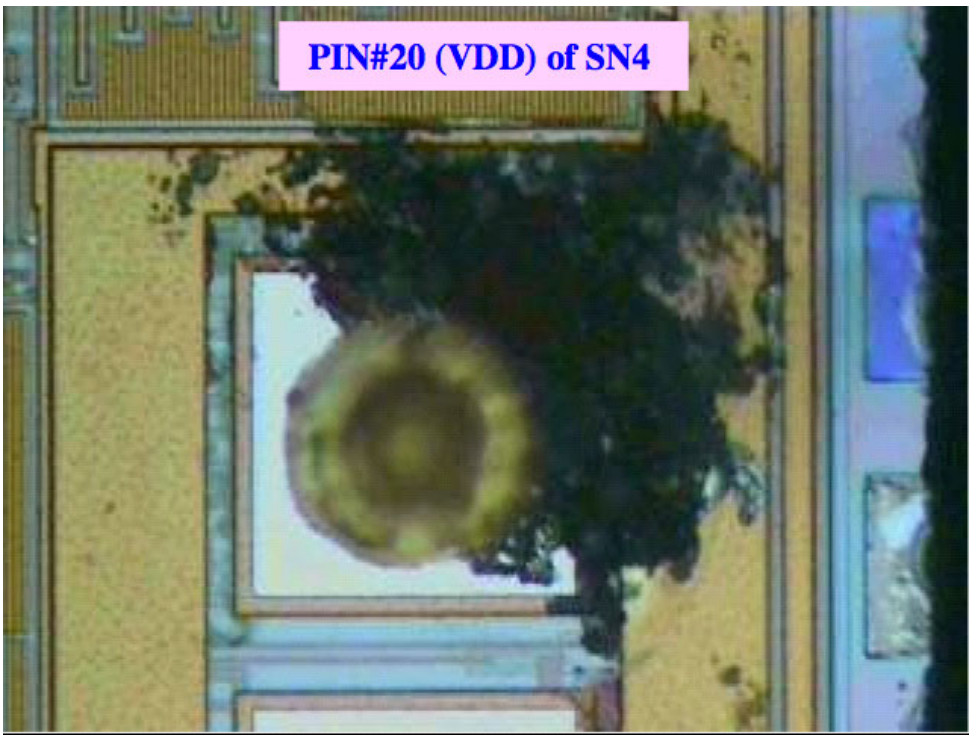


**FIGURE 8: METAL CONNECTING I/O PAD TO DEVICE MELTED OR VAPORIZED**

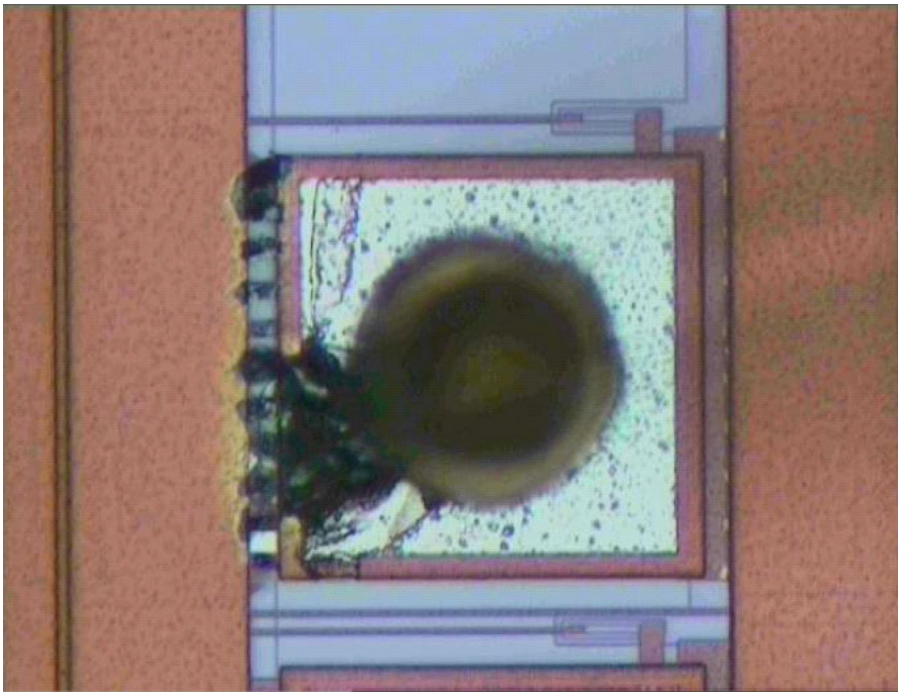


**FIGURE 9: INTERNAL METAL LINE MELTED DUE TO HIGH CURRENT ON SUPPLY PIN**

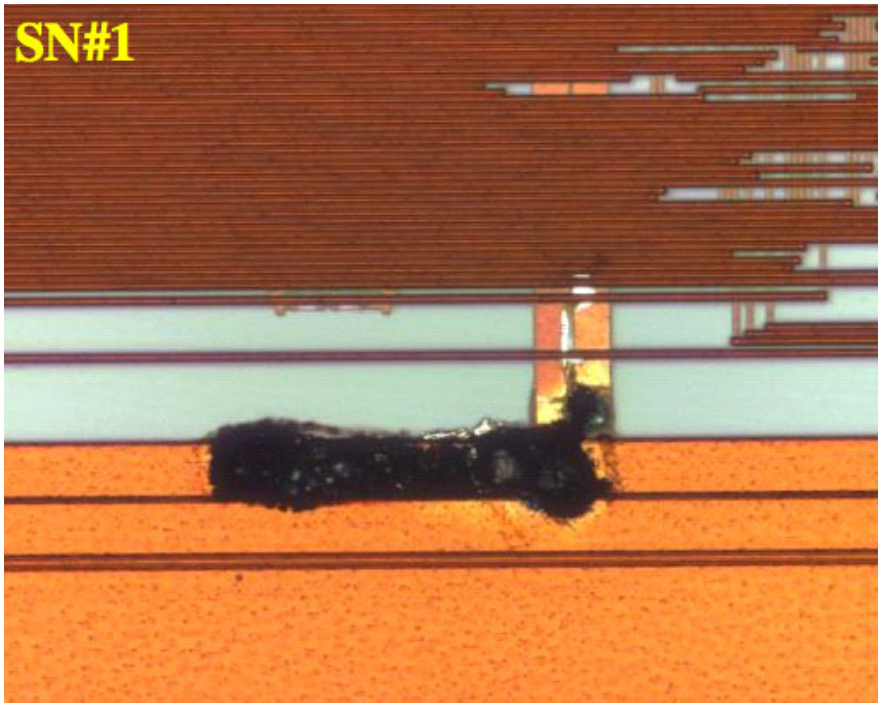


**FIGURE 10: MELTED AND DISCOLORED METAL IN COMBINATION WITH CARBONIZED MOLD COMPOUND**

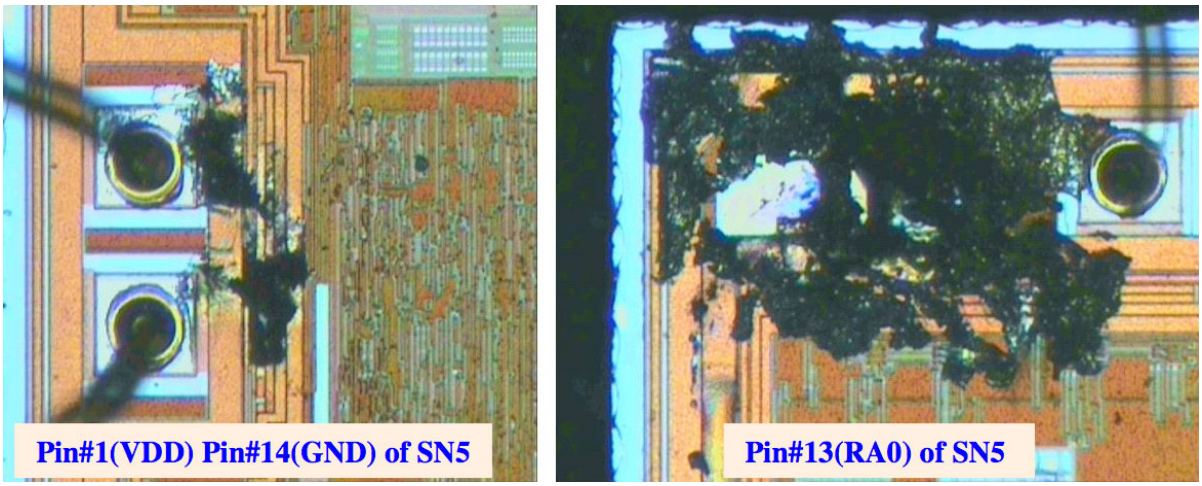



**FIGURE 11: CARBONIZED MOLD COMPOUND, MELTED AND DISCOLORED METAL**

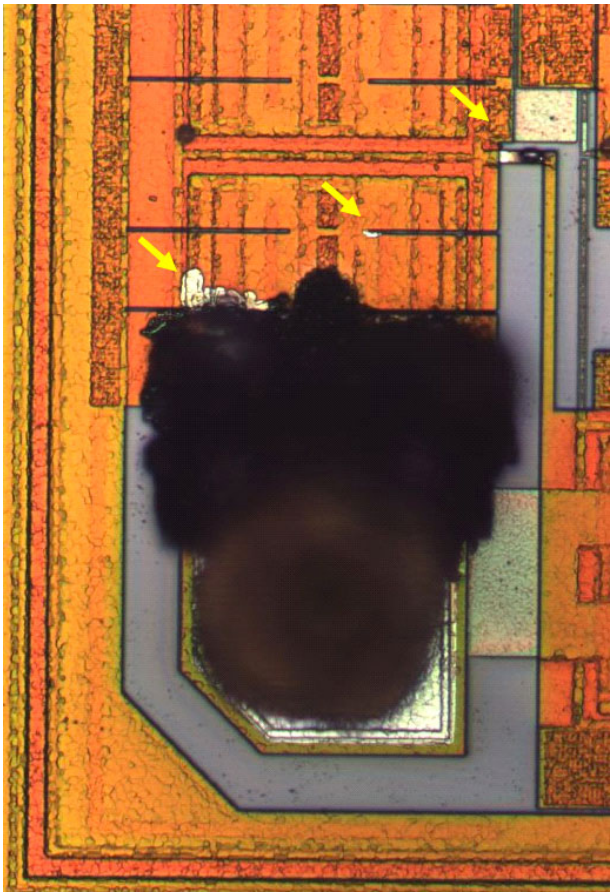


**FIGURE 12: EOS DAMAGE TO PACKAGING**

## ESD AND EOS TESTING

### Device Robustness Design

Microchip devices are designed with protection circuitry to avoid damage due to an ESD event during the handling and assembly process. As part of the quality process, all Microchip devices are tested against two JEDEC standards, as described below.

### Device Testing

All of the Microchip Technology devices are designed to withstand ESD testing according to the following standards:

#### COMMERCIAL AND INDUSTRIAL

- ANSI/ESDA/JEDEC JS-001 for Electrostatic Discharge Sensitivity Testing, Human Body Model (HBM) – Component Level
- ANSI/ESDA/JEDEC JS-002 for Electrostatic Discharge Sensitivity Testing, Charged Device Model (CDM) – Component Level
- JESD78, IC Latch-Up Test Aerospace and Military
- MIL-STD 883 Method 3015.9 “Military Standard for Test Methods and Procedures Microelectronics: ESD Sensitivity Classification”
- MIL-STD 883 Method 3023.2 *“Military Standard for Test Methods and Procedures Microelectronics: Static latch-up measurements for digital CMOS microelectronic devices”*

#### AEROSPACE AND MILITARY

- MIL-STD 883 Method 3015.9 “*Military Standard for Test Methods and Procedures Microelectronics: ESD Sensitivity Classification*”
- MIL-STD 883 Method 3023.2 “*Military Standard for Test Methods and Procedures Microelectronics: Static latch-up measurements for digital CMOS microelectronic devices*”

#### AUTOMOTIVE

- AEC - Q100-002 for Human Body Model Electrostatic Discharge Test
- AEC - Q100-011 for Charged Device Model (CDM)
- AEC – Q100-004 for IC Latch-up Test

#### ELECTROSTATIC DISCHARGE TEST

Minimum Guidelines or Otherwise stated
MM not required per industry and as stated in their final MM spec revision.

- 2000V – HBM Sample: 12 (3 per voltage level)
- 750V All pins – CDM Sample: 9 (3 per voltage level)
- ±105 mA and an overvoltage of 1.5*$V_{MAX}$ or MSV – LU Sample: 6 (3 per temperature (Ambient/Max Ambient).

#### MINIMUM GUIDELINES

2000V – HBM Sample: 12 (3 per voltage level)
500V – (corner pins: 750V) CDM Sample: 5

## Human Body Model (HBM)

The Human Body Model (HBM) is the most widely used and quoted model for ESD testing.

The HBM simulates a human body discharging accumulated static charge through a grounded device.

The graph in Figure 14 shows the characteristics of the HBM test waveform. The Human Body Model has a peak of 1.2 to 1.3A for a 2 kV test. The rise time is 2 to 10 ns, with the waveform decaying to 50% by 150 ns. The entire cycle is 500 ns.

**FIGURE 13: HUMAN BODY MODEL (HBM)**

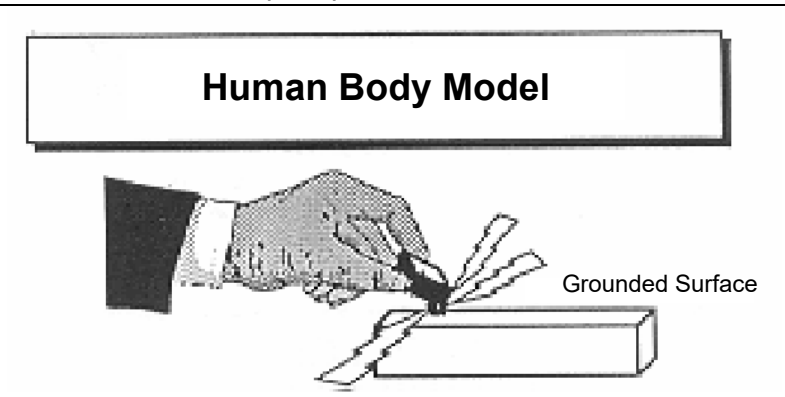
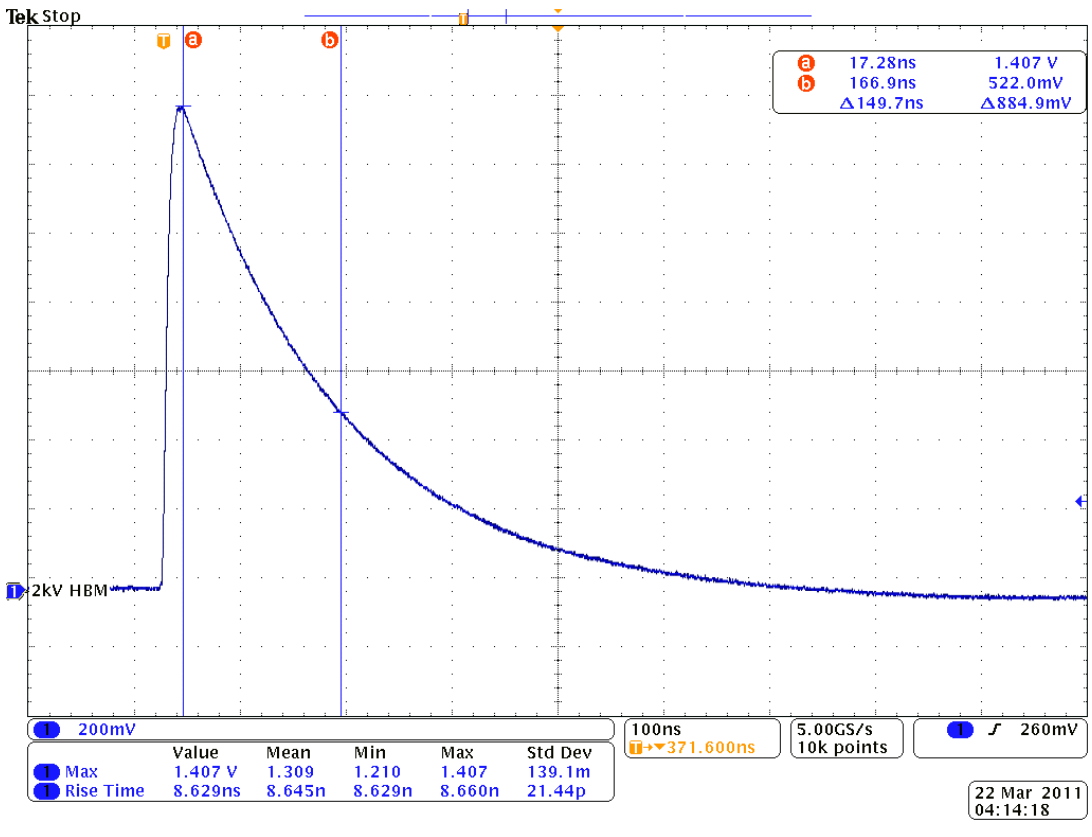



**FIGURE 14: HBM TEST WAVEFORM GRAPH CHARACTERISTICS**

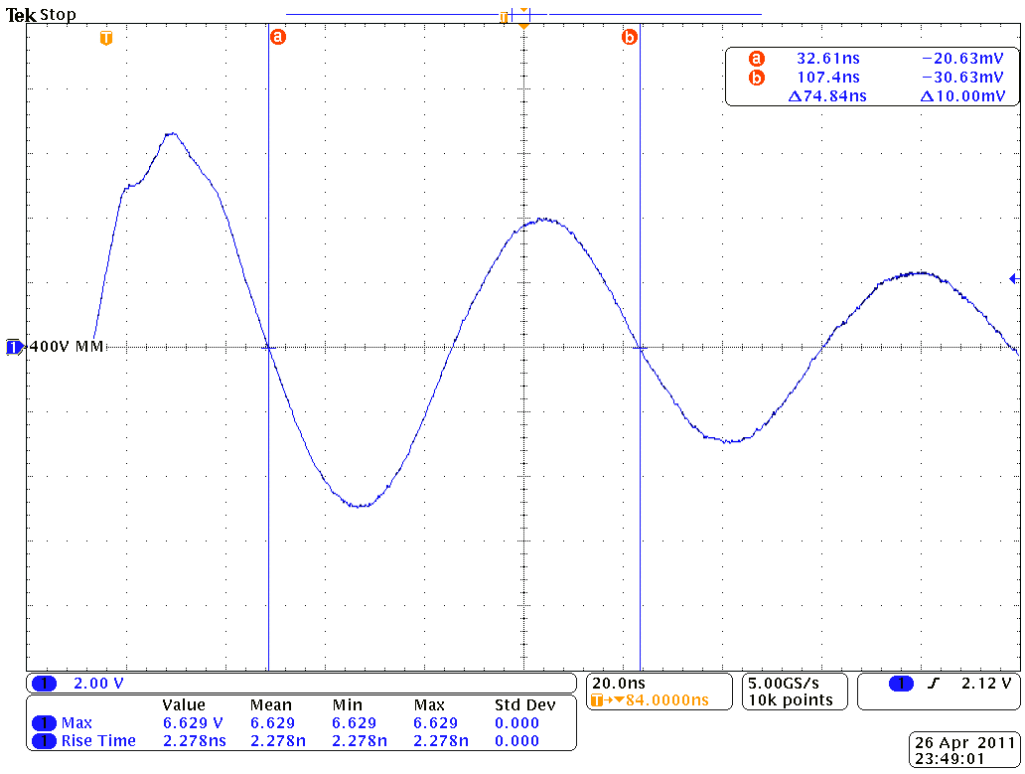


## Machine Model (MM)

The Machine Model (MM) simulates a metal to metal Electrostatic Discharge. This model was developed to simulate a person seated at a workbench and using tools.

The Machine Model uses 0 Ohms (see Figure 16) in the test setup, the discharge current exhibits LC tank behavior. Rise time is between 5 and 15 ns. The waveform duration, peak and rise time are dependent on the parasitic inductance and capacitance in the DUT.

**FIGURE 15: MACHINE MODEL TYPICAL CURRENT PULSE**

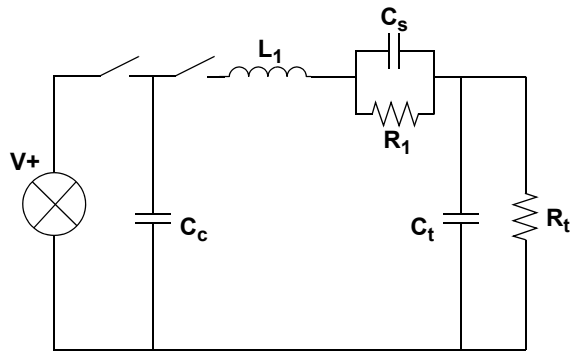



Both the Human Body and Machine Models are the same test with different values for the test setup. The basic test circuit setup is detailed below.

In the circuit, $R_1$ is the body resistance set to mimic the resistance of a human body or the tools being used to handle the device.

$C_c$ is the body capacitance set to mimic the total capacity of the human body. In a Machine Model, the capacitance is higher since the person is seated.

**FIGURE 16: BASIC TEST CIRCUIT SETUP**




$C_c$ = Capacitance of Human Body/Machine
HBM = 100 pF
MM = 200 pF

$L_1$ = Parasitic Line Inductance
$R_1$ = Source Resistance:
HBM = 1500Ω
MM = 0Ω

$C_s$ = Resistor Self-Capacitance
$C_t$ = DUT Parasitic Capacitance
$R_t$ = DUT Load in Clamp Mode

## Charged Device Model (CDM)

A device can accumulate charge while moving in contact with another object. This can be the case during production when in contact with the track or feeder. If the device then contacts another object at a lower potential, the charge discharges into the object. This ESD is known as the Charged Device Model (CDM). CDM typically causes damage to sensitive thin gate oxides.

A typical setup is shown in Figure 17 and depicts a contact discharge. Another setup is the spark gap discharge, which uses a discharge electrode to generate the ESD spark.

In the typical CDM current pulse, the rise time is typically <1 ns with a duration of only a few nanoseconds. The peak current is at 1000V and is about 9A.

The electrical model is shown in Figure 18. $C_1$, $L_1$ and $R_1$ are all parasitic components. $C_c$ is the device capacitance; this capacitance will vary from product to product, depending on the package used.

**FIGURE 17: TYPICAL CDM CURRENT PULSE**

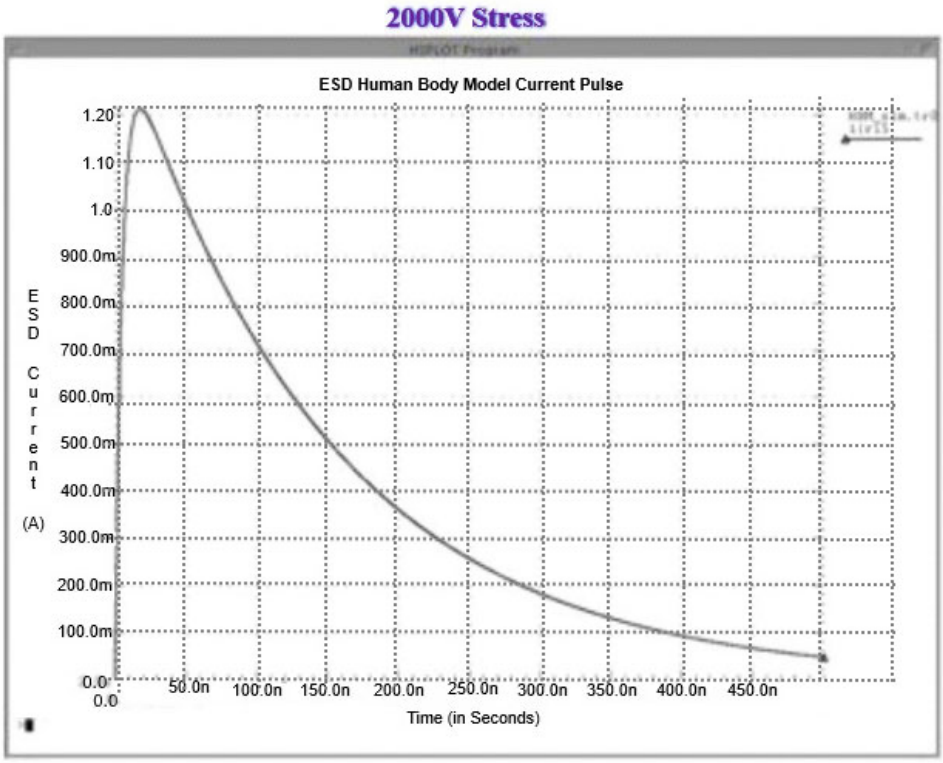



**FIGURE 18: ELECTRICAL MODEL**

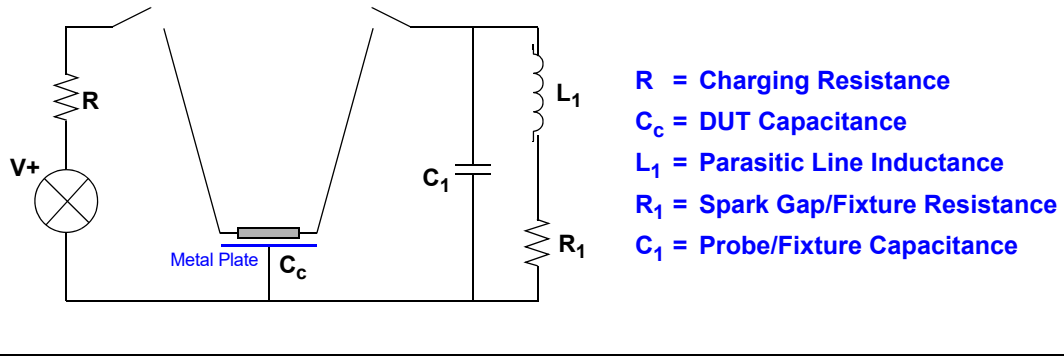


**TABLE 2: SUMMARY OF ESD MODELS**

| | HBM | MM | CDM |
|---|---|---|---|
| Stress Voltage Levels (V) | 250<br>500<br>1000<br>2000<br>4000<br>8000 (opt.) | 25 (E)<br>50 (E)<br>100 (J+E)<br>200 (J+E)<br>400 (J+E) | 100 (J) 125 (E)<br>200 (J) 250 (E)<br>500 (J+E) 750 (A)<br>1000 (J+E)<br>1500 (E)<br>2000 (J+E) |
| Charge Capacitance (pF) | 100 | 200 | DUT (Varies) |
| Series Resistance (Ohms) | 1500 | 0 | 0 |
| Number of Zaps | 1 | 1 | 3 |
| Number of Samples | 3 | 3 | 3 |
| Delay Between Zaps (S) | 0.1 | 0.5 | 0.2 |
| Rise Time (ns) | 2-10 | — | 0.2-0.25 |
| Pulse Width @ 36.8% Ip (ns) | 130-170 | — | — |
| Pulse Period @ Zero Cross (ns) | — | 63-91 | — |
| Pulse Width (ns) | — | — | 0.4-1.5 |

## ESD CONTROL MECHANISMS

Electrostatic Discharges can come from a variety of sources. The traditional ESD pulse is caused by a body at a very high potential coming into contact, or near contact, with a grounded object. This could be a human body, a piece of electrical equipment or even a piece of furniture.

In a dry environment, where static dissipation is low, a human body can develop tens of thousands of volts of potential. Incorrectly placed ionizers, meant to improve static dissipation, can build large potentials on office or laboratory furniture. Any person touching such a piece of furniture might feel a shock. Any devices being placed on a table with a large potential can suffer damage.

### Personnel Grounding Devices

The potential for ESD damage at assembly can be avoided by careful personnel grounding procedures. Ground straps for manual handling of devices is essential. Other procedures include grounded tables and work surfaces with anti-static surfaces, such as specifically designed plastic mats.

In addition, static dissipative garments can help drain any charge assembly personnel may accumulate.

Other preventative measures include:

- Static Dissipative Floors
- Floor Mats
- Ionizers
- ESD Footwear
- Glove and Finger Cots
- Awareness Symbols

A Faraday cage can be used to protect devices on the board. The devices can be microprobed in the Faraday cage room and then stored in the cage room.

An ESD gun can be unintentionally used to create failures. Check these into proper locations if applicable.

### ESD Packaging

Protective material packaging techniques are essential to prevent any ESD damage. Packaging can be in the form of bags, package filler, magazines, boxes, carriers, trays, etc. They all must protect from the following very distinct threats:

- Direct Discharge:
  - An ESD discharge directly to the bag or container
- Static Fields:
  - Static fields can induce destructive currents within the circuit or device
- Triboelectric Charging:
  - Contact between the bag or container and the device can produce damaging static voltage and fields

When selecting appropriate packaging, it is important to differentiate between static dissipative and anti-static materials as they each work differently.

An anti-static material has the ability to suppress charge generation or to prevent static buildup. The material will not safely attract or decay a static charge before discharging it randomly. Anti-static materials have an electrical resistance in the range of 1 to $1x10^{10}$ Ohms.

The most common example of an anti-static material is the “pink” poly bags. They will not charge up when coming into contact with other materials. The drawback is that they have no shielding ability; a static field can penetrate the bag and cause harm to the contents.

Anti-static materials are useful for packing items that have no static susceptibility or for support packing. The main use is in processing material that will be in close proximity to static-sensitive devices, so as to keep static generating materials away from sensitive contents.

Conductive materials have a lower resistance than “static dissipative” materials, in the range of 200 kOhms. They offer the lowest charge generation and quickest charge dissipation. An example of these materials is the “black” poly bags. With these bags, any charge will dissipate very fast, which also significantly reduces the potential for a “spark” or ESD event. Since the material is conductive, it provides some shielding of the contents, but still the charge may be transferred to the device.

Static dissipative materials can safely discharge any electrostatic buildup to ground. Static dissipative materials have an electrical resistance in the range of 1 to $1x10^{6}$ Ohms. Resistance in this range is desired to safely drain the ESD buildup without generating a large spike or discharge.

Static shielding bags and containers provide an excellent level of protection, since they provide both dissipative and anti-static protection to the contents. In addition, they include a metal shield and a dielectric to stop static from entering the bag.

### ESD in Test and Production Equipment

ESD failures can occur in any equipment that handles, tests, processes or comes in contact with unprotected devices if the device picks up a charge by:

- Contacting an insulator
- Contacting an ungrounded conductor
- Coming in close proximity to a charged surface

then discharges when it subsequently touches a grounded metal surface, such as an electrical test head.

Most equipment manufacturers are not yet designing their equipment to be CDM resistant. There are no industry equipment design rules being followed to minimize CDM problems; therefore, it is up to the user to verify that CDM problems are not present in any equipment being used in the production line.

### How to Make Equipment ESD Resistant

The following guidelines will help minimize the probability of ESD issues in the production line:

- Equipment should be checked for any insulator materials which come in close contact with, or are in close proximity (6 inches) to, devices as they pass through the equipment.
- If possible, replace the insulators with static dissipative materials.
- Where not possible, use an anti-static or air ionizer to neutralize surfaces that generate static charges.
- Make sure all metal which comes in contact with devices is grounded. Do not depend on visual verification; use an ohmmeter. Check all metal in the path of devices as they move through the equipment.
- Make sure the equipment itself is properly grounded.

There are many circuit examples that can help an application to reduce the effect of ESD/EOS from the outside world. These circuit examples help reduce the energy transferred from the ESD/EOS phenomenon to the microcontroller circuit. Some of the circuit examples are:

- A series resistor on the input pin of a microcontroller reduces the current flowing into the input pin due to an ESD event. A typical value range is from 1-10 kOhms.
- An R-C-R pie filter on the Input pins of a microcontroller
- Transorbs/protection diodes/diode clamps
- ESD spark gaps on the PCB
- Power supply decoupling capacitors
- Spacing between HV lines (UL spacing standards) and PIC® MCU pins

## EOS CONTROL MECHANISMS

Care should be taken during product assembly and testing to prevent any potential voltage or current spikes that may cause an EOS failure on the device.

Most failures can be traced to flaws in the equipment ground or electrical connections, such as:

- Poor Test Equipment Grounding
- Multiple Ground Connections:
  - Can cause a voltage differential between two ground connections
- Ground Loop Currents:
  - Mix-ups between a chassis ground and electrical safety ground

Other factors to consider during programming and testing of devices:

- AC power line surges (large switching currents) on test equipment
- Inductive/capacitive loads
- Connecting long cables to active circuits; programming and testing cables to the device should be short
- Damaged or poorly maintained sockets on programmers
- Incorrect insertion into programmer sockets
- Component board is mounted in the wrong orientation
- Neutral/ground reversal
- Current Induction:
  - Motors or other inductive components connected to the test equipment can generate strong magnetic fields, which can produce currents and voltages that can spread through wires, and other connections

For an in-depth discussion of transient suppression mechanisms, which can be used to prevent ESD or EOS events in an application, please refer to the *"EMC Newsletter 3"* at https://ww1.microchip.com/downloads/en/Market_Communication/EMC%20Newsletter%20Issue%203.pdf.

### Product/Application Level

Circuit design and PCB layout are fundamental in preventing EOS conditions from reaching the device. There are several publications that offer great advice on properly designing circuits to prevent overstress conditions.

The recommendations in the publications concentrate on the following:

- Clean VCC and VSS Supplies:
  - Avoid excessive ringing and power-up overshoot/undershoot
- Controlled VCC Ramp at Power-up and Power-Down:
  - Too fast power-up or power-down could cause excessive inrush currents through the circuit
- Proper Power/Ground:
  - Avoid ground loops and ground differentials
- Correct Decoupling Capacitor Values:
  - Essential for filtering high-frequency spikes
- Data Bus Contentions
- Connecting External Cable to an Unprotected I/O Port
- Proper Component Placement
- Short Trace Lengths

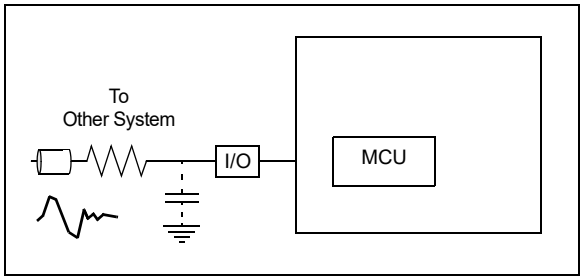
### RECOMMENDED READING

*"EMC and the Printed Circuit Board: Design, Theory and Layout Made Simple"* by Mark I. Montrose. Wiley Interscience/IEEE Press, 1998, ISBN 0-7803-4703-X

## ESD AND EOS CONTROL CIRCUIT EXAMPLES

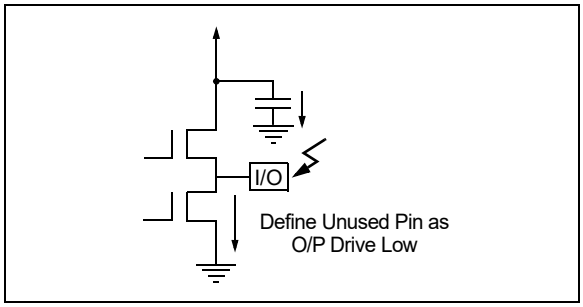
Description: Figure 19 shows an example of the protection of an I/O pin using a ferrite bead at the source and a current-limiting resistor. There is a capacitor to ground connection to filter high-frequency transients by creating an LRC filter.

**FIGURE 19: I/O PIN USING FERRITE BEAD AND CURRENT-LIMITING RESISTOR**



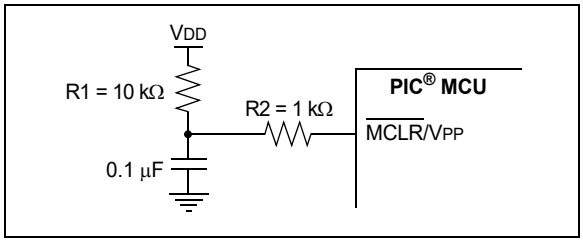

Description: Unused pins should have a pull-up or pull-down resistor to keep the I/O in a known state. If this is cost-prohibitive, an alternative is to have an unused pin configured as an output driven logic low (see Figure 20). This will protect the microcontroller from external sources of transients on these pins by directing the transient to ground. Note that until the I/Os are initialized during application start-up, the I/O pins are configured as inputs by default, making any unused pin susceptible to EOS/ESD during power-up.

**FIGURE 20: CONFIGURING AN UNUSED PIN AS AN OUTPUT DRIVEN LOGIC LOW**



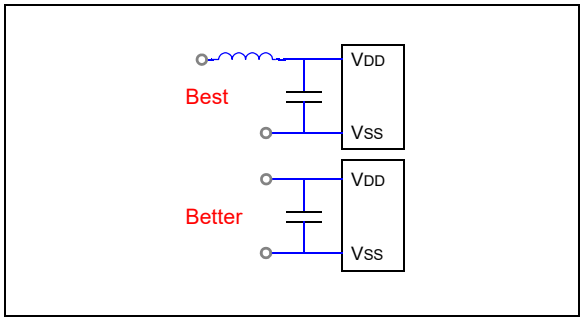
Description: In PIC microcontrollers, $\overline{MCLR}$ also serves as a VPP pin. This pin has no internal ESD clamping diodes. It is necessary then, to protect the pin from ESD or EOS events. A current-limiting resistor, as shown (R2) in Figure 21, will limit the energy transferred to the $\overline{MCLR}$ pin during an ESD or EOS event.

**FIGURE 21: USE OF CURRENT-LIMITING RESISTOR AND $\overline{MCLR}$**



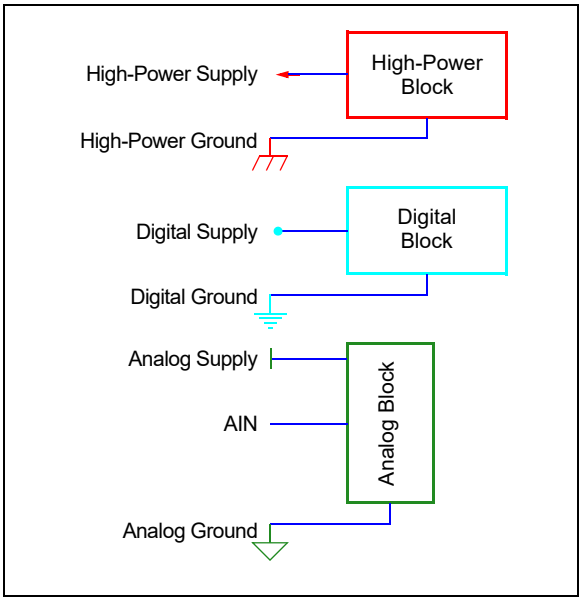

Description: Figure 22 shows an example of decoupling the power supply line. It is important to maintain a clean power feed to the microcontroller. Use a decoupling capacitor close to the device's VDD and VSS input pins to filter out transients, and noise to the device. The best practice is to add a ferrite bead close to the power source to create an LC filter. Note that many devices may have more than one VDD and VSS pin. Each pin pair should have a decoupling capacitor as a standard practice.

**FIGURE 22: DECOUPLING OF POWER SUPPLY LINE**



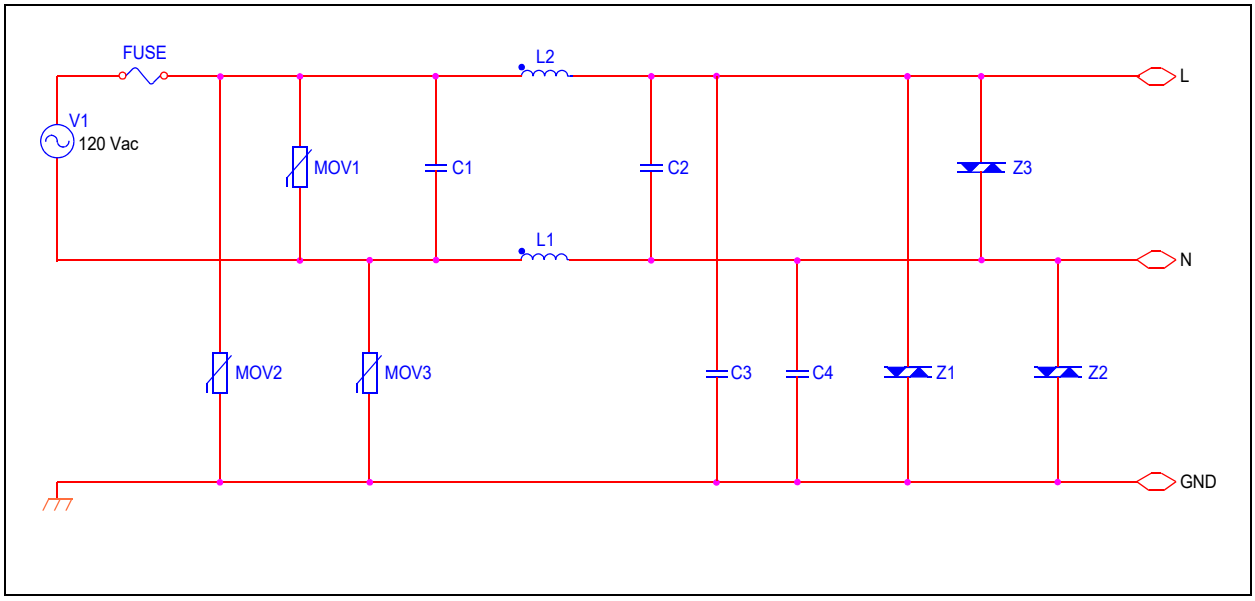

Description: Figure 23 shows an example layout. The return paths for the high-power, digital and analog blocks of the application circuit must be separated. This will reduce the amount of switching noise, voltage spikes or transients transferred from one circuit block to another. The grounds should be connected together at the power supply entry point.

**FIGURE 23: LAYOUT CONSIDERATIONS**



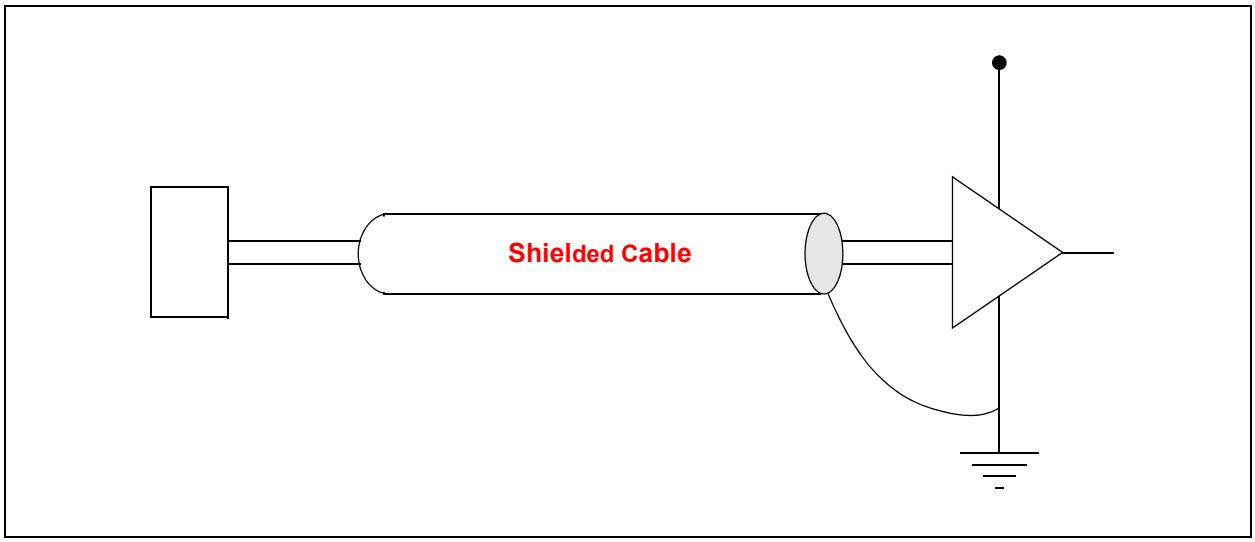
Description: The transient suppressor devices have limited current capability. Line impedance can be extremely low, so it is often necessary to include some limiting resistance in series with the supply lines to reduce the stress on the shunt suppressors. Although resistors can be used, it is recommended that inductors be used to increase efficiency and also add filtering (see Figure 24). This will help to reject line-borne noise and will filter out power supply generated noise. The winding resistance and inductance can provide the necessary series impedance to limit the transient current for efficient transient suppression.

**FIGURE 24: EFFICIENT TRANSIENT SUPPRESSION**



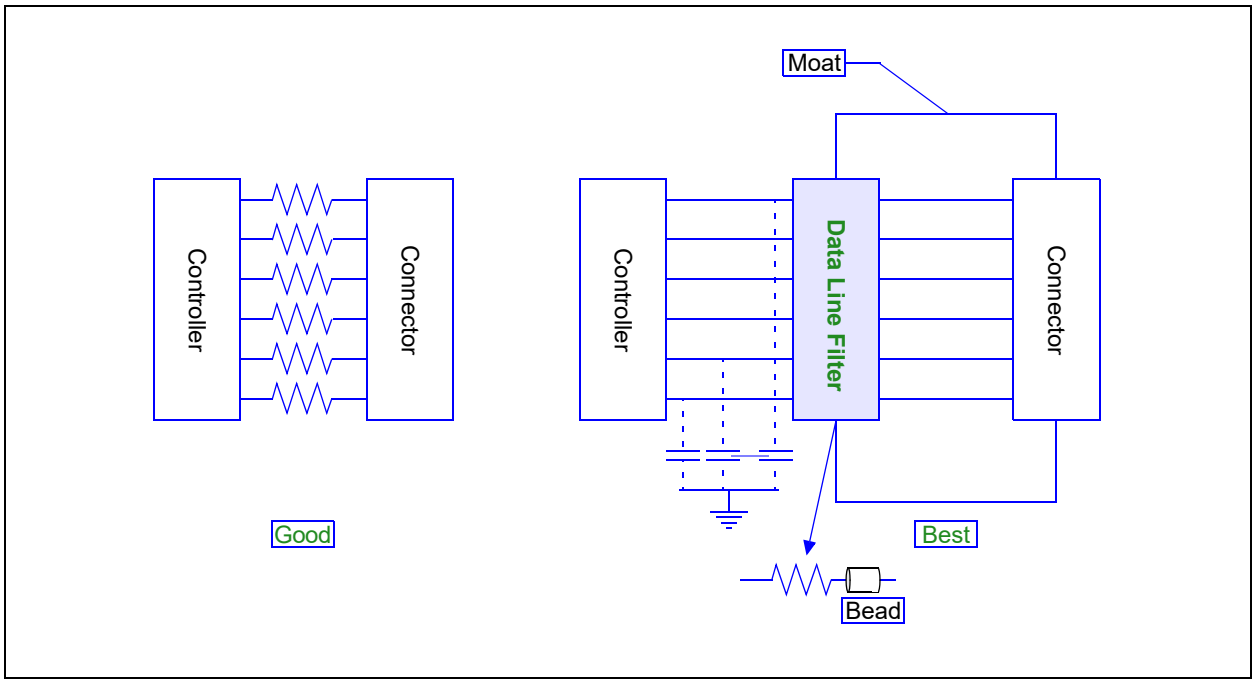

Description: When using cables to connect to sensors, make sure to use the proper termination. Shielded cabling is recommended (see Figure 25). In cases where a long cable is used, a 100 Ohm series resistor, close to the microcontroller input, can help minimize the impact of ESD events that may occur at the far end of the cable.

**FIGURE 25: SHIELDED CABLING EXAMPLE**



Description: Cable connectors should have filters. The simplest method is by using current-limiting resistors. Adding a full LCR filter on the lines, as shown in Figure 26, can fully protect the controller from spurious spikes and transients that can occur when a connector is connected or disconnected.

**FIGURE 26: USE OF A FULL LCR FILTER**



## EXAMPLE FA REPORT

### EOS Failure

BACKGROUND

A customer returned one USB82640AM unit for failure analysis. USB Pins 3, 4 and 42 are shorted to ground. Power Pins 5, 15, 34, 26, 25, 16 and 12 are shorted to ground.

SUMMARY

Failure analysis was able to confirm a failure for the returned unit. The device arrived with a crater in the package. There was no apparent damage to the leads. Several shorts were observed during curve tracer analysis, including I/Os (Pins 3, 4 and 42) as well as power pins (Pins 5, 12, 15, 16, 25, 26 and 34). Anomalies were observed during X-ray analysis. The anomalies appear at the location of the package damage. Acoustic microscopy revealed an anomaly at the location of the package damage. SN#1 was decapsulated using red fuming nitric acid. The unit was then thoroughly inspected with a low-power microscope. EOS damage was observed. The failure mechanism for SN#1 is damage by Electrical Overstress.

ANALYSIS

EXTERNAL VISUAL: The device arrived with a crater in the package. There was no apparent damage to the leads (see Figure 27).

CURVE TRACE: Several shorts were observed during curve tracer analysis, including I/Os (Pins 3, 4 and 42) as well as power pins (Pins 5, 12, 15, 16, 25, 26 and 34). The short observed on the mentioned pins is represented in Figure 28.

X-RAY/C-SAM ANALYSIS: Anomalies observed during X-ray analysis. The anomalies appear at the location of the package damage (see Figure 29). Acoustic microscopy revealed an anomaly at the location of the package damage (see Figure 30 and Figure 31).

DECAPSULATION/ OPTICAL INSPECTION: SN#1 was decapsulated using heated, fuming nitric acid. The unit was then thoroughly inspected with a low-power microscope. EOS damage was observed (Figure 32).

CONCLUSION: The failure mechanism for SN#1 is damage by Electrical Overstress.

**FIGURE 27: OPTICAL IMAGE OF SN#1**

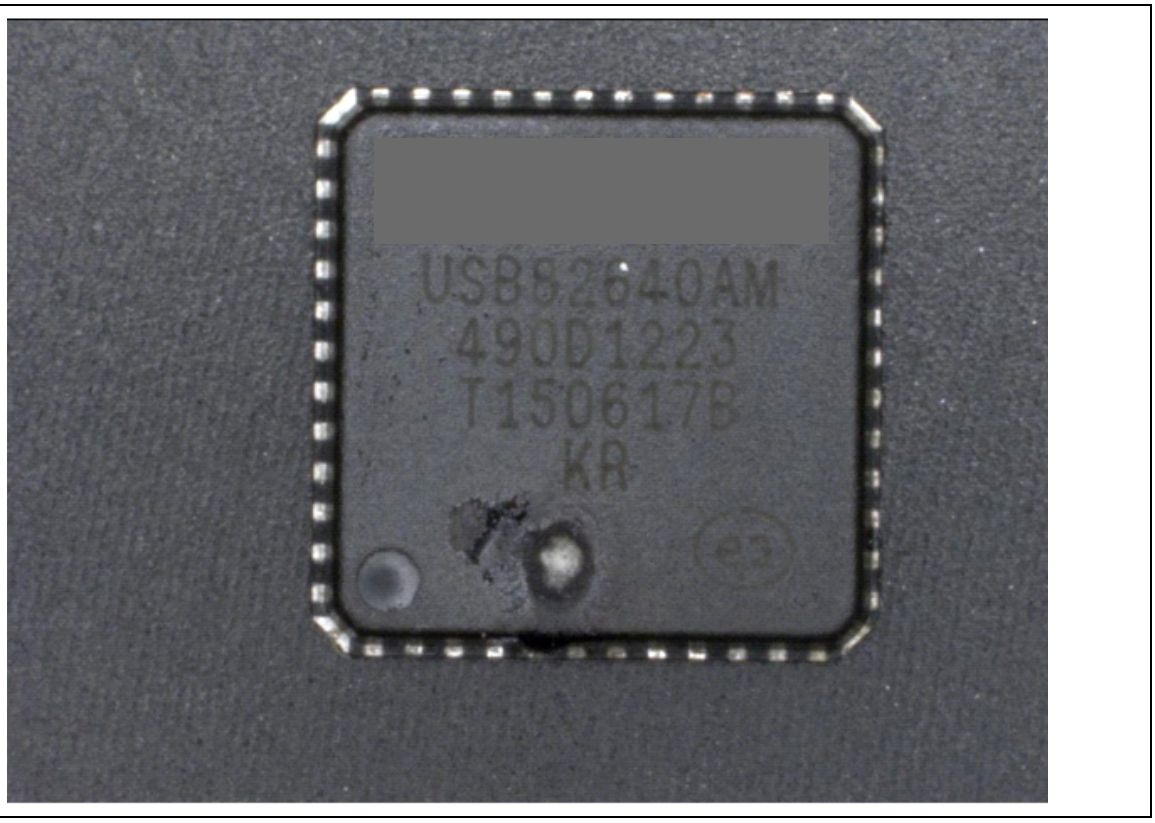



**FIGURE 28: IMAGE OF SHORT OBSERVED ON SEVERAL I/O PINS AND POWER PINS**

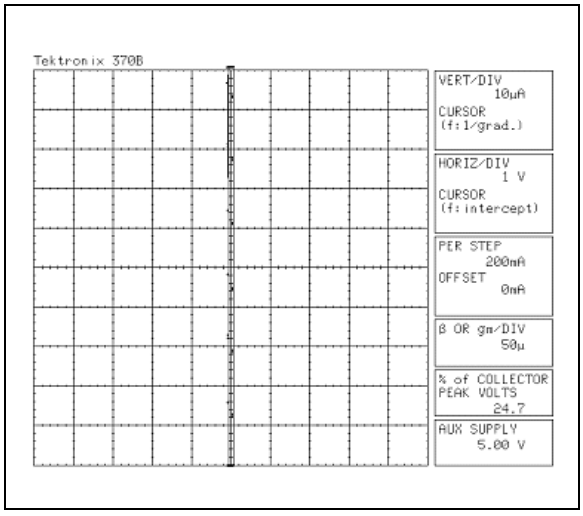



**FIGURE 29: X-RAY IMAGE OF SN#1**

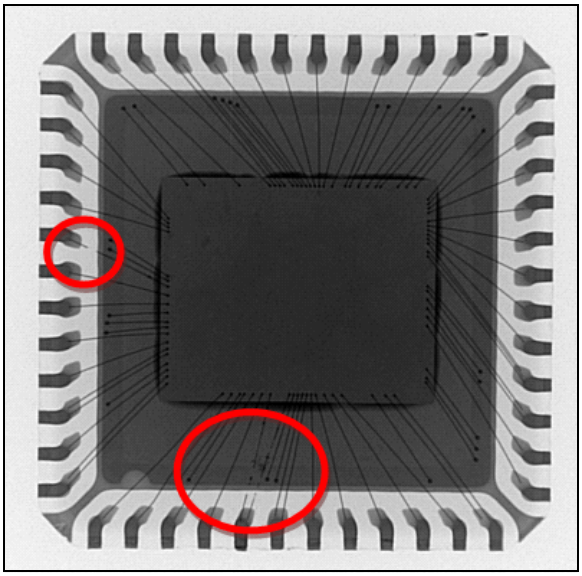


**FIGURE 30: TOP C-SAM IMAGE OF SN#1**

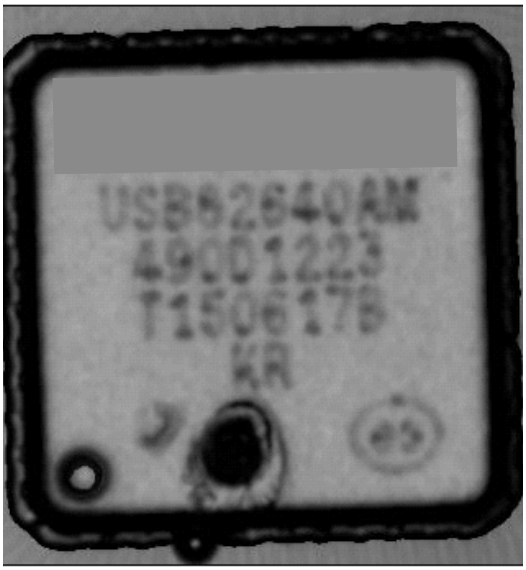
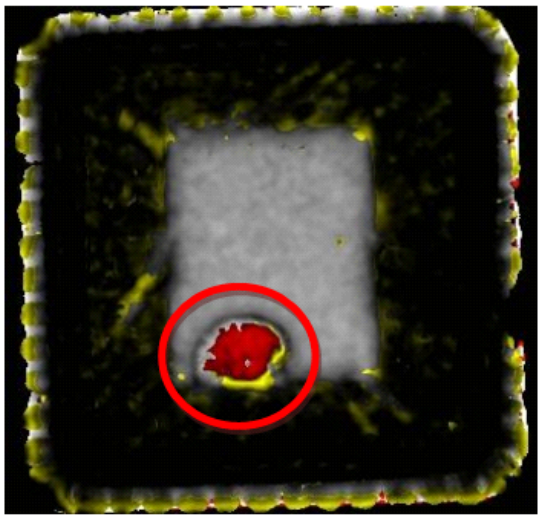
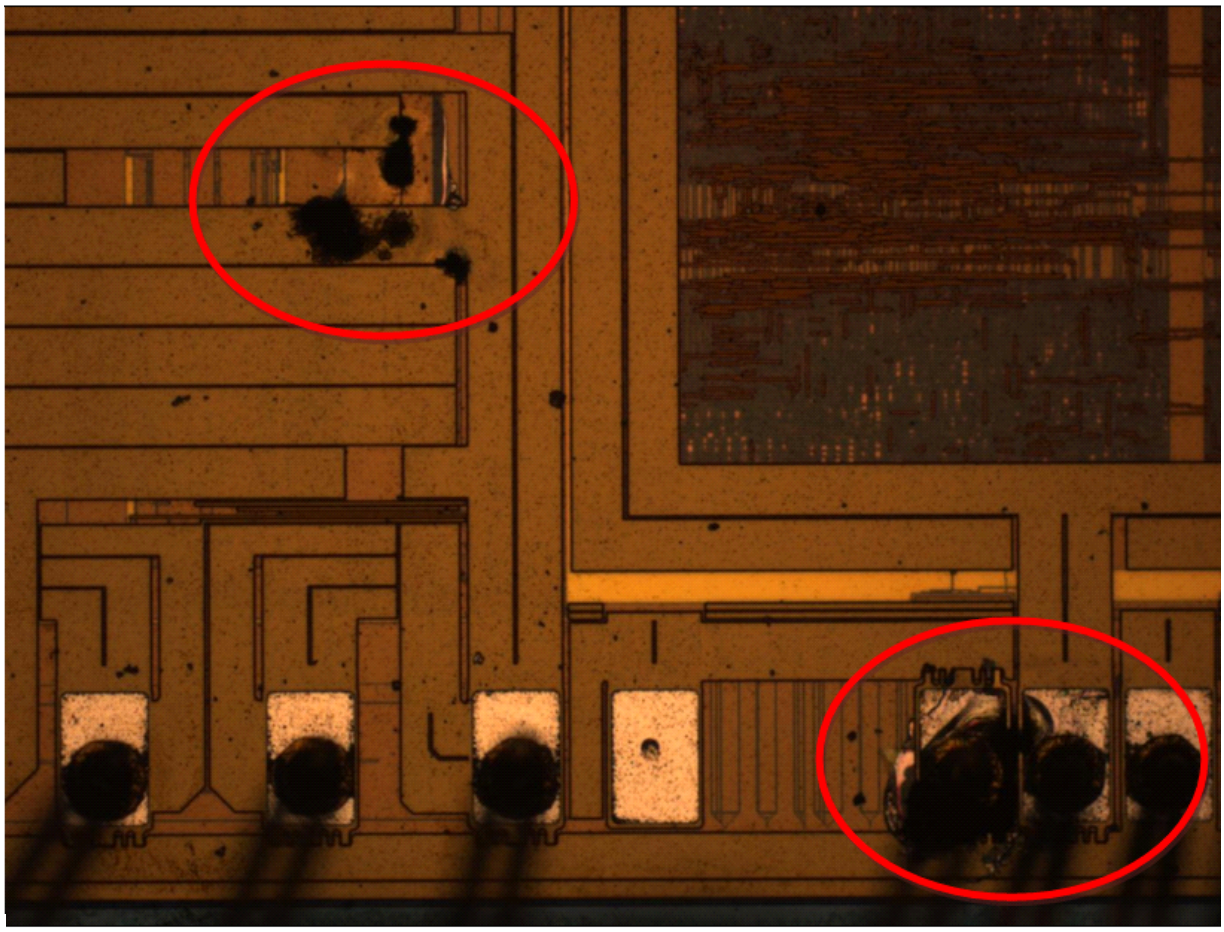



**FIGURE 31: DIE C-SAM IMAGE OF SN#1(1)**



**Note 1:** An anomaly was observed at the location of the package damage (same orientation as Figure 30).

**FIGURE 32: 50x IMAGE OF EOS DAMAGE ON SN#1**



## SAMPLE FA REPORT (Page 1 of 3)

MICROCHIP
The Embedded Control Solutions Company

**Quality and Reliability**
**Failure Analysis Group**

**FA Report #: XXXXX**
August 6, 2013
Page 1 of 3

| | | | |
|---|---|---|---|
| **Customer:** | Chandler Reliability | **Microchip Part #:** | MCP14DEx |
| **Rev#:** | B0 | **Package Type:** | 8 lead Side Braised |
| **Test chip #:** | 14 | **Mask #:** | ABCD |
| **Quantity:** | 2 (1 non failing device also provided) | **Lot#** | Not provided |
| **Point of Failure:** | ESD-HBM | **Date Received:** | 7/29/2013 |
| **Contacts:** Engineer 1 (Requestor), Engineer 2 (Reviewer), Engineer 3 (FA) | | | |

## Background

Two MCP14Dx devices were submitted for failure analysis post ESD-HBM testing.

## Analysis

**EXTERNAL VISUAL INSPECTION:** The devices arrived with identifying number #7 and #9. One known good device was also included for comparison purposes.

**CURVE TRACE:** The devices showed normal pin characteristics when compared with the known good device.

**VISUAL EXAMINATION:** The devices was de-lidded. (One device, device 7 was inadvertently destroyed during the de-lidding process) A magnified visual inspection was then performed on device #9. No visible damage or defects in the device circuitry was seen.

**LEM ANALYSIS:** Light emission analysis showed one distinct abnormal light emission when compared with a known good unit. Figures 1shows the abnormal light emission.

**CHEMICAL DEPROCESS:** A chemical deprocess was performed. Figure 2 and 3 show photo's of the damage seen.

## Summary

ESD damage was confirmed on SN#9.

| SN(s) | Markings | | Failure Mode | Failure Mechanism |
|---|---|---|---|---|
| | Top | Bottom | | |
| #9 | NA | NA | Leakage | ESD |

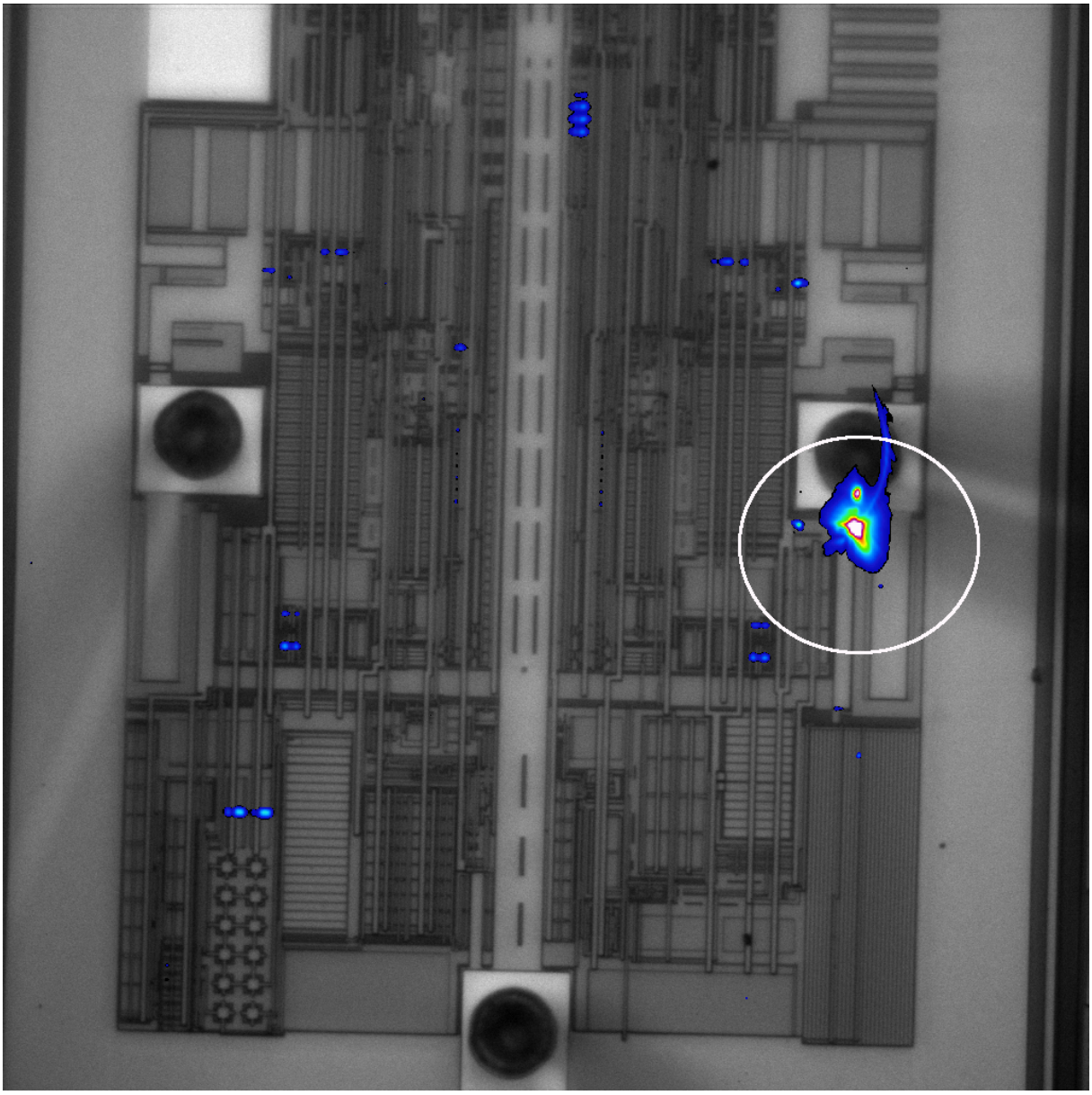
## SAMPLE FA REPORT (Page 2 of 3)

MICROCHIP
The Embedded Control Solutions Company

*Quality and Reliability*
*Failure Analysis Group*

**FA Report #: XXXXX**
August 6, 2013
Page 2 of 3

**Figure 1:** Shows the abnormal light emission seen on SN#9.



## SAMPLE FA REPORT (Page 3 of 3)

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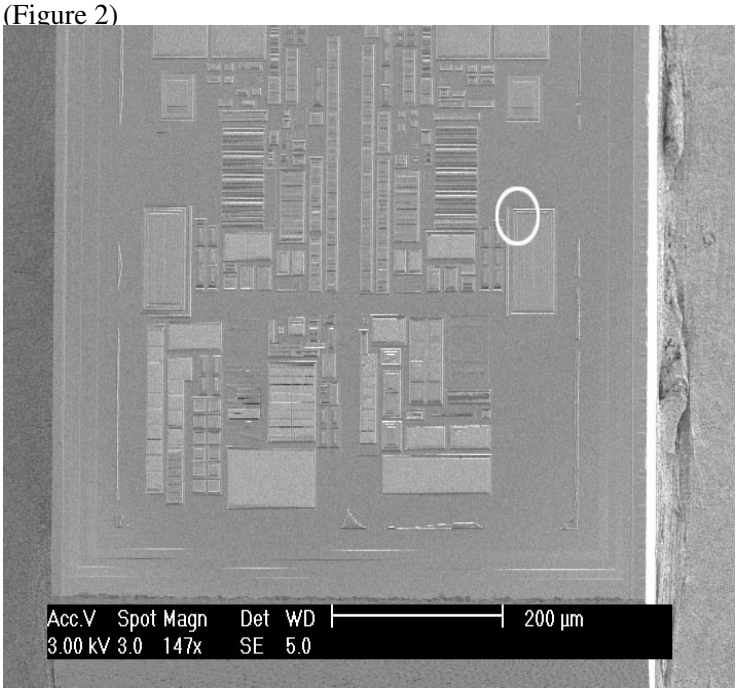
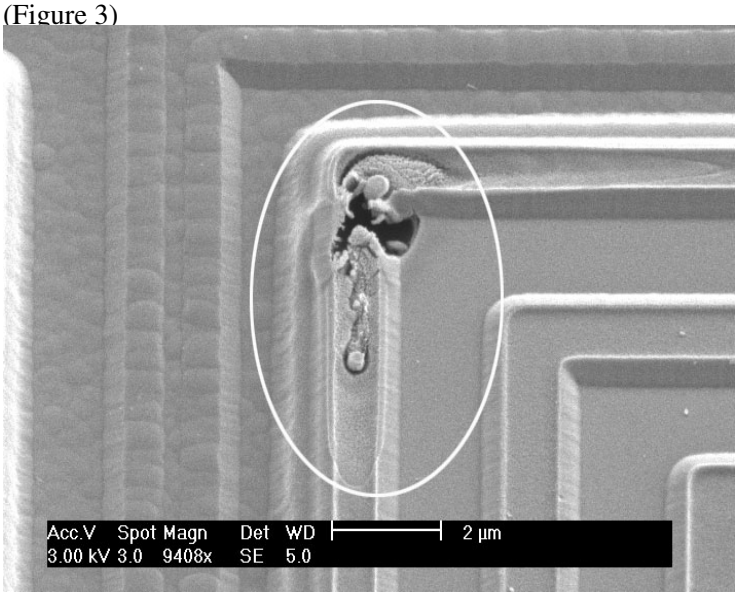
*Quality and Reliability*
*Failure Analysis Group*

**FA Report #: XXXXX**
August 6, 2013
Page 3 of 3

**Figure 2 and 3: S**how the location and damage to SN#9.
(Figure 2)




(Figure 3)



## REFERENCES:


1. JEP161: System Level ESD Part 1: Common Misconceptions and Recommended Basic Approaches
2. JEP162A-01: System Level ESD: Part II: Implementation of Effective ESD Robust Designs
3. JEP164: System Level ESD Part III: Review of ESD Testing and Impact on System-Efficient ESD Design (SEED)
4. JEP174, *"White Paper 4: Understanding Electrical Overstress - EOS"* (revision 1.2), Industry Council on ESD Target Levels, August 2016.
5. Microchip Quality and Reliability web page: www.microchip.com/quality.

**NOTES:**

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