AVR500: Migration between ATmega64 and ATmega645

8-bit AVR® Microcontrollers

Application Note

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Introduction

This application note is a guide to assist a current ATmega64 user in converting existing designs to ATmega645, and vice versa. ATmega64 and ATmega645 coexisting devices and they are not designed to be a replacement device for each other. They are however pin compatible for all but a few pins, and have a very similar feature set.

The information regarding ATmega64 also applies to ATmega128, as the two devices are functionally equal and pin compatible. The information regarding ATmega645 also applies to ATmega165 and ATmega325, as the three devices are functionally equal and pin compatible. Note that differences in memory sizes should be considered in all cases.

ATmega64 has in general more peripheral modules and features, while ATmega645 uses less power. With a few modifications to the I/O register access, ATmega64 and ATmega645 can be exchanged on existing circuit boards. In addition to the functional changes, the electrical characteristics of the two devices are different. Check the datasheet for detailed information.

Features that are identical, or just have their I/O registers and bits at different addresses and positions, are not in general covered by the scope of this document.

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General Porting Considerations

To make the porting process as easy as possible, always refer to registers and bit positions using their defined names. Avoid using absolute addresses and values. In most cases, the register and bit names are unchanged from device to device. When you are porting a design, it is more convenient to include the correct definition file for the new device, rather than manually changing all your addresses and bit values. It is also considered good programming practice to use named references instead of absolute values. An example is shown below.

```
TCCR1A |= (1<<COM1A1) | (1<<WGM11) | (0<<WGM10); // Setup timer1.
```

To avoid conflicts with added features and register functionality, never access registers that are marked as reserved. Reserved bits should always be written to zero if accessed. This ensures forward compatibility, and added features will stay in their default states when unused.

Note that the ATmega103 compatibility mode in ATmega64 is not available in ATmega645.

Pinout

Because of the different feature sets, the alternate functions of the general I/O pins are different on ATmega64 and ATmega645. This will normally not create any problems when porting the code, as long as unused peripheral modules are not enabled.

The following subsections discuss issues concerning the pinout that the designer should consider when porting designs between ATmega64 and ATmega645.

Timer Oscillator pins

ATmega64 shares the timer oscillator pins TOSC1 and TOSC2 with I/O pins PG3 and PG4. In ATmega645, the timer oscillator pins are shared with the XTAL1 and XTAL2 pins. This means that ATmega64 designs using the timer oscillator must be modified so that the timer crystal is connected to the XTAL pins. This also means that ATmega645 must be configured to use the internal RC oscillator as system clock source if the timer oscillator is used.

ISP Programming pin mapping

On ATmega64, the ISP programming interface is not located on the same pins as the on-chip SPI module, except the SCK line. The MOSI and MISO lines for serial programming is located on the PDI and PDO pins, shared with PE0 and PE1. On ATmega645, the ISP programming lines are shared with the on-chip SPI module. This means that the ISP connection, if used, needs to be modified when porting the design.

Other moved pins

A few other signals are located on different pins. These are shown in Table 1 below.

Table 1. Signals located on different pins

Signal name	ATmega64 pin mapping	ATmega645 pin mapping
INT0 (External Interrupt 0)	Pin 25 (PD0)	Pin 26 (PD1)
IC1 (Input Capture 1) [1]	Pin 29 (PD4)	Pin 25 (PD0)
T1 (Timer/Counter1 external clock)	Pin 31 (PD6)	Pin 18 (PG3)

Notes: 1. Named ICP1 on ATmega645

Timer/Counters and Prescalers

Timer/Counter3 is available in ATmega64 only. Depending on your design, it could be possible to implement the operations performed by this timer in ATmega64 using one of the existing timers in ATmega645.

Timer/Counter1 have three Output Compare channels in ATmega64 (OC1A, OC1B and OC1C), and two in ATmega645 (OC1A and OC1B).

The Output Compare Modulator in ATmega64 is not available in ATmega645. Depending on your requirements, it could be possible to implement modulation with one ATmega645 Timer/Counter in combination with software.

Timer/Counter0 in ATmega64 has the same functionality and settings as Timer/Counter2 in ATmega645, and vice versa. This means that asynchronous clocking (e.g. real-time clock) is available for T/C0 in ATmega64 and for T/C2 in ATmega645. Timer/Counter2 in ATmega645 can also be clocked using an external clock signal instead of a 32kHz crystal oscillator.

When using Timer/Counter1 in PWM mode with the Toggle Output on Compare Match setting enabled, the functionality is slightly different on the two devices. Refer to the Compare Output Mode tables in the datasheets for details.

Power Management

ATmega64 and ATmega645 have the same Sleep Modes, except the Extended Sleep Mode, which only ATmega64 has.

ATmega645, on the other hand, has the possibility to turn off power to a set of peripheral modules, namely Timer/Counter1, the SPI module, USART0 and the ADC. The control bits for these modules are located in the Power Reduction Register (PRR). It is also possible to disable the Digital Input circuitry for the IO pins that are shared with the ADC channels. This also reduces overall power consumption for the device.

TWI and USI

The Two-Wire Interface (TWI) module in ATmega64 is not available in ATmega645. However, a Universal Serial Interface (USI) module is implemented. The USI module is designed to emulate both TWI and SPI functionality.

To port designs using the TWI module from ATmega64 to ATmega645, the low level TWI driver software needs to be rewritten for the USI module. Please refer to application notes AVR310 “Using the USI module as a TWI master” and AVR312 “Using the USI module as a TWI slave”.

ATmega645 designs using the USI module as a second SPI module could use the synchronous mode of the ATmega64 USARTs to emulate SPI.

USART

ATmega64 has two USART modules, while ATmega645 has one. Designs using both USARTS on ATmega64 could be modified to use the USI module in ATmega645 instead of the second USART. Please refer to application note AVR307 “Half duplex UART using the Universal Serial Interface”. Note that full duplex UART operation is not possible with the USI module.

If the existing ATmega64 design uses the TWI module and both USARTS, a solution is to implement the second UART in software. Please refer to application note AVR304 “Half duplex Interrupt Driven Software UART” or AVR305 “Half Duplex Compact Software UART”.

Analog Comparator

For designs using the internal bandgap reference voltage as the positive input to the comparator, the designer should be aware that the bandgap voltage is different on the two devices. The characteristics are shown in Table 2 below.

Table 2. Bandgap reference voltages

Device	Min	Typical	Max
ATmega64	1.15V	1.23V	1.40V
ATmega645	1.0V	1.1V	1.2V

Analog to Digital Converter

For designs using the internal voltage reference with the Analog to Digital Converter (ADC), the designer should be aware that the voltage reference is different on the two devices. ATmega645 uses the internal bandgap reference directly, while ATmega64 uses a fixed amplification of its internal bandgap voltage. The characteristics are shown in Table 3 below.

Table 3. ADC Internal voltage references

Device	Min	Typical	Max
ATmega64	2.3V	2.56V	2.7V
ATmega645	1.0V	1.1V	1.2V

The gain amplifier is not available when using differential measurements with the ATmega645 ADC.

External and Pin Change Interrupts

ATmega64 has 8 External Interrupt lines, while ATmega645 has one. However, ATmega645 has 16 Pin Change Interrupts, which are slightly different from External Interrupts.

How to port designs using External or Pin Change Interrupts between ATmega64 and ATmega645 depends strongly on your requirements. If an existing ATmega645 design is using more than 8 interrupt lines, some of them need to be combined or implemented as software-polled in ATmega64.

Clock Control Settings

The internal RC oscillators have different settings and characteristics in the two devices. However, the same CPU frequencies are achievable. The crystal oscillator and start-up time settings (CKSEL and SUT fuses) are also different. Refer to the datasheets for details.

ATmega645 cannot use an external RC oscillator.

External SRAM Interface

ATmega645 does not have an external SRAM interface. It is therefore not possible to port ATmega64 designs using external SRAM to ATmega645.

General Purpose I/O Registers

ATmega64 has no equivalent to the General Purpose I/O registers in ATmega645. Use SRAM variables instead.

Operating Ranges

Both ATmega64 and ATmega645 can operate at frequencies up to 8 MHz with at least 2.7V supply voltage, and up to 16 MHz with at least 4.5V supply voltage.

If lower operating voltages are required, ATmega645 can operate with supply voltages down to 1.8V, with operating frequency limited to maximum 4 MHz. Due to the extended operating ranges, the Brown-out Detector (BOD) has a third selectable trigger level at 1.8V.

Programming Interface

The programming interfaces are different on the two devices, but as long as standard programming tools are used there should be no problems. Designers should be aware that the ISP programming lines are located on different pins. Refer to the datasheets and the “Differences in Pinout” section above for details.

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