AT04470: Differences between SAM D21 Variants A, B, and L

32-bit Microcontroller

Introduction

This application note describes the differences between A, B, and L variants of SAM D21 devices. For more detailed information, refer to the device datasheet of particular SAM D21 variant.

The A and B variants are general purpose mass market product devices and the L variant is target at lighting, motor control, and other applications that need the additional timers and AC in 32 and 48 pin packages.

The first section of the application note lists the differences between variant A and variant B of SAM D21 devices. The second section list the difference of A/B variants with L variant of SAM D21 devices.

Each section describes the added/removed features for the peripherals. It also highlights the new device packages and new pin functionalities.

1 Differences between SAM D21 A and B Variants

This chapter describe how Atmel® SAM D21 B variants differ from Atmel SAM D21 A variant and what are the additional features that have been added in Atmel SAM D21 B variant.

1.1 Pin Functionality Differences

There are no pinout changes from Atmel SAM D21 A variant to Atmel SAM D21 B variant.
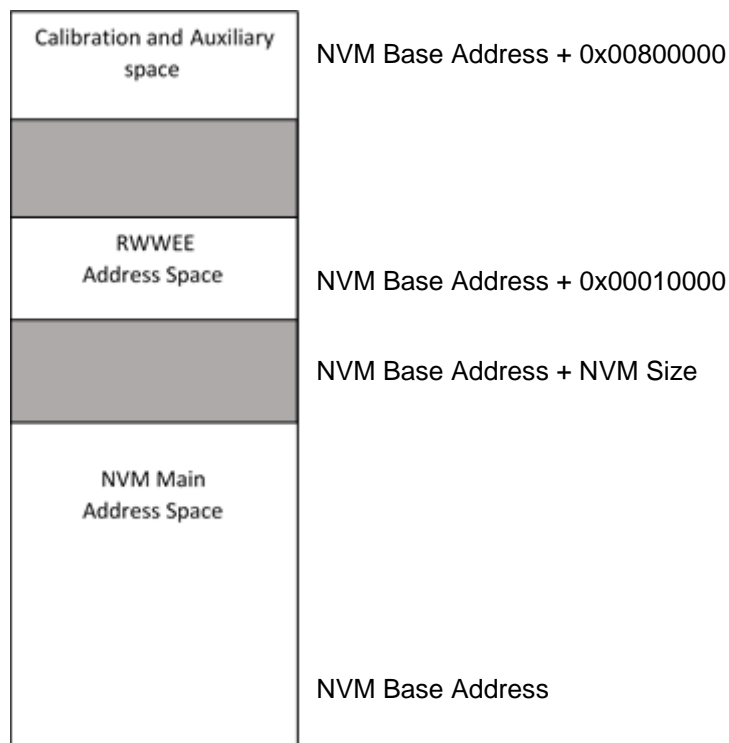
1.2 Peripheral Differences

This section summarizes the enhancements or added features in Atmel SAM D21 B variant compared to Atmel SAM D21 A variant. The B variant devices are binary compatible with A variant devices if the application does not use the additional features of B variant.

1.2.1 Internal High-speed Flash with Read-While-Write (RWW)

The non-volatile memory of the SAM D21 B variant features a Read-While-Write EEPROM Emulation (RWWEE) section. This section is intended for EEPROM emulation and can be programmed at the same time as reading the main array. This is a separate array intended for the RWW EEPROM emulation, and can be programmed while reading the main array. Figure 1-1 NVM Memory Organization shows the organization of the non-volatile memory of the SAM D21 B variant. The EEPROM emulation space is memory mapped in the same way as the main array. For the SAM D21 B variant devices, the RWWEE address space is located at NVM Base Address + 0x000100000.

Figure 1-1.   NVM Memory Organization

Calibration and Auxiliary space — NVM Base Address + 0x00800000

RWWEE Address Space — NVM Base Address + 0x00010000

NVM Base Address + NVM Size

NVM Main Address Space

NVM Base Address

In legacy implementations of the NVM controller, the EEPROM emulation area was only available as a part of the main area, which meant that while this was being programmed, all code fetching and execution would stop. The RWWEE section featured in the SAM D21 B variant can be written at the same time as the main area can be read. In addition, it is still possible to use a part of the main area for EEPROM emulation. The size of this

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area can be configured with the EEPROM bits in the NVM User Row. When reading from the RWWEE area, it is not possible to program the main array. For more details, refer the application note [2].

2   Differences between SAM D21 A/B and L Variants

This chapter describe the differences between L variant and A/B variants devices.

The L variant devices are ATSAMD21E15L, ATSAMD21E16L, and ATSAMD21G16L. These will be compared to similar A and B variants devices.

The A variant devices used for comparison are ATSAMD21E15A, ATSAMD21E16A, and ATSAMD21G16A. The B variant devices used for comparison are ATSAMD21E15B, ATSAMD21E16B, and ATSAMD21G16B.

2.1   Pin Functionality Differences

2.1.1   Added/Modified Pin Functionality

2.1.1.1   Differences between ATSAMD21E15A/16A/15B/16B and ATSAMD21E15/16L

The pinouts of ATSAMD21E15/16L is different from ATSAMD21E15A/16A/15B/16B devices. The L variant devices are not drop-in replacements for A/B variants devices.

Table 2-1 shows the pin differences between ATSAMD21E15A/16A/15B/16B and AT-SAMD21E15/16L devices.

- Analog port pins PB02, PB03, PB04, and PB05 are newly added in physical pins Pin31, Pin32, Pin3, and Pin4 respectively
- PA02, PA03, RESETN, GND, VDDCORE, PA30, and PA31 pins are rearranged
- PA00, PA01, PA28, and VDDIN pins are removed to accomplish the above mentioned pins changes

Table 2-1.   Pin Functionality Differences between ATSAMD21E15A/16A/15B/16B and ATSAMD21E15/16L

32-pin QFN/TQFP package	ATSAMD21E15A/16A/15B/16B	ATSAMD21E15/16L
Pin1	PA00	PA02
Pin2	PA01	PA03
Pin3	PA02	PB04
Pin4	PA03	PB05
Pin25	PA27	RESETN
Pin26	RESETN	GND
Pin27	PA28	VDDCORE
Pin28	GND	VDDIO
Pin29	VDDCORE	PA30
Pin30	VDDIN	PA31
Pin31	PA30	PB02
Pin32	PA31	PB03

2.1.1.2 Differences between ATSAMD21G16A/16B and ATSAMD21G16L

The pinout of ATSAMD21G16L is different from the pinout of ATSAMD21G16A/ ATSAMD21G16B devices. The L variant devices are not drop-in replacements for A/B variant devices.

Table 2-2 shows the pin differences between ATSAMD21G16A/16B and ATSAMD21G16L devices.

- Analog port pins PB00, PB01, PB04, and PB05 are newly added in physical pins Pin45, Pin46, Pin3, and Pin4 respectively
- PA02, PA03, RESETN, GND, VDDCORE, VDDIN, PA27, PA28, PA30, and PA31 pins are rearranged
- PA00, PA01, PB22, and PB23 pins are removed to accomplish the above mentioned pins changes

Table 2-2.   Pin Functionality Differences between ATSAMD21G16A/16B and ATSAMD21G16L

48-pin QFN/TQFP package	ATSAMD21G16A/16B	ATSAMD2121G16L
Pin1	PA00	PA02
Pin2	PA01	PA03
Pin3	PA02	PB04
Pin4	PA03	PB05
Pin37	PB22	PA27
Pin38	PB23	RESETN
Pin39	PA27	PA28
Pin40	RESETN	GND
Pin41	PA28	VDDCORE
Pin42	GND	VDDIN
Pin43	VDDCORE	PA30
Pin44	VDDIN	PA31
Pin45	PA30	PB00
Pin46	PA31	PB01

2.2   Added Packages

2.2.1   Packages added for ATSAMD21E15/16L

Table 2-3 shows the ATSAMD21E15/16L device packages with grade and the respective ordering codes.

Table 2-3.   Added Packages for ATSAMD21E15/16L

F = -40 to 125ºC Matte Sn Plating	N = -40 to 105ºC Matte Sn Plating
ATSAMD21E15L-AFT	ATSAMD21E15L-MNT
ATSAMD21E15L-MFT	ATSAMD21E16L-MNT
ATSAMD21E16L-AFT	
ATSAMD21E16L-MFT	

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2.2.2 Packages added for ATSAMD21G16L

Table 2-4 shows the ATSAMD21G16L device packages with grade and the respective ordering codes.

Table 2-4.   Added Packages for ATSAMD21G16L

F = -40 to 125⁰C Matte Sn Plating	N = -40 to 105⁰C Matte Sn Plating
ATSAMD21G16L-MFT	ATSAMD21G16L-MNT

2.3   Peripheral Differences

2.3.1   Differences between ATSAMD21E15A/16A/15B/16B and ATSAMD21E15/16L

This section summarizes the enhancements or added features in Atmel ATSAMD21E15/16L with respect to ATSAMD21E15A/16A/15B/16B devices. The source code compatibility is guaranteed between L variant and A/B variant devices, but it is not binary compatible. So the source code for A/B variants must be recompiled for L variant devices. The differences are highlighted in Table 2-5.

Table 2-5.   Peripheral Differences between ATSAMD21E15A/16A/15B/16B and ATSAMD21E15/16L

Peripheral	ATSAMD21E15A/16A/15B/16B	ATSAMD21E15/16L
Timer Counter (TC) instances	3	3
Waveform output channels per TC instance	2	2
Timer Counter for Control (TCC) instances	3	3
Waveform channels PWM per TCC	4/2/2	4/2/2
Waveform outputs PWM per TCC	6/4/2	**8/4/2**
DMA channels	12	12
USB interface	1	**NA**
Serial Communication Interface (SERCOM) instances	4	**5**
Inter-IC Sound (I²S) interface	1	**NA**
Analog-to-Digital Converter (ADC) channels	10	**14**
Analog Comparators (AC)	2	**4**
Digital-to-Analog Converter (DAC) channels	1	1
Real-Time Counter (RTC)	Yes	Yes
RTC alarms	1	1
RTC compare values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values
External Interrupt lines	16	16
Peripheral Touch Controller (PTC) X- and Y-lines	10x6	**NA**

Peripheral	ATSAMD21E15A/16A/15B/16B	ATSAMD21E15/16L
Oscillators	32.768kHz crystal oscillator (XOSC32K)	**NA**
	0.4-32MHz crystal oscillator (XOSC)	0.4-32MHz crystal oscillator (XOSC)
	32kHz ultra-low-power internal oscillator (OSCULP32K)	32kHz ultra-low-power internal oscillator (OSCULP32K)
	8MHz high-accuracy internal oscillator (OSC8M)	8MHz high-accuracy internal oscillator (OSC8M)
	48MHz Digital Frequency Locked Loop (DFLL48M)	48MHz Digital Frequency Locked Loop (DFLL48M)
	96MHz Fractional Digital Phased Locked Loop (FDPLL96M)	96MHz Fractional Digital Phased Locked Loop (FDPLL96M)
Event System channels	12	12
Watchdog Timer (WDT)	Yes	Yes

2.3.2 Differences between ATSAMD21G16A/16B and ATSAMD21G16L

This section summarizes the enhancements or added features in Atmel ATSAMD21G16L with respect to ATSAMD21G16A/16B devices. The source code compatibility is guaranteed between L variant and A/B variants devices, but it is not binary compatible. So the source code for A/B variants must be recompiled for L variant devices. The differences are highlighted in Table 2-6.

Table 2-6.   Peripheral Differences between ATSAMD21G16A/16B and ATSAMD21G16L

Peripheral	ATSAMD21G16A/16B	ATSAMD21G16L
Timer Counter (TC) instances	3	**5**
Waveform output channels per TC instance	2	2
Timer Counter for Control (TCC) instances	3	3
Waveform channels PWM per TCC	4/2/2	4/2/2
Waveform outputs PWM per TCC	8/4/2	8/4/2
DMA channels	12	12
USB interface	1	**NA**
Serial Communication Interface (SERCOM) instances	6	**5**
Inter-IC Sound (I2S) interface	1	**NA**
Analog-to-Digital Converter (ADC) channels	14	**18**
Analog Comparators (AC)	2	**4**
Digital-to-Analog Converter (DAC) channels	1	1
Real-Time Counter (RTC)	Yes	Yes

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Peripheral	ATSAMD21G16A/16B	ATSAMD21G16L
RTC alarms	1	1
RTC compare values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values
External Interrupt lines	16	16
Peripheral Touch Controller (PTC) X and Y lines	10x6	**NA**
Oscillators	32.768kHz crystal oscillator (XOSC32K)	**NA**
	0.4-32MHz crystal oscillator (XOSC)	0.4-32MHz crystal oscillator (XOSC)
	32kHz ultra-low-power internal oscillator (OSCULP32K)	32kHz ultra-low-power internal oscillator (OSCULP32K)
	8MHz high-accuracy internal oscillator (OSC8M)	8MHz high-accuracy internal oscillator (OSC8M)
	48MHz Digital Frequency Locked Loop (DFLL48M)	48MHz Digital Frequency Locked Loop (DFLL48M)
	96MHz Fractional Digital Phased Locked Loop (FDPLL96M)	96MHz Fractional Digital Phased Locked Loop (FDPLL96M)
Event System channels	12	12
Watchdog Timer (WDT)	Yes	Yes

The ATSAMD21E15/16L and ATSAMD21G16L have enhanced features in the following peripherals such as:

- Internal high-speed flash with Read-While-Write (RWW) capability on section of the array

Note: This RWW feature is also available on ATSAMD21E15B/16B and ATSAMD21G16B.

- Analog comparator AC1 with window compare function
- Added features in Timer/Counters for Control (TCC)

2.3.3   Internal High-speed Flash with Read-While-Write (RWW)

The non-volatile memory of the ATSAMD21E15/16L and ATSAMD21G16L devices features a Read-While-Write EEPROM Emulation (RWWEE) section. This section is intended for EEPROM emulation and can be programmed at the same time as reading the main array. This is a separate array intended for the RWW EEPROM emulation, and can be programmed while reading the main array. Figure 2-1 NVM Memory Organization shows the organization of the non-volatile memory of the ATSAMD21E15/16L and ATSAMD21G16L. The EEPROM emulation space is memory mapped in the same way as the main array. For the ATSAMD21E15/16L and ATSAMD21G16L devices, the RWWEE address space is located at NVM Base Address + 0x000100000.

Figure 2-1.   NVM Memory Organization
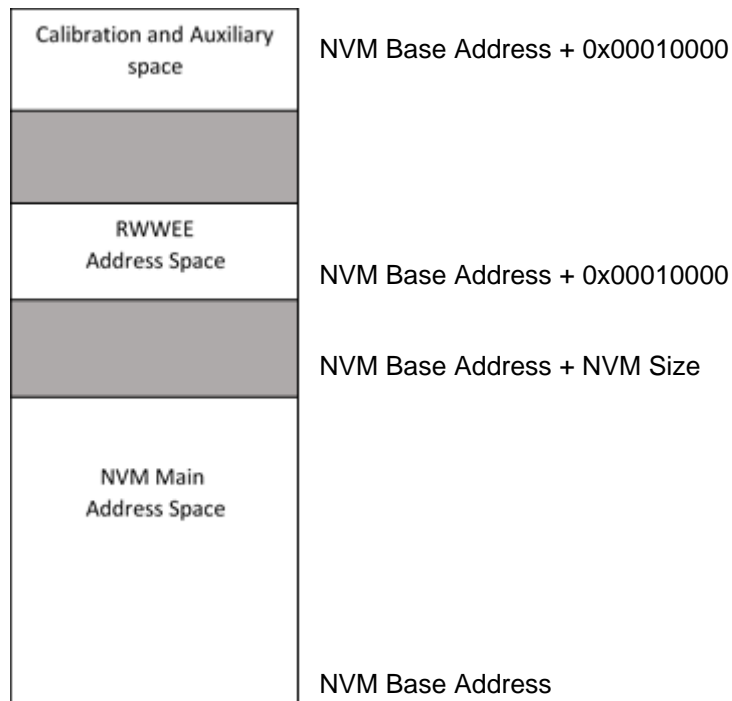
In legacy implementations of the NVM controller, the EEPROM emulation area was only available as a part of the main area, which meant that while this was being programmed, all code fetching and execution would stop. The RWWEE section featured in the ATSAMD21E15/16L and ATSAMD21G16L devices can be written at the same time as the main area can be read. In addition, it is still possible to use a part of the main area for EEPROM emulation. The size of this area can be configured with the EEPROM bits in the NVM User Row. When reading from the RWWEE area, it is not possible to program the main array. For more details, refer the application note [2].

2.3.4   Analog Comparator AC1

In ATSAMD21E15/16L and ATSAMD21G16L devices the Analog Comparator (AC) supports two individual comparators namely AC0 and AC1. The pinout for the AC1 is multiplexed with the PORTB. For more details, refer the device datasheet [3].

2.3.5   Enhancement in TCC

There are few enhanced features in TCC such as Critical RAMP2 (RAMP2C) Operation, Time-stamp Capture, and DMA Operation with circular buffer, DMA operation with circular buffer in RAMP and RAMP2A modes, and DMA operation with circular buffer in DSBOTH mode.

The above features are explained in detail in the application note [4] "Atmel SAMD21E1xL Application note on New TCC features".

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3   References

[1] Atmel SAM D21 Device Datasheet.

[2] Atmel AT03974: Read While Write EEPROM.

[3] Atmel SAM D21EL / SAM D21GL Device datasheet.

[4] Atmel SAMD21E1xL Application note on New TCC features.

4   Revision History

Doc Rev.	Date	Comments
32219A	05/2016	Initial document release.

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