AN2316

Configuration Options for the USB58xx and USB59xx

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INTRODUCTION

The Microchip USB58xx/USB59xx are a family of highly customizable USB 3.1 Gen 1 hubs. These configuration options are modifiable through any of the following methods:

- **SMBus:** SMBus configuration of the hub must be completed every time hub is powered on or reset.
- **OTP Memory:** The USB58xx/USB59xx have 8 kB internal One-Time Programmable memory. Configuration settings made via OTP memory writes are permanent and may only be undone by a subsequent OTP write with the default configuration setting.
- **SPI ROM:** An external SPI ROM loaded with an image of the hub's base firmware may be used for configuration settings. The the external SPI ROM emulates the operation of the firmware executing from the hub's internal ROM. Configuration settings added to the base firmware image executing from the SPI ROM emulate the operation of the hub's OTP memory, but have the advantage of being written and erased an unlimited number of times.
- **USB Command**: All registers can be accessed via USB command while the hub is enumerated to a USB host.

SECTIONS

This document covers the following topics:

REFERENCES

The following documents should be referenced when using this application note. See your Microchip representative for availability.

- *USB5807 7-Port USB 3.1 Gen 1 Hub Data Sheet*
- *USB5806 6-Port USB 3.1 Gen 1 Smart Hub Datasheet*
- *USB5816 6-Port USB 3.1 Gen 1 Smart Hub with Support for a Single USB Type-C™DFP Data Sheet*
- *USB5826 6-Port USB 3.1 Gen 1 Smart Hub with Support for Dual USB Type-CT™ DFPs Data Sheet*
- *USB5906 6-Port USB 3.1 Gen 1 Smart Hub with Support for a Single USB Type-C™ UFP Datasheet*
- *USB5916 6-Port USB 3.1 Gen 1 Smart Hub with Support for a USB Type-C™UFP and DFP Data Sheet*
- *USB5926 6-Port USB 3.1 Gen 1 Smart Hub with Support for Multiple USB Type-C™UFP and DFP Data Sheet*
- *System Management Bus Specification*, Version 1.0, http://smbus.org/specs

1.0 CONFIGURATION SEQUENCE AND PRIORITY

The USB58xx/USB59xx follow a specific sequence during initialization and configuration. It is important to consider this sequence when configuring the hub, especially if a combination of configuration options are used.

1.1 Configuration Straps

Upon power-on, the hub will check all pin straps. Generally, pin strapping is recommended only if other methods of configuration will not be used. If, for example, using a SPI ROM for firmware, or if the OTP is be programmed, it is recommended to perform all configuration using those methods to avoid any possible collisions.

1.2 SPI ROM Check

After checking Configuration Straps, the hub will check the presence of an SPI ROM with a valid signature. If a valid firmware file is detected, the hub will execute the firmware from the SPI ROM device.

Note that Internal OTP is ignored when executing from a SPI ROM device. Instead, the SPI ROM has a memory space allocated within the SPI memory which can be loaded with “pseudo-OTP” configuration data. An OTP file can be loaded into this space and will configure the hub in a manner which is equivalent to the Internal OTP.

1.3 SMBus Configuration during SOC_CFG stage

After SPI ROM is checked, the hub will check the SMBus pins for the presence of pull-up resistors to 3.3V. If pull-ups are detected on both the SDA and SCL lines, the hub will enter the SOC_CFG stage and wait indefinitely for configuration to occur.

During this stage, the internal register data can be modified from the default values.

1.4 Internal OTP

After SMBus configuration is completed and the special SMBus attach command is sent, the OTP memory is read and any registers configured by the internal OTP will be modified. This will overwrite any modifications done to these registers during SOC_CFG. Only registers specifically configured in the OTP configuration data will be modified. All others will load with internal ROM defaults or with the changes made during SOC_CFG.

1.5 Runtime Configuration

After OTP memory is loaded, the hub will enter Runtime. Any register may be modified during this time via SMBus or through USB via bridging through the internal Hub Feature Controller device.

While any register may be modified during runtime, certain functional changes are forbidden during runtime. For example, USB ports cannot be disabled or enabled during runtime as there is no mechanism within the USB specification to allow for changes to the number of ports while actively enumerated to a USB host.

2.0 CONFIGURATION REGISTER MAP

Below is a list of the configuration registers and their addresses. The default column displays the values that will be loaded if no modification is made to the register during the configuration stage.

TABLE 1: CONFIGURATION REGISTER MEMORY MAP

ADDR	R/W	Name	Function	Default
0800h	R	DEV_REV	Device Silicon Revision Register	**Note 4**
0801h	R/W	DEV_ID	Device Identification Register	00h
0804h	R/W	CLOCK_CTL	MCU Clock Control 1	**Note 10**
080Ah	R/W	UTIL_CONFIG1	Utility Configuration Register 1	**Note 10**
080Bh	R	CLOCK_DETECT	Clock Detect Indicator	**Note 10**
082Dh	R/W	GPIO_16_23_PD	GPIO 16-23 Pull-Down Register **(Note 1)**	00h
082Eh	R/W	GPIO_8_12_PD	GPIO 8-12 Pull-Down Register **(Note 1)**	00h
082Fh	R/W	GPIO_1_7_PD	GPIO 1-7 Pull-Down Register **(Note 1)**	00h
0831h	R/W	GPIO_16_23_DIR	GPIO 16-23 Direction Control Register **(Note 1)**	00h
0832h	R/W	GPIO_8_12_DIR	GPIO 8-12 Direction Control Register **(Note 1)**	00h
0833h	R/W	GPIO_1_7_DIR	GPIO 1-7 Direction Control Register **(Note 1)**	00h
0835h	R/W	GPIO_16_23_OUT	GPIO 16-23 Output State Control Register **(Note 1)**	00h
0836h	R/W	GPIO_8_12_OUT	GPIO 8-12 Output State Control Register **(Note 1)**	00h
0837h	R/W	GPIO_1_7_OUT	GPIO 1-7 Output State Control Register **(Note 1)**	00h
0839h	R	GPIO_16_23_IN	GPIO 16-23 Input State Read Register **(Note 1)**	00h

Note 1: See *Microchip AN1997 USB to GPIO Bridging with Microchip USB 3.1 Gen 1 Hubs* for details on how to configure the hub for GPIO control.

2: The Vendor ID LSB and MSB must be assigned the same value for both the USB 2.0 Hub and USB 3.0 Hub registers. Failure to correctly modify these registers may result in unpredictable behavior.

3: The default value of the PID registers are dependent on part number. USB5806 = 0x2806, USB5807 = 0x2807, USB5816 = 0x2816, USB5826 = 0x2826, USB5906 = 0x2906, USB5916 = 0x2916, USB5926 = 0x2926.

4: The default value of this register will vary dependent on the device firmware and silicon revision.

5: The default value of this register is dependent on part number. USB5807 = 0x20, USB5806/USB5816/ USB5826/USB5906/USB5916/USB5917 = 0x28.

6: The default value of this register is dependent on part number. USB5807 = 0x00, USB5806/USB5816/ USB5826/USB5906/USB5916/USB5917 = 0x20.

7: The Non-Removable Device settings must be assigned the same value for both the USB 2.0 Hub and USB 3.0 Hub registers. Failure to correctly modify these registers may result in unpredictable behavior.

8: The Port Disable/Remap settings must be assigned the same value for both the USB 2.0 Hub and USB 3.0 Hub registers. Failure to correctly modify these registers may result in unpredictable behavior.

9: The default value of the PID registers are dependent on part number. USB5806 = 0x5806, USB5807 = 0x5807, USB5816 = 0x5816, USB5826 = 0x5826, USB5906 = 0x5906, USB5916 = 0x5916, USB5926 = 0x5926.

10: Depends on device state of operation or hardware strap selection options.

11: Modified by device strap settings.

TABLE 1: CONFIGURATION REGISTER MEMORY MAP (CONTINUED)

ADDR	R/W	Name	Function	Default
083Ah	R	GPIO_8_12_IN	GPIO 8-12 Input State Read Register **(Note 1)**	00h
083Bh	R	GPIO_1_7_IN	GPIO 1-7 Input State Read Register **(Note 1)**	00h
083Dh	R	GPIO_16_23_PU	GPIO 8-12 Pull-Up Register **(Note 1)**	00h
083Eh	R/W	GPIO_8_12_PU	GPIO 16-23 Pull-Up Register **(Note 1)**	00h
083Fh	R/W	GPIO_1_7_PU	GPIO 1-7 Pull-Up Register **(Note 1)**	00h
0900h	R/W	USB2_OCS_STAT	USB 2.0 OCS Status Register	00h
0902h	R/W	USB3_OCS_STAT	USB 3.0 OCS Status Register	00h
096Eh	R/W	GPIO_72_PD	GPIO 72 Pull-Down Register **(Note 1)**	00h
096Fh	R/W	GPIO_64_71_PD	GPIO 64-71 Pull-Down Register **(Note 1)**	00h
0972h	R/W	GPIO_72_DIR	GPIO 72 Direction Control Register **(Note 1)**	00h
0973h	R/W	GPIO_64_71_DIR	GPIO 64-71 Direction Control Register **(Note 1)**	00h
0976h	R/W	GPIO_72_OUT	GPIO 72 Output State Control Register **(Note 1)**	00h
0977h	R/W	GPIO_64_71_OUT	GPIO 64-71 Output State Control Register **(Note 1)**	00h
097Ah	R	GPIO_72_IN	GPIO 72 Input State Read Register **(Note 1)**	00h
097Bh	R	GPIO_64_71_IN	GPIO 64-71 Input State Read Register **(Note 1)**	00h

Note 1: See *Microchip AN1997 USB to GPIO Bridging with Microchip USB 3.1 Gen 1 Hubs* for details on how to configure the hub for GPIO control.

2: The Vendor ID LSB and MSB must be assigned the same value for both the USB 2.0 Hub and USB 3.0 Hub registers. Failure to correctly modify these registers may result in unpredictable behavior.

3: The default value of the PID registers are dependent on part number. USB5806 = 0x2806, USB5807 = 0x2807, USB5816 = 0x2816, USB5826 = 0x2826, USB5906 = 0x2906, USB5916 = 0x2916, USB5926 = 0x2926.

4: The default value of this register will vary dependent on the device firmware and silicon revision.

5: The default value of this register is dependent on part number. USB5807 = 0x20, USB5806/USB5816/ USB5826/USB5906/USB5916/USB5917 = 0x28.

6: The default value of this register is dependent on part number. USB5807 = 0x00, USB5806/USB5816/ USB5826/USB5906/USB5916/USB5917 = 0x20.

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11: Modified by device strap settings.

TABLE 1: CONFIGURATION REGISTER MEMORY MAP (CONTINUED)

ADDR	R/W	Name	Function	Default
097Eh	R/W	GPIO_72_PU	GPIO 72 Pull-Up Register (**Note 1**)	00h
097Fh	R/W	GPIO_64_71_PU	GPIO 64-71 Pull-Up Register (**Note 1**)	00h
0A10h	R/W	PF0_CTL	Programmable Function Pin 0 Control Register	00h
0A11h	R/W	PF1_CTL	Programmable Function Pin 1 Control Register	00h
0A12h	R/W	PF2_CTL	Programmable Function Pin 2 Control Register	00h
0A13h	R/W	PF3_CTL	Programmable Function Pin 3 Control Register	00h
0A14h	R/W	PF4_CTL	Programmable Function Pin 4 Control Register	00h
0A15h	R/W	PF5_CTL	Programmable Function Pin 5 Control Register	00h
0A16h	R/W	PF6_CTL	Programmable Function Pin 6 Control Register	00h
0A17h	R/W	PF7_CTL	Programmable Function Pin 7 Control Register	**Note 4**
0A18h	R/W	PF8_CTL	Programmable Function Pin 8 Control Register	**Note 4**
0A19h	R/W	PF9_CTL	Programmable Function Pin 9 Control Register	00h
0A1Ah	R/W	PF10_CTL	Programmable Function Pin 10 Control Register	**Note 4**
0A1Bh	R/W	PF11_CTL	Programmable Function Pin 11 Control Register	**Note 4**
0A1Ch	R/W	PF12_CTL	Programmable Function Pin 12 Control Register	00h
0A1Dh	R/W	PF13_CTL	Programmable Function Pin 13 Control Register	00h
0A1Eh	R/W	PF14_CTL	Programmable Function Pin 14 Control Register	00h
0A1Fh	R/W	PF15_CTL	Programmable Function Pin 15 Control Register	00h
0A20h	R/W	PF16_CTL	Programmable Function Pin 16 Control Register	00h
3000h	R/W	USB2_VIDL	USB 2.0 Hub Vendor ID LSB (**Note 2**)	24h
3001h	R/W	USB2_VIDM	USB 2.0 Hub Vendor ID MSB (**Note 2**)	04h
3002h	R/W	USB2_PIDL	USB 2.0 Hub Product ID LSB	**Note 3**
3003h	R/W	USB2_PIDM	USB 2.0 Hub Product ID MSB	**Note 3**

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2: The Vendor ID LSB and MSB must be assigned the same value for both the USB 2.0 Hub and USB 3.0 Hub registers. Failure to correctly modify these registers may result in unpredictable behavior.

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11: Modified by device strap settings.

TABLE 1: CONFIGURATION REGISTER MEMORY MAP (CONTINUED)

ADDR	R/W	Name	Function	Default
3004h	R/W	USB2_DIDL	USB 2.0 Hub Device ID LSB	**Note 4**
3005h	R/W	USB2_DIDM	USB 2.0 Hub Device ID MSB	**Note 4**
3006h	R/W	HUB_CFG_1	USB 2.0 Hub Configuration 1	9Bh
3007h	R/W	HUB_CFG_2	USB 2.0 Hub Configuration 2	**Note 4**
3008h	R/W	HUB_CFG_3	USB 2.0 Hub Configuration 3	09h
3009h	R/W	USB2_NRD	USB 2.0 Hub Non-Removable Device **(Note 2)**	**Note 4**
300Ah	R/W	PDS	USB 2.0 Port Disable (Self-Powered)	00h
300Bh	R/W	PDB	USB 2.0 Port Disable (Bus-Powered)	00h
3013h	R/W	MFR_STR_INDEX	USB 2.0 Hub Manufacturer String Index	01h
3014h	R/W	PRD_STR_INDEX	USB 2.0 Hub Product String Index	02h
3015h	R/W	SER_STR_INDEX	USB 2.0 Hub Serial String Index	00h
30D0h	R/W	BC	Battery Charing	00h
30E1h	R/W	START_LOCKOUT_TIM-ER_REG	Overcurrent Lockout Timer Register	0Ah
30EAh	R/W	OCS_MIN_WIDTH	Overcurrent Minimum Pulse Width Register	05h
30EB	R/W	OCS_INACTIVE_TIMER	Overcurrent Inactive Timer	14h
30FAh	R/W	PRT_SWAP	USB 2.0 DP/DM Port Swap	00h
30FBh	R/W	USB2_PRT_REMAP_12	USB 2.0 Port 1 / Port 2 Remap **(Note 8)**	**Note 4**
30FCh	R/W	USB2_PRT_REMAP_34	USB 2.0 Port 3 / Port 4 Remap **(Note 8)**	**Note 4**
30FDh	R/W	USB2_PRT_REMAP_56	USB 2.0 Port 5 / Port 6 Remap **(Note 8)**	**Note 4**
30FEh	R/W	USB2_PRT_REMAP_7	USB 2.0 Port 7 Remap **(Note 8)**	**Note 4**
30FFh	R/W	HUB_CMD_STAT	USB Hub Command/Status Register	00h
3100h	R	USB2_LINK_STATE1_3	USB 2.0 Link State Ports 0 – 3	**Note 10**

Note 1: See *Microchip AN1997 USB to GPIO Bridging with Microchip USB 3.1 Gen 1 Hubs* for details on how to configure the hub for GPIO control.

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11: Modified by device strap settings.

TABLE 1: CONFIGURATION REGISTER MEMORY MAP (CONTINUED)

ADDR	R/W	Name	Function	Default
3101h	R	USB2_LINK_STATE4_7	USB 2.0 Link State Ports 4 – 7	**Note 10**
3104h	R/W	USB2_HUB_CTL	USB 2.0 Hub Control	00h
3108h	R/W	USB2_BCDUSB_MSB	USB 2.0 Hub Version BCD MSB	02h
3109h	R/W	USB2_BCDUSB_LSB	USB 2.0 Hub Version BCD LSB	10h
3150h	R	USB2_HUB_ADDR	USB 2.0 Hub Address Register	00h
3151h	R	USB2_REMOTE_WAKE	USB 2.0 Hub Remote Wakeup Register	00h
318Ch	R/W	EMBED_TEST	USB 2.0 Embedded Test Mode Control	00h
318Dh	R/W	EMBED_TEST_PORT_SEL	USB 2.0 Embedded Test Mode Port Select	00h
318Eh	R/W	CONNECT_CFG	FlexConnect Configuration Register	00h
3194h	R	USB20_HUB_STAT	USB 2.0 Hub Status	00h
3195h	R	USB20_HUB_DN_DEV_-TYPE1	USB 2.0 Hub Downstream Port Device Speed Ports 1– 4	00h
3196h	R	USB20_HUB_DN_DEV_-TYPE2	USB 2.0 Hub Downstream Port Device Speed Ports 5 – 7	00h
3197h	R	USB2_SUSP_IND	USB2 Suspend Indicator	00h
3840h	R/W	USB3_HUB_CTL	USB3 Hub Control Register 1	20h
3841h	R/W	USB3_HUB_CTL2	USB3 Hub Control Register 2	01h
3842h	R/W	USB3_HUB_CTL3	USB3 Hub Control Register 3	01h
3843h	R/W	USB3_VBUS_DEB_PERIOD	USB3 VBUS Debounce Period Register	64h
3844h	R/W	USB3_HUB_CTL4	USB3 Hub Control Register 4	01h
3849h	R/W	USB3_HUB_CTL5	USB3 Hub Control Register 5	00h
3851h	R	USB30_HUB_STAT	USB 3.1 Gen 1 Hub Status Register	00h
3852h	R/W	USB30_HUB_DN_-SPEED_IND	USB 3.1 Gen 1 Hub Downstream Speed Indicator Register	**Note 10**
3855h	R/W	DISABLE_USB3P1_D-SPORT	USB3 Disable USB3.1 DSPORT State Machine Register	**Note 4**
3857h	R	USB3_SUSP_IND	USB3 Suspend Indicator	00h

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2: The Vendor ID LSB and MSB must be assigned the same value for both the USB 2.0 Hub and USB 3.0 Hub registers. Failure to correctly modify these registers may result in unpredictable behavior.

3: The default value of the PID registers are dependent on part number. USB5806 = 0x2806, USB5807 = 0x2807, USB5816 = 0x2816, USB5826 = 0x2826, USB5906 = 0x2906, USB5916 = 0x2916, USB5926 = 0x2926.

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11: Modified by device strap settings.

TABLE 1: CONFIGURATION REGISTER MEMORY MAP (CONTINUED)

ADDR	R/W	Name	Function	Default
3858h	R/W	USB3_PRT_REMAP_EN	USB3 Port Remap Enable Register	**Note 4**
3860h	R/W	USB3_PRT_REMA_P1_P2	USB3 Port Remap Ports 1 and 2 **(Note 8)**	**Note 4**
3861h	R/W	USB3_PRT_REMAP_P3_P4	USB3 Port Remap Ports 3 and 4 **(Note 8)**	**Note 4**
3862h	R/W	USB3_PRT_REMAP_P5_P6	USB3 Port Remap Ports 5 and 6 **(Note 8)**	**Note 4**
3863h	R/W	USB3_PRT_REMAP_P7	USB3 Port Remap Port 7	**Note 4**
3870h	R/W	LINK_PWR_STATE1	USB 3.0 Link Low Power State 1	**Note 10**
3874h	R/W	LINK_PWR_STATE2	USB 3.0 Link Low Power State 2	**Note 10**
3878h	R/W	PENDING_HP_MAX_VAL-UE_LSB	USB HP Pending Timer ECN Register LSB	5Fh
3879h	R/W	PENDING_HP_MAX_VAL-UE_MSB	USB HP Pending Timer ECN Register MSB	05h
387Ah	R/W	PM_ENTRY_AND_U1_RESI-DENCY_TIME	PM Entry and U1 Residency Time Register	49h
387Bh	R/W	U1_LFPS_EXIT_LSB	U1 LFPS Exit Time LSB	77h
387Ch	R/W	U1_LFPS_EXIT_MSB	U1 LFPS Exit Time MSB	00h
387Dh	R/W	PM_LC_TIME_IN_US_LSB	PM LC Time in Microseconds LSB Register	71h
387Eh	R/W	PM_LC_TIME_IN_US_MSB	PM LC Time in Microseconds MSB Register	02h
3C00h	R/W	USB3_PRT_CFG_SEL1	USB 3.1 Gen 1 Port 1 Configuration Select **(Note 8)**	83h
3C04h	R/W	USB3_PRT_CFG_SEL2	USB 3.1 Gen 1 Port 2 Configuration Select **(Note 8)**	83h
3C08h	R/W	USB3_PRT_CFG_SEL3	USB 3.1 Gen 1 Port 3 Configuration Select **(Note 8)**	83h
3C0Ch	R/W	USB3_PRT_CFG_SEL4	USB 3.1 Gen 1 Port 4 Configuration Select **(Note 8)**	83h

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ADDR	R/W	Name	Function	Default
3C10h	R/W	USB3_PRT_CFG_SEL5	USB 3.1 Gen 1 Port 5 Configuration Select **(Note 8)**	83h
3C14h	R/W	USB3_PRT_CFG_SEL6	USB 3.1 Gen 1 Port 6 Configuration Select **(Note 8)**	83h
3C18h	R/W	USB3_PRT_CFG_SEL7	USB 3.1 Gen 1 Port 7 Configuration Select **(Note 8)**	**Note 4**
3C20h	R/W	OCS_SEL1	Port 1 Overcurrent Sense Source Select	01h
3C24h	R/W	OCS_SEL2	Port 2 Overcurrent Sense Source Select	01h
3C28h	R/W	OCS_SEL3	Port 3 Overcurrent Sense Source Select	01h
3C2Ah	R/W	OCS_SEL4	Port 4 Overcurrent Sense Source Select	01h
3C30h	R/W	OCS_SEL5	Port 5 Overcurrent Sense Source Select	01h
3C34h	R/W	OCS_SEL6	Port 6 Overcurrent Sense Source Select	01h
3C38h	R/W	OCS_SEL7	Port 7 Overcurrent Sense Source Select	01h
3C48h	R/W	USB3_PORT_SPLIT_EN	USB3 Port Split Enable Register	00h
411Ah	R/W	FLEX_CFG1	FlexConnect Configuration 1	00h
411Bh	R/W	FLEX_CFG2	FlexConnect Configuration 2	01h
411Dh	R/W	RUNTIME_FLAGS2	USB2 Hub Default PID MSB	85h
411Eh	R	USB2_DEFAULT_PIDM	USB2 Hub Default PID MSB	28h
411Fh	R	USB2_DEFAULT_PIDL	USB2 Hub Default PID LSB	**Note 4**
4120h	R	USB3_DEFAULT_PIDM	USB3 Hub Default PID MSB	58h
4121h	R	USB3_DEFAULT_PIDL	USB3 Hub Default PID LSB	**Note 4**
4130h	RR/W	HFC_EN	Hub Feature Controller Enable	00h
4134h	R/W	RUNTIME_FLAGS	Hub Runtime Flags Register 1	41h
4135h	R/W	BC_VBUS_DIS_TIME	Battery Charging DCP TO CDP VBUS Discharge Time Register	78h
413Ch	R/W	DETACH_TIMER_A_LSB	Billboard Detach Timer A LSB	07h
413Dh	R/W	DETACH_TIMER_A_MSB	Billboard Detach Timer A MSB	D0h

Note 1: See *Microchip AN1997 USB to GPIO Bridging with Microchip USB 3.1 Gen 1 Hubs* for details on how to configure the hub for GPIO control.

2: The Vendor ID LSB and MSB must be assigned the same value for both the USB 2.0 Hub and USB 3.0 Hub registers. Failure to correctly modify these registers may result in unpredictable behavior.

3: The default value of the PID registers are dependent on part number. USB5806 = 0x2806, USB5807 = 0x2807, USB5816 = 0x2816, USB5826 = 0x2826, USB5906 = 0x2906, USB5916 = 0x2916, USB5926 = 0x2926.

4: The default value of this register will vary dependent on the device firmware and silicon revision.

5: The default value of this register is dependent on part number. USB5807 = 0x20, USB5806/USB5816/USB5826/USB5906/USB5916/USB5917 = 0x28.

6: The default value of this register is dependent on part number. USB5807 = 0x00, USB5806/USB5816/USB5826/USB5906/USB5916/USB5917 = 0x20.

7: The Non-Removable Device settings must be assigned the same value for both the USB 2.0 Hub and USB 3.0 Hub registers. Failure to correctly modify these registers may result in unpredictable behavior.

8: The Port Disable/Remap settings must be assigned the same value for both the USB 2.0 Hub and USB 3.0 Hub registers. Failure to correctly modify these registers may result in unpredictable behavior.

9: The default value of the PID registers are dependent on part number. USB5806 = 0x5806, USB5807 = 0x5807, USB5816 = 0x5816, USB5826 = 0x5826, USB5906 = 0x5906, USB5916 = 0x5916, USB5926 = 0x5926.

10: Depends on device state of operation or hardware strap selection options.

11: Modified by device strap settings.

TABLE 1: CONFIGURATION REGISTER MEMORY MAP (CONTINUED)

ADDR	R/W	Name	Function	Default
413Eh	R/W	DETACH_TIMER_B_LSB	Billboard Detach Timer B LSB	07h
413Fh	R/W	DETACH_TIMER_B_MSB	Billboard Detach Timer B MSB	D0h
4142h	R/W	BB_PF_PIN	Billboard Device Enable Pin Control Select	00h
414Eh	R/W	OTP_LOCK	OTP Lock Register	00h
416Ah	R/W	PRTPWR1_USB3_SPLIT	Port Split PRTPWR1_USB3_SPLIT Control Select	00h
416Bh	R/W	PRTPWR2_USB3_SPLIT	Port Split PRTPWR2_USB3_SPLIT Control Select	00h
416Ch	R/W	PRTPWR3_USB3_SPLIT	Port Split PRTPWR3_USB3_SPLIT Control Select	00h
416Dh	R/W	PRTPWR4_USB3_SPLIT	Port Split PRTPWR4_USB3_SPLIT Control Select	00h
416Eh	R/W	PRTPWR5_USB3_SPLIT	Port Split PRTPWR5_USB3_SPLIT Control Select	00h
416Fh	R/W	PRTPWR6_USB3_SPLIT	Port Split PRTPWR6_USB3_SPLIT Control Select	00h
4170h	R/W	PRTPWR7_USB3_SPLIT	Port Split PRTPWR7_USB3_SPLIT Control Select	00h
4171h	R/W	USB3_PORT_SPLIT_TIME-OUT	USB3 Port Split Link Timeout	05h
4175h	R/W	BC_CDP2SDP_DIS_TIME	Battery Charging CDP TO SDP VBUS Discharge Time Register	00h
4176h	R/W	USB3_PORT_SPLIT_TOG-GLE_TIME	USB3 Port Split Toggle Time	23h
4178h	R/W	BC_CFG_P1	Battery Charging Port 1 Configuration	**Note 10**
4179h	R/W	BC_CFG_P2	Battery Charging Port 2 Configuration	**Note 10**
417Ah	R/W	BC_CFG_P3	Battery Charging Port 3 Configuration	**Note 10**
417Bh	R/W	BC_CFG_P4	Battery Charging Port 4 Configuration	**Note 10**
417Ch	R/W	BC_CFG_P5	Battery Charging Port 5 Configuration	**Note 10**
417Dh	R/W	BC_CFG_P6	Battery Charging Port 6 Configuration	**Note 10**
417Eh	R/W	BC_CFG_P7	Battery Charging Port 7 Configuration	**Note 10**
42D0h	R/W	UDC_BCD_USB_LSB	Hub Feature Controller BCD USB LSB Register	01h
42D1h	R/W	HFC_BCD_USB_MSB	Hub Feature Controller BCD USB MSB Register	02h
42D6h	R/W	HFC_VID_MSB	Hub Feature Controller Vendor ID LSB	24h

Note 1: See *Microchip AN1997 USB to GPIO Bridging with Microchip USB 3.1 Gen 1 Hubs* for details on how to configure the hub for GPIO control.

2: The Vendor ID LSB and MSB must be assigned the same value for both the USB 2.0 Hub and USB 3.0 Hub registers. Failure to correctly modify these registers may result in unpredictable behavior.

3: The default value of the PID registers are dependent on part number. USB5806 = 0x2806, USB5807 = 0x2807, USB5816 = 0x2816, USB5826 = 0x2826, USB5906 = 0x2906, USB5916 = 0x2916, USB5926 = 0x2926.

4: The default value of this register will vary dependent on the device firmware and silicon revision.

5: The default value of this register is dependent on part number. USB5807 = 0x20, USB5806/USB5816/ USB5826/USB5906/USB5916/USB5917 = 0x28.

6: The default value of this register is dependent on part number. USB5807 = 0x00, USB5806/USB5816/ USB5826/USB5906/USB5916/USB5917 = 0x20.

7: The Non-Removable Device settings must be assigned the same value for both the USB 2.0 Hub and USB 3.0 Hub registers. Failure to correctly modify these registers may result in unpredictable behavior.

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10: Depends on device state of operation or hardware strap selection options.

11: Modified by device strap settings.

TABLE 1: CONFIGURATION REGISTER MEMORY MAP (CONTINUED)

ADDR	R/W	Name	Function	Default
42D7h	R/W	HFC_VID_MSB	Hub Feature Controller Vendor ID MSB	04h
42D8h	R/W	HFC_PID_MSB	Hub Feature Controller Product ID LSB	**Note 9**
42D9h	R/W	HFC_PID_MSB	Hub Feature Controller Product ID MSB	**Note 9**
42DAh	R/W	HFC_DID_MSB	Hub Feature Controller Device ID LSB	**Note 4**
42DBh	R/W	HFC_DID_MSB	Hub Feature Controller Device ID MSB	**Note 4**
4442h	R/W	USB3_BCD_USB_LSB	USB 3.0 Hub BCD USB LSB Register	02h
4443h	R/W	USB3_BCD_USB_MSB	USB 3.0 Hub BCD USB MSB Register	03h
4448h	R/W	USB3_VID_LSB	USB 3.0 Hub Vendor ID LSB **(Note 2)**	24h
4449h	R/W	USB3_VID_MSB	USB 3.0 Hub Vendor ID MSB **(Note 2)**	04h
444Ah	R/W	USB3_PID_LSB	USB 3.0 Hub Product ID LSB	**Note 9**
444Bh	R/W	USB3_PID_MSB	USB 3.0 Hub Product ID MSB	**Note 9**
444Ch	R/W	USB3_DID_LSB	USB 3.0 Hub Device ID LSB	**Note 4**
444Dh	R/W	USB3_DID_MSB	USB 3.0 Hub Device ID MSB	**Note 4**
44A2h	R/W	USB3_NBR_PRTS	USB 3.0 Number of Ports **(Note 8)**	**Note 4**/ **Note 10**
44A3h	R/W	USB3_COMPOUND	USB 3.0 Hub Compound Device **(Note 7)**	**Note 4**/ **Note 10**
44A5h	R/W	USB3_BPWRON2PWR-GOOD	USB 3.0 Hub Power On-to-Power Good Descriptor	FFh
44AAh	R/W	USB3_NRD	USB 3.0 Hub Non-Removable Device **(Note 7)**	**Note 11**
6086h	R/W	SS_P0_AFE_TEST_IN4	USB3 Port 0 TX Pre-Driver	00h
60C8h	R/W	UP_RISE_FALL_ADJ	USB 2.0 Upstream Rise-and-Fall Adjustment Register	00h
60CAh	R/W	HS_UP_BOOST	USB 2.0 Upstream PHYBoost Register	00h
60CCh	R/W	HS_UP_SENSE	USB 2.0 Upstream Varisense Register	00h

Note 1: See *Microchip AN1997 USB to GPIO Bridging with Microchip USB 3.1 Gen 1 Hubs* for details on how to configure the hub for GPIO control.

2: The Vendor ID LSB and MSB must be assigned the same value for both the USB 2.0 Hub and USB 3.0 Hub registers. Failure to correctly modify these registers may result in unpredictable behavior.

3: The default value of the PID registers are dependent on part number. USB5806 = 0x2806, USB5807 = 0x2807, USB5816 = 0x2816, USB5826 = 0x2826, USB5906 = 0x2906, USB5916 = 0x2916, USB5926 = 0x2926.

4: The default value of this register will vary dependent on the device firmware and silicon revision.

5: The default value of this register is dependent on part number. USB5807 = 0x20, USB5806/USB5816/USB5826/USB5906/USB5916/USB5917 = 0x28.

6: The default value of this register is dependent on part number. USB5807 = 0x00, USB5806/USB5816/USB5826/USB5906/USB5916/USB5917 = 0x20.

7: The Non-Removable Device settings must be assigned the same value for both the USB 2.0 Hub and USB 3.0 Hub registers. Failure to correctly modify these registers may result in unpredictable behavior.

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9: The default value of the PID registers are dependent on part number. USB5806 = 0x5806, USB5807 = 0x5807, USB5816 = 0x5816, USB5826 = 0x5826, USB5906 = 0x5906, USB5916 = 0x5916, USB5926 = 0x5926.

10: Depends on device state of operation or hardware strap selection options.

11: Modified by device strap settings.

TABLE 1: CONFIGURATION REGISTER MEMORY MAP (CONTINUED)

ADDR	R/W	Name	Function	Default
61C0h	R	SS_P0_LTSSM_STATE	USB3 Upstream LTSSM State	**Note 10**
61C1h	R/W	SS_P0_TEST_PIPE_DC	USB3 Upstream DC Test Register	00h
61C3h	R/W	SS_P0_TEST_PIPE_TX-_PAT	USB3 Upstream TX Test Pattern Register	00h
61D0h	R/W	SS_P0_TEST_PIPE_PIPE_CTL_0	USB3 Upstream TX_MARGIN	00h
6486h	R/W	SS_P1_AFE_TEST_IN4	USB3 Port 1 TX Pre-Driver	00h
64C8h	R/W	P1_RISE_FALL_ADJ	USB 2.0 Downstream Port 1 Rise-and-Fall Adjustment Register	00h
64CAh	R/W	HS_P1_BOOST	USB 2.0 Downstream Port 1 PHYBoost Register	00h
64CCh	R/W	HS_P1_SENSE	USB 2.0 Downstream Port 1 Varisense Register	00h
65C0h	R	SS_P1_LTSSM_STATE	USB3 Port 1 LTSSM State	**Note 10**
65C1h	R/W	SS_P1_TEST_PIPE_DC	USB3 Port 1 DC Test Register	00h
65C3h	R/W	SS_P1_TEST_PIPE_TX-_PAT	USB3 Port 1 TX Test Pattern Register	00h
65D0h	R/W	SS_P1_TEST_PIPE_PIPE_CTL_0	USB3 Port 1 TX_MARGIN	00h
6886h	R/W	SS_P2_AFE_TEST_IN4	USB3 Port 2 TX Pre-Driver	00h
68C8h	R/W	P2_RISE_FALL_ADJ	USB 2.0 Downstream Port 2 Rise-and-Fall Adjustment Register	00h
68CAh	R/W	HS_P2_BOOST	USB 2.0 Downstream Port 2 PHYBoost Register	00h
68CCh	R/W	HS_P2_SENSE	USB 2.0 Downstream Port 2 Varisense Register	00h
69C0h	R	SS_P2_LTSSM_STATE	USB3 Port 2 LTSSM State	**Note 10**
69C1h	R/W	SS_P2_TEST_PIPE_DC	USB3 Port 2 DC Test Register	00h
69C3h	R/W	SS_P2_TEST_PIPE_TX-_PAT	USB3 Port 2 TX Test Pattern Register	00h
69D0h	R/W	SS_P2_TEST_PIPE_PIPE_CTL_0	USB3 Port 2 TX_MARGIN	00h

Note 1: See *Microchip AN1997 USB to GPIO Bridging with Microchip USB 3.1 Gen 1 Hubs* for details on how to configure the hub for GPIO control.

2: The Vendor ID LSB and MSB must be assigned the same value for both the USB 2.0 Hub and USB 3.0 Hub registers. Failure to correctly modify these registers may result in unpredictable behavior.

3: The default value of the PID registers are dependent on part number. USB5806 = 0x2806, USB5807 = 0x2807, USB5816 = 0x2816, USB5826 = 0x2826, USB5906 = 0x2906, USB5916 = 0x2916, USB5926 = 0x2926.

4: The default value of this register will vary dependent on the device firmware and silicon revision.

5: The default value of this register is dependent on part number. USB5807 = 0x20, USB5806/USB5816/USB5826/USB5906/USB5916/USB5917 = 0x28.

6: The default value of this register is dependent on part number. USB5807 = 0x00, USB5806/USB5816/USB5826/USB5906/USB5916/USB5917 = 0x20.

7: The Non-Removable Device settings must be assigned the same value for both the USB 2.0 Hub and USB 3.0 Hub registers. Failure to correctly modify these registers may result in unpredictable behavior.

8: The Port Disable/Remap settings must be assigned the same value for both the USB 2.0 Hub and USB 3.0 Hub registers. Failure to correctly modify these registers may result in unpredictable behavior.

9: The default value of the PID registers are dependent on part number. USB5806 = 0x5806, USB5807 = 0x5807, USB5816 = 0x5816, USB5826 = 0x5826, USB5906 = 0x5906, USB5916 = 0x5916, USB5926 = 0x5926.

10: Depends on device state of operation or hardware strap selection options.

11: Modified by device strap settings.

TABLE 1: CONFIGURATION REGISTER MEMORY MAP (CONTINUED)

ADDR	R/W	Name	Function	Default
6C86h	R/W	SS_P3_AFE_TEST_IN4	USB3 Port 3 TX Pre-Driver	00h
6CC8h	R/W	P3_RISE_FALL_ADJ	USB 2.0 Downstream Port 3 Rise-and-Fall Adjustment Register	00h
6CCAh	R/W	HS_P3_BOOST	USB 2.0 Downstream Port 3 PHYBoost Register	00h
6CCCh	R/W	HS_P3_SENSE	USB 2.0 Downstream Port 3 Varisense Register	00h
6DC0h	R	SS_P3_LTSSM_STATE	USB3 Port 3 LTSSM State	**Note 10**
6DC1h	R/W	SS_P3_TEST_PIPE_DC	USB3 Port 3 DC Test Register	00h
6DC3h	R/W	SS_P3_TEST_PIPE_TX_PAT	USB3 Port 3 TX Test Pattern Register	00h
6DD0h	R/W	SS_P3_TEST_PIPE_PIPE_CTL_0	USB3 Port 3 TX_MARGIN	00h
7086h	R/W	SS_P4_AFE_TEST_IN4	USB3 Port 4 TX Pre-Driver	00h
70C8h	R/W	P4_RISE_FALL_ADJ	USB 2.0 Downstream Port 4 Rise-and-Fall Adjustment Register	00h
70CAh	R/W	HS_P4_BOOST	USB 2.0 Downstream Port 4 PHYBoost Register	00h
70CCh	R/W	HS_P4_SENSE	USB 2.0 Downstream Port 4 Varisense Register	00h
71C0h	R	SS_P4_LTSSM_STATE	USB3 Port 4 LTSSM State	**Note 10**
71C1h	R/W	SS_P4_TEST_PIPE_DC	USB3 Port 4 DC Test Register	00h
71C3h	R/W	SS_P4_TEST_PIPE_TX_PAT	USB3 Port 4 TX Test Pattern Register	00h
71D0h	R/W	SS_P4_TEST_PIPE_PIPE_CTL_0	USB3 Port 4 TX_MARGIN	00h
7486h	R/W	SS_P5_AFE_TEST_IN4	USB3 Port 5 TX Pre-Driver	00h
74C8h	R/W	P5_RISE_FALL_ADJ	USB 2.0 Downstream Port 5 Rise-and-Fall Adjustment Register	00h
74CAh	R/W	HS_P5_BOOST	USB 2.0 Downstream Port 5 PHYBoost Register	00h
74CCh	R/W	HS_P5_SENSE	USB 2.0 Downstream Port 5 Varisense Register	00h
75C0h	R	SS_P5_LTSSM_STATE	USB3 Port 5 LTSSM State	**Note 10**

Note 1: See *Microchip AN1997 USB to GPIO Bridging with Microchip USB 3.1 Gen 1 Hubs* for details on how to configure the hub for GPIO control.

2: The Vendor ID LSB and MSB must be assigned the same value for both the USB 2.0 Hub and USB 3.0 Hub registers. Failure to correctly modify these registers may result in unpredictable behavior.

3: The default value of the PID registers are dependent on part number. USB5806 = 0x2806, USB5807 = 0x2807, USB5816 = 0x2816, USB5826 = 0x2826, USB5906 = 0x2906, USB5916 = 0x2916, USB5926 = 0x2926.

4: The default value of this register will vary dependent on the device firmware and silicon revision.

5: The default value of this register is dependent on part number. USB5807 = 0x20, USB5806/USB5816/USB5826/USB5906/USB5916/USB5917 = 0x28.

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10: Depends on device state of operation or hardware strap selection options.

11: Modified by device strap settings.

TABLE 1: CONFIGURATION REGISTER MEMORY MAP (CONTINUED)

ADDR	R/W	Name	Function	Default
75C1h	R/W	SS_P5_TEST_PIPE_DC	USB3 Port 5 DC Test Register	00h
75C3h	R/W	SS_P5_TEST_PIPE_TX-_PAT	USB3 Port 5 TX Test Pattern Register	00h
75D0h	R/W	SS_P5_TEST_PIPE_PIPE_CTL_0	USB3 Port 5 TX_MARGIN	00h
7886h	R/W	SS_P6_AFE_TEST_IN4	USB3 Port 6 TX Pre-Driver	00h
78C8h	R/W	P6_RISE_FALL_ADJ	USB 2.0 Downstream Port 6 Rise-and-Fall Adjustment Register	00h
78CAh	R/W	HS_P6_BOOST	USB 2.0 Downstream Port 6 PHYBoost Register	00h
78CCh	R/W	HS_P6_SENSE	USB 2.0 Downstream Port 6 Varisense Register	00h
79C0h	R	SS_P6_LTSSM_STATE	USB3 Port 6 LTSSM State	**Note 10**
79C1h	R/W	SS_P6_TEST_PIPE_DC	USB3 Port 6 DC Test Register	00h
79C3h	R/W	SS_P6_TEST_PIPE_TX-_PAT	USB3 Port 6 TX Test Pattern Register	00h
79D0h	R/W	SS_P6_TEST_PIPE_PIPE_CTL_0	USB3 Port 6 TX_MARGIN	00h
7C86h	R/W	SS_P7_AFE_TEST_IN4	USB3 Port 7 TX Pre-Driver	00h
7CC8h	R/W	P7_RISE_FALL_ADJ	USB 2.0 Downstream Port 7 Rise-and-Fall Adjustment Register	00h
7CCAh	R/W	HS_P7_BOOST	USB 2.0 Downstream Port 7 PHYBoost Register	00h
7CCCh	R/W	HS_P7_SENSE	USB 2.0 Downstream Port 7 Varisense Register	00h
7DC0h	R	SS_P7_LTSSM_STATE	USB3 Port 7 LTSSM State	**Note 10**
7DC1h	R/W	SS_P7_TEST_PIPE_DC	USB3 Port 7 DC Test Register	00h
7DC3h	R/W	SS_P7_TEST_PIPE_TX-_PAT	USB3 Port 7 TX Test Pattern Register	00h
7DD0h	R/W	SS_P7_TEST_PIPE_PIPE_CTL_0	USB3 Port 7 TX_MARGIN	00h

Note 1: See *Microchip AN1997 USB to GPIO Bridging with Microchip USB 3.1 Gen 1 Hubs* for details on how to configure the hub for GPIO control.

2: The Vendor ID LSB and MSB must be assigned the same value for both the USB 2.0 Hub and USB 3.0 Hub registers. Failure to correctly modify these registers may result in unpredictable behavior.

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4: The default value of this register will vary dependent on the device firmware and silicon revision.

5: The default value of this register is dependent on part number. USB5807 = 0x20, USB5806/USB5816/USB5826/USB5906/USB5916/USB5917 = 0x28.

6: The default value of this register is dependent on part number. USB5807 = 0x00, USB5806/USB5816/USB5826/USB5906/USB5916/USB5917 = 0x20.

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10: Depends on device state of operation or hardware strap selection options.

11: Modified by device strap settings.

2.1 Register Definitions

TABLE 2: DEVICE SILICON REVISION REGISTER

DEV_REV (0800h)			Device Silicon Revision Register Default = Depends on silicon revision of device
BIT	**Name**	**R/W**	**Description**
7:0	REV	R	Silicon Revision of the device B0 = Revision B0 silicon C0 = Revision C0 silicon

TABLE 3: DEVICE IDENTIFICATION REGISTER

DEV_ID (0801h)			Device Identification Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:0	ID	R/W	Not used. May be used by system integrator to store information.

TABLE 4: MCU CLOCK CONTROL 1

CLOCK_CTL (0804h)			MCU Clock Control Default = Depends on device state of operation
BIT	**Name**	**R/W**	**Description**
7	XTAL_SUSP_DIS	R/W	Crystal suspend disable ‘0’ = Normal Crystal driver operation ‘1’ = Crystal is never suspended Note that when using the I^2C/SMBus Slave interface of the hub, this bit should be set = 1 so that the SMBus Slave interface can remain active while the hub is in the USB Suspend state.
6:5	Reserved	R	Always ‘0’
4	PLL125_EN	R/W	125 MHz PLL Enable Always controlled by firmware. Do not attempt to manually override during runtime.
3	PLL125_STABLE	R	PLL 125 MHz stable ‘1’ = 125 MHz oscillator is stable. ‘0’ = 125 MHz oscillator is not stable.
2	ROSC_EN	R/W	Ring Oscillator Enable. Always controlled by firmware. Do not attempt to manually override during runtime.
1	PLL60_EN	R/W	60 MHz PLL Enable. Always controlled by firmware. Do not attempt to manually override during runtime.

TABLE 5: UTILITY CONFIGURATION REGISTER 1

UTIL_CONFIG1 (080Ah)			Device Identification Register Default = 00h if external FW image through SPI I/F is executing, 04h if no external SPI FW is detected
BIT	**Name**	**R/W**	**Description**
7	Reserved	R	Always ‘0’
6	DEV_RESET	R/W	Setting this bit to “1” resets the hub and sets all of the registers into the default known state as specified in each register. This bit is cleared when the RESET process has completed.
5:3	Reserved	R	Always ‘0’
2	SPI_MASTER_DIS	R/W	After reset the SPI interface is always enabled. If the firmware does not detect a SPI ROM externally, it sets this bit. This disable the SPI interface, and enables PIO4 and PIO5.
1	Reserved	R	Always ‘0’
0	HUB_RESUME_INHIBIT	R/W	Hub Resume Inhibit ‘0’ = Normal resume activity per the USB2.0 specification ‘1’ = Alternate resume behavior

TABLE 6: CLOCK DETECT INDICATOR

CLOCK_DETECT (080Bh)			MCU Clock Control Clock Detect Default = Depends on device state of operation
BIT	**Name**	**R/W**	**Description**
7:1	Reserved	R	Always ‘0’
0	REFCLK_DETECTED	R	External REFCLK detection indicator ‘1’ = External REFCLK detected ‘0’ = External REFCLK NOT detected

TABLE 7: GPIO 16-23 PULL-DOWN REGISTER

GPIO_16_23_PD (082Dh)			GPIO 16-23 Pull-Down Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7	GPIO_23_PD	R/W	Set bit to enable GPIO23 Pull-down resistor.
6	GPIO_22_PD	R/W	Set bit to enable GPIO22 Pull-down resistor.
5	GPIO_21_PD	R/W	Set bit to enable GPIO21 Pull-down resistor.
4	GPIO_20_PD	R/W	Set bit to enable GPIO20 Pull-down resistor.
3	GPIO_19_PD	R/W	Set bit to enable GPIO19 Pull-down resistor.
2	GPIO_18_PD	R/W	Set bit to enable GPIO18 Pull-down resistor.
1	GPIO_17_PD	R/W	Set bit to enable GPIO17 Pull-down resistor.
0	GPIO_16_PD	R/W	Set bit to enable GPIO16 Pull-down resistor.

TABLE 8: GPIO 8-12 PULL-DOWN REGISTER

GPIO_8_12_PD (082Eh)			GPIO 8-12 Pull-Down Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:5	Reserved	R	Reserved
4	GPIO_12_PD	R/W	—
3	Reserved	R	Reserved

TABLE 8: GPIO 8-12 PULL-DOWN REGISTER

GPIO_8_12_PD (082Eh)			GPIO 8-12 Pull-Down Register Default = 00h
BIT	**Name**	**R/W**	**Description**
2	GPIO_10_PD	R/W	Set bit to enable GPIO10 Pull-down resistor.
1	GPIO_9_PD	R/W	Set bit to enable GPIO9 Pull-down resistor.
0	GPIO_8_PD	R/W	Set bit to enable GPIO8 Pull-down resistor.

TABLE 9: GPIO 1-7 PULL-DOWN REGISTER

GPIO_1_7_PD (082Fh)			GPIO 1-7 Pull-Down Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7	GPIO_7_PD	R/W	Set bit to enable GPIO7 Pull-down resistor.
6	GPIO_6_PD	R/W	Set bit to enable GPIO6 Pull-down resistor.
5	GPIO_5_PD	R/W	Set bit to enable GPIO5 Pull-down resistor.
4	GPIO_4_PD	R/W	Set bit to enable GPIO4 Pull-down resistor.
3	GPIO_3_PD	R/W	Set bit to enable GPIO3 Pull-down resistor.
2	GPIO_2_PD	R/W	Set bit to enable GPIO2 Pull-down resistor.
1	GPIO_1_PD	R/W	Set bit to enable GPIO1 Pull-down resistor.
0	Reserved	R	Reserved

TABLE 10: GPIO 16-23 DIRECTION CONTROL REGISTER

GPIO_16_23_DIR (0831h)			GPIO 16-23 Direction Control Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7	GPIO_23_DIR	R/W	Set bit to configure GPIO23 as an output. Clear to set as Input.
6	GPIO_22_DIR	R/W	Set bit to configure GPIO22 as an output. Clear to set as Input.
5	GPIO_21_DIR	R/W	Set bit to configure GPIO21 as an output. Clear to set as Input.
4	GPIO_20_DIR	R/W	Set bit to configure GPIO20 as an output. Clear to set as Input.
3	GPIO_19_DIR	R/W	Set bit to configure GPIO19 as an output. Clear to set as Input.
2	GPIO_18_DIR	R/W	Set bit to configure GPIO18 as an output. Clear to set as Input.
1	GPIO_17_DIR	R/W	Set bit to configure GPIO17 as an output. Clear to set as Input.
0	GPIO_16_DIR	R/W	Set bit to configure GPIO16 as an output. Clear to set as Input.

TABLE 11: GPIO 8-12 DIRECTION CONTROL REGISTER

GPIO_8_12_DIR (0832h)			GPIO 8-12 Direction Control Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:5	Reserved	R	Reserved
4	GPIO_12_DIR	R/W	Set bit to configure GPIO12 as an output. Clear to set as Input.
3	Reserved	R	Reserved
2	GPIO_10_DIR	R/W	Set bit to configure GPIO10 as an output. Clear to set as Input.
1	GPIO_9_DIR	R/W	Set bit to configure GPIO9 as an output. Clear to set as Input.
0	GPIO_8_DIR	R/W	Set bit to configure GPIO8 as an output. Clear to set as Input.

TABLE 12: GPIO 1-7 DIRECTION CONTROL REGISTER

GPIO_1_7_DIR (0833h)			GPIO 1-7 Direction Control Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7	GPIO_7_DIR	R/W	Set bit to configure GPIO7 as an output. Clear to set as Input.
6	GPIO_6_DIR	R/W	Set bit to configure GPIO6 as an output. Clear to set as Input.
5	GPIO_5_DIR	R/W	Set bit to configure GPIO5 as an output. Clear to set as Input.
4	GPIO_4_DIR	R/W	Set bit to configure GPIO4 as an output. Clear to set as Input.
3	GPIO_3_DIR	R/W	Set bit to configure GPIO3 as an output. Clear to set as Input.
2	GPIO_2_DIR	R/W	Set bit to configure GPIO2 as an output. Clear to set as Input.
1	GPIO_1_DIR	R/W	Set bit to configure GPIO1 as an output. Clear to set as Input.
0	Reserved	R	Reserved

TABLE 13: GPIO 16-23 OUTPUT STATE CONTROL REGISTER

GPIO_16_23_OUT (0835h)			GPIO 16-23 Output State Control Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7	GPIO_23_OUT	R/W	Sets the state of GPIO23 when configured as an output
6	GPIO_22_OUT	R/W	Sets the state of GPIO22 when configured as an output
5	GPIO_21_OUT	R/W	Sets the state of GPIO21 when configured as an output
4	GPIO_20_OUT	R/W	Sets the state of GPIO20 when configured as an output
3	GPIO_19_OUT	R/W	Sets the state of GPIO19 when configured as an output
2	GPIO_18_OUT	R/W	Sets the state of GPIO18 when configured as an output
1	GPIO_17_OUT	R/W	Sets the state of GPIO17 when configured as an output
0	GPIO_16_OUT	R/W	Sets the state of GPIO16 when configured as an output

TABLE 14: GPIO 8-12 OUTPUT STATE CONTROL REGISTER

GPIO_8_12_OUT (0836h)			GPIO 8-12 Output State Control Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:5	Reserved	R	Reserved
4	GPIO_12_OUT	R/W	Sets the state of GPIO12 when configured as an output
3	Reserved	R	Reserved
2	GPIO_10_OUT	R/W	Sets the state of GPIO10 when configured as an output
1	GPIO_9_OUT	R/W	Sets the state of GPIO9 when configured as an output
0	GPIO_8_OUT	R/W	Sets the state of GPIO8 when configured as an output

TABLE 15: GPIO 1-7 OUTPUT STATE CONTROL REGISTER

GPIO_1_7_OUT (0837h)			GPIO 1-7 Output State Control Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7	GPIO_7_OUT	R/W	Sets the state of GPIO7 when configured as an output
6	GPIO_6_OUT	R/W	Sets the state of GPIO6 when configured as an output
5	GPIO_5_OUT	R/W	Sets the state of GPIO5 when configured as an output

TABLE 15: GPIO 1-7 OUTPUT STATE CONTROL REGISTER

GPIO_1_7_OUT (0837h)			GPIO 1-7 Output State Control Register Default = 00h
BIT	**Name**	**R/W**	**Description**
4	GPIO_4_OUT	R/W	Sets the state of GPIO4 when configured as an output
3	GPIO_3_OUT	R/W	Sets the state of GPIO3 when configured as an output
2	GPIO_2_OUT	R/W	Sets the state of GPIO2 when configured as an output
1	GPIO_1_OUT	R/W	Sets the state of GPIO1 when configured as an output
0	Reserved	R	Reserved

TABLE 16: GPIO 16-23 INPUT STATE READ REGISTER

GPIO_16_23_IN (0839h)			GPIO 16-23 Input State Read Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7	GPIO_23_IN	R	Reads back the state of GPIO23 when configured as an input
6	GPIO_22_IN	R	Reads back the state of GPIO22 when configured as an input
5	GPIO_21_IN	R	Reads back the state of GPIO21 when configured as an input
4	GPIO_20_IN	R	Reads back the state of GPIO20 when configured as an input
3	GPIO_19_IN	R	Reads back the state of GPIO19 when configured as an input
2	GPIO_18_IN	R	Reads back the state of GPIO18 when configured as an input
1	GPIO_17_IN	R	Reads back the state of GPIO17 when configured as an input
0	GPIO_16_IN	R	Reads back the state of GPIO16 when configured as an input

TABLE 17: GPIO 8-12 INPUT STATE READ REGISTER

GPIO_8_12_IN (083Ah)			GPIO 8-12 Input State Read Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:5	Reserved	R	Reserved
4	GPIO_12_IN	R	Reads back the state of GPIO12 when configured as an input
3	Reserved	R	Reserved
2	GPIO_10_IN	R	Reads back the state of GPIO10 when configured as an input
1	GPIO_9_IN	R	Reads back the state of GPIO9 when configured as an input
0	GPIO_8_IN	R	Reads back the state of GPIO8 when configured as an input

TABLE 18: GPIO 1-7 INPUT STATE READ REGISTER

GPIO_1_7_IN (083Bh)			GPIO 1-7 Input State Read Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7	GPIO_7_IN	R/W	Reads back the state of GPIO7 when configured as an input
6	GPIO_6_IN	R/W	Reads back the state of GPIO6 when configured as an input
5	GPIO_5_IN	R/W	Reads back the state of GPIO5 when configured as an input
4	GPIO_4_IN	R/W	Reads back the state of GPIO4 when configured as an input
3	GPIO_3_IN	R	Reads back the state of GPIO3 when configured as an input
2	GPIO_2_IN	R	Reads back the state of GPIO2 when configured as an input
1	GPIO_1_IN	R	Reads back the state of GPIO1 when configured as an input

TABLE 18: GPIO 1-7 INPUT STATE READ REGISTER (CONTINUED)

GPIO_1_7_IN (083Bh)			GPIO 1-7 Input State Read Register Default = 00h
BIT	**Name**	**R/W**	**Description**
0	Reserved	R	Reserved

TABLE 19: GPIO 16-23 PULL-UP REGISTER

GPIO_16_23_PU (083Dh)			GPIO 16-23 Pull-Up Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7	GPIO_23_PU	R/W	Set bit to enable GPIO23 Pull-up resistor.
6	GPIO_22_PU	R/W	Set bit to enable GPIO22 Pull-up resistor.
5	GPIO_21_PU	R/W	Set bit to enable GPIO21 Pull-up resistor.
4	GPIO_20_PU	R/W	Set bit to enable GPIO20 Pull-up resistor.
3	GPIO_19_PU	R/W	Set bit to enable GPIO19 Pull-up resistor.
2	GPIO_18_PU	R/W	Set bit to enable GPIO18 Pull-up resistor.
1	GPIO_17_PU	R/W	Set bit to enable GPIO17 Pull-up resistor.
0	GPIO_16_PU	R/W	Set bit to enable GPIO16 Pull-up resistor.

TABLE 20: GPIO 8-12 PULL-UP REGISTER

GPIO_8_12_PU (083Eh)			GPIO 8-12 Pull-Up Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:5	Reserved	R	Reserved
4	GPIO_12_PU	R/W	Set bit to enable GPIO12 Pull-up resistor.
3	Reserved	R	Reserved
2	GPIO_10_PU	R/W	Set bit to enable GPIO10 Pull-up resistor.
1	GPIO_9_PU	R/W	Set bit to enable GPIO9 Pull-up resistor.
0	GPIO_8_PU	R/W	Set bit to enable GPIO8 Pull-up resistor.

TABLE 21: GPIO 1-7 PULL-UP REGISTER

GPIO_1_7_PU (083Fh)			GPIO 1-7 Pull-Up Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7	GPIO_7_PU	R/W	Set bit to enable GPIO7 Pull-up resistor.
6	GPIO_6_PU	R/W	Set bit to enable GPIO6 Pull-up resistor.
5	GPIO_5_PU	R/W	Set bit to enable GPIO5 Pull-up resistor.
4	GPIO_4_PU	R/W	Set bit to enable GPIO4 Pull-up resistor.
3	GPIO_3_PU	R/W	Set bit to enable GPIO3 Pull-up resistor.
2	GPIO_2_PU	R/W	Set bit to enable GPIO2 Pull-up resistor.
1	GPIO_1_PU	R/W	Set bit to enable GPIO1 Pull-up resistor.
0	Reserved	R	Reserved

TABLE 22: USB 2.0 OCS STATUS REGISTER

USB2_OCS_STAT (0900h)			USB 2.0 PHYSICAL OCS Status Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7	USB2_OCS_STAT_P7	R	Indicates if the physical USB 2.0 downstream port 7 had an OCS event. The bit stays asserted until it is cleared and the OCS even ceases. 0 = No OCS Condition 1 = OCS Condition
6	USB2_OCS_STAT_P6	R	Indicates if the physical USB 2.0 downstream port 6 had an OCS event. The bit stays asserted until it is cleared and the OCS even ceases. 0 = No OCS Condition 1 = OCS Condition
5	USB2_OCS_STAT_P5	R	Indicates if the physical USB 2.0 downstream port 5 had an OCS event. The bit stays asserted until it is cleared and the OCS even ceases. 0 = No OCS Condition 1 = OCS Condition
4	USB2_OCS_STAT_P4	R	Indicates if the physical USB 2.0 downstream port 4 had an OCS event. The bit stays asserted until it is cleared and the OCS even ceases. 0 = No OCS Condition 1 = OCS Condition
3	USB2_OCS_STAT_P3	R	Indicates if the physical USB 2.0 downstream port 3 had an OCS event. The bit stays asserted until it is cleared and the OCS even ceases. 0 = No OCS Condition 1 = OCS Condition
2	USB2_OCS_STAT_P2	R	Indicates if the physical USB 2.0 downstream port 2 had an OCS event. The bit stays asserted until it is cleared and the OCS even ceases. 0 = No OCS Condition 1 = OCS Condition
1	USB2_OCS_STAT_P1	R	Indicates if the physical USB 2.0 downstream port 1 had an OCS event. The bit stays asserted until it is cleared and the OCS even ceases. 0 = No OCS Condition 1 = OCS Condition
0	Reserved	R	Reserved

TABLE 23: USB 3.0 OCS STATUS REGISTER

USB3_OCS_STAT (0902h)			Physical USB 3.0 OCS Status Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7	USB3_OCS_STAT_P7	R	Indicates if the physical USB 3.0 downstream port 7 had an OCS event. The bit stays asserted until it is cleared and the OCS even ceases. 0 = No OCS Condition 1 = OCS Condition
4	USB3_OCS_STAT_P6	R	Indicates if the physical USB 3.0 downstream port 6 had an OCS event. The bit stays asserted until it is cleared and the OCS even ceases. 0 = No OCS Condition 1 = OCS Condition
4	USB3_OCS_STAT_P5	R	Indicates if the physical USB 3.0 downstream port 5 had an OCS event. The bit stays asserted until it is cleared and the OCS even ceases. 0 = No OCS Condition 1 = OCS Condition
4	USB3_OCS_STAT_P4	R	Indicates if the physical USB 3.0 downstream port 4 had an OCS event. The bit stays asserted until it is cleared and the OCS even ceases. 0 = No OCS Condition 1 = OCS Condition
3	USB3_OCS_STAT_P3	R	Indicates if the physical USB 3.0 downstream port 3 had an OCS event. The bit stays asserted until it is cleared and the OCS even ceases. 0 = No OCS Condition 1 = OCS Condition
2	USB3_OCS_STAT_P2	R	Indicates if the physical USB 3.0 downstream port 2 had an OCS event. The bit stays asserted until it is cleared and the OCS even ceases. 0 = No OCS Condition 1 = OCS Condition
1	USB3_OCS_STAT_P1	R	Indicates if the physical USB 3.0 downstream port 1 had an OCS event. The bit stays asserted until it is cleared and the OCS even ceases. 0 = No OCS Condition 1 = OCS Condition
0	Reserved	R	Reserved

TABLE 24: GPIO 72 PULL-DOWN REGISTER

GPIO_72_PD (096Eh)			GPIO 72 Pull-Down Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:1	Reserved	R	Reserved
0	GPIO_72_PD	R/W	Set bit to enable GPIO72 pull-down resistor.

TABLE 25: GPIO 64-71 PULL-DOWN REGISTER

GPIO_64_71_PD (096Fh)			GPIO 64-71 Pull-Down Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7	GPIO_71_PD	R/W	Set bit to enable GPIO71 pull-down resistor.
6	GPIO_70_PD	R/W	Set bit to enable GPIO70 pull-down resistor.
5	GPIO_69_PD	R/W	Set bit to enable GPIO69 pull-down resistor.
4	GPIO_68_PD	R/W	Set bit to enable GPIO68 pull-down resistor.
3	GPIO_67_PD	R/W	Set bit to enable GPIO67 pull-down resistor.
2	GPIO_66_PD	R/W	Set bit to enable GPIO66 pull-down resistor.
1	GPIO_65_PD	R/W	Set bit to enable GPIO65 pull-down resistor.
0	GPIO_64_PD	R/W	Set bit to enable GPIO64 pull-down resistor.

TABLE 26: GPIO 72 DIRECTION CONTROL REGISTER

GPIO_72_DIR (0972h)			GPIO 72 Direction Control Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:1	Reserved	R	Reserved
0	GPIO_72_DIR	R/W	Set bit to configure GPIO72 as an output. Clear to set as Input.

TABLE 27: GPIO 64-71 DIRECTION CONTROL REGISTER

GPIO_64_71_DIR (0973h)			GPIO 64-71 Direction Control Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7	GPIO_71_DIR	R/W	Set bit to configure GPIO71 as an output. Clear to set as Input.
6	GPIO_70_DIR	R/W	Set bit to configure GPIO70 as an output. Clear to set as Input.
5	GPIO_69_DIR	R/W	Set bit to configure GPIO69 as an output. Clear to set as Input.
4	GPIO_68_DIR	R/W	Set bit to configure GPIO68 as an output. Clear to set as Input.
3	GPIO_67_DIR	R/W	Set bit to configure GPIO67 as an output. Clear to set as Input.
2	GPIO_66_DIR	R/W	Set bit to configure GPIO66 as an output. Clear to set as Input.
1	GPIO_65_DIR	R/W	Set bit to configure GPIO65 as an output. Clear to set as Input.
0	GPIO_64_DIR	R/W	Set bit to configure GPIO64 as an output. Clear to set as Input.

TABLE 28: GPIO 72 OUTPUT STATE CONTROL REGISTER

GPIO_72_OUT (0976h)			GPIO 72 Output State Control Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:1	Reserved	R	Reserved
0	GPIO_72_OUT	R/W	Sets the state of GPIO72 when configured as an output

TABLE 29: GPIO 64-71 OUTPUT STATE CONTROL REGISTER

GPIO_64_71_OUT (0977h)			GPIO 64-71 Output State Control Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7	GPIO_71_OUT	R/W	Sets the state of GPIO71 when configured as an output
6	GPIO_70_OUT	R/W	Sets the state of GPIO70 when configured as an output
5	GPIO_69_OUT	R/W	Sets the state of GPIO69 when configured as an output
4	GPIO_68_OUT	R/W	Sets the state of GPIO68 when configured as an output
3	GPIO_67_OUT	R/W	Sets the state of GPIO67 when configured as an output
2	GPIO_66_OUT	R/W	Sets the state of GPIO66 when configured as an output
1	GPIO_65_OUT	R/W	Sets the state of GPIO65 when configured as an output
0	GPIO_64_OUT	R/W	Sets the state of GPIO64 when configured as an output

TABLE 30: GPIO 72 INPUT STATE READ REGISTER

GPIO_72_IN (097Ah)			GPIO 72 Input State Read Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:1	Reserved	R	Reserved
0	GPIO_72_IN	R	Reads back the state of GPIO72 when configured as an input

TABLE 31: GPIO 64-71 INPUT STATE READ REGISTER

GPIO_64_71_IN (097Bh)			GPIO 64-71 Input State Read Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7	GPIO_71_IN	R	Reads back the state of GPIO71 when configured as an input
6	GPIO_70_IN	R	Reads back the state of GPIO70 when configured as an input
5	GPIO_69_IN	R	Reads back the state of GPIO69 when configured as an input
4	GPIO_68_IN	R	Reads back the state of GPIO68 when configured as an input
3	GPIO_67_IN	R	Reads back the state of GPIO67 when configured as an input
2	GPIO_66_IN	R	Reads back the state of GPIO66 when configured as an input
1	GPIO_65_IN	R	Reads back the state of GPIO65 when configured as an input
0	GPIO_64_IN	R	Reads back the state of GPIO64 when configured as an input

TABLE 32: GPIO 72 PULL-UP REGISTER

GPIO_72_PU (097Eh)			GPIO 72 Pull-Up Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:1	Reserved	R	Reserved
0	GPIO_72_PU	R/W	Set bit to enable GPIO72 pull-up resistor.

TABLE 33: GPIO 64-71 PULL-UP REGISTER

GPIO_64_71_PU (097Fh)			GPIO 64-71 Pull-up Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7	GPIO_71_PU	R/W	Set bit to enable GPIO71 pull-up resistor.
6	GPIO_70_PU	R/W	Set bit to enable GPIO70 pull-up resistor.
5	GPIO_69_PU	R/W	Set bit to enable GPIO69 pull-up resistor.
4	GPIO_68_PU	R/W	Set bit to enable GPIO68 pull-up resistor.
3	GPIO_67_PU	R/W	Set bit to enable GPIO67 pull-up resistor.
2	GPIO_66_PU	R/W	Set bit to enable GPIO66 pull-up resistor.
1	GPIO_65_PU	R/W	Set bit to enable GPIO65 pull-up resistor.
0	GPIO_64_PU	R/W	Set bit to enable GPIO64 pull-up resistor.

TABLE 34: PROGRAMMABLE FUNCTION PIN 0 CONTROL REGISTER

PF0_CTL (0A10h)			Programmable Function Pin 0 Control Default = 00h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	SELECT	R/W	000 = GPIO64 001 – 111 = Reserved

TABLE 35: PROGRAMMABLE FUNCTION PIN 1 CONTROL REGISTER

PF1_CTL (0A11h)			Programmable Function Pin 1 Control Default = 00h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	SELECT	R/W	000 = GPIO1 001 – 111 = Reserved

TABLE 36: PROGRAMMABLE FUNCTION PIN 2 CONTROL REGISTER

PF2_CTL (0A12h)			Programmable Function Pin 2 Control Default = 00h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	SELECT	R/W	000 = GPIO2 001 – 111 = Reserved

TABLE 37: PROGRAMMABLE FUNCTION PIN 3 CONTROL REGISTER

PF3_CTL (0A13h)			Programmable Function Pin 3 Control Default = 00h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	SELECT	R/W	000 = GPIO3 001 – 111 = Reserved

TABLE 38: PROGRAMMABLE FUNCTION PIN 4 CONTROL REGISTER

PF4_CTL (0A14h)			Programmable Function Pin 4 Control Default = 00h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	SELECT	R/W	000 = GPIO65 001 = CLOCK_OUT– A buffered version of the XTAL clock driven out. For test/debug purposes only. 011 – 111 = Reserved

TABLE 39: PROGRAMMABLE FUNCTION PIN 5 CONTROL REGISTER

PF5_CTL (0A15h)			Programmable Function Pin 5 Control Default = 00h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	SELECT	R/W	000 = GPIO66 001 – 111 = Reserved

TABLE 40: PROGRAMMABLE FUNCTION PIN 6 CONTROL REGISTER

PF6_CTL (0A16h)			Programmable Function Pin 6 Control Default = 00h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	SELECT	R/W	000 = GPIO67 001 = Reserved 010 = Reserved 011 = Spare I^2C Data - Additional I^2C master. Requires custom FW for use. 001 – 111 = Reserved

TABLE 41: PROGRAMMABLE FUNCTION PIN 7 CONTROL REGISTER

PF7_CTL (0A17h)			Programmable Function Pin 7 Control Default = 02h for USB5807, 00h for all others
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	SELECT	R/W	000 = GPIO23 001 = Reserved 010 = PRT_CTL7 (for USB5807 devices only) 011 = Spare I2C Alert - Additional I^2C master. Requires custom FW for use. 100 – 111 = Reserved

TABLE 42: PROGRAMMABLE FUNCTION PIN 8 CONTROL REGISTER

PF8_CTL (0A18h)			Programmable Function Pin 8 Control Default = 02h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	SELECT	R/W	000 = GPIO8 001 = Reserved 010 = SMBCLK - USB-to-I^{2}C Bridge Clock 011 – 111 = Reserved

TABLE 43: PROGRAMMABLE FUNCTION PIN 9 CONTROL REGISTER

PF9_CTL (0A19h)			Programmable Function Pin 9 Control Default = 00h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	SELECT	R/W	000 – 111 = Reserved

TABLE 44: PROGRAMMABLE FUNCTION PIN 10 CONTROL REGISTER

PF10_CTL (0A1Ah)			Programmable Function Pin 10 Control Default = 03h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	SELECT	R/W	000 = GPIO68 001 = USB3_SUSP_IND – USB 3 hub Suspend state indicator 010 = USB2_SUSP_IND – USB 2 hub Suspend state indicator 011 = Logical OR of USB3_SUSP_IND and USB2_SUSP_IND 100 – 111 = Reserved Note that suspend indicators will assert to ‘1’ when suspended. A ‘0’ indicates that the hub is not in a Suspended state.

TABLE 45: PROGRAMMABLE FUNCTION PIN 11 CONTROL REGISTER

PF11_CTL (0A1Bh)			Programmable Function Pin 11 Control Default = 02h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	SELECT	R/W	000 = GPIO6 001 = Reserved 010 = SMBDATA – USB-to-I^{2}C Bridge Data 011 – 111 = Reserved

TABLE 46: PROGRAMMABLE FUNCTION PIN 12 CONTROL REGISTER

PF12_CTL (0A1Ch)			Programmable Function Pin 12 Control Default = 00h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’

TABLE 46: PROGRAMMABLE FUNCTION PIN 12 CONTROL REGISTER (CONTINUED)

PF12_CTL (0A1Ch)			Programmable Function Pin 12 Control Default = 00h
BIT	**Name**	**R/W**	**Description**
3:0	SELECT	R/W	000 = GPIO69 001 = Reserved 010 = Reserved 011 = Spare I2C Clock – Additional I^2C master. Requires custom FW for use. 100 – 111 = Reserved

TABLE 47: PROGRAMMABLE FUNCTION PIN 13 CONTROL REGISTER

PF13_CTL (0A1Dh)			Programmable Function Pin 13 Control Default = 00h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	SELECT	R/W	000 = GPIO70 001 – 111 = Reserved

TABLE 48: PROGRAMMABLE FUNCTION PIN 14 CONTROL REGISTER

PF14_CTL (0A1Eh)			Programmable Function Pin 14 Control Default = 00h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	SELECT	R/W	000 = GPIO71 001 – 111 = Reserved

TABLE 49: PROGRAMMABLE FUNCTION PIN 15 CONTROL REGISTER

PF15_CTL (0A1Fh)			Programmable Function Pin 15 Control Default = 00h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	SELECT	R/W	000 = GPIO5 001 – 111 = Reserved

TABLE 50: PROGRAMMABLE FUNCTION PIN 16 CONTROL REGISTER

PF16_CTL (0A20h)			Programmable Function Pin 16 Control Default = 00h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	SELECT	R/W	000 = GPIO4 001 – 111 = Reserved

TABLE 51: USB 2.0 HUB VENDOR ID LSB

USB2_VIDL (3000h)			USB 2.0 Hub Vendor ID LSB Default = 24h
BIT	**Name**	**R/W**	**Description**
7:0	VID_LSB	R/W	Least Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB Interface Forum). If this register is modified, the contents of the USB 3.0 Hub Vendor ID LSB register should also be identically modified.

TABLE 52: USB 2.0 HUB VENDOR ID MSB

USB2_VIDM (3001h)			USB 2.0 Hub Vendor ID MSB Default = 04h
BIT	**Name**	**R/W**	**Description**
7:0	VID_MSB	R/W	Most Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB Interface Forum). If this register is modified, the contents of the USB 3.0 Hub Vendor ID MSB register should also be identically modified.

TABLE 53: USB 2.0 HUB PRODUCT ID LSB

USB2_PIDL (3002h)			USB 2.0 Hub Product ID LSB Default = 07h for USB5807, 06h for USB5806/USB5906, 16h for USB5816/USB5916, 26h for USB5826/USB5926
BIT	**Name**	**R/W**	**Description**
7:0	PID_LSB	R/W	Least Significant Byte of the Product ID. This is a 16-bit value that the Vendor can assign to uniquely identify this particular product (assigned by OEM). Note that when ports are disabled on USB58xx/USB59xx hubs via port disable strapping option, the PID LSB value is decrease by 1 for each disabled port. Example: A USB5806 device with two ports disabled by strap will enumerate with a PID = 2804h

TABLE 54: USB 2.0 HUB PRODUCT ID MSB

USB2_PIDM (3003h)			USB 2.0 Hub Product ID MSB Default = 28h for USB5807/USB5806/USB5816/USB5826, 29h for USB5907/USB5906/USB5916/USB5926
BIT	**Name**	**R/W**	**Description**
7:0	PID_MSB	R/W	Most Significant Byte of the Product ID. This is a 16-bit value that the Vendor can assign to uniquely identify this particular product (assigned by OEM).

TABLE 55: USB 2.0 HUB DEVICE ID LSB

USB2_DIDL (3004h)			USB 2.0 Hub Device ID LSB Default = varies depending device variant and silicon revision
BIT	**Name**	**R/W**	**Description**
7:0	DID_LSB	R/W	Least Significant Byte of the Device ID. This is a 16-bit device release number in BCD format (assigned by OEM).

TABLE 56: USB 2.0 HUB DEVICE ID MSB

USB2_DIDM (3005h)			USB 2.0 Hub Product ID MSB Default = varies depending device variant and silicon revision
BIT	**Name**	**R/W**	**Description**
7:0	DID_MSB	R/W	Most Significant Byte of the Device ID. This is a 16-bit device release number in BCD format (assigned by OEM).

TABLE 57: USB 2.0 HUB CONFIGURATION 1

HUB_CFG_1 (3006h)			USB 2.0 Hub Configuration 1 Default = 9Bh
BIT	**Name**	**R/W**	**Description**
7	SELF_BUS_PWR	R/W	Self-powered or Bus-powered: Selects between self-powered and bus-powered operations. The Hub is either Self-Powered (draws less than 2 mA of upstream bus power) or bus-powered (limited to a 100 mA maximum of upstream power prior to being configured by the host controller). When configured as a bus-powered device, the Microchip hub consumes less than 100 mA of current prior to being configured. After configuration, the bus-powered Microchip hub (along with all associated hub circuitry, any embedded devices if part of a compound device, and 100 mA per externally available downstream port) must consume no more than 500 mA of upstream VBUS current. The current consumption is system dependent, and the OEM must ensure that the USB2.0 specifications are not violated. When configured as a self-powered device, <1 mA of upstream VBUS current is consumed and all ports are available, with each port being capable of sourcing 500 mA of current. ‘0’ = Bus-powered operation ‘1’ = Self-powered operation
6	VSM_DISABLE	R/W	‘0’ = VSM Messaging is supported. ‘1’ = VSM Messaging is disabled. When VSM is disabled, all vendor-specific messaging to the hub endpoint will be ignored with no ill effect.
5	HS_DISABLE	R/W	High-Speed Disable: Disables the capability to attach as either a High-Speed or Full-Speed device, and forces attachment as Full-Speed only (i.e. no High-Speed support). ‘0’ = High-Speed or Full-Speed ‘1’ = Full-Speed-Only (High-Speed disabled)

TABLE 57: USB 2.0 HUB CONFIGURATION 1 (CONTINUED)

HUB_CFG_1 (3006h)			USB 2.0 Hub Configuration 1 Default = 9Bh
BIT	**Name**	**R/W**	**Description**
4	MTT_ENABLE	R/W	Multi-TT enable: Enables one transaction translator per port operation. Selects between a mode where only one transaction translator is available for all ports (Single-TT), or each port gets a dedicated transaction translator (Multi-TT). **Note:** The host may force Single-TT mode only. '0' = single TT for all ports. '1' = one TT per port (multiple TT's supported)
3	EOP_DISABLE	R/W	EOP Disable: Disables EOP generation of EOF1 when in Full-Speed mode. During FS operation only, this permits the Hub to send EOP if no downstream traffic is detected at EOF1. See *Section 11.3.1 of the USB 2.0 Specification* for additional details. Note that generation of an EOP at the EOF1 point may prevent a Host controller (operating in FS mode) from placing the USB bus in Suspended state. '0' = An EOP is generated at the EOF1 point if no traffic is detected. '1' = EOP generation at EOF1 is disabled (Note: this is normal USB operation.) Note that this is a rarely used feature in the PC environment, existing drivers may not have been thoroughly debugged with this feature enabled. It is included because it is a permitted feature in Chapter 11 of the USB specification.
2:1	CURRENT_SNS	R/W	Over Current Sense: Selects current sensing on a port-by-port basis, all ports ganged, or none (only for bus-powered hubs). The ability to support current sensing on a port or ganged basis is hardware implementation dependent. 00 = Ganged sensing (all ports together). 01 = Individual port-by-port 1x = Over current sensing not supported (must only be used with bus-powered configurations)
0	PORT_PWR	R/W	Port Power Switching: Enables power switching on all ports simultaneously (ganged), or port power is individually switched on and off on a port-by-port basis (individual). The ability to support power enabling on a port or ganged basis is hardware implementation dependent. '0' = Ganged switching (all ports together) '1' = Individual port-by-port switching

TABLE 58: USB 2.0 HUB CONFIGURATION 2

HUB_CFG_2 (3007h)			USB 2.0 Hub Configuration 2 Default = 20h for USB5807, 28h for USB5806/USB5816/USB5826/USB5906/USB5916/USB5926
BIT	**Name**	**R/W**	**Description**
7	Reserved	R	Reserved
6	Reserved	R	Reserved

TABLE 58: USB 2.0 HUB CONFIGURATION 2 (CONTINUED)

HUB_CFG_2 (3007h)			USB 2.0 Hub Configuration 2 Default = 20h for USB5807, 28h for USB5806/USB5816/USB5826/USB5906/USB5916/USB5926
BIT	**Name**	**R/W**	**Description**
5:4	OC_TIMER	R/W	Overcurrent Timer delay. This measures the minimum pulse width for which a pulse is considered valid. 00 = 3 Clock samples 01 = 6 Clock samples 10 = 12 Clock Samples 11 = 24 Clock Samples
3	COMPOUND	R/W	Compound Device: Allows the OEM to indicate that the Hub is part of a compound device. (See *USB Specification* for definition.) The applicable port(s) must also be defined as having a “Non-Removable Device”. Note that when configured via strapping options, declaring a port as non-removable automatically causes the hub controller to report that it is part of a compound device. ‘0’ = No ‘1’ = Yes. Hub is part of a compound device. If this register is modified, the USB 3.0 hub equivalent must also be modified in the register.
2:0	Reserved	R	Reserved

TABLE 59: USB 2.0 HUB CONFIGURATION 3

HUB_CFG_3 (3008h)			USB 2.0 Hub Configuration 3 Default = 09h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3	PRTMAP_EN	R/W	Port Re-Mapping enable: Selects the method used by the hub to assign port numbers and disable ports. ‘0’ = Standard Mode. Ports are numbered as defined in the data sheet. If a port is disabled, higher numbered ports are re-numbered in order to maintain contiguous port numbering. ‘1’ = Port Re-Map mode. This mode enables remapping via port remapping registers.
2	BOS_DISABLE	R/W	0 = BOS Descriptor Enabled. BOS commands processed by hardware. 1 = BOS Descriptor Enabled. BOS commands return STALL response.
1	Reserved	R	Reserved
0	STRING_EN		Enables String Descriptor Support ‘0’ = String Support Disabled ‘1’ = String Support Enabled

TABLE 60: USB 2.0 HUB NON-REMOVABLE DEVICE

USB2_NRD (3009h)			USB 2.0 Hub Non-Removable Device Default = depends on non-removable port strap setting
BIT	**Name**	**R/W**	**Description**
7:0	NR_DEVICE	R/W	Non-Removable Device: Indicates which port(s) include non-removable devices. '0' = port is removable, '1' = port is non- removable. This register informs the Host if one of the active ports has a permanent device that is undetachable from the Hub. The ports may also be configured as non-removable using the hardware strapping option described in the respective hub data sheet. Bit 7 = 1; Logical port 7 non-removable Bit 6 = 1; Logical port 6 non-removable Bit 5 = 1; Logical port 5 non-removable Bit 4 = 1; Logical port 4 non-removable Bit 3 = 1; Logical port 3 non-removable Bit 2 = 1; Logical port 2 non-removable Bit 1 = 1; Logical port 1 non removable Bit 0 = Reserved. always = '0' If this register is modified, the USB 3.0 Hub equivalent must also be modified in the register.

TABLE 61: USB 2.0 PORT DISABLE (SELF-POWERED)

PDS (300Ah)			Port Disable for Self-Powered Operation Default = 00h
BIT	**Name**	**R/W**	**Description**
7:0	PORT_DIS_SP	R/W	Port Disable Self-Powered: Disables 1 or more ports. '0' = port is available, '1' = port is disabled. Bit 7 = 1; Physical port 7 is disabled Bit 6 = 1; Physical port 6 is disabled Bit 5 = 1; Physical port 5 is disabled Bit 4 = 1; Physical port 4 is disabled Bit 3 = 1; Physical port 3 is disabled Bit 2 = 1; Physical port 2 is disabled Bit 1 = 1; Physical port 1 is disabled Bit 0 = Reserved. always = '0'

TABLE 62: USB 2.0 PORT DISABLE (BUS-POWERED)

PDB (300Bh)			Port Disable for Bus-Powered Operation Default = 00h
BIT	**Name**	**R/W**	**Description**
7:0	PORT_DIS_SP	R/W	Port Disable Bus-Powered: Disables 1 or more ports. '0' = port is available, '1' = port is disabled. Bit 7 = 1; Physical port 7 is disabled Bit 6 = 1; Physical port 6 is disabled Bit 5 = 1; Physical port 5 is disabled Bit 4 = 1; Physical port 4 is disabled Bit 3 = 1; Physical port 3 is disabled Bit 2 = 1; Physical port 2 is disabled Bit 1 = 1; Physical port 1 is disabled Bit 0 = Reserved. always = '0'

TABLE 63: USB 2.0 HUB MANUFACTURER STRING INDEX

MFR_STR_INDEX (3013h)			USB 2.0 Hub Manufacturer String Index Register Default = 01h
BIT	**Name**	**R/W**	**Description**
7:0	MFR_STR_LEN	R/W	Manufacturer String Index. The index number for the manufacturer string.

TABLE 64: USB 2.0 HUB PRODUCT STRING INDEX

PRD_STR_INDEX (3014h)			USB 2.0 Hub Product String Index Register Default = 02h
BIT	**Name**	**R/W**	**Description**
7:0	PRD_STR_LEN	R/W	Product String Index. The index number for the product string.

TABLE 65: USB 2.0 HUB SERIAL STRING INDEX

SER_STR_INDEX (3015h)			USB 2.0 Hub Serial String Index Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:0	SER_STR_LEN	R/W	Serial String Index. The index number for the serial string.

TABLE 66: BATTERY CHARING

BC (30D0h)			Battery Charging Enable Register Default = depends on battery charging strap setting
BIT	**Name**	**R/W**	**Description**
7:0	BC_EN	R/W	These bits reflect the state of the battery charging enable strap options. They have no effect on the battery charging activity. Downstream battery charging will be handled in the firmware. Bit 7 = Physical Port 7 Battery Charging Enabled Bit 6 = Physical Port 6 Battery Charging Enabled Bit 5 = Physical Port 5 Battery Charging Enabled Bit 4 = Physical Port 4 Battery Charging Enabled Bit 3 = Physical Port 3 Battery Charging Enabled Bit 2 = Physical Port 2 Battery Charging Enabled Bit 1 = Physical Port 1 Battery Charging Enabled Bit 0 = Reserved

TABLE 67: OVERCURRENT LOCKOUT TIMER REGISTER

START_LOCKOUT_TIMER_REG (30E1h)			Overcurrent Start Lockout Timer Register Default = 0Ah
BIT	**Name**	**R/W**	**Description**
7:0	START_LOCKOUT_TIMER	R/W	The start lockout timer blocks an overcurrent event from being detected immediately after port power is turned on. Any overcurrent event within this timer value is ignored. The timer can be incremented in 1 ms steps. The default value is 10 ms (0 Ah). This register should never be set to 00h.

TABLE 68: OVERCURRENT MINIMUM PULSE WIDTH REGISTER

OCS_MIN_WIDTH (30EAh)			Overcurrent Detection Pulse Window Default = 05h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3:0	OCS_MIN_WIDTH	R/W	The minimum overcurrent detection pulse width (t_{ocs_single}) is configured in this register. The range can be configured in 1 ms increments from 0 ms to 5 ms. 0000 = 0 ms minimum overcurrent detection pulse width 0001 = 1 ms minimum overcurrent detection pulse width 0010 = 2 ms minimum overcurrent detection pulse width 0011 = 3 ms minimum overcurrent detection pulse width 0100 = 4 ms minimum overcurrent detection pulse width 0101 = 5 ms minimum overcurrent detection pulse width [Default]

TABLE 69: OVERCURRENT INACTIVE TIMER

OCS_INACTIVE_TIMER (30EBh)			Overcurrent Inactive Timer After First Overcurrent Detection Default = 14h
BIT	**Name**	**R/W**	**Description**
7:0	OCS_INACT	R/W	This timer counts the inactivity time of second OCS event detection time within which second OCS event will be detected. Configurable values from 0 to 255 Default value is 20 ms.

TABLE 70: USB 2.0 DP/DM PORT SWAP

PRT_SWAP (30FAh)			USB 2.0 DP/DM Port Swap Default = 00h
BIT	**Name**	**R/W**	**Description**
7:0	PRT_SWAP	R/W	Port Swap: Swaps the upstream and downstream USB DP and DM pins for ease of board routing to devices and connectors. ‘0’ = USB D+ functionality is associated with the DP pin, and D– functionality is associated with the DM pin. ‘1’ = USB D+ functionality is associated with the DM pin, and D– functionality is associated with the DP pin Bit 7 = ‘1’: Physical Port 7 DP/DM is swapped Bit 6 = ‘1’: Physical Port 6 DP/DM is swapped Bit 5 = ‘1’: Physical Port 5 DP/DM is swapped Bit 4 = ‘1’: Physical Port 4 DP/DM is swapped Bit 3 = ‘1’: Physical Port 3 DP/DM is swapped Bit 2 = ‘1’: Physical Port 2 DP/DM is swapped Bit 1 = ‘1’: Physical Port 1 DP/DM is swapped Bit 0 = ‘1’: Upstream Port DP/DM is swapped

TABLE 71: USB 2.0 PORT 1 / PORT 2 REMAP

USB2_PRT_REMAP_12 (30FBh)			USB2.0 Port 1/2 Remap Default = 21h for USB5807/USB5806/USB5906, 61h for USB5816/USB5916, 51h for USB5826/USB5926
BIT	**Name**	**R/W**	**Description**
7:4	PRT_2_DIS	R/W	0000 = Physical port 2 is disabled. 0001 = Physical port 2 is mapped to logical port 1. 0010 = Physical port 2 is mapped to logical port 2. 0011 = Physical port 2 is mapped to logical port 3. 0100 = Physical port 2 is mapped to logical port 4. 0101 = Physical port 2 is mapped to logical port 5. 0110 = Physical port 2 is mapped to logical port 6. 0111 = Physical port 2 is mapped to logical port 7. 0111 – 1111 = Reserved. Note that if this register is modified, the total number of USB 3.0 ports must be updated in Table 179 and the USB 3.0 Equivalent must also be configured in the USB 3.1 Gen 1 Port 2 Configuration Select register.

TABLE 71: USB 2.0 PORT 1 / PORT 2 REMAP (CONTINUED)

USB2_PRT_REMAP_12 (30FBh)			USB2.0 Port 1/2 Remap Default = 21h for USB5807/USB5806/USB5906, 61h for USB5816/USB5916, 51h for USB5826/USB5926
BIT	**Name**	**R/W**	**Description**
3:0	PRT_1_DIS	R/W	0000 = Physical port 1 is disabled. 0001 = Physical port 1 is mapped to logical port 1. 0010 = Physical port 1 is mapped to logical port 2. 0011 = Physical port 1 is mapped to logical port 3. 0100 = Physical port 1 is mapped to logical port 4. 0101 = Physical port 1 is mapped to logical port 5. 0110 = Physical port 1 is mapped to logical port 6. 0111 = Physical port 1 is mapped to logical port 7. 0111 – 1111 = Reserved Note that if this register is modified, the total number of USB 3.0 ports must be updated in Table 179 and the USB 3.0 Equivalent must also be configured in the USB 3.1 Gen 1 Port 1 Configuration Select register.

TABLE 72: USB 2.0 PORT 3 / PORT 4 REMAP

USB2_PRT_REMAP_34 (30FCh)			Port 3/4 Disable and Remap Default = 43h for USB5807/USB5806/USB5906, 32h for USB5816/USB5916, 26h for USB5826/USB5926
BIT	**Name**	**R/W**	**Description**
7:4	PRT_4_DIS	R/W	0000 = Physical port 4 is disabled 0001 = Physical port 4 is mapped to logical port 1. 0010 = Physical port 4 is mapped to logical port 2. 0011 = Physical port 4 is mapped to logical port 3. 0100 = Physical port 4 is mapped to logical port 4. 0101 = Physical port 4 is mapped to logical port 5. 0110 = Physical port 4 is mapped to logical port 6. 0111 = Physical port 4 is mapped to logical port 7. 0111 – 1111 = Reserved Note that if this register is modified, the total number of USB 3.0 ports must be updated in Table 179 and the USB 3.0 Equivalent must also be configured in the USB 3.1 Gen 1 Port 4 Configuration Select register.
3:0	PRT_3_DIS	R/W	0000 = Physical port 3 is disabled 0001 = Physical port 3 is mapped to logical port 1. 0010 = Physical port 3 is mapped to logical port 2. 0011 = Physical port 3 is mapped to logical port 3. 0100 = Physical port 3 is mapped to logical port 4. 0101 = Physical port 3 is mapped to logical port 5. 0110 = Physical port 3 is mapped to logical port 6. 0111 = Physical port 3 is mapped to logical port 7. 0111 – 1111 = Reserved Note that If this register is modified, the total number of USB 3.0 ports must be updated in Table 179 and the USB 3.0 Equivalent must also be configured in the USB 3.1 Gen 1 Port 3 Configuration Select register.

TABLE 73: USB 2.0 PORT 5 / PORT 6 REMAP

USB2_PRT_REMAP_56 (30FDh)			Port 5/6 Disable and Remap Default = 65h for USB5807/USB5806/USB5906, 54h for USB5816/USB5916, 43h for USB5826/USB5926
BIT	**Name**	**R/W**	**Description**
7:4	PRT_6_DIS	R/W	0000 = Physical port 6 is disabled. 0001 = Physical port 6 is mapped to logical port 1. 0010 = Physical port 6 is mapped to logical port 2. 0011 = Physical port 6 is mapped to logical port 3. 0100 = Physical port 6 is mapped to logical port 4. 0101 = Physical port 6 is mapped to logical port 5. 0110 = Physical port 6 is mapped to logical port 6. 0111 = Physical port 6 is mapped to logical port 7. 0111 – 1111 = Reserved Physical port 6 should only be remapped to logical port 5 on USB5826 or USB5926. If this register is modified, the total number of USB 3.0 ports must be updated in Table 179 and the USB 3.0 equivalent must also be configured in the USB 3.1 Gen 1 Port 4 Configuration Select register.
3:0	PRT_5_DIS	R/W	0000 = Physical port 5 is disabled 0001 = Physical port 5 is mapped to logical port 1. 0010 = Physical port 5 is mapped to logical port 2. 0011 = Physical port 5 is mapped to logical port 3. 0100 = Physical port 5 is mapped to logical port 4. 0101 = Physical port 5 is mapped to logical port 5. 0110 = Physical port 5 is mapped to logical port 6. 0111 = Physical port 5 is mapped to logical port 7. 0111 – 1111 = Reserved Physical port 5 should only be remapped to logical port 6 on USB5826 or USB5926. If this register is modified, the total number of USB 3.0 ports must be updated in Table 179 and the USB 3.0 equivalent must also be configured in the USB 3.1 Gen 1 Port 3 Configuration Select register.

TABLE 74: USB 2.0 PORT 7 REMAP

USB2_PRT_REMAP_7 (30FEh)			Port 7 Disable and Remap Default = 07h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved

TABLE 74: USB 2.0 PORT 7 REMAP (CONTINUED)

USB2_PRT_REMAP_7 (30FEh)			Port 7 Disable and Remap Default = 07h
BIT	**Name**	**R/W**	**Description**
3:0	PRT_7_DIS	R/W	0000 = Physical port 7 is disabled 0001 = Physical port 7 is mapped to logical port 1. 0010 = Physical port 7 is mapped to logical port 2. 0011 = Physical port 7 is mapped to logical port 3. 0100 = Physical port 7 is mapped to logical port 4. 0101 = Physical port 7 is mapped to logical port 5. 0110 = Physical port 7 is mapped to logical port 6. 0111 = Physical port 7 is mapped to logical port 7. 0111 = 1111 – Reserved Note that if this register is modified, the total number of USB 3.0 ports must be updated in Table 179 and the USB 3.0 Equivalent must also be configured in the USB 3.1 Gen 1 Port 3 Configuration Select register. This register only pertains to USB5807.

TABLE 75: USB HUB COMMAND/STATUS REGISTER

HUB_CMD_STAT (30FFh)			USB Hub Command/Status Register Default = 00h if in configuration stage, 01h if in runtime stage
BIT	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2	INTFW_PW_DN	R/W	Disable the hub register access by disabling the clock running its configuration space. This bit should only be set more than 1 µs after the USB_ATTACH bit has been set. This ensures that configuration is complete before clock is disabled. This bit can only be written once and can only be cleared by assertion of external RESET_N pin.
1	RESET	R/W	Reset the internal memory back to default settings. ‘0’ = Normal Run/Idle State ‘1’ = Force a reset. This bit is automatically cleared to its default value of ‘0’ when set. Note that this bit has no effect once the hub is configured and the USB_ATTACH bit is set and the configuration data has been loaded.
0	USB_ATTACH	R/W	USB Attach. ‘0’ = Hub is in Configuration state. ‘1’ = Hub will signal a USB attach (D+ asserted high) event to an upstream device and will exit Configuration state.

TABLE 76: USB 2.0 LINK STATE PORTS 0 – 3

USB2_LINK_STATE0_3 (3100H)			Port 0-3 USB 2.0 Link States Default = depends on state of operation
BIT	**Name**	**R/W**	**Description**
7:6	L_STATE3	R	Indicates state of downstream physical port 3 00 = L0 Normal Operation 01 = L1 Sleep 10 = L2 Suspend 11 = L3 Off
5:4	L_STATE2	R	Indicates state of downstream physical port 2 00 = L0 Normal Operation 01 = L1 Sleep 10 = L2 Suspend 11 = L3 Off
3:2	L_STATE1	R	Indicates state of downstream physical port 1 00 = L0 Normal Operation 01 = L1 Sleep 10 = L2 Suspend 11 = L3 Off
1:0	L_STATE0	R	Indicates state of upstream physical port 0 00 = L0 Normal Operation 01 = L1 Sleep 10 = L2 Suspend 11 = L3 Off

TABLE 77: USB 2.0 LINK STATE PORTS 4 – 7

USB2_LINK_STATE4_7 (3101h)			Port 4-7 USB 2.0 Link States Default = depends on state of operation
BIT	**Name**	**R/W**	**Description**
7:6	L_STATE7	R	Indicates state of downstream physical port 7 00 = L0 Normal Operation 01 = L1 Sleep 10 = L2 Suspend 11 = L3 Off
5:4	L_STATE6	R	Indicates state of downstream physical port 6 00 = L0 Normal Operation 01 = L1 Sleep 10 = L2 Suspend 11 = L3 Off
3:2	L_STATE5	R	Indicates state of downstream physical port 5 00 = L0 Normal Operation. 01 = L1 Sleep. 10 = L2 Suspend. 11 = L3 Off.
1:0	L_STATE4	R	Indicates state of upstream physical port 4 00 = L0 Normal Operation 01 = L1 Sleep 10 = L2 Suspend 11 = L3 Off

TABLE 78: USB 2.0 HUB CONTROL

USB2_HUB_CTL (3104h)			USB 2.0 Hub Control Default = 00h
BIT	**Name**	**R/W**	**Description**
7:4	HIRD	R	Host Initiated Resume Duration. This is a direct read of the Host Initiated Resume Duration sent by the USB 2.0 host. This field indicates the minimum amount of time the host will drive the K-state during a resume. A value 0000b equals 50 µs and each additional increment adds 75 µs.
3:2	Reserved	R	Reserved
1	LPM_DISABLE	R/W	Disables Link Power Management
0	RESET	R/W	Setting this bit will keep the USB 2.0 Hub in reset.

TABLE 79: USB 2.0 HUB VERSION BCD MSB

USB2_BCDUSB_MSB (3108h)			USB 2.0 Version BCD MSB Default = 02h
BIT	**Name**	**R/W**	**Description**
7:0	USBVCD	R/W	MSB USB Specification Release Number in BCD format. It is not recommended to change this value.

TABLE 80: USB 2.0 HUB VERSION BCD LSB

USB2_BCDUSB_LSB (3109h)			USB 2.0 Version BCD LSB Default = 10h
BIT	**Name**	**R/W**	**Description**
7:0	USBVCD	R/W	LSB of USB Specification Release Number in BCD format. It is not recommended to change this value.

TABLE 81: USB 2.0 HUB ADDRESS REGISTER

USB2_HUB_ADDR (3150h)			USB 2.0 Hub Address Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7	USB2_CONFIGURED	R/W	Direct read of the USB 2.0 configured bit. Indicates when the host has sent the SET_CONFIG command to the USB 2.0 hub.
6:0	USB2_ADDRESS	R	Direct read of the USB address assigned to the hub by the host. Address = 0 means that the host has not yet assigned an address to the USB 2.0 hub.

TABLE 82: USB 2.0 HUB REMOTE WAKEUP REGISTER

USB2_REMOTE_WAKE (3151h)			USB 2.0 Remote Wakeup Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:1	Reserved	R	Reserved
0	REMOTE_WAKEUP	R	Direct read of the remote wakeup enable bit set by the USB 2.0 host.

TABLE 83: USB 2.0 EMBEDDED TEST MODE CONTROL

USB2_EMBED_TES (318Ch)			USB 2.0 Embedded Test Mode Control Default = 00h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3:1	EMBEDETEST	R/W	Embedded Host Compliance Testing Modes. Enables test modes on ports. To facilitate embedded host compliance testing, the SOC may select any of the following test modes using the serial port interface. This is a better alternative to modifying the embedded host stack to accomplish the same modes using USB communication to the hub controller with standard SETUP packet commands. Both methods can be used for embedded host compliance testing with equivalent results. The Test Modes described below are related to Section 7.1.20 of the *USB 2.0 Specification* and associated errata. Encoded values match the low nibble of the PID asserted by the HS-OPT when it requests the host to enter the associated test mode. When the test mode is entered, the hub will remain in the configured test mode for the selected ports until the bits are reset back to '000.' 0 (000) = Default Operation – No test mode asserted 1 (001) = TEST_SE0_NAK – Hub enters High-Speed receive and drives SE0 on the hub's downstream port. 2 (010) = TEST_J – Hub's downstream port enters High-Speed J state 3 (011) = TEST_K – Hub's downstream port enters High-Speed K state 4 (100) = TEST_PACKET – Sends test packets on downstream port All others Reserved Note that the port in use is selected using the USB2_EMBED_TEST_PORT_SEL register. Changing the USB2_EMBED_TEST_PORT_SEL should not change the state a particular port is left in. This will allow all ports to be put in identical or different states as it is a required for testing.

TABLE 84: USB 2.0 EMBEDDED TEST MODE PORT SELECT

USB2_EMBED_TEST_PORT_SEL (318Dh)			USB 2.0 Embedded Test Mode Port Select Default = 00h
BIT	**Name**	**R/W**	**Description**
7	Reserved	R	Reserved
6:0	PORT_SEL	R/W	Enables a port at the particular bit position. Any combination is permissible, some example are as follows: 0000000 = Normal operation 0000001 = Physical downstream port 1 0000010 = Physical downstream port 2 0000100 = Physical downstream port 3 0001000 = Physical downstream port 4 0010000 = Physical downstream port 5 0100000 = Physical downstream port 6 1000000 = Physical downstream port 7 0000011 = Physical downstream port 1 amd port 2 0000111 = Physical downstream port 1, port 2, and port 3 0001111 = Physical downstream port 1, port 2, port 3, and port 4 1111111 = Physical downstream port 1, port 2, port 3, port 4, port 5, port 6, and port 7 To enable testing of the upstream port, use the FlexConnect feature to swap port 1 with the upstream port, and then run the EMBEDTEST on port 1.

TABLE 85: FLEXCONNECT CONFIGURATION REGISTER

CONNECT_CFG (318Eh)			FlexConnect Configuration Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7	HIRD_TIMR_SEL	R/W	HIRD Timer selection register ‘0’ = Use Alternate HIRD definition (up to 9.95 ms) ‘1’ = Use Original HIRD definition (up to 1.2 ms)
6:1	Reserved	R	Reserved
0	FLEXCONNECT	R/W	FlexConnect Control. When asserted, the USB58xx/59xx changes their hub connections so that the Swap port (physical port 1) changes from its default behavior of a downstream port to an upstream port. The Flex Port (physical port 0) transitions from an upstream port to a downstream port. ‘0’ Flex Port = Up (physical port 0) Swap Port = Down (physical port 1) ‘1’ Flex Port = Down (physical port 1) Swap Port = Up (physical port 0) This setting can be used to select whether the Flex Port is an upstream or downstream port.

TABLE 86: USB 2.0 HUB STATUS

USB20_HUB_STAT (3194h)			USB 2.0 Hub Status Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7	USB2_DN_CONNECT_-DETECT7	R	Physical Port 7 USB Device connected on Hub downstream port ‘1’ = Device Connected ‘0’ = Disconnected
6	USB2_DN_CONNECT_-DETECT6	R	Physical Port 6 USB Device connected on Hub downstream port ‘1’ = Device Connected ‘0’ = Disconnected
5	USB2_DN_CONNECT_-DETECT5	R	Physical Port 5 USB Device connected on Hub downstream port ‘1’ = Device Connected ‘0’ = Disconnected
4	USB2_DN_CONNECT_-DETECT4	R	Physical Port 4 USB Device connected on Hub downstream port ‘1’ = Device Connected ‘0’ = Disconnected
3	USB2_DN_CONNECT_-DETECT3	R	Physical Port 3 USB Device connected on Hub downstream port ‘1’ = Device Connected ‘0’ = Disconnected
2	USB2_DN_CONNECT_-DETECT2	R	Physical Port 2 USB Device connected on Hub downstream port ‘1’ = Device Connected ‘0’ = Disconnected
1	USB2_DN_CONNECT_-DETECT1	R	Physical Port 1 USB Device connected on Hub downstream port ‘1’ = Device Connected ‘0’ = Disconnected
0	USB2_HOST_DETECT	R	Upstream port connected to USB 2.0 host ‘1’ = USB 2.0 Host Connected ‘0’ = No Host Connected

TABLE 87: USB 2.0 HUB DOWNSTREAM PORT DEVICE SPEED PORTS 1– 4

USB20_HUB_DN_DEV_TYPE1 (3195h)			USB 2.0 Hub Downstream Port Device Speed Ports 1 – 4 Default = 00h
BIT	**Name**	**R/W**	**Description**
7:6	USB2_DN4_DEV_SPEED	R	USB2 device speed on physical downstream port 4 00 = “NO CONNECT 01 = LS 10 = FS 11 = HS

TABLE 87: USB 2.0 HUB DOWNSTREAM PORT DEVICE SPEED PORTS 1– 4 (CONTINUED)

USB20_HUB_DN_DEV_TYPE1 (3195h)			USB 2.0 Hub Downstream Port Device Speed Ports 1 – 4 Default = 00h
BIT	**Name**	**R/W**	**Description**
5:4	USB2_DN3_DEV_SPEED	R	USB2 device speed on physical downstream port 3 00 = “NO CONNECT” 01 = LS 10 = FS 11 = HS
3:2	USB2_DN2_DEV_SPEED	R	USB2 device speed on physical downstream port 2 00 = “NO CONNECT” 01 = LS 10 = FS 11 = HS
1:0	USB2_DN1_DEV_SPEED	R	USB2 device speed on physical downstream port 1 00 = “NO CONNECT” 01 = LS 10 = FS 11 = HS

TABLE 88: USB 2.0 HUB DOWNSTREAM PORT DEVICE SPEED PORTS 5 – 7

USB20_HUB_DN_DEV_TYPE2 (3196h)			USB 2.0 Hub Downstream Port Device Speed Ports 5 – 7 Default = 00h
BIT	**Name**	**R/W**	**Description**
7:6	Reserved	R	Reserved
5:4	USB2_DN7_DEV_SPEED	R	USB2 device speed on physical downstream port 7 00 = “NO CONNECT” 01 = LS 10 = FS 11 = HS
3:2	USB2_DN6_DEV_SPEED	R	USB2 device speed on physical downstream port 6 00 = “NO CONNECT” 01 = LS 10 = FS 11 = HS
1:0	USB2_DN5_DEV_SPEED	R	USB2 device speed on physical downstream port 5 00 = “NO CONNECT” 01 = LS 10 = FS 11 = HS

TABLE 89: USB2 SUSPEND INDICATOR

USB2_SUSP_IND (3197h)			USB 2.0 Suspend Indicator Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:1	Reserved	R	Always ‘0’

TABLE 89: USB2 SUSPEND INDICATOR (CONTINUED)

USB2_SUSP_IND (3197h)			USB 2.0 Suspend Indicator Register Default = 00h
BIT	**Name**	**R/W**	**Description**
0	USB3_SUSP_IND	R	'0' = USB3 is in Functional state '1' = USB3 is in Suspend state

TABLE 90: USB3 HUB CONTROL REGISTER 1

USB3_HUB_CTL (3840h)			USB3 Hub Control 1 Default = 20h
BIT	**Name**	**R/W**	**Description**
7:6	Reserved	R	Always '0'
5	SCRAMBLE_EN	R/W	'0' = Scrambling Disabled (only for test cases) '1' = Scrambling Enabled
4	GANG_OVR_CURRENT	R/W	'0' = Individual Overcurrent '1' = Gang Overcurrent
3	BUS_POWERED	R/W	'0' = Self-Powered Hub '1' = Bus-Powered Hub
2:0	Reserved	R	Always '0'

TABLE 91: USB3 HUB CONTROL REGISTER 2

USB3_HUB_CTL2 (3841h)			USB3 Hub Control 2 Default = 01h
BIT	**Name**	**R/W**	**Description**
7	HUB_DS_PROP_RST_C-TRL	R/W	USB3 Hub Reset propagation behavior '0' = If a propagated reset ends up as Warm Reset on DFP, CCS is made low. '1' = If a propagated reset ends up as Warm Reset on DFP, CCS remains high. This behavior matches with the specifications where CCS should be 1 in DS Port Resetting state.
6	HUB_U3_RMT_WKUP_EN	R/W	USB3 Hub configuration bit. Remote Wakeup behavior. '1' = Hub has to be enabled for Remote Wakeup to allow for propaga-tion of downstream port wakeup signals. '0' = Propagating DS Wakeup does not depend on hub Remote Wakeup enable.
5	HUB_U1_U2_EXI T_FAILED	R/W	USB3 Hub Configuration bit. U1, U2 exit failure control. '1' = On a U1/U2 exit fail link transitions to Recovery '0' = On a U1/U2 exit fail link transitions to SS_INACTIVE
4	HUB_PING_TO_500MS	R/W	USB3 Hub Configuration bit. Downstream port U1 ping receive timeout. '0' = Ping receive timeout is 300 ms '1' = Ping receive timeout is 500 ms
3	HUB_STALL_EP0_HALT	R/W	USB3 Hub Configuration bit. Stall behavior. '0' = Hub does STALL SetfeatureHalt(EP0) '1' = Hub does not STALL SetfeatureHalt(EP0)
2	HUB_UX_EXIT_CTRL	R/W	USB3 Hub Exit control
1	Reserved	R	Always '0'

TABLE 91: USB3 HUB CONTROL REGISTER 2 (CONTINUED)

USB3_HUB_CTL2 (3841h)			USB3 Hub Control 2 Default = 01h
BIT	**Name**	**R/W**	**Description**
0	USB3_HUB_ENABLE	R/W	This bit enables the USB3 Hub. The hub should only be enabled after the configuration SRAM has been initialized. '0' = Hub is held in reset. '1' = Hub is operational.

TABLE 92: USB3 HUB CONTROL REGISTER 3

USB3_HUB_CTL3 (3842h)			USB3 Hub Control 3 Default = 01h
BIT	**Name**	**R/W**	**Description**
7	HUB_7PORT_2BYTES	R/W	If set to '0' for 7, port configuration returns 1 byte interrupt message. If set to '1' for 7, port configuration returns 2 byte interrupt message.
6	FORCE_U1_U2_FF	R/W	U1, U2 timer force bit. 0b0 = Downstream port U1/U2 timers follow normal operation. 0b1 = Downstream port U1/U2 timers will be forced to 0xFF.
5:4	HUB_SCALEDOWN	R/W	0b00 = Disables all scale-downs. Actual timing values are used. 0b01 = Enables scaled down SS timing and repeat values including: Number of TxEq training sequences reduce to 8 = LFPS polling burst time reduced to 100 nS = LFPS warm reset receive reduced to 30 µs 0b10 = No TxEq training sequences are sent. Overrides Bit 4. 0b11 = Enables bit 0 and bit 1 scale-down timing values.
3	DISABLE_U1_U2	R/W	U1/U2 entry is enabled as per USB specification. '1' = The hub upstream and downstream ports do not request a low power entry (U1/U2) and also reject any low power entry request from their link partners.
2	DISABLE_P3	R/W	R/W When set, this bits prevents the phys from going into P3 state in suspend.
1	USB3_BIAS_ON	R/W	This bit forces the USB3 bias request on. Bias will not be shut down in global P3.
0	USB3_XTAL_ON	R/W	If this bit is set, the USB3 will not request crystal shutdown. (The PMT will be bypassed). Firmware should keep this bit set to a '1' at all time

TABLE 93: USB3 VBUS DEBOUNCE PERIOD REGISTER

USB3_VBUS_DEB_PERIOD (3843h)			USB3 VBUS Debounce Period Register Default = 64h
BIT	**Name**	**R/W**	**Description**
7:0	DEBOUNCE	R/W	De-bounce period to be used for VBUS de-bounce for the USB3 Hub in VBUS Bypass mode. This register only takes effect if USB3_PASS_THRU is set in VBUS_PASS_THRU register. This value is in units of 1 ms. The default value is 100 ms.

TABLE 94: USB3 HUB CONTROL REGISTER 4

USB3_HUB_CTL4 (3844h)			USB3 Hub Control Register 4 Default = 01h
BIT	**Name**	**R/W**	**Description**
7:6	Reserved	R	Always '0'
5:4	USB3_SC_TIMER	R/W	USB 3.0 Over Current Timer: Over Current Timer delay when operating in USB 3.0 mode. 00b = 750 ns 01b = 1000 ns 10b = 1250 ns 11b = 1500 ns
3	USB3_GANG_PWR_EN	R/W	'0' = Individual power switching is enabled. '1' = Ganged mode. All USB3 downstream ports will have power turned on if host enables power on any of the USB3 downstream ports If a port is to be disabled in Ganged mode, the PRT_SEL for that port must be set to 0x0 to disable port power.
2	HUB_DIS_DSPORT_ECR	R/W	'0' = DSPORT ECR states are enabled. hub_enable_vbus_off_ecr (bit 1) can be used to enable/disable vbus_off arc. The DSPORT SM complies with ECN 010. '1' = DSPORT ECR states are disabled and DSPORT state machine should operate per DSPORT State Machine in the original USB3 spec with ECN 003.
1	HUB_DIS_VBUS_OFF_ECR	R/W	This bit is a don't care if hub_disable_dsport_ecr (bit 2) is high. '1' = DSPORT will go to DSPORT_Powered-off state when upstream VBUS is off. '0' = DSPORT will go to DSPORT_Powered-off-reset state when upstream vbus is off and upstream port was connected at SS and DS power switches are not supported (HUB_DS_POWR_SW_EN=0).
0	HUB_DS_POWR_SW_EN	R/W	'0' = The USB 3.0 Downstream Facing Hub Port state. The machine assumes downstream port power switches are not supported. '1' = The USB 3.0 Downstream Facing Hub Port state. The machine assumes downstream port power switches are supported. This bit doesn't have any effect if HUB_DIS_DSPORT_ECR (bit 2) or HUB_DIS_VBUS_OFF_ECR (bit 1) are set.

TABLE 95: USB3 HUB CONTROL REGISTER 5

USB3_HUB_CTL5 (3849h)			USB3 Hub Control Register 5 Default = 00h
BIT	**Name**	**R/W**	**Description**
7	Reserved	R	Always ‘0’
6	DISABLE_HP_PENDING_FIX	R/W	‘0’ = Pending HP count is reset when the link receives the LGOOD advertisement when it enters U0. So, when link comes back from Recovery due to Pending HP timeout to U0 and LGOOD advertisement is successfully received from the link partner, the next Recovery due to Pending HP timeout will not be considered consecutive. ‘1’ = The link goes to the Inactive state when there are 4 consecutive Recoveries due to the pending HP timeout even though the link might be stable in U0 and transfers data between these Recoveries.
5:4	US_SET_FTR_FC_EN	R/W	Places EP0 in flow control during the status stage of these commands: set_feature[PORT_LINK_STATE] or set_feature[PORT_U2_TIMEOUT] or set_feature[FORCE_LINKPM_ACCEPT]. Adds a timed hardware flow control during the status state of such commands will keep the host from proceeding further and thus will avoid potential race condition between the host setting the feature and host getting a port status. The hub will send NRDY during the Status stage and will start the timer. When timer expires, hub sends ERDY and then ACKs the STATUS TP. ‘00’ = Do not enter flow control ‘01’ = 1 msec ‘10’ = 4 msec ‘11’ = 16 msec
3	Reserved	R	Always ‘0’
2	LINK_ULORU2_UL_TIMEOUT_WKP_EN	R/W	‘0’ = The DFP will not leave U1 or U2 if u1_timeout is updated through SetPortFeature(PORT_U1_TIMEOUT). ‘1’ = The DFP will wakeup from U1 or U2 when host issues SetPortFeature(PORT_U1_TIMEOUT).
1	DS_LINK_CONFIG_FAIL_CTRL	R/W	‘0’ = If downstream port didn't finish link configuration - no packets will be sent to that port. ‘1’ = Packets are sent to the DFP that didn't finish the link configuration.
0	US_LINKCONFIG_FAIL_CTRL	R/W	When this bit is ‘0’—if upstream port didn't finish link configuration—the packets to the DS ports will be discarded. When this bit is ‘1,’ revert the above fix so UFP forwards the packets to the DFPs before it completes the link configuration.

TABLE 96: USB 3.1 GEN 1 HUB STATUS REGISTER

USB30_HUB_STAT (3851h)			USB 3.1 Gen 1 Hub Status Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7	USB3_DN_CONNECT_-DETECT7	R	Physical Port 7 USB Device connected on hub downstream port ‘1’ = Device Connected ‘0’ = Disconnected
6	USB3_DN_CONNECT_-DETECT6	R	Physical Port 6 USB Device connected on hub downstream port ‘1’ = Device Connected ‘0’ = Disconnected
5	USB3_DN_CONNECT_-DETECT5	R	Physical Port 5 USB Device connected on hub downstream port ‘1’ = Device Connected ‘0’ = Disconnected
4	USB3_DN_CONNECT_-DETECT4	R	Physical Port 4 USB Device connected on Hub downstream port ‘1’ = Device Connected ‘0’ = Disconnected
3	USB3_DN_CONNECT_-DETECT3	R	Physical Port 3 USB Device connected on Hub downstream port ‘1’ = Device Connected ‘0’ = Disconnected
2	USB3_DN_CONNECT_-DETECT2	R	Physical Port 2 USB Device connected on Hub downstream port ‘1’ = Device Connected ‘0’ = Disconnected
1	USB3_DN_CONNECT_-DETECT1	R	Physical Port 1 USB Device connected on Hub downstream port ‘1’ = Device Connected ‘0’ = Disconnected
0	USB3_HOST_DETECT	R	Upstream port connected to USB3 host ‘1’ = USB3 Host Connected ‘0’ = No Host Connected

TABLE 97: USB 3.1 GEN 1 HUB DOWNSTREAM SPEED INDICATOR REGISTER

USB30_HUB_DN_SPEED_IND (3852h)			USB 3.1 Gen 1 Hub Downstream Speed Indicator Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7	USB3_DN_-SPEED_IND_P7	R	Physical USB3 Port 7 USB Device Speed Indicator ‘1’ = SuperSpeed Device Connected ‘0’ = No SuperSpeed Device Connected
6	USB3_DN_-SPEED_IND_P6	R	Physical USB3 Port 6 USB Device Speed Indicator ‘1’ = SuperSpeed Device Connected ‘0’ = No SuperSpeed Device Connected
5	USB3_DN_-SPEED_IND_P5	R	Physical USB3 Port 5 USB Device Speed Indicator ‘1’ = SuperSpeed Device Connected ‘0’ = No SuperSpeed Device Connected
4	USB3_DN_-SPEED_IND_P4	R	Physical USB3 Port 4 USB Device Speed Indicator ‘1’ = SuperSpeed Device Connected ‘0’ = No SuperSpeed Device Connected
3	USB3_DN_-SPEED_IND_P3	R	Physical USB3 Port 3 USB Device Speed Indicator ‘1’ = SuperSpeed Device Connected ‘0’ = No SuperSpeed Device Connected
2	USB3_DN_-SPEED_IND_P2	R	Physical USB3 Port 2 USB Device Speed Indicator ‘1’ = SuperSpeed Device Connected ‘0’ = No SuperSpeed Device Connecte
1	USB3_DN_-SPEED_IND_P1	R	Physical USB3 Port 1 USB Device Speed Indicator ‘1’ = SuperSpeed Device Connected ‘0’ = No SuperSpeed Device Connecte
0	Reserved	R	Always ‘0’

TABLE 98: USB3 DISABLE USB3.1 DSPORT STATE MACHINE REGISTER

DISABLE_USB3P1_D-SPORT (3855h)			USB 3.0 Disable USB3.1 DSPORT State Machine Register Default = 06h for revision C silicon, Revision B silicon does not include this register
BIT	**Name**	**R/W**	**Description**
7:3	Reserved	R	Always ‘0’
2	EN_US_PORT_P-WR_ON_RX_TERM	R/W	Enables detection of receiver terminations when USPORT is in Pow-ered-on state. ‘0’ = Detection is disabled. ‘1’ = RX term detection is enabled.
1	EN_U1_MIN_RESIDEN-CY_ECN	R/W	U1 Minimum Residency Time ECN update enable. ‘0’ = ECN support is disabled. ‘1’ = ECN support is enabled.

TABLE 98: USB3 DISABLE USB3.1 DSPORT STATE MACHINE REGISTER (CONTINUED)

DISABLE_USB3P1_D-SPORT (3855h)			USB 3.0 Disable USB3.1 DSPORT State Machine Register Default = 06h for revision C silicon, Revision B silicon does not include this register
BIT	**Name**	**R/W**	**Description**
0	DISABLE_USB3P1_D-SPORT	R/W	To disable USB3.1 downstream port changes and therefore enable USB3.0 state machine operation. '0' = USB3.1 downstream port state machines updates for Revision C silicon are enabled. '1' = USB3.0 downstream port state machine changes are enabled.

TABLE 99: USB3 SUSPEND INDICATOR

USB3_SUSP_IND (3857h)			USB 3.0 Suspend Indicator Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:1	Reserved	R	Always '0'
0	USB3_SUSP_IND	R	'0' = USB3 is in Functional state. '1' = USB3 is in Suspend state.

TABLE 100: USB3 PORT REMAP ENABLE REGISTER

USB3_PRT_REMAP (3858h)			USB3 Port Remap Enable Register Default = 01h
BIT	**Name**	**R/W**	**Description**
7:1	Reserved	R	Always '0'
0	USB3_PRT_REMAP_EN	R/W	0 = Port remap is disabled 1 = Port remap is enabled. Downstream ports are re-mapped in the order of port remapped registers value. **Note 1:** If USB3_PRT_REMAP_EN ='1', then the physical port can only be disabled through the USB3_PRT_REMAP registers. If USB3_PRT_REMAP_EN = '0', then physical ports can only be disabled through PORT_CONFIGURATION_SEL_[7:1] registers. **2:** Care must be taken to ensure that any USB 3.1 Gen 1 port that is remapped is also identically remapped in the USB 2.0 portion of the hub to ensure that same numbered USB 2.0 and USB 3.1 Gen 1 ports are connected to the same physical port. **3:** Do not remap ports that are associated with USB Type-C operation (i.e.: Port 1 and/or Port 2 of USB5816, USB5826, USB5916, and USB5926 devices).

TABLE 101: USB3 PORT REMAP PORTS 1 AND 2

USB3_PRT_REMAP_P1_P2 (3860h)			USB3 Port Remap Ports 1 and 2 Default = Changes based upon part number. See Section 11.0, "Physical and Logical Port Mapping"
BIT	**Name**	**R/W**	**Description**
7:4	PRT_2_MAP	R/W	0000 = Physical port 2 is disabled. 0001 = Physical port 2 is mapped to logical port 1. 0010 = Physical port 2 is mapped to logical port 2. 0011 = Physical port 2 is mapped to logical port 3. 0100 = Physical port 2 is mapped to logical port 4. 0101 = Physical port 2 is mapped to logical port 5. 0110 = Physical port 2 is mapped to logical port 6. 0111 = Physical port 2 is mapped to logical port 7.
3:0	PRT_1_MAP	R/W	0000 = Physical port 1 is disabled. 0001 = Physical port 1 is mapped to logical port 1. 0010 = Physical port 1 is mapped to logical port 2. 0011 = Physical port 1 is mapped to logical port 3. 0100 = Physical port 1 is mapped to logical port 4. 0101 = Physical port 1 is mapped to logical port 5. 0110 = Physical port 1 is mapped to logical port 6. 0111 = Physical port 1 is mapped to logical port 7.

TABLE 102: USB3 PORT REMAP PORTS 3 AND 4

USB3_PRT_REMAP_P3_P4 (3861h)			USB3 Port Remap Ports 3 and 4 Default = Changes based upon part number. See Section 11.0, "Physical and Logical Port Mapping"
BIT	**Name**	**R/W**	**Description**
7:4	PRT_4_MAP	R/W	0000 = Physical port 4 is disabled. 0001 = Physical port 4 is mapped to logical port 1. 0010 = Physical port 4 is mapped to logical port 2. 0011 = Physical port 4 is mapped to logical port 3. 0100 = Physical port 4 is mapped to logical port 4. 0101 = Physical port 4 is mapped to logical port 5. 0110 = Physical port 4 is mapped to logical port 6. 0111 = Physical port 4 is mapped to logical port 7.
3:0	PRT_3_MAP	R/W	0000 = Physical port 3 is disabled. 0001 = Physical port 3 is mapped to logical port 1. 0010 = Physical port 3 is mapped to logical port 2. 0011 = Physical port 3 is mapped to logical port 3. 0100 = Physical port 3 is mapped to logical port 4. 0101 = Physical port 3 is mapped to logical port 5. 0110 = Physical port 3 is mapped to logical port 6. 0111 = Physical port 3 is mapped to logical port 7.

TABLE 103: USB3 PORT REMAP PORTS 5 AND 6

USB3_PRT_REMAP_P5_P6 (3862h)			USB3 Port Remap Ports 5 and 6 Default = Changes based upon part number. See Section 11.0, "Physical and Logical Port Mapping"
BIT	**Name**	**R/W**	**Description**
7:4	PRT_6_MAP	R/W	0000 = Physical port 6 is disabled. 0001 = Physical port 6 is mapped to logical port 1. 0010 = Physical port 6 is mapped to logical port 2. 0011 = Physical port 6 is mapped to logical port 3. 0100 = Physical port 6 is mapped to logical port 4. 0101 = Physical port 6 is mapped to logical port 5. 0110 = Physical port 6 is mapped to logical port 6. 0111 = Physical port 6 is mapped to logical port 7.
3:0	PRT_5_MAP	R/W	0000 = Physical port 5 is disabled. 0001 = Physical port 5 is mapped to logical port 1. 0010 = Physical port 5 is mapped to logical port 2. 0011 = Physical port 5 is mapped to logical port 3. 0100 = Physical port 5 is mapped to logical port 4. 0101 = Physical port 5 is mapped to logical port 5. 0110 = Physical port 5 is mapped to logical port 6. 0111 = Physical port 5 is mapped to logical port 7.

TABLE 104: USB3 PORT REMAP PORT 7

USB3_PRT_REMAP_P7 (3863h)			USB3 Port Remap Port 7 Default = Changes based upon part number. See Section 11.0, "Physical and Logical Port Mapping"
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3:0	PRT_7_MAP	R/W	0000 = Physical port 7 is disabled. 0001 = Physical port 7 is mapped to logical port 1. 0010 = Physical port 7 is mapped to logical port 2. 0011 = Physical port 7 is mapped to logical port 3. 0100 = Physical port 7 is mapped to logical port 4. 0101 = Physical port 7 is mapped to logical port 5. 0110 = Physical port 7 is mapped to logical port 6. 0111 = Physical port 7 is mapped to logical port 7.

TABLE 105: USB 3.0 LINK LOW POWER STATE 1

LINK_PWR_STATE1 (3870h)			USB 3.0 Link Low Power State 1 Default = changes dynamically during runtime
BIT	**Name**	**R/W**	**Description**
7:6	P_STATE3	R	Indicates state of downstream physical port 3 00 = U0 Normal Operation 01 = U1 Low Recovery Time Latency 10 = U2 Longer Recovery Time Latency 11 = U3 Lowest Power state
5:4	P_STATE2	R	Indicates state of downstream physical port 2 00 = U0 Normal Operation 01 = U1 Low Recovery Time Latency 10 = U2 Longer Recovery Time Latency 11 = U3 Lowest Power State

TABLE 105: USB 3.0 LINK LOW POWER STATE 1

LINK_PWR_STATE1 (3870h)			USB 3.0 Link Low Power State 1 Default = changes dynamically during runtime
BIT	**Name**	**R/W**	**Description**
3:2	P_STATE1	R	Indicates state of downstream physical port 1 00 = U0 Normal Operation 01 = U1 Low Recovery Time Latency 10 = U2 Longer Recovery Time Latency 11 = U3 Lowest Power state
1:0	P_STATE0	R	Indicates state of the upstream physical port 0 00 = U0 Normal Operation 01 = U1 Low Recovery Time Latency 10 = U2 Longer Recovery Time Latency 11 = U3 Lowest Power state

TABLE 106: USB 3.0 LINK LOW POWER STATE 2

LINK_PWR_STATE2 (3874h)			USB 3.0 Link Low Power State 2 Default = Status indicator; changes dynamically during runtime
BIT	**Name**	**R/W**	**Description**
7:6	P_STATE7	R	Indicates state of downstream physical port 7 00 = U0 Normal Operation 01 = U1 Low Recovery Time Latency 10 = U2 Longer Recovery Time Latency 11 = U3 Lowest Power state
5:4	P_STATE6	R	Indicates state of downstream physical port 6 00 = U0 Normal Operation 01 = U1 Low Recovery Time Latency 10 = U2 Longer Recovery Time Latency 11 = U3 Lowest Power state
3:2	P_STATE5	R	Indicates state of downstream physical port 5 00 = U0 Normal Operation 01 = U1 Low Recovery Time Latency 10 = U2 Longer Recovery Time Latency 11 = U3 Lowest Power state
1:0	P_STATE4	R	Indicates state of downstream physical port 4 00 = U0 Normal Operation 01 = U1 Low Recovery Time Latency 10 = U2 Longer Recovery Time Latency 11 = U3 Lowest Power state

TABLE 107: USB HP PENDING TIMER ECN REGISTER LSB

PENDING_HP_MAX_VALUE_LSB (3878h)			Pending HP Timer Max Value LSB Default = 5Fh *(Revision C silicon only)*
BIT	**Name**	**R/W**	**Description**
7:0	PENDING_HP_MAX_VALUE_LSB	R/W	Pending HP Timer max value LSB. This register was added in revision C silicon to address a change to the *USB3.1 Specifications* applied via ECN. The value is pre-configured to the optimal setting and is not recommended to be modified.

TABLE 108: USB HP PENDING TIMER ECN REGISTER MSB

PENDING_HP_MAX_VALUE_MSB (3879h)			Pending HP Timer Max Value MSB Default = 05h *(revision C silicon only)*
BIT	**Name**	**R/W**	**Description**
7:0	PENDING_HP_MAX_VALUE_MSB	R/W	Pending HP Timer max value MSB. This register was added in revision C silicon to address a change to the *USB3.1 Specifications* applied via ECN. The value is pre-configured to the optimal setting and is not recommended to be modified.

TABLE 109: PM ENTRY AND U1 RESIDENCY TIME REGISTER

PM_ENTRY_AND_U1_RESIDENCY_TIME (387Ah)			PM Entry and U1 Residency Time Register Default = 49h *(revision C silicon only)*
BIT	**Name**	**R/W**	**Description**
7:4	U1_MIN_RESIDENCY_TIME_IN_US	R/W	U1 MIN Residency time in microseconds Default = 4h This register was added in Revision C silicon to address a change to the *USB3.1 Specifications* applied via ECN. The value is pre-configured to the optimal setting and is not recommended to be modified.
3:0	PM_ENTRY_TIME_IN_US	R/W	R/W PM Entry time in microseconds Default = 9h This register was added in revision C silicon to address a change to the *USB3.1 Specifications* applied via ECN. The value is pre-configured to the optimal setting and is not recommended to be modified.

TABLE 110: U1 LFPS EXIT TIME LSB

U1_LFPS_EXIT_LSB (387Bh)			U1 LFPS Exit Time LSB Default = 77h *(revision C silicon only)*
BIT	**Name**	**R/W**	**Description**
7:0	L1_LFPS_EXIT_LSB	R/W	U1 LFPS Exit Time LSB This register was added in Revision C silicon to address a change to the *USB3.1 Specifications* applied via ECN. The value is pre-configured to the optimal setting and is not recommended to be modified.

TABLE 111: U1 LFPS EXIT TIME MSB

U1_LFPS_EXIT_MSB (387Ch)			U1 LFPS Exit Time MSB Default = 00h *(revision C silicon only)*
BIT	**Name**	**R/W**	**Description**
7:0	L1_LFPS_EXIT_MSB	R/W	U1 LFPS Exit Time MSB This register was added in Revision C silicon to address a change to the *USB3.1 Specification*s applied via ECN. The value is pre-configured to the optimal setting and is not recommended to be modified.

TABLE 112: PM LC TIME IN MICROSECONDS LSB REGISTER

PM_LC_TIME_IN_US_LSB (387Dh)			PM LC Time in Microseconds LSB Register Default = 71h *(Revision C silicon only)*
BIT	**Name**	**R/W**	**Description**
7:0	PM_LC_TIME_IN_US_LSB	R/W	PM LC Time in microseconds LSB This register was added in revision C silicon to address a change to the USB3.1 specification applied via ECN. The value is pre-configured to the optimal setting and is not recommended to be modified.

TABLE 113: PM LC TIME IN MICROSECONDS MSB REGISTER

PM_LC_TIME_IN_US_MSB (387Eh)			PM LC Time in Microseconds MSB Register Default = 02h *(revision C silicon only)*
BIT	**Name**	**R/W**	**Description**
7:0	PM_LC_- TIME_IN_US_MSB	R/W	PM LC Time in microseconds MSB This register was added in Revision C silicon to address a change to the *USB3.1 Specifications* applied via ECN. The value is pre-configured to the optimal setting and is not recommended to be modified.

TABLE 114: USB 3.1 GEN 1 PORT 1 CONFIGURATION SELECT

USB3_PRT_CFG_SEL1 (3C00h)			Physical Port 1 Configuration Select Default = 83h
BIT	**Name**	**R/W**	**Description**
7	COMBINED_MODE	R/W	‘0’ = The port power and overcurrent sense use separate pins. ‘1’ = The port power and overcurrent sense use the same pins.
6	GANG_PIN	R/W	When this bit is set, the port will be connected to the GANG_PWR pin.
5	DISABLED	R/W	When set, this bit disables the port. Note that if this register is modified, the total number of USB 3.0 ports must be updated in Table 179. The USB 2.0 Equivalent must also be configured in the USB 2.0 Port 1 / Port 2 Remap register.
4	PERMANENT	R/W	When set, this bit indicates this port has a permanently attached device.

TABLE 114: USB 3.1 GEN 1 PORT 1 CONFIGURATION SELECT

USB3_PRT_CFG_SEL1 (3C00h)			Physical Port 1 Configuration Select Default = 83h
BIT	**Name**	**R/W**	**Description**
3:0	Reserved	R	This selects the source for the port power for port 1. 0000b = Port power is disabled for this port. 0001b = Port is on if USB2 port power is on. 0010b = Port is on if USB3 port power is on. 0011 = Port is on if USB2 or USB3 port power is on. 0100b = Port is on if designated GPIO is on. All other values are reserved.

TABLE 115: USB 3.1 GEN 1 PORT 2 CONFIGURATION SELECT

USB3_PRT_CFG_SEL2 (3C04h)			Physical Port 2 Configuration Select Default = 83h
BIT	**Name**	**R/W**	**Description**
7	COMBINED_MODE	R/W	'0' = The port power and overcurrent sense use separate pins. '1' = The port power and overcurrent sense use the same pins.
7	Reserved	R/W	Reserved. Should always be set to '1'.
6	GANG_PIN	R/W	When this bit is set, the port will be connected to the GANG_PWR pin.
5	DISABLED	R/W	When set, this bit disables the port. Note that if this register is modified, the total number of USB 3.0 ports must be updated in Table 179.The USB 2.0 Equivalent must also be configured in the USB 2.0 Port 1 / Port 2 Remap register.
4	PERMANENT	R/W	When set, this bit indicates this port has a permanently attached device.
3:0	Reserved	R	This selects the source for the port power for port N. 0000b = Port power is disabled for this port. 0001b = Port is on if USB2 port power is on. 0010b = Port is on if USB3 port power is on. 0011 = Port is on if USB2 or USB3 port power is on. 0100b = Port is on if designated GPIO is on. All other values are reserved.

TABLE 116: USB 3.1 GEN 1 PORT 3 CONFIGURATION SELECT

USB3_PRT_CFG_SEL3 (3C08h)			Physical Port 3 Configuration Select Default = 83h
BIT	**Name**	**R/W**	**Description**
7	COMBINED_MODE	R/W	'0' = The port power and overcurrent sense use separate pins. '1' = The port power and overcurrent sense use the same pins.
6	GANG_PIN	R/W	When this bit is set, the port will be connected to the GANG_PWR pin.
5	DISABLED	R/W	When set, this bit disables the port. Note that if this register is modified, the total number of USB 3.0 ports must be updated in Table 179. The USB 2.0 Equivalent must also be configured in the USB 2.0 Port 3 / Port 4 Remap register.
4	PERMANENT	R/W	When set, this bit indicates this port has a permanently attached device.

TABLE 116: USB 3.1 GEN 1 PORT 3 CONFIGURATION SELECT (CONTINUED)

USB3_PRT_CFG_SEL3 (3C08h)			Physical Port 3 Configuration Select Default = 83h
BIT	**Name**	**R/W**	**Description**
3:0	Reserved	R	This selects the source for the port power for port N. 0000b = Port power is disabled for this port. 0001b = Port is on if USB2 port power is on. 0010b = Port is on if USB3 port power is on. 0011 = Port is on if USB2 or USB3 port power is on. 0100b = Port is on if designated GPIO is on. All other values are reserved.

TABLE 117: USB 3.1 GEN 1 PORT 4 CONFIGURATION SELECT

USB3_PRT_CFG_SEL4 (3C0Ch)			Physical Port 4 Configuration Select Default = 83h
BIT	**Name**	**R/W**	**Description**
7	COMBINED_MODE	R/W	'0' = The port power and over-current sense use separate pins. '1' = The port power and over-current sense use the same pins.
6	GANG_PIN	R/W	When this bit is set, the port will be connected to the GANG_PWR pin.
5	DISABLED	R/W	When set, this bit disables the port. Note that if this register is modified, the total number of USB 3.0 ports must be updated in Table 179. The USB 2.0 Equivalent must also be configured in the USB 2.0 Port 3 / Port 4 Remap register.
4	PERMANENT	R/W	When set, this bit indicates this port has a permanently attached device.
3:0	Reserved	R	This selects the source for the port power for port N. 0000b = Port power is disabled for this port. 0001b = Port is on if USB2 port power is on. 0010b = Port is on if USB3 port power is on. 0011 = Port is on if USB2 or USB3 port power is on. 0100b = Port is on if designated GPIO is on. All other values are reserved.

TABLE 118: USB 3.1 GEN 1 PORT 5 CONFIGURATION SELECT

USB3_PRT_CFG_SEL5 (3C10h)			Physical Port 5 Configuration Select Default = 83h
BIT	**Name**	**R/W**	**Description**
7	COMBINED_MODE	R/W	'0' = The port power and overcurrent sense use separate pins. '1' = The port power and overcurrent sense use the same pins.
6	GANG_PIN	R/W	When this bit is set, the port will be connected to the GANG_PWR pin.
5	DISABLED	R/W	When set, this bit disables the port. Note that if this register is modified, the total number of USB 3.0 ports must be updated in Table 179.The USB 2.0 Equivalent must also be configured in the USB 2.0 Port 3 / Port 4 Remap register.
4	PERMANENT	R/W	When set, this bit indicates this port has a permanently attached device.

TABLE 118: USB 3.1 GEN 1 PORT 5 CONFIGURATION SELECT (CONTINUED)

USB3_PRT_CFG_SEL5 (3C10h)			Physical Port 5 Configuration Select Default = 83h
BIT	**Name**	**R/W**	**Description**
3:0	Reserved	R	This selects the source for the port power for port N. 0000b = Port power is disabled for this port. 0001b = Port is on if USB2 port power is on. 0010b = Port is on if USB3 port power is on. 0011 = Port is on if USB2 or USB3 port power is on. 0100b = Port is on if designated GPIO is on. All other values are reserved.

TABLE 119: USB 3.1 GEN 1 PORT 6 CONFIGURATION SELECT

USB3_PRT_CFG_SEL6 (3C14h)			Physical Port 6 Configuration Select Default = 83h
BIT	**Name**	**R/W**	**Description**
7	COMBINED_MODE	R/W	'0' = The port Power and over-current sense use separate pins. '1' = The port power and over-current sense use the same pins.
6	GANG_PIN	R/W	When this bit is set, the port will be connected to the GANG_PWR pin.
5	DISABLED	R/W	When set, this bit disables the port. Note that if this register is modified, the total number of USB 3.0 ports must be updated in Table 179. The USB 2.0 Equivalent must also be configured in the USB 2.0 Port 3 / Port 4 Remap register.
4	PERMANENT	R/W	When set, this bit indicates this port has a permanently attached device.
3:0	Reserved	R	This selects the source for the port power for port N. 0000b = Port power is disabled for this port. 0001b = Port is on if USB2 port power is on. 0010b = Port is on if USB3 port power is on. 0011 = Port is on if USB2 or USB3 port power is on. 0100b = Port is on if designated GPIO is on. All other values are reserved.

TABLE 120: USB 3.1 GEN 1 PORT 7 CONFIGURATION SELECT

USB3_PRT_CFG_SEL7 (3C18h)			Physical Port 7 Configuration Select Default = 83h for USB5807, 10h for USB5806/USB5816/USB5826/USB5906/USB5916/USB5926
BIT	**Name**	**R/W**	**Description**
7	COMBINED_MODE	R/W	0 = The port power and overcurrent sense use separate pins. 1 = The port power and overcurrent sense use the same pins.
6	GANG_PIN	R/W	When this bit is set, the port will be connected to the GANG_PWR pin.
5	DISABLED	R/W	When set, this bit disables the port. Note that if this register is modified, the total number of USB 3.0 ports must be updated in USB 3.0 Number of Ports. The USB 2.0 Equivalent must also be configured in the USB 2.0 Port 3 / Port 4 Remap register.
4	PERMANENT	R/W	When set, this bit indicates that this port has a permanently attached device.

TABLE 120: USB 3.1 GEN 1 PORT 7 CONFIGURATION SELECT

USB3_PRT_CFG_SEL7 (3C18h)			Physical Port 7 Configuration Select Default = 83h for USB5807, 10h for USB5806/USB5816/USB5826/USB5906/USB5916/USB5926
BIT	**Name**	**R/W**	**Description**
3:0	Reserved	R	This selects the source for the port power for port N. 0000b = Port power is disabled for this port. 0001b = Port is on if USB2 port power is on. 0010b = Port is on if USB3 port power is on. 0011 = Port is on if USB2 or USB3 port power is on. 0100b = Port is on if designated GPIO is on. All other values are reserved.

TABLE 121: PORT 1 OVERCURRENT SENSE SOURCE SELECT

OCS_SEL1 (3C20h)			Physical Port 1 OCS Source Select Default = 01h
BIT	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always ‘0’
3:0	PRT_SEL	R/W	This selects the source for the port power for port 1: 0000b = The port is disabled 0001b = OCS comes from OCS pin 0010b = Reserved 0011b = OCS comes from GANG_PWR pin 1111b = Reserved All other values are reserved.

TABLE 122: PORT 2 OVERCURRENT SENSE SOURCE SELECT

OCS_SEL2 (3C24h)			Physical Port 2 OCS Source Select Default = 01h
BIT	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always ‘0’
3:0	PRT_SEL	R/W	This selects the source for the port power for port 2. 0000b = The port is disabled. 0001b = OCS comes from OCS pin. 0010b = Reserved 0011b = OCS comes from GANG_PWR pin. 1111b = Reserved All other values are reserved.

TABLE 123: PORT 3 OVERCURRENT SENSE SOURCE SELECT

OCS_SEL3 (3C28h)			Physical Port 3 OCS Source Select Default = 01h
BIT	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always ‘0’

TABLE 123: PORT 3 OVERCURRENT SENSE SOURCE SELECT (CONTINUED)

OCS_SEL3 (3C28h)			Physical Port 3 OCS Source Select Default = 01h
BIT	**Name**	**R/W**	**Description**
3:0	PRT_SEL	R/W	This selects the source for the port power for port 3. 0000b = The port is disabled. 0001b = OCS comes from OCS pin. 0010b = Reserved 0011b = OCS comes from GANG_PWR pin. 1111b = Reserved All other values are reserved.

TABLE 124: PORT 4 OVERCURRENT SENSE SOURCE SELECT

OCS_SEL4 (3C2Ah)			Physical Port 4 OCS Source Select Default = 01h
BIT	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always ‘0’
3:0	PRT_SEL	R/W	This selects the source for the port power for port 4. 0000b = The port is disabled. 0001b = OCS comes from OCS pin. 0010b = Reserved. 0011b = OCS comes from GANG_PWR pin. 1111b = Reserved. All other values are reserved.

TABLE 125: PORT 5 OVERCURRENT SENSE SOURCE SELECT

OCS_SEL5 (3C30h)			Physical Port 5 OCS Source Select Default = 01h
BIT	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always ‘0’
3:0	PRT_SEL	R/W	This selects the source for the port power for port 5. 0000b = The port is disabled. 0001b = OCS comes from OCS pin. 0010b = Reserved 0011b = OCS comes from GANG_PWR pin. 1111b = Reserved All other values are reserved.

TABLE 126: PORT 6 OVERCURRENT SENSE SOURCE SELECT

OCS_SEL6 (3C34h)			Physical Port 6 OCS Source Select Default = 01h
BIT	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always ‘0’
3:0	PRT_SEL	R/W	This selects the source for the port power for port 6. 0000b = The port is disabled. 0001b = OCS comes from OCS pin. 0010b = Reserved 0011b = OCS comes from GANG_PWR pin. 1111b = Reserved All other values are reserved.

TABLE 127: PORT 7 OVERCURRENT SENSE SOURCE SELECT

OCS_SEL7 (3C38h)			Physical Port 7 OCS Source Select Default = 01h for USB5807, 00h for USB5806/USB5816/USB5826/USB5906/USB5916/USB5926
BIT	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always ‘0’
3:0	PRT_SEL	R/W	This selects the source for the port power for port 7. 0000b = The port is disabled. 0001b = OCS comes from OCS pin. 0010b = Reserved 0011b = OCS comes from GANG_PWR pin. 1111b = Reserved All other values are reserved.

TABLE 128: USB3 PORT SPLIT ENABLE REGISTER

USB3_PORT_SPLIT_EN (3C48h)			USB3 Physical Port Split Enable Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:1	Reserved	R/W	Port Split Enable on a port by port basis. When = ‘1’, the Port Control to the USB3 port can be controlled independently through a separate GPIO which is mapped specifically for the split port. ‘0’ = Port splitting on that port is disabled ‘1’ = Port splitting on that port is enabled.’ Bit [0] – Reserved [1] – PHYSICAL PORT 1 [2] – PHYSICAL PORT 2 [3] – PHYSICAL PORT 3 [4] – PHYSICAL PORT 4 [5] – PHYSICAL PORT 5 [6] – PHYSICAL PORT 6 [7] – PHYSICAL PORT 7
0	Reserved	R	Always ‘0’

TABLE 129: FLEXCONNECT CONFIGURATION 1

FLEX_CFG1 (411Ah)			FlexConnect Configuration 1 Default = 00h
BIT	**Name**	**R/W**	**Description**
7	CHNG_PIN_FUNCT	R/W	This bit will change the digital pin controls back to the default states. For example, VBUS_DET has the same functionality regardless of the FLEX state.
6	FLEXCONNECT	R/W	The value of FLEXCONNECT after the Hub is reattached
5	DIS_P5	R/W	Disabled internal Hub Controller on port 5 after entering the “flexed” state. If this disabled, then no commands can be sent to the Hub Controller when in the “flexed” state.
4	DIS_P4	R/W	Disabled downstream port 4 after switching directions
3	DIS_P3	R/W	Disabled downstream port 3 after switching directions
2	DIS_P2	R/W	Disabled downstream port 2 after switching directions

TABLE 129: FLEXCONNECT CONFIGURATION 1 (CONTINUED)

FLEX_CFG1 (411Ah)			FlexConnect Configuration 1 Default = 00h
BIT	**Name**	**R/W**	**Description**
1	DIS_P1	R/W	Disabled downstream port 1 after switching directions
0	Reserved	R	Reserved

TABLE 130: FLEXCONNECT CONFIGURATION 2

FLEX_CFG2 (411Bh)			FlexConnect Configuration 2 Default = 01h
BIT	**Name**	**R/W**	**Description**
7	Reserved	R	Reserved. This bit must always read ‘1’.
6	DCP_EN	R/W	Enables the universal dedicated charging algorithm to be used on disabled ports. This will cause the hub to enumerate limited ports, but the VBUS and battery charging handshake will still be present on the disabled ports.
3:5	Reserved	R	Reserved
0:2	HD_TIMER	R/W	Host Detect Timeout: The time the hub will wait for a Host to enumerate before returning to the Default state. 000 = No timeout 001 = 10 ms 010 = 100 ms 011 = 500 ms 100 = 1s 101 = 5s 110 = 10s 111 = 20s

TABLE 131: RUNTIME FLAGS REGISTER 2

RUNTIME_FLAGS2 (411Dh)			Runtime Flags Register 2 Default = 85h
BIT	**Name**	**R/W**	**Description**
7	EN_BC_UNIVERSAL	R/W	Reserved. This bit must always read ‘1’.
6	RFL@_BC_ENABLE_NEW_TRANSITION_TIMER	R/W	‘1’ = If enabled separates VBUS discharge timers for DCP > CDP and CDP > SDP transition, can be configured through 4135h and 4175h registers. ‘0’ = Only one timer for both DCP > CDP and CDP > SDP transitions can be configured through 0x4135 register. Default for this bit is ‘0’ in Firmware
5	BYTE_FLASH_EN	R/W	‘1’ = Byte flash mode is enabled for SPI Flash. ‘0’ = Byte flash mode is disabled.
4	DISABLE_USB3_HUB	R/W	‘0’ = USB3 hub will be enabled by default. ‘1’ = USB3_HUB_ENABLE in USB3_HUB_CTL2 register will not be set and also suspend clock will not be enabled (unless downstream battery charging is enabled).
3	BYPASS_UDC_SUSPEND	R/W	‘0’ = Default UDC suspend handling ‘1’ = MCU will not handle UDC suspend.

TABLE 131: RUNTIME FLAGS REGISTER 2 (CONTINUED)

RUNTIME_FLAGS2 (411Dh)			Runtime Flags Register 2 Default = 85h
BIT	**Name**	**R/W**	**Description**
2	TARGET_OTP	R/W	Set Target OTP '0' = Any command targeted to OTP (OTP Read, OTP programming, etc.) is redirected to the pseudo OTP in SPI flash physical address 0x10000 to 0x11FFF. '1' = Any command targeted to OTP (OTP Read, OTP programming, etc.) is directed to the OTP.
1	CFG_FROM_SPI	R/W	Load Configuration from SPI '1' = Configuration settings loaded from pseudo OTP in SPI. '0' = Configuration settings will not be loaded from pseudo OTP in SPI.
0	CFG_FROM_OTP	R/W	Load Config from OTP '1' = Firmware will load configuration settings from OTP. '0' = Configuration settings will not be loaded from OTP.

TABLE 132: USB2 HUB DEFAULT PID MSB

USB2_DEFAULT_PIDM (411Eh)			USB2 Hub Default PID MSB Default = 28h
BIT	**Name**	**R/W**	**Description**
7:0	USB2_DEFAULT_PIDM	R/W	Default USB2 Hub PID MSB, regardless of what was programmed into OTP and reported to the USB host during enumeration

TABLE 133: USB2 HUB DEFAULT PID LSB

USB2_DEFAULT_PIDL (411Fh)			USB2 Hub Default PID LSB Default = 07h for USB5807, 06h for USB5806 and USB5906, 16h for USB5816 and USB5916, 26h for USB5826 and USB5926
BIT	**Name**	**R/W**	**Description**
7:0	USB2_DEFAULT_PIDL	R/W	Default USB2 Hub PID LSB, regardless of what was programmed into OTP and reported to the USB host during enumeration

TABLE 134: USB3 HUB DEFAULT PID MSB

USB3_DEFAULT_PIDM (4120h)			USB3 Hub Default PID MSB Default = 58h
BIT	**Name**	**R/W**	**Description**
7:0	USB2_DEFAULT_PIDM	R/W	Default USB3 Hub PID MSB, regardless of what was programmed into OTP and reported to the USB host during enumeration

TABLE 135: USB3 HUB DEFAULT PID LSB

USB3_DEFAULT_PIDL (4121h)			USB3 Hub Default PID LSB Default = 07h for USB5807, 06h for USB5806 and USB5906, 16h for USB5816 and USB5916, 26h for USB5826 and USB5926
BIT	**Name**	**R/W**	**Description**
7:0	USB3_DEFAULT_PIDL	R/W	Default USB3 Hub PID LSB, regardless of what was programmed into OTP and reported to the USB host during enumeration

TABLE 136: HUB FEATURE CONTROLLER ENABLE

HFC_ENABLE (4130h)			Hub Feature Controller Enable Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2:0	HFC_ENABLE_DISABLE	R/W	Allows Hub Feature Controller to be disabled 00b = Default behavior (disabled for USB5807, enabled for USB5806/ USB5816/USB5826/USB5906/USB5916/USB5926) 01b = Always enable Hub Feature Controller enumeration 10b = Always disable Hub Feature Controller enumeration Do not attempt to enable the Hub Feature Controller on hub devices with seven total downstream ports (i.e.: USB58xx/USB59xx part numbers ending in ‘7’ such as USB5807).

TABLE 137: HUB RUNTIME FLAGS REGISTER 1

RUNTIME_FLAGS1 (4134h)			Hub Runtime Flags Register 1 Default = 41h
BIT	**Name**	**R/W**	**Description**
7	HUB_CFG_CLK	R/W	Enable Hubcfg Interface power down: ‘1’ = Clock to hub configuration registers is turned off after Hub attach to USB. ‘0’ = Clock to hub configuration registers is left turned on.
6	CONFIG_FLAG	R/W	‘1’ = Port configuration parameters must come through OTP or SMBus except UDC Port of USB2 Hub. ‘0’ = Firmware will do port configuration of USB2 and USB3 Hubs.
5	Reserved	R	Always ‘0’
4	SUSP_CLK_OFF	R/W	Suspend clock always OFF: ‘1’ = Suspend clock is forcefully turned off irrespective of presence of USB3 hub or battery charging. ‘0’ = Suspend clock is left turned on/off depending on downstream battery charging and USB3 hub.

TABLE 137: HUB RUNTIME FLAGS REGISTER 1 (CONTINUED)

RUNTIME_FLAGS1 (4134h)			Hub Runtime Flags Register 1 Default = 41h
BIT	**Name**	**R/W**	**Description**
3	USB23_WAKEUP	R/W	Enable_USB23_WAKEUP: '1' = USB2_WAKEUP and USB3_WAKEUP interrupt mask is set to '0' (Interrupt is enabled.). '0' = USB2_WAKEUP and USB3_WAKEUP interrupt mask is set to '1' (Interrupt is disabled.).
2	RESET_OTP	R/W	Enable OTP reset: '1' = Reset is issued to the OTP macro before accessing OTP for the first time after power on. '0' = Reset is not issued to the OTP macro.
1	DISABLE_BC	R/W	Disable Battery Charging: '1' = Battery charging logic is completely disabled globally. '0' = Battery charging logic is left enabled based on standard battery charging configuration registers.
0	Reserved	R	Always '0'

TABLE 138: BATTERY CHARGING DCP TO CDP VBUS DISCHARGE TIME REGISTER

BC_DCP2CDP_DIS_TIME (4135h)			Battery Charging DCP to CDP VBUS Discharge Time Register Default = 78h
BIT	**Name**	**R/W**	**Description**
7:0	BC_VBUS_DCP2CD-P_DIS_TIME	R/W	Firmware variable that is used to control the VBUS discharge time during a DCP to CDP transition. In units of heartbeat steps (5ms or 10ms, depending on setting).

TABLE 139: BILLBOARD DETACH TIMER A LSB

DETACH_TIMER_A_LSB (413Ch)			Billboard Detach Timer A LSB Default = 07h
BIT	**Name**	**R/W**	**Description**
7:0	TIMEOUT	R/W	This feature is only supported on USB5806, USB5816, USB5826, USB5906, USB5916, and USB5926 devices. Timer A is started as soon as the Hub Feature Controller's Billboard Class Device is set by the host. Once this timer expires, the Billboard Class Device will automatically detach from the host and re-attach as the default WinUSB device. Increments of 10 ms can be set. The default value of 413Ch = D0h, 413Dh = 07h, the equivalent to a 20s timeout (07D0h = 2000d)

TABLE 140: BILLBOARD DETACH TIMER A MSB

DETACH_TIMER_A_MSB (413Dh)			Billboard Detach Timer A MSB Default = D0h
BIT	**Name**	**R/W**	**Description**
7:0	TIMEOUT	R/W	This feature is only supported on USB5806, USB5816, USB5826, USB5906, USB5916, and USB5926 devices. Timer A is started as soon as the Hub Feature Controller's Billboard Class Device is set by the host. Once this timer expires, the Billboard Class Device will automatically detach from the host and re-attach as the default WinUSB device. Increments of 10 ms can be set. The default value of 413Ch = D0h, 413Dh = 07h, the equivalent to a 20s timeout (07D0h = 2000d)

TABLE 141: BILLBOARD DETACH TIMER B LSB

DETACH_TIMER_B_LSB (413Eh)			Billboard Detach Timer B LSB Default = 07h
BIT	**Name**	**R/W**	**Description**
7:0	TIMEOUT	R/W	This feature is only supported on USB5806, USB5816, USB5826, USB5906, USB5916, and USB5926 devices. Timer B is started as soon as the host requests iAlternateModeString. Once the timer expires, the Billboard Class Device will automatically detach from the host and re-attach as the default WinUSB device. Increments of 10 ms can be set. The default value of 413Eh = D0h, 413Fh = 07h, the equivalent to a 20s timeout (07D0h = 2000d)

TABLE 142: BILLBOARD DETACH TIMER B MSB

DETACH_TIMER_B_MSB (413Fh)			Billboard Detach Timer B MSB Default = D0h
BIT	**Name**	**R/W**	**Description**
7:0	TIMEOUT	R/W	This feature is only supported on USB5806, USB5816, USB5826, USB5906, USB5916, and USB5926 devices. Timer B is started as soon as the host requests iAlternateModeString. Once the timer expires, the Billboard Class Device will automatically detach from the host and re-attach as the default WinUSB device. Increments of 10 ms can be set. The default value of 413Eh = D0h, 413Fh = 07h, the equivalent to a 20s timeout (07D0h = 2000d)

TABLE 143: BILLBOARD DEVICE ENABLE PIN CONTROL SELECT

BB_PF_PIN (4142h)			Billboard Device Enable Pin Control Select Default = 00h
BIT	**Name**	**R/W**	**Description**
7:0	BB_PF_PIN	R/W	This register selects which GPIO to assign the role of the Billboard device enable. Examples: 0000 0100 = Select GPIO4 0000 0101 = Select GPIO5 0000 0110 = Select GPIO6 0100 0010 = Select GPIO66 The system integrator is responsible for making selection which does not collide with an existing function on the selected GPIO.

TABLE 144: OTP LOCK REGISTER

OTP_LOCK (414Eh)			OTP Lock Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7	OTP_LOCK	R/W	'0' = OTP is not locked '1' = OTP is locked from any further modification
6:0	Reserved	R	Always '0'

TABLE 145: PORT SPLIT PRTPWR1_USB3_SPLIT CONTROL SELECT

PRTPWR1_USB3_SPLIT (416Ah)			Port Split PRTPWR1_USB3_SPLIT Control Select Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:0	PORT_SPLIT_A_SELECT	R/W	This register selects which GPIO to assign the role of the PRTPWRx-_USB3_SPLIT for physical port 1 if Port Splitting is enabled for port 1. Examples: 0000 0100 = Select GPIO4 0000 0101 = Select GPIO5 0000 0110 = Select GPIO6 0100 0010 = Select GPIO66 The system integrator is responsible for making selection which does not collide with an existing function on the selected GPIO.

TABLE 146: PORT SPLIT PRTPWR2_USB3_SPLIT CONTROL SELECT

PRTPWR2_USB3_SPLIT (416Bh)			Port Split PRTPWR2_USB3_SPLIT Control Select Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:0	PORT_SPLIT_A_SELECT	R/W	This register selects which GPIO to assign the role of the PRTPWRx-_USB3_SPLIT for physical port 2 if Port Splitting is enabled for port 2. Examples: 0000 0100 = Select GPIO4 0000 0101 = Select GPIO5 0000 0110 = Select GPIO6 0100 0010 = Select GPIO66 The system integrator is responsible for making selection which does not collide with an existing function on the selected GPIO.

TABLE 147: PORT SPLIT PRTPWR3_USB3_SPLIT CONTROL SELECT

PRTPWR3_USB3_SPLIT (416Ch)			Port Split PRTPWR3_USB3_SPLIT Control Select Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:0	PORT_SPLIT_A_SELECT	R/W	This register selects which GPIO to assign the role of the PRTPWRx-_USB3_SPLIT for physical port 3 if Port Splitting is enabled for port 3. Examples: 0000 0100 = Select GPIO4 0000 0101 = Select GPIO5 0000 0110 = Select GPIO6 0100 0010 = Select GPIO66 The system integrator is responsible for making selection which does not collide with an existing function on the selected GPIO.

TABLE 148: PORT SPLIT PRTPWR4_USB3_SPLIT CONTROL SELECT

PRTPWR4_USB3_SPLIT (416Dh)			Port Split PRTPWR4_USB3_SPLIT Control Select Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:0	PORT_SPLIT_A_SELECT	R/W	This register selects which GPIO to assign the role of the PRTPWRx-_USB3_SPLIT for physical port 4 if Port Splitting is enabled for port 4. Examples: 0000 0100 = Select GPIO4 0000 0101 = Select GPIO5 0000 0110 = Select GPIO6 0100 0010 = Select GPIO66 The system integrator is responsible for making selection which does not collide with an existing function on the selected GPIO.

TABLE 149: PORT SPLIT PRTPWR5_USB3_SPLIT CONTROL SELECT

PRTPWR5_USB3_SPLIT (416Eh)			Port Split PRTPWR5_USB3_SPLIT Control Select Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:0	PORT_SPLIT_A_SELECT	R/W	This register selects which GPIO to assign the role of the PRTPWRx_USB3_SPLIT for physical port 5 if Port Splitting is enabled for port 5. Examples: 0000 0100 = Select GPIO4 0000 0101 = Select GPIO5 0000 0110 = Select GPIO6 0100 0010 = Select GPIO66 The system integrator is responsible for making selection which does not collide with an existing function on the selected GPIO.

TABLE 150: PORT SPLIT PRTPWR6_USB3_SPLIT CONTROL SELECT

PRTPWR6_USB3_SPLIT (416Fh)			Port Split PRTPWR6_USB3_SPLIT Control Select Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:0	PORT_SPLIT_A_SELECT	R/W	This register selects which GPIO to assign the role of the PRTPWRx_USB3_SPLIT for physical port 6 if Port Splitting is enabled for port 6. Examples: 0000 0100 = Select GPIO4 0000 0101 = Select GPIO5 0000 0110 = Select GPIO6 0100 0010 = Select GPIO66 The system integrator is responsible for making selection which does not collide with an existing function on the selected GPIO.

TABLE 151: PORT SPLIT PRTPWR7_USB3_SPLIT CONTROL SELECT

PRTPWR7_USB3_SPLIT (4170h)			Port Split PRTPWR7_USB3_SPLIT Control Select Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:0	PORT_SPLIT_A_SELECT	R/W	This register selects which GPIO to assign the role of the PRTPWRx_USB3_SPLIT for physical port 7 if Port Splitting is enabled for port 7. Examples: 0000 0100 = Select GPIO4 0000 0101 = Select GPIO5 0000 0110 = Select GPIO6 0100 0010 = Select GPIO66 The system integrator is responsible for making selection which does not collide with an existing function on the selected GPIO.

TABLE 152: USB3 PORT SPLIT LINK TIMEOUT

USB3_PORT_SPLIT_TIMEOUT (4171h)			USB3 Port Split Link Timeout Register Default = 05h
BIT	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2:0	PORT_SPLIT_TIME-OUT[2:0]	R/W	Global USB Port Splitting Link Timeout Value If Port Splitting is enabled on a port and there is no valid USB 3.x Link fort he configured amount of time, then the associated PRTPWRx-_USB3_SPLIT pin will be toggled in an attempt to reset the embedded USB 3.x device and re-establish the USB 3.x Link. The timer is always reset and restarted whenever the timeout occurs. 000b = No Timeout, never toggle PRTPWRx_USB3_SPLIT 001b = 100 ms 010b = 250 ms 011b = 500 ms 100b = 750 ms 101b = 1 second 110b = 2 seconds 111b = Reserved

TABLE 153: BATTERY CHARGING CDP TO SDP VBUS DISCHARGE TIME REGISTER

BC_CDP2SDP_DIS_TIME (4175h)			Battery Charging CDP to SDP VBUS Discharge Time Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:0	BC_VBUS_CDP2SD-P_DIS_TIME	R/W	Firmware variable that is used to control the VBUS discharge time during a CDP-to-SDP transition. In units of heartbeat steps (5 ms or 10 ms, depending on the setting).

TABLE 154: USB3 PORT SPLIT TOGGLE TIME

USB3_PORT_SPLIT_TOGGLE_TIME (4176h)			USB3 Port Split Toggle Time Register Default = 05h
BIT	**Name**	**R/W**	**Description**
7:0	PORT_SPLIT_TIME-OUT[7:0]	R/W	The PORT_SPLIT_TOGGLE_TIME is used to control the length of the time port power is toggled off. This is specific to the “PRTPWRx-_USB3_SPLIT” pin, and is only used in conjunction with register 4171h. The timer is always reset whenever the toggle completes. The minimum toggle time is 350 ms and is represented by 0000 0000b. Each incremental value will add 10 ms to the 350 ms minimum value.

TABLE 155: BATTERY CHARGING PORT 1 CONFIGURATION

BC_CFG_P1 (4178h)			Battery Charging Physical Port 1 Configuration Default = Depends on BC strap settings
BIT	**Name**	**R/W**	**Description**
7	BCDCP_DIS_PRTS_EN	R/W	'1' = When this port is disabled, DCP mode will be enabled on this port. The mode of operation will be determined from Bits 5:0 of this register. '0' = When the port is disabled, DCP mode will not be enabled.
6	Reserved	R	Reserved
5	BC12_CDCP	R/W	When set, enables BC 1.2 DCP mode. If Bit 4 is set, this bit will be ignored.
4	CHINA	R/W	When set, enables China mode.
3	Reserved	R	Reserved
2:1	SE1_MODE	R/W	SE1 mode sets the DP/DM signals to static voltages for charging certain devices that do not follow the BC1.2 standard. 00 = SE1 mode is disabled. 01 = SE1 1 A mode. DP = 2.0V, DM = 2.7V 10 = SE1 2 A mode. DP = 2.7V, DM = 2.0V 11 = SE1 2.5 A mode. DP = DM = 2.7V Note that when both SE1 mode and BC1.2 modes are enabled, the port will automatically switch between the two modes of operation every time a device is connected. This is mean to supply the appropriate handshake for the device. See the battery charging section in the data sheet for additional details.
0	BC_EN	R/W	'1' = Enables battery charging on port 1. '0' = Disables battery charging on port 1.

TABLE 156: BATTERY CHARGING PORT 2 CONFIGURATION

BC_CFG_P2 (4179h)			Battery Charging Physical Port 2 Configuration Default = Depends on BC strap settings
BIT	**Name**	**R/W**	**Description**
7	BCDCP_DIS_PRTS_EN	R/W	'1' = When this port is disabled, DCP mode will be enabled on this port. The mode of operation will be determined from Bits 5:0 of this register. '0' = When the port is disabled, DCP mode will not be enabled.
6	Reserved	R	Reserved
5	BC12_CDCP	R/W	When set, enables BC 1.2 DCP mode. If Bit 4 is set, this bit will be ignored.
4	CHINA	R/W	When set, this enables China mode.
3	Reserved	R	Reserved

TABLE 156: BATTERY CHARGING PORT 2 CONFIGURATION (CONTINUED)

BC_CFG_P2 (4179h)			Battery Charging Physical Port 2 Configuration Default = Depends on BC strap settings
BIT	**Name**	**R/W**	**Description**
2:1	SE1_MODE	R/W	SE1 mode sets the DP/DM signals to static voltages for charging certain devices that do not follow the BC1.2 standard. 00 = SE1 mode is disabled. 01 = SE1 1 A mode. DP = 2.0V, DM = 2.7V 10 = SE1 2 A mode. DP = 2.7V, DM = 2.0V 11 = SE1 2.5 A mode. DP = DM = 2.7V Note that when both SE1 mode and BC1.2 modes are enabled, the port will automatically switch between the two modes of operation every time a device is connected. This is mean to supply the appropriate handshake for the device. See the battery charging section in the data sheet for additional details.
0	BC_EN	R/W	'1' = Enables battery charging on port 2. '0' = Disables battery charging on port 2.

TABLE 157: BATTERY CHARGING PORT 3 CONFIGURATION

BC_CFG_P3 (417Ah)			Battery Charging Physical Port 3 Configuration Default = Depends on BC strap settings
BIT	**Name**	**R/W**	**Description**
7	BCDCP_DIS_PRTS_EN	R/W	'1' = When this port is disabled, DCP mode will be enabled on this port. The mode of operation will be determined from Bits 5:0 of this register. '0' = When the port is disabled, DCP mode will not be enabled.
6	Reserved	R	Reserved
5	BC12_CDCP	R/W	When set, enables BC 1.2 DCP mode. If Bit 4 is set, this bit will be ignored.
4	CHINA	R/W	When set, enables China mode.
3	Reserved	R	Reserved
2:1	SE1_MODE	R/W	SE1 mode sets the DP/DM signals to static voltages for charging certain devices that do not follow the BC1.2 standard. 00 = SE1 mode is disabled. 01 = SE1 1 A mode. DP = 2.0V, DM = 2.7V 10 = SE1 2 A mode. DP = 2.7V, DM = 2.0V 11 = SE1 2.5 A mode. DP = DM = 2.7V Note that when both SE1 mode and BC1.2 modes are enabled, the port will automatically switch between the two modes of operation every time a device is connected. This is mean to supply the appropriate handshake for the device. See the battery charging section in the data sheet for additional details.
0	BC_EN	R/W	'1' = Enables battery charging on port 3. '0' = Disables battery charging on port 3.

TABLE 158: BATTERY CHARGING PORT 4 CONFIGURATION

BC_CFG_P4 (417Bh)			Battery Charging Physical Port 4 Configuration Default = Depends on BC strap settings
BIT	**Name**	**R/W**	**Description**
7	BCDCP_DIS_PRTS_EN	R/W	'1' = When this port is disabled, DCP mode will be enabled on this port. The mode of operation will be determined from Bits 5:0 of this register. '0' = When the port is disabled, DCP mode will not be enabled.
6	Reserved	R	Reserved
5	BC12_CDCP	R/W	When set, enables BC 1.2 DCP mode. If Bit 4 is set, this bit will be ignored.
4	CHINA	R/W	When set, enables China mode.
3	Reserved	R	Reserved
2:1	SE1_MODE	R/W	SE1 mode sets the DP/DM signals to static voltages for charging certain devices that do not follow the BC1.2 standard. 00 = SE1 mode is disabled. 01 = SE1 1 A mode. DP = 2.0V, DM = 2.7V 10 = SE1 2 A mode. DP = 2.7V, DM = 2.0V 11 = SE1 2.5 A mode. DP = DM = 2.7V Note that when both SE1 mode and BC1.2 modes are enabled, the port will automatically switch between the two modes of operation every time a device is connected. This is mean to supply the appropriate handshake for the device. See the battery charging section in the data sheet for additional details.
0	BC_EN	R/W	'1' = Enables battery charging on port 4. '0' = Disables battery charging on port 4.

TABLE 159: BATTERY CHARGING PORT 5 CONFIGURATION

BC_CFG_P5 (417Ch)			Battery Charging Physical Port 5 Configuration Default = Depends on BC strap settings
BIT	**Name**	**R/W**	**Description**
7	BCDCP_DIS_PRTS_EN	R/W	'1' = When this port is disabled, DCP mode will be enabled on this port. The mode of operation will be determined from Bits 5:0 of this register. '0' = When the port is disabled, DCP mode will not be enabled.
6	Reserved	R	Reserved
5	BC12_CDCP	R/W	When set, enables BC 1.2 DCP mode. If Bit 4 is set, this bit will be ignored.
4	CHINA	R/W	When set, enables China mode.
3	Reserved	R	Reserved

TABLE 159: BATTERY CHARGING PORT 5 CONFIGURATION (CONTINUED)

BC_CFG_P5 (417Ch)			Battery Charging Physical Port 5 Configuration Default = Depends on BC strap settings
BIT	**Name**	**R/W**	**Description**
2:1	SE1_MODE	R/W	SE1 mode sets the DP/DM signals to static voltages for charging certain devices that do not follow the BC1.2 standard. 00 = SE1 mode is disabled. 01 = SE1 1 A mode. DP = 2.0V, DM = 2.7V 10 = SE1 2 A mode. DP = 2.7V, DM = 2.0V 11 = SE1 2.5 A mode. DP = DM = 2.7V Note that when both SE1 mode and BC1.2 modes are enabled, the port will automatically switch between the two modes of operation every time a device is connected. This is mean to supply the appropriate handshake for the device. See the battery charging section in the data sheet for additional details.
0	BC_EN	R/W	'1' = Enables battery charging on port 4. '0' = Disables battery charging on port 4.

TABLE 160: BATTERY CHARGING PORT 6 CONFIGURATION

BC_CFG_P6 (417Dh)			Battery Charging Physical Port 6 Configuration Default = Depends on BC strap settings
BIT	**Name**	**R/W**	**Description**
7	BCDCP_DIS_PRTS_EN	R/W	'1' = When this port is disabled, DCP mode will be enabled on this port. The mode of operation will be determined from Bits 5:0 of this register. '0' = When the port is disabled, DCP mode will not be enabled.
6	Reserved	R	Reserved
5	BC12_CDCP	R/W	When set, enables BC 1.2 DCP mode. If Bit 4 is set, this bit will be ignored.
4	CHINA	R/W	When set, enables China mode.
3	Reserved	R	Reserved
2:1	SE1_MODE	R/W	SE1 mode sets the DP/DM signals to static voltages for charging certain devices that do not follow the BC1.2 standard. 00 = SE1 mode is disabled. 01 = SE1 1 A mode. DP = 2.0V, DM = 2.7V 10 = SE1 2 A mode. DP = 2.7V, DM = 2.0V 11 = SE1 2.5 A mode. DP = DM = 2.7V Note that when both SE1 mode and BC1.2 modes are enabled, the port will automatically switch between the two modes of operation every time a device is connected. This is mean to supply the appropriate handshake for the device. See the battery charging section in the data sheet for additional details.
0	BC_EN	R/W	'1' = Enables battery charging on port 4. '0' = Disables battery charging on port 4.

TABLE 161: BATTERY CHARGING PORT 7 CONFIGURATION

BC_CFG_P7 (417Eh)			Battery Charging Physical Port 7 Configuration Default = Depends on BC strap settings
BIT	**Name**	**R/W**	**Description**
7	BCDCP_DIS_PRTS_EN	R/W	'1' = When this port is disabled, DCP mode will be enabled on this port. The mode of operation will be determined from Bits 5:0 of this register. '0' = When the port is disabled, DCP mode will not be enabled.
6	Reserved	R	Reserved
5	BC12_CDCP	R/W	When set, enables BC 1.2 DCP mode. If Bit 4 is set, this bit will be ignored.
4	CHINA	R/W	When set, enables China mode.
3	Reserved	R	Reserved
2:1	SE1_MODE	R/W	SE1 mode sets the DP/DM signals to static voltages for charging certain devices that do not follow the BC1.2 standard. 00 = SE1 mode is disabled. 01 = SE1 1 A mode. DP = 2.0V, DM = 2.7V 10 = SE1 2 A mode. DP = 2.7V, DM = 2.0V 11 = SE1 2.5 A mode. DP = DM = 2.7V Note that when both SE1 mode and BC1.2 modes are enabled, the port will automatically switch between the two modes of operation every time a device is connected. This is mean to supply the appropriate handshake for the device. See the battery charging section in the data sheet for additional details.
0	BC_EN	R/W	'1' = Enables battery charging on port 4. '0' = Disables battery charging on port 4.

TABLE 162: HUB FEATURE CONTROLLER BCD USB LSB REGISTER

HFC_BCD_USB_LSB (42D0h)			Hub Feature Controller BCD USB LSB Register Default = 01h
BIT	**Name**	**R/W**	**Description**
7:0	HFC_BCD_USB_LSB	R/W	Least Significant Byte of the USB Specification indicated for the Hub Feature Controller (UDC) device.

TABLE 163: HUB FEATURE CONTROLLER BCD USB MSB REGISTER

HFC_BCD_USB_MSB (42D1h)			Hub Feature Controller BCD USB MSB Register Default = 02h
BIT	**Name**	**R/W**	**Description**
7:0	HFC_BCD_USB_MSB	R/W	Most Significant Byte of the USB Specification indicated for the Hub Feature Controller (UDC) device.

TABLE 164: HUB FEATURE CONTROLLER VENDOR ID LSB

HFC_VID_LSB (42D6h)			Hub Feature Controller Vendor ID LSB Default = 24h
BIT	**Name**	**R/W**	**Description**
7:0	HFC_VID_LSB	R/W	Least Significant Byte of the Hub Feature Controller Vendor ID. This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB Interface Forum).

TABLE 165: HUB FEATURE CONTROLLER VENDOR ID MSB

HFC_VID_MSB (42D7h)			Hub Feature Controller Vendor ID MSB Default = 04h
BIT	**Name**	**R/W**	**Description**
7:0	HFC_VID_MSB	R/W	Most Significant Byte of the Hub Feature Controller Vendor ID. This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB Interface Forum).

TABLE 166: HUB FEATURE CONTROLLER PRODUCT ID LSB

HFC_PID_LSB (42D8h)			Hub Feature Controller Product ID LSB Default = 40h
BIT	**Name**	**R/W**	**Description**
7:0	HFC_PID_LSB	R/W	Least Significant Byte of the Hub Feature Controller Product ID. This is a 16-bit value that the Vendor can assign to uniquely identify this particular product (assigned by OEM).

TABLE 167: HUB FEATURE CONTROLLER PRODUCT ID MSB

HFC_PID_MSB (42D9h)			Hub Feature Controller Product ID MSB Default = 28h
BIT	**Name**	**R/W**	**Description**
7:0	HFC_PID_MSB	R/W	Most Significant Byte of the Hub Feature Controller Product ID. This is a 16-bit value that the Vendor can assign to uniquely identify this particular product (assigned by OEM).

TABLE 168: HUB FEATURE CONTROLLER DEVICE ID LSB

HFC_DID_LSB (42DAh)			Hub Feature Controller Product ID LSB Default = Depends on device firmware/silicon revision
BIT	**Name**	**R/W**	**Description**
7:0	HFC_DID_LSB	R/W	Least Significant Byte of the Hub Feature Controller Device ID. This is a 16-bit device release number in BCD format (assigned by OEM).

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TABLE 169: HUB FEATURE CONTROLLER DEVICE ID MSB

HFC_DID_MSB (42DBh)			Hub Feature Controller Product ID MSB Default = Depends on device firmware/silicon revision
BIT	**Name**	**R/W**	**Description**
7:0	HFC_DID_MSB	R/W	Most Significant Byte of the Hub Feature Controller Device ID. This is a 16-bit device release number in BCD format (assigned by OEM).

TABLE 170: USB 3.0 HUB BCD USB LSB REGISTER

USB3_BCD_USB_LSB (4442h)			USB 3.0 Hub BCD USB LSB Register Default = 02h
BIT	**Name**	**R/W**	**Description**
7:0	USB3_BCD_USB_LSB	R/W	Least Significant Byte of the USB Specification indicated for the USB3 Hub

TABLE 171: USB 3.0 HUB BCD USB MSB REGISTER

USB3_BCD_USB_MSB (4443h)			USB 3.0 Hub BCD USB MSB Register Default = 03h
BIT	**Name**	**R/W**	**Description**
7:0	USB3_BCD_USB_MSB	R/W	Most Significant Byte of the USB Specification indicated for the USB3 Hub

TABLE 172: USB 3.0 HUB VENDOR ID LSB

USB3_VID_LSB (4448h)			USB 3.0 Hub Vendor ID LSB Default = 24h
BIT	**Name**	**R/W**	**Description**
7:0	USB3_VID_LSB	R/W	Least Significant Byte of the USB3 Hub Vendor ID. This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB Interface Forum). Note that if this register is modified, the contents of the USB 2.0 Hub Vendor ID MSB register must also be identically modified.

TABLE 173: USB 3.0 HUB VENDOR ID MSB

USB3_VID_MSB (4449h)			USB 3.0 Hub Vendor ID MSB Default = 04h
BIT	**Name**	**R/W**	**Description**
7:0	USB3_VID_MSB	R/W	Most Significant Byte of the USB3 Hub Vendor ID. This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB Interface Forum). Note that if this register is modified, the contents of the USB 2.0 Hub Vendor ID MSB register must also be identically modified.

TABLE 174: USB 3.0 HUB PRODUCT ID LSB

USB3_PID_LSB (444Ah)			USB 3.0 Hub Product ID LSB Default = 07h for USB5807, 06h for USB5806/USB5906, 16h for USB5816/USB5916, 26h for USB5826/USB5926
BIT	**Name**	**R/W**	**Description**
7:0	USB3_PID_LSB	R/W	Least Significant Byte of the USB3 Hub Product ID. This is a 16-bit value that the Vendor can assign to uniquely identify this particular product (assigned by OEM).

TABLE 175: USB 3.0 HUB PRODUCT ID MSB

USB3_PID_MSB (444Bh)			USB 3.0 Hub Product ID MSB Default = 58h for USB5807/USB5806/USB5816/USB5826, 59h for USB5907/USB5906/USB5916/USB5926,
BIT	**Name**	**R/W**	**Description**
7:0	USB3_PID_MSB	R/W	Most Significant Byte of the USB3 Hub Product ID. This is a 16-bit value that the Vendor can assign to uniquely identify this particular product (assigned by OEM).

TABLE 176: USB 3.0 HUB DEVICE ID LSB

USB3_DID_LSB (444Ch)			USB 3.0 Hub Product ID LSB Default = Varies by firmware and silicon revision
BIT	**Name**	**R/W**	**Description**
7:0	USB3_DID_LSB	R/W	Least Significant Byte of the USB3 Hub Device ID. This is a 16-bit device release number in BCD format (assigned by OEM).

TABLE 177: USB 3.0 HUB DEVICE ID MSB

USB3_DID_MSB (444Dh)			USB 3.0 Hub Product ID MSB Default = Varies by firmware and silicon revision
BIT	**Name**	**R/W**	**Description**
7:0	USB3_DID_MSB	R/W	Most Significant Byte of the USB3 Hub Device ID. This is a 16-bit device release number in BCD format (assigned by OEM).

TABLE 178: USB 3.0 NUMBER OF PORTS

USB3_NBR_PRTS (44A2h)			USB 3.0 Number of Ports Default = 07h if USB5807, 06h if USB5806/USB95906 05h if USB5816/USB5916 04h if USB5826/USB5926
BIT	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
0:3	Number of Ports	R/W	111 = 7 Ports Enabled 110 = 6 Ports Enabled 101 = 5 Ports Enabled 100 = 4 Ports Enabled 011 = 3 Ports Enabled 010 = 2 Ports Enabled 001 = 1 Port Enabled 000 = No Ports Enabled If this register is modified, the specific ports to be disabled must be modified in their respective port configuration registers.

TABLE 179: USB 3.0 HUB COMPOUND DEVICE

USB3_COMPOUND (44A3h)			USB 3.0 Hub Compound Device Default = 09h
BIT	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2	COMPOUND_DEVICE	R/W	0 = Hub is not part of a compound device. 1 = Hus is part of a compound device. If this register is modified, the USB 2.0 Hub equivalent must also be modified in the USB 2.0 Hub Configuration 2 register.
1:0	Reserved	R	Reserved

TABLE 180: USB 3.0 HUB POWER ON-TO-POWER GOOD DESCRIPTOR

USB3_BPWRON2PWRGOOD (44A5h)			USB 3.0 Hub Power On-to-Power Good Default = FFh
BIT	**Name**	**R/W**	**Description**
7:0	USB3_HUB_PWR2PWR-GOOD	R/W	Time in 2 ms intervals from the time the power-on sequence begins on a port until power is good on that port. The USB system software uses this value to determine how long to wait before accessing a powered-on port.This value should be set to zero if power switching is not supported in the system design.

TABLE 181: USB 3.0 HUB NON-REMOVABLE DEVICE

USB3_NRD (44AAh)			USB 3.0 Hub Non-Removable Device (Note 11)
BIT	**Name**	**R/W**	**Description**
7:1	NR_DEVICE	R/W	Non-Removable Device: Indicates which port(s) include non-removable devices. ‘0’ = port is removable; ‘1’ = port is non-removable. It informs the host if one of the active ports has a permanent device that is undetachable from the hub. The ports may also be configured as non-removable using the hardware strapping option described in the data sheet. Bit 7 = 1; Logical port 7 non-removable Bit 6 = 1; Logical port 6 non-removable Bit 5 = 1; Logical port 5 non-removable Bit 4 = 1; Logical port 4 non-removable Bit 3 = 1; Logical port 3 non-removable Bit 2 = 1; Logical port 2 non-removable Bit 1 = 1; Logical port 1 non removable If this register is modified, the USB 2.0 Hub equivalent must also be modified in the register.
0	Reserved	R	Reserved

TABLE 182: USB3 PORT 0 TX PRE-DRIVER

SS_P0_AFE_TEST_IN4 (6086h)			USB3 Physical Port 0 TX Pre-Driver Default = 00h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved. Do not modify.
2:1	Length	R/W	Physical port 0 transmitter pre-driver current adjust 00 = 100 µA (default biasing) 01 = 125 µA 10 = 87.5 µA 11 =112.5 µA
0	Reserved	R	Reserved. Do not modify.

TABLE 183: USB 2.0 UPSTREAM RISE-AND-FALL ADJUSTMENT REGISTER

UP_RISEFALL_ADJ (60C8h)			USB 2.0 Upstream Rise-and-Fall Adjust Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3:2	HS_TX_RISEFALL_ADJUST	R/W	High-Speed TX Rise/Fall adjust 00 = Default 01 = +18% 10 = –18% 11 = –12%
1:0	LS_TX_RISEFALL_ADJUST	R/W	Low-Speed/Full-Speed TX Rise/Fall adjust 00 =Default 01 = +100% 10 = –30% 11 = –50%

TABLE 184: USB 2.0 UPSTREAM PHYBOOST REGISTER

HS_UP_BOOST (60CAh)			USB 2.0 Upstream PHYBoost Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2:0	HS_BOOST	R/W	HS Output Current Adjustment 000b = Nominal 001b = Decrease by 5% 00b = Increase by 10% 011b = Increase by 5% 100b = Increase by 20% 101b = Increase by 15% 110b = Increase by 30% 111b = Increase by 25%

TABLE 185: USB 2.0 UPSTREAM VARISENSE REGISTER

HS_UP_SENSE (60CCh)			USB 2.0 Upstream VariSense Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE		USB 2.0 AFE HS Disconnect Tune – Revision C silicon only Allows the HS disconnect threshold to be increased. Recommended to only be used when PHYBoost is also set. 0 = Nominal 575 mV Trip Point 1 = Increase by 50 mV 2 = Increase by 100 mV 3 = Increase by 125 mV
5:3	Reserved	R	Reserved
2:0	HS_SENSE	R/W	HS VariSense Tune (Squelch Tune) 000b = Nominal (100 mV Trip Point) 001b = Decrease by 12.5 mV 00b = Decrease by 25 mV 011b = Decrease by 37.5 mV 100b = Decrease by 50 mV 101b = Decrease by 62.5 mV 110b = Increase by 25 mV 111b = Increase by 12.5 mV

TABLE 186: USB3 UPSTREAM LTSSM STATE

SS_P0_LTSSM_State (61C0h)			USB3 Upstream Physical Port 0 LTSSM State Default = Depends on device operation state
Bit	**Name**	**R/W**	**Description**
7:4	LTSSM_STATE	R	Physical Port 0 LTSSM state 0000b = U0 (no sub-states) 0001b = U1 (no sub-states) 0010b = U2 (no sub-states) 0011b = U3 (no sub-states) 0100b = SIS.Disabled (see sub-state below) 0101b = Rx.Detect (see sub-state below) 0110b = SS.Inactive (see sub-state below) 0111b = Polling (see sub-state below) 1000b = Recovery (see sub-state below) 1001b = HotReset (see sub-state below) 1010b = Compliance (no sub-states) 1011b = Loopback (no sub-states)
3	Reserved	R	Always ‘0’

TABLE 186: USB3 UPSTREAM LTSSM STATE (CONTINUED)

SS_P0_LTSSM_State (61C0h)			USB3 Upstream Physical Port 0 LTSSM State Default = Depends on device operation state
Bit	**Name**	**R/W**	**Description**
2:0	LTSSM_SUB_STATE	R	Physical Port 0 LTSSM sub-state. Undefined values are invalid. SIS.Disabled sub-states: 000b = SSD.Power3 001b = SSD.Power3A 010b = SSD.Main Rx.Detect sub-states: 000b = Rx.Detect.Init 001b = Rx.Detect.Power2 010b = Rx.Detect.Reset 011b = Rx.Detect.Reset_T 100b = Rx.Detect.Active0 101b = Rx.Detect.Active1 110b = Rx.Detect.Quiet SS.Inactive sub-states: 000b = SS.Inactive.Reset 001b = SS.Inactive.Power2 010b = SS.Inactive.Quite0 011b = SS.Inactive.Quiet1 100b = SS.Inactive.Disconnect.Detect0 100b = SS.Inactive.Disconnect.Detect1 Polling sub-states: 000b = Polling.Reset 001b = Polling.Power0 010b = Polling.LFPS 011b = Polling.RxEQ 100b = Polling.Active 101b = Polling.Configuration 110b = Polling.Idle Recovery sub-states: 000b = Recovery.Reset 001b = Recovery.Power0 010b = Recovery.Active 011b = Recovery.Cofiguration 100b = Recovery.Idle HotReset sub-states: 000b = HotReset.Reset 001b = HotReset.Go 010b = HotReset.Active1 011b = HotReset.Active2 100b = HotReset.Exit

TABLE 187: USB3 UPSTREAM DC TEST REGISTER

SS_PO_TEST_PIPE_DC (61C1h)			USB3 Upstream Physical Port 0 DC Test Register Default = 00h
Bit	**Name**	**R/W**	**Description**
7	PIPE_TX_DE-TR_LPBK	R/W	Transmit Detect Receiver and Loopback Mode. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. Used to tell the PHY to begin receiver loopback or to signal LFPS during polling.
6	PIPE_RX_TERMINA-TION	R/W	Receiver Termination Control. This signal is asynchronous. Controls presence of receiver terminations. ‘0’ = Terminations removed ‘1’ = Terminations present
5:4	PIPE_TX_DEEMPH	R/W	Transmit De-Emphasis Level Control. This signal is synchronous. 00 = –6.0 dB de-emphasis (Normal mode) 01 = –3.5 dB 10 = None 11 = Reserved
3	PIPE_TX_SWING	R/W	Transmit Swing Control. This signal is asynchronous. 0 = Full Swing 1 = Low Swing
2	PIPE_TX-C_DRIVE_HI GH	R/W	Set the DC State of the TX Output. 0: TXP = 0, TXN = 1 1: TXP = 1, TXN = 0
1	PIPE_TXDC_EN ABLE	R/W	Enable Transmitter DC Drive Mode.
0	PIPE_TX_ELEC_I-DLE	R/W	Transmit Electrical Idle. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. This signal is used in conjunction with pow-er_down[1:0] and tx_detrx_lpbk to set the state of the transmitter (either Normal Transmit mode, electrical idle, LFPS transmission, or receiver detection).

TABLE 188: USB3 UPSTREAM TX TEST PATTERN REGISTER

SS_PO_TEST_PIPE_TX_PAT (61C3h)			USB3 Upstream Physical Port 0 TX Pattern Register Default = 00h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always ‘0’
4	PIPE_TX_CGEN_EN	R/W	Internal Transmit Pattern Generator Enable. This signal is asynchronous. ‘0’ = Disable pattern generator (Normal mode. Transmit data driven over the tx_data interface) ‘1’ = Enable pattern generator

TABLE 188: USB3 UPSTREAM TX TEST PATTERN REGISTER (CONTINUED)

SS_PO_TEST_PIPE_TX_PAT (61C3h)			USB3 Upstream Physical Port 0 TX Pattern Register Default = 00h
Bit	**Name**	**R/W**	**Description**
3:0	PIPE_TX_CPGEN_-SEL	R/W	Internal Transmit Pattern Generator Select. This signal is asynchronous. 0 = CP0 (D0.0, scrambled, no SKP) 1 = CP1 (D10.2, Nyquist frequency) 2 = CP2 (D24.3, Nyquist/2 frequency) 3 = CP3 (K28.5, COM pattern) 4 = CP4 (LFPS) 5 = CP5 (K28.7, with de-emphasis) 6 = CP5 (K28.7, without de-emphasis) 7 = CP7 (50-250 1's and 0's, with de-emphasis) 8 = CP8 (50-250 1's and 0's, no de-emphasis) 9 = TSEQ 10 = TS1 11 = TS2 12 = Logical Idles (D0.0) 13 to 15 = Reserved

TABLE 189: USB3 UPSTREAM TX_MARGIN

SS_PO_TEST_PIPE_CTL_0 (61D0h)			USB3 Upstream Physical Port 0 TX Margin Default = 00h
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always ‘0’ (do not modify)
6:4	Length	R/W	Physical port 0 transmitter biasing and amplitude adjust 000 = 0% change (default) 001 = +11% 010 = +21% 011 =+33% 100 = –67% 101 = –64% 110 = –61% 111 = –57%
3:0	Reserved	R	Always ‘0’ (do not modify)

TABLE 190: USB3 PORT 1 TX PRE-DRIVER

SS_P1_AFE_TEST_IN4 (6486h)			USB3 Physical Port 1 TX Pre-Driver Default = 00h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved. Do not modify.
2:1	Length	R/W	Physical port 1 transmitter pre-driver current adjust 00 = 100 µA (default biasing) 01 = 125 µA 10 = 87.5 µA 11 = 112.5 µA
0	Reserved	R	Reserved. Do not modify.

TABLE 191: USB 2.0 DOWNSTREAM PORT 1 RISE-AND-FALL ADJUSTMENT REGISTER

P1_RISE_FALL_ADJ (64C8h)			USB 2.0 Downstream Physical Port 1 Rise/Fall Adjust Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3:2	HS_TX_RISEFALL_ADJUST	R/W	High-Speed TX Rise/Fall adjust 00 = Default 01 = +18% 10 = –18% 11 = –12%
1:0	LS_TX_RISEFALL_ADJUST	R/W	Low-Speed/Full-Speed TX Rise/Fall adjust 00 = Default 01 = +100% 10 = –30% 11 = –50%

TABLE 192: USB 2.0 DOWNSTREAM PORT 1 PHYBOOST REGISTER

HS_P1_BOOST (64CAh)			USB 2.0 Downstream Physical Port 1 PHYBoost Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2:0	HS_BOOST	R/W	HS Output Current Adjustment 000b = Nominal 001b = Decrease by 5% 00b = Increase by 10% 011b = Increase by 5% 100b = Increase by 20% 101b = Increase by 15% 110b = Increase by 30% 111b = Increase by 25%

TABLE 193: USB 2.0 DOWNSTREAM PORT 1 VARISENSE REGISTER

HS_P1_SENSE (64CCh)			USB 2.0 Downstream Physical Port 1 VariSense Register
BIT	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE	R/W	USB 2.0 AFE HS Disconnect Tune - revision C silicon only Allows the HS disconnect threshold to be increased. Recommended to only be used when PHYBoost is also set. 0 = Nominal 575 mV Trip Point 1 = Increase by 50 mV 2 = Increase by 100 mV 3 = Increase by 125 mV
5:3	Reserved	R	Reserved

TABLE 193: USB 2.0 DOWNSTREAM PORT 1 VARISENSE REGISTER (CONTINUED)

HS_P1_SENSE (64CCh)			USB 2.0 Downstream Physical Port 1 VariSense Register
BIT	**Name**	**R/W**	**Description**
2:0	HS_SENSE	R/W	HS VariSense Tune (Squelch Tune) 000b = Nominal (100 mV Trip Point) 001b = Decrease by 12.5 mV 00b = Decrease by 25 mV 011b = Decrease by 37.5 mV 100b = Decrease by 50 mV 101b = Decrease by 62.5 mV 110b = Increase by 25 mV 111b = Increase by 12.5 mV

TABLE 194: USB3 PORT 1 LTSSM STATE

SS_P1_LTSSM_State (65C0h)			USB3 Physical Port 1 LTSSM State Default = Depends on device operation state
Bit	**Name**	**R/W**	**Description**
7:4	LTSSM_STATE	R	Physical Port 1 LTSSM state 0000b = U0 (no sub-states) 0001b = U1 (no sub-states) 0010b = U2 (no sub-states) 0011b = U3 (no sub-states) 0100b = SIS.Disabled (See sub-state below.) 0101b = Rx.Detect (See sub-state below.) 0110b = SS.Inactive (See sub-state below.) 0111b = Polling (See sub-state below.) 1000b = Recovery (See sub-state below.) 1001b = HotReset (See sub-state below.) 1010b = Compliance (no sub-states) 1011b = Loopback (no sub-states)
3	Reserved	R	Always ‘0’

TABLE 194: USB3 PORT 1 LTSSM STATE

SS_P1_LTSSM_State (65C0h)			USB3 Physical Port 1 LTSSM State Default = Depends on device operation state
Bit	**Name**	**R/W**	**Description**
2:0	LTSSM_SUB_STATE	R	Physical Port 1 LTSSM sub-state. Undefined values are invalid. SIS.Disabled sub-states: 000b = SSD.Power3 001b = SSD.Power3A 010b = SSD.Main Rx.Detect sub-states: 000b = Rx.Detect.Init 001b = Rx.Detect.Power2 010b = Rx.Detect.Reset 011b = Rx.Detect.Reset_T 100b = Rx.Detect.Active0 101b = Rx.Detect.Active1 110b = Rx.Detect.Quiet SS.Inactive sub-states: 000b = SS.Inactive.Reset 001b = SS.Inactive.Power2 010b = SS.Inactive.Quite0 011b = SS.Inactive.Quiet1 100b = SS.Inactive.Disconnect.Detect0 100b = SS.Inactive.Disconnect.Detect1 Polling sub-states: 000b = Polling.Reset 001b = Polling.Power0 010b = Polling.LFPS 011b = Polling.RxEQ 100b = Polling.Active 101b = Polling.Configuration 110b = Polling.Idle Recovery sub-states: 000b = Recovery.Reset 001b = Recovery.Power0 010b = Recovery.Active 011b = Recovery.Cofiguration 100b = Recovery.Idle HotReset sub-states: 000b = HotReset.Reset 001b = HotReset.Go 010b = HotReset.Active1 011b = HotReset.Active2 100b = HotReset.Exit

TABLE 195: USB3 PORT 1 DC TEST REGISTER

SS_P1_TEST_PIPE_DC (65C1h)			USB3 Physical Port 1 DC Test Register Default = 00h
Bit	**Name**	**R/W**	**Description**
7	PIPE_TX_DE-TR_LPBK	R/W	Transmit Detect Receiver and Loopback Mode. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. Used to tell the PHY to begin receiver loopback or to signal LFPS during polling.
6	PIPE_RX_TERMINA-TION	R/W	Receiver Termination Control. This signal is asynchronous. Controls presence of receiver terminations. ‘0’ = Terminations removed ‘1’ = Terminations present
5:4	PIPE_TX_DEEMPH	R/W	Transmit De-Emphasis Level Control. This signal is synchronous. 00 = –6.0dB de-emphasis (Normal mode) 01 = –3.5dB 10 = None 11 = reserved
3	PIPE_TX_SWING	R/W	Transmit Swing Control. This signal is asynchronous. ‘0’ = Full Swing ‘ ‘1’ = Low Swing
2	PIPE_TX-C_DRIVE_HI GH	R/W	Set the DC State of the TX Output. 0: TXP = 0, TXN = 1 1: TXP = 1, TXN = 0
1	PIPE_TXDC_EN ABLE	R/W	Enable Transmitter DC Drive mode.
0	PIPE_TX_ELEC_I-DLE	R/W	Transmit Electrical Idle. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. This signal is used in conjunction with pow-er_down[1:0] and tx_detrx_lpbk to set the state of the transmitter (either normal transmit mode, electrical idle, LFPS transmission, or receiver detection).

TABLE 196: USB3 PORT 1 TX TEST PATTERN REGISTER

SS_P1_TEST_PIPE_TX_PAT (65C3h)			USB3 Physical Port 1 TX Pattern Register Default = 00h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always ‘0’
4	PIPE_TX_CGEN_EN	R/W	Internal Transmit Pattern Generator Enable. This signal is asynchronous. ‘0’ = Disable pattern generator (Normal mode. Transmit data driven over the tx_data interface) ‘1’ = Enable pattern generator

TABLE 196: USB3 PORT 1 TX TEST PATTERN REGISTER (CONTINUED)

SS_P1_TEST_PIPE_TX_PAT (65C3h)			USB3 Physical Port 1 TX Pattern Register Default = 00h
Bit	**Name**	**R/W**	**Description**
3:0	PIPE_TX_CPGEN_-SEL	R/W	Internal Transmit Pattern Generator Select. This signal is asynchronous. 0 = CP0 (D0.0, scrambled, no SKP) 1 = CP1 (D10.2, Nyquist frequency) 2 = CP2 (D24.3, Nyquist/2 frequency) 3 = CP3 (K28.5, COM pattern) 4 = CP4 (LFPS) 5 = CP5 (K28.7, with de-emphasis) 6 = CP5 (K28.7, without de-emphasis) 7 = CP7 (50-250 1's and 0's, with de-emphasis) 8 = CP8 (50-250 1's and 0's, no de-emphasis) 9 = TSEQ 10 = TS1 11 = TS2 12 = Logical Idles (D0.0) 13 to 15 = Reserved

TABLE 197: USB3 PORT 1 TX_MARGIN

SS_P1_TEST_PIPE_CTL_0 (65D0h)			USB3 Physical Port 1 TX Margin Default = 00h
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always ‘0’ (Do not modify.)
6:4	Length	R/W	Physical port 1 transmitter biasing and amplitude adjust 000 = 0% change (default) 001 = +11% 010 = +21% 011 = +33% 100 = –67% 101 = –64% 110 = –61% 111 = –57%
3:0	Reserved	R	Always ‘0’ (Do not modify.)

TABLE 198: USB3 PORT 2 TX PRE-DRIVER

SS_P2_AFE_TEST_IN4 (6886h)			USB3 Physical Port 2 TX Pre-Driver Default = 00h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved. Do not modify.
2:1	Length	R/W	Physical port 2 transmitter pre-driver current adjust 00 = 100 µA (default biasing) 01 = 125 µA 10 = 87.5 µA 11 = 112.5 µA
0	Reserved	R	Reserved. Do not modify.

TABLE 199: USB 2.0 DOWNSTREAM PORT 2 RISE-AND-FALL ADJUSTMENT REGISTER

P2_RISEFALL_ADJ (68C8h)			USB 2.0 Downstream Physical Port 2 Rise/Fall Adjust Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3:2	HS_TX_RISEFALL_ADJUST	R/W	High-Speed TX Rise/Fall adjust. 00 = Default 01 = +18% 10 = –18% 11 = –12%
1:0	LS_TX_RISEFALL_ADJUST	R/W	Low-Speed/Full-Speed TX Rise/Fall adjust. 00 = Default 01 = +100% 10 = –30% 11 = –50%

TABLE 200: USB 2.0 DOWNSTREAM PORT 2 PHYBOOST REGISTER

HS_P2_BOOST (68CAh)			USB 2.0 Downstream Physical Port 2 PHYBoost Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2:0	HS_BOOST	R/W	HS Output Current Adjustment 000b = Nominal 001b = Decrease by 5% 00b = Increase by 10% 011b = Increase by 5% 100b = Increase by 20% 101b = Increase by 15% 110b = Increase by 30% 111b = Increase by 25%

TABLE 201: USB 2.0 DOWNSTREAM PORT 2 VARISENSE REGISTER

HS_P2_SENSE (68CCh)			USB 2.0 Downstream Physical Port 2 VariSense Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE		USB 2.0 AFE HS Disconnect Tune – Revision C silicon only Allows the HS disconnect threshold to be increased. Recommended to only be used when PHYBoost is also set. 0 = Nominal 575 mV Trip Point 1 = Increase by 50 mV 2 = Increase by 100 mV 3 = Increase by 125 mV
5:3	Reserved	R	Reserved

TABLE 201: USB 2.0 DOWNSTREAM PORT 2 VARISENSE REGISTER (CONTINUED)

HS_P2_SENSE (68CCh)			USB 2.0 Downstream Physical Port 2 VariSense Register Default = 00h
BIT	**Name**	**R/W**	**Description**
2:0	HS_SENSE	R/W	HS VariSense Tune (Squelch Tune) 000b = Nominal (100 mV Trip Point) 001b = Decrease by 12.5 mV 00b = Decrease by 25 mV 011b = Decrease by 37.5 mV 100b = Decrease by 50 mV 101b = Decrease by 62.5 mV 110b = Increase by 25 mV 111b = Increase by 12.5 mV

TABLE 202: USB3 PORT 2 LTSSM STATE

SS_P2_LTSSM_State (69C0h)			USB3 Physical Port 2 LTSSM State Default = Depends on device operation state
Bit	**Name**	**R/W**	**Description**
7:4	LTSSM_STATE	R	Physical Port 2 LTSSM state 0000b = U0 (no sub-states) 0001b = U1 (no sub-states) 0010b = U2 (no sub-states) 0011b = U3 (no sub-states) 0100b = SIS.Disabled (See sub-state below.) 0101b = Rx.Detect (See sub-state below.) 0110b = SS.Inactive (See sub-state below.) 0111b = Polling (See sub-state below.) 1000b = Recovery (See sub-state below.) 1001b = HotReset (See sub-state below.) 1010b = Compliance (no sub-states) 1011b = Loopback (no sub-states)
3	Reserved	R	Always ‘0’

TABLE 202: USB3 PORT 2 LTSSM STATE

SS_P2_LTSSM_State (69C0h)			USB3 Physical Port 2 LTSSM State Default = Depends on device operation state
Bit	**Name**	**R/W**	**Description**
2:0	LTSSM_SUB_STATE	R	Physical Port 2 LTSSM sub-state. Undefined values are invalid. SIS.Disabled sub-states: 000b = SSD.Power3 001b = SSD.Power3A 010b = SSD.Main Rx.Detect sub-states: 000b = Rx.Detect.Init 001b = Rx.Detect.Power2 010b = Rx.Detect.Reset 011b = Rx.Detect.Reset_T 100b = Rx.Detect.Active0 101b = Rx.Detect.Active1 110b = Rx.Detect.Quiet SS.Inactive sub-states: 000b = SS.Inactive.Reset 001b = SS.Inactive.Power2 010b = SS.Inactive.Quite0 011b = SS.Inactive.Quiet1 100b = SS.Inactive.Disconnect.Detect0 100b = SS.Inactive.Disconnect.Detect1 Polling sub-states: 000b = Polling.Reset 001b = Polling.Power0 010b = Polling.LFPS 011b = Polling.RxEQ 100b = Polling.Active 101b = Polling.Configuration 110b = Polling.Idle Recovery sub-states: 000b = Recovery.Reset 001b = Recovery.Power0 010b = Recovery.Active 011b = Recovery.Cofiguration 100b = Recovery.Idle HotReset sub-states: 000b = HotReset.Reset 001b = HotReset.Go 010b = HotReset.Active1 011b = HotReset.Active2 100b = HotReset.Exit

TABLE 203: USB3 PORT 2 DC TEST REGISTER

SS_P2_TEST_PIPE_DC (69C1h)			USB3 Physical Port 2 DC Test Register Default = 00h
Bit	**Name**	**R/W**	**Description**
7	PIPE_TX_DE-TR_LPBK	R/W	Transmit Detect Receiver and Loopback Mode. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. Used to tell the PHY to begin receiver loopback or to signal LFPS during polling.
6	PIPE_RX_TERMINA-TION	R/W	Receiver Termination Control. This signal is asynchronous. Controls presence of receiver terminations. ‘0’ = Terminations removed ‘1’ = Terminations present
5:4	PIPE_TX_DEEMPH	R/W	Transmit De-Emphasis Level Control. This signal is synchronous. 00 = –6.0 dB de-emphasis (normal mode) 01 = –3.5 dB 10 = None 11 = Reserved
3	PIPE_TX_SWING	R/W	Transmit Swing Control. This signal is asynchronous. ‘0’ = Full Swing ‘1’ = Low Swing
2	PIPE_TX-C_DRIVE_HI GH	R/W	Set the DC State of the TX Output. 0: TXP = 0, TXN = 1 1: TXP = 1, TXN = 0
1	PIPE_TXDC_EN ABLE	R/W	Enable Transmitter DC Drive mode.
0	PIPE_TX_ELEC_I-DLE	R/W	Transmit Electrical Idle. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. This signal is used in conjunction with pow-er_down[1:0] and tx_detrx_lpbk to set the state of the transmitter (either normal transmit mode, electrical idle, LFPS transmission, or receiver detection).

TABLE 204: USB3 PORT 2 TX TEST PATTERN REGISTER

SS_P2_TEST_PIPE_TX_PAT (69C3h)			USB3 Physical Port 2 TX Pattern Register Default = 00h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always ‘0’
4	PIPE_TX_CGEN_EN	R/W	Internal Transmit Pattern Generator Enable. This signal is asynchronous. ‘0’ = Disable pattern generator (normal mode. Transmit data driven over the tx_data interface) ‘1’ = Enable pattern generator

TABLE 204: USB3 PORT 2 TX TEST PATTERN REGISTER (CONTINUED)

SS_P2_TEST_PIPE_TX_PAT (69C3h)			USB3 Physical Port 2 TX Pattern Register Default = 00h
Bit	**Name**	**R/W**	**Description**
3:0	PIPE_TX_CPGEN_-SEL	R/W	Internal Transmit Pattern Generator Select. This signal is asynchronous. 0 = CP0 (D0.0, scrambled, no SKP) 1 = CP1 (D10.2, Nyquist frequency) 2 = CP2 (D24.3, Nyquist/2 frequency) 3 = CP3 (K28.5, COM pattern) 4 = CP4 (LFPS) 5 = CP5 (K28.7, with de-emphasis) 6 = CP5 (K28.7, without de-emphasis) 7 = CP7 (50-250 1's and 0's, with de-emphasis) 8 = CP8 (50-250 1's and 0's, no de-emphasis) 9 = TSEQ 10 = TS1 11 = TS2 12 = Logical Idles (D0.0) 13 to 15 =Reserved

TABLE 205: USB3 PORT 2 TX_MARGIN

SS_P2_TEST_PIPE_CTL_0 (69D0h)			USB3 Physical Port 2 TX Margin Default = 00h
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always ‘0’ (Do not modify.)
6:4	Length	R/W	Physical port 2 transmitter biasing and amplitude adjust 000 = 0% change (default) 001 = +11% 010 = +21% 011 = +33% 100 = –67% 101 = –64% 110 = –61% 111= –57%
3:0	Reserved	R	Always ‘0’ (Do not modify.)

TABLE 206: USB3 PORT 3 TX PRE-DRIVER

SS_P3_AFE_TEST_IN4 (6C86h)			USB3 Physical Port 3 TX Pre-Driver Default = 00h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved. Do not modify.
2:1	Length	R/W	Physical port 3 transmitter pre-driver current adjust 00 =100 µA (default biasing) 01 = 125 µA 10 = 87.5 µA 11 = 112.5 µA
0	Reserved	R	Reserved. Do not modify.

TABLE 207: USB 2.0 DOWNSTREAM PORT 3 RISE-AND-FALL ADJUSTMENT REGISTER

P3_RISEFALL_ADJ (6CC8h)			USB 2.0 Downstream Physical Port 3 Rise-and-Fall Adjust Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3:2	HS_TX_RISEFALL_ADJUST	R/W	High-Speed TX Rise/Fall adjust 00 = Default 01 = +18% 10 = –18% 11 = –12%
1:0	LS_TX_RISEFALL_ADJUST	R/W	Low-Speed/Full-Speed TX Rise/Fall adjust 00 = Default 01 = +100% 10 = –30% 11 = –50%

TABLE 208: USB 2.0 DOWNSTREAM PORT 3 PHYBOOST REGISTER

HS_P3_BOOST (6CCAh)			USB 2.0 Downstream Physical Port 3 PHYBoost Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2:0	HS_BOOST	R/W	HS Output Current Adjustment 000b = Nominal 001b = Decrease by 5% 00b = Increase by 10% 011b = Increase by 5% 100b = Increase by 20% 101b = Increase by 15% 110b = Increase by 30% 111b = Increase by 25%

TABLE 209: USB 2.0 DOWNSTREAM PORT 3 VARISENSE REGISTER

HS_P3_SENSE (6CCCh)			USB 2.0 Downstream Physical Port 3 VariSense Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE	R/W	USB 2.0 AFE HS Disconnect Tune – Revision C silicon only Allows the HS disconnect threshold to be increased. Recommended to only be used when PHYBoost is also set. 0 = Nominal 575 mV trip point 1 = Increase by 50 mV 2 = Increase by 100 mV 3 = Increase by 125 mV
5:3	Reserved	R	Reserved

TABLE 209: USB 2.0 DOWNSTREAM PORT 3 VARISENSE REGISTER (CONTINUED)

HS_P3_SENSE (6CCCh)			USB 2.0 Downstream Physical Port 3 VariSense Register Default = 00h
BIT	**Name**	**R/W**	**Description**
2:0	HS_SENSE	R/W	HS VariSense Tune (Squelch Tune) 000b = Nominal (100 mV Trip Point) 001b = Decrease by 12.5 mV 00b = Decrease by 25 mV 011b = Decrease by 37.5 mV 100b = Decrease by 50 mV 101b = Decrease by 62.5 mV 110b = Increase by 25 mV 111b = Increase by 12.5 mV

TABLE 210: USB3 PORT 3 LTSSM STATE

SS_P3_LTSSM_State (6DC0h)			USB3 Physical Port 3 LTSSM State Default = Depends on device operation state
Bit	**Name**	**R/W**	**Description**
7:4	LTSSM_STATE	R	Physical Port 3 LTSSM state. 0000b = U0 (no sub-states) 0001b = U1 (no sub-states) 0010b = U2 (no sub-states) 0011b = U3 (no sub-states) 0100b = SIS.Disabled (See sub-state below.) 0101b = Rx.Detect (See sub-state below.) 0110b = SS.Inactive (See sub-state below.) 0111b = Polling (See sub-state below.) 1000b = Recovery (See sub-state below.) 1001b = Hot Reset (See sub-state below.) 1010b = Compliance (no sub-states) 1011b = Loopback (no sub-states)
3	Reserved	R	Always ‘0’

TABLE 210: USB3 PORT 3 LTSSM STATE

SS_P3_LTSSM_State (6DC0h)			USB3 Physical Port 3 LTSSM State Default = Depends on device operation state
Bit	**Name**	**R/W**	**Description**
2:0	LTSSM_SUB_STATE	R	Physical Port 3 LTSSM substate. Undefined values are invalid. SIS.Disabled sub-states: 000b = SSD.Power3 001b = SSD.Power3A 010b = SSD.Main Rx.Detect sub-states: 000b = Rx.Detect.Init 001b = Rx.Detect.Power2 010b = Rx.Detect.Reset 011b = Rx.Detect.Reset_T 100b = Rx.Detect.Active0 101b = Rx.Detect.Active1 110b = Rx.Detect.Quiet SS.Inactive sub-states: 000b = SS.Inactive.Reset 001b = SS.Inactive.Power2 010b = SS.Inactive.Quite0 011b = SS.Inactive.Quiet1 100b = SS.Inactive.Disconnect.Detect0 100b = SS.Inactive.Disconnect.Detect1 Polling sub-states: 000b = Polling.Reset 001b = Polling.Power0 010b = Polling.LFPS 011b = Polling.RxEQ 100b = Polling.Active 101b = Polling.Configuration 110b = Polling.Idle Recovery sub-states: 000b = Recovery.Reset 001b = Recovery.Power0 010b = Recovery.Active 011b = Recovery.Cofiguration 100b = Recovery.Idle HotReset sub-states: 000b = HotReset.Reset 001b = HotReset.Go 010b = HotReset.Active1 011b = HotReset.Active2 100b = HotReset.Exit

TABLE 211: USB3 PORT 3 DC TEST REGISTER

SS_P3_TEST_PIPE_DC (6DC1h)			USB3 Physical Port 3 DC Test Register Default = 00h
Bit	**Name**	**R/W**	**Description**
7	PIPE_TX_DE-TR_LPBK	R/W	Transmit Detect Receiver and Loopback mode. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. Used to tell the PHY to begin receiver loopback or to signal LFPS during polling.
6	PIPE_RX_TERMINA-TION	R/W	Receiver Termination Control. This signal is asynchronous. Controls presence of receiver terminations. ‘0’ = Terminations removed ‘1’ = Terminations present
5:4	PIPE_TX_DEEMPH	R/W	Transmit De-Emphasis Level Control. This signal is synchronous. 00 = –6.0 dB de-emphasis (Normal mode) 01 = –3.5 dB 10 = None 11 = Reserved
3	PIPE_TX_SWING	R/W	Transmit Swing Control. This signal is asynchronous. 0 = Full Swing 1 = Low Swing
2	PIPE_TX-C_DRIVE_HI GH	R/W	Set the DC State of the TX Output. 0: TXP = 0, TXN = 1 1: TXP = 1, TXN = 0
1	PIPE_TXDC_EN ABLE	R/W	Enable Transmitter DC Drive mode.
0	PIPE_TX_ELEC_I-DLE	R/W	Transmit Electrical Idle. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. This signal is used in conjunction with pow-er_down[1:0] and tx_detrx_lpbk to set the state of the transmitter (either normal transmit mode, electrical idle, LFPS transmission, or receiver detection).

TABLE 212: USB3 PORT 3 TX TEST PATTERN REGISTER

SS_P3_TEST_PIPE_TX_PAT (6DC3h)			USB3 Physical Port 3 TX Pattern Register Default = 00h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always ‘0’
4	PIPE_TX_CGEN_EN	R/W	Internal Transmit Pattern Generator Enable. This signal is asynchronous. ‘0’ = Disable pattern generator (Normal mode. Transmit data driven over the tx_data interface) ‘1’ = Enable pattern generator

TABLE 212: USB3 PORT 3 TX TEST PATTERN REGISTER (CONTINUED)

SS_P3_TEST_PIPE_TX_PAT (6DC3h)			USB3 Physical Port 3 TX Pattern Register Default = 00h
Bit	**Name**	**R/W**	**Description**
3:0	PIPE_TX_CPGEN_-SEL	R/W	Internal Transmit Pattern Generator Select. This signal is asynchronous. 0 = CP0 (D0.0, scrambled, no SKP) 1 = CP1 (D10.2, Nyquist frequency) 2 = CP2 (D24.3, Nyquist/2 frequency) 3 = CP3 (K28.5, COM pattern) 4 = CP4 (LFPS) 5 = CP5 (K28.7, with de-emphasis) 6 = CP5 (K28.7, without de-emphasis) 7 = CP7 (50-250 1's and 0's, with de-emphasis) 8 = CP8 (50-250 1's and 0's, no de-emphasis) 9 = TSEQ 10 = TS1 11 = TS2 12 = Logical Idles (D0.0) 13 to 15 = Reserved

TABLE 213: USB3 PORT 3 TX_MARGIN

SS_P3_TEST_PIPE_CTL_0 (6DD0h)			USB3 Physical Port 3 TX Margin Default = 00h
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always ‘0’ (Do not modify.)
6:4	Length	R/W	Physical port 3 transmitter biasing and amplitude adjust 000 = 0% change (default) 001 = +11% 010 = +21% 011 = +33% 100 = –67% 101 = –64% 110 = –61% 111 = –57%
3:0	Reserved	R	Always ‘0’ (Do not modify.)

TABLE 214: USB3 PORT 4 TX PRE-DRIVER

SS_P4_AFE_TEST_IN4 (7086h)			USB3 Physical Port 4 TX Pre-Driver Default = 00h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved. Do not modify.
2:1	Length	R/W	Physical port 0 transmitter pre-driver current adjust 00 = 100 µA (default biasing) 01 = 125 µA 10 = 87.5 µA 11 = 112.5 µA
0	Reserved	R	Reserved. Do not modify.

TABLE 215: USB 2.0 DOWNSTREAM PORT 4 RISE-AND-FALL ADJUSTMENT REGISTER

P4_RISE_FALL_ADJ (70C8h)			USB 2.0 Downstream Physical Port 4 Rise-and-Fall Adjust Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3:2	HS_TX_RISEFALL_ADJUST	R/W	High-Speed TX Rise/Fall adjust 00 = Default 01 = +18% 10 = –18% 11 = –12%
1:0	LS_TX_RISEFALL_ADJUST	R/W	Low-Speed/Full-Speed TX Rise/Fall adjust 00 = Default 01 = +100% 10 = –30% 11 = –50%

TABLE 216: USB 2.0 DOWNSTREAM PORT 4 PHYBOOST REGISTER

HS_P4_BOOST (70CAh)			USB 2.0 Downstream Physical Port 4 PHYBoost Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2:0	HS_BOOST	R/W	HS Output Current Adjustment 000b = Nominal 001b = Decrease by 5% 00b = Increase by 10% 011b = Increase by 5% 100b = Increase by 20% 101b = Increase by 15% 110b = Increase by 30% 111b = Increase by 25%

TABLE 217: USB 2.0 DOWNSTREAM PORT 4 VARISENSE REGISTER

HS_P4_SENSE (70CCh)			USB 2.0 Downstream Physical Port 4 VariSense Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE		USB 2.0 AFE HS Disconnect Tune – Revision C silicon only Allows the HS disconnect threshold to be increased. Recommended to only be used when PHYBoost is also set. 0 = Nominal 575 mV trip point 1 = Increase by 50 mV 2 = Increase by 100 mV 3 = Increase by 125 mV
5:3	Reserved	R	Reserved

TABLE 217: USB 2.0 DOWNSTREAM PORT 4 VARISENSE REGISTER (CONTINUED)

HS_P4_SENSE (70CCh)			USB 2.0 Downstream Physical Port 4 VariSense Register Default = 00h
BIT	**Name**	**R/W**	**Description**
2:0	HS_SENSE	R/W	HS VariSense Tune (Squelch Tune) 000b = Nominal (100 mV Trip Point) 001b = Decrease by 12.5 mV 00b = Decrease by 25 mV 011b = Decrease by 37.5 mV 100b = Decrease by 50 mV 101b = Decrease by 62.5 mV 110b = Increase by 25 mV 111b = Increase by 12.5 mV

TABLE 218: USB3 PORT 4 LTSSM STATE

SS_P4_LTSSM_State (71C0h)			USB3 Physical Port 4 LTSSM State Default = Depends on device operation state
Bit	**Name**	**R/W**	**Description**
7:4	LTSSM_STATE	R	Physical Port 4 LTSSM state. 0000b = U0 (no sub-states) 0001b = U1 (no sub-states) 0010b = U2 (no sub-states) 0011b = U3 (no sub-states) 0100b = SIS.Disabled (See sub-state below.) 0101b = Rx.Detect (See sub-state below.) 0110b = SS.Inactive (See sub-state below.) 0111b = Polling (See sub-state below.) 1000b = Recovery (See sub-state below.) 1001b = HotReset (See sub-state below.) 1010b = Compliance (no sub-states) 1011b = Loopback (no sub-states)
3	Reserved	R	Always ‘0’

TABLE 218: USB3 PORT 4 LTSSM STATE

SS_P4_LTSSM_State (71C0h)			USB3 Physical Port 4 LTSSM State Default = Depends on device operation state
Bit	**Name**	**R/W**	**Description**
2:0	LTSSM_SUB_STATE	R	Physical Port 4 LTSSM sub-state. Undefined values are invalid. SIS.Disabled sub-states: 000b = SSD.Power3 001b = SSD.Power3A 010b = SSD.Main Rx.Detect sub-states: 000b = Rx.Detect.Init 001b = Rx.Detect.Power2 010b = Rx.Detect.Reset 011b = Rx.Detect.Reset_T 100b = Rx.Detect.Active0 101b = Rx.Detect.Active1 110b = Rx.Detect.Quiet SS.Inactive sub-states: 000b = SS.Inactive.Reset 001b = SS.Inactive.Power2 010b = SS.Inactive.Quite0 011b = SS.Inactive.Quiet1 100b = SS.Inactive.Disconnect.Detect0 100b = SS.Inactive.Disconnect.Detect1 Polling sub-states: 000b = Polling.Reset 001b = Polling.Power0 010b = Polling.LFPS 011b = Polling.RxEQ 100b = Polling.Active 101b = Polling.Configuration 110b = Polling.Idle Recovery sub-states: 000b = Recovery.Reset 001b = Recovery.Power0 010b = Recovery.Active 011b = Recovery.Cofiguration 100b = Recovery.Idle HotReset sub-states: 000b = HotReset.Reset 001b = HotReset.Go 010b = HotReset.Active1 011b = HotReset.Active2 100b = HotReset.Exit

TABLE 219: USB3 PORT 4 DC TEST REGISTER

SS_P4_TEST_PIPE_DC (71C1h)			USB3 Physical Port 4 DC Test Register Default = 00h
Bit	**Name**	**R/W**	**Description**
7	PIPE_TX_DE-TR_LPBK	R/W	Transmit Detect Receiver and Loopback Mode. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. Used to tell the PHY to begin receiver loopback or to signal LFPS during polling.
6	PIPE_RX_TERMINA-TION	R/W	Receiver Termination Control. This signal is asynchronous. Controls presence of receiver terminations. ‘0’ = Terminations removed ‘1’ = Terminations present
5:4	PIPE_TX_DEEMPH	R/W	Transmit De-Emphasis Level Control. This signal is synchronous. 00 = –6.0 dB de-emphasis (Normal mode) 01 = –3.5 dB 10 = None 11 = Reserved
3	PIPE_TX_SWING	R/W	Transmit Swing Control. This signal is asynchronous. ‘0’ = Full Swing ‘1’ = Low Swing
2	PIPE_TX-C_DRIVE_HI GH	R/W	Set the DC State of the TX Output. 0: TXP = 0, TXN = 1 1: TXP = 1, TXN = 0
1	PIPE_TXDC_EN ABLE	R/W	Enable Transmitter DC Drive mode.
0	PIPE_TX_ELEC_I-DLE	R/W	Transmit Electrical Idle. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. This signal is used in conjunction with pow-er_down[1:0] and tx_detrx_lpbk to set the state of the transmitter (either normal transmit mode, electrical idle, LFPS transmission, or receiver detection).

TABLE 220: USB3 PORT 4 TX TEST PATTERN REGISTER

SS_P4_TEST_PIPE_TX_PAT (71C3h)			USB3 Physical Port 4 TX Pattern Register Default = 00h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always ‘0’
4	PIPE_TX_CGEN_EN	R/W	Internal Transmit Pattern Generator Enable. This signal is asynchronous. ‘0’ = Disable pattern generator (Normal mode. Transmit data driven over the tx_data interface.) ‘1’ = Enable pattern generator
3:0	PIPE_TX_CPGEN_-SEL	R/W	Internal Transmit Pattern Generator Select. This signal is asynchronous. 0 = CP0 (D0.0, scrambled, no SKP) 1 = CP1 (D10.2, Nyquist frequency) 2 = CP2 (D24.3, Nyquist/2 frequency) 3 = CP3 (K28.5, COM pattern) 4 = CP4 (LFPS) 5 = CP5 (K28.7, with de-emphasis) 6 = CP5 (K28.7, without de-emphasis) 7 = CP7 (50-250 1's and 0's, with de-emphasis) 8 = CP8 (50-250 1's and 0's, no de-emphasis) 9 = TSEQ 10 = TS1 11 = TS2 12 = Logical Idles (D0.0) 13 to 15 = Reserved

TABLE 221: USB3 PORT 4 TX_MARGIN

SS_P4_TEST_PIPE_CTL_0 (71D0h)			USB3 Physical Port 4 TX Margin Default = 00h
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always ‘0’. Do not modify.
6:4	Length	R/W	Physical port 4 transmitter biasing and amplitude adjust 000 = 0% change (default) 001 = +11% 010 = +21% 011 = +33% 100 = –67% 101 = –64% 110 = –61% 111 = –57%
3:0	Reserved	R	Always ‘0’. Do not modify.

TABLE 222: USB3 PORT 5 TX PRE-DRIVER

SS_P5_AFE_TEST_IN4 (7486h)			USB3 Physical Port 5 TX Pre-Driver Default = 00h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved. Do not modify.
2:1	Length	R/W	Physical port 0 transmitter pre-driver current adjust 00 = 100 µA (default biasing) 01 = 125 µA 10 = 87.5 µA 11 =112.5 µA
0	Reserved	R	Reserved. Do not modify.

TABLE 223: USB 2.0 DOWNSTREAM PORT 5 RISE-AND-FALL ADJUSTMENT REGISTER

P5_RISE_FALL_ADJ (74C8h)			USB 2.0 Downstream Physical Port 5 Rise/Fall Adjust Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3:2	HS_TX_RISEFALL_ADJUST	R/W	High-Speed TX Rise/Fall adjust 00 = Default 01 = +18% 10 = –18% 11 = –12%
1:0	LS_TX_RISEFALL_ADJUST	R/W	Low-Speed/Full-Speed TX Rise/Fall adjust 00 = Default 01 = +100% 10 = -30% 11 = –50%

TABLE 224: USB 2.0 DOWNSTREAM PORT 5 PHYBOOST REGISTER

HS_P5_BOOST (74CAh)			USB 2.0 Downstream Physical Port 5 PHYBoost Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2:0	HS_BOOST	R/W	HS Output Current Adjustment 000b = Nominal 001b = Decrease by 5% 00b = Increase by 10% 011b = Increase by 5% 100b = Increase by 20% 101b = Increase by 15% 110b = Increase by 30% 111b = Increase by 25%

TABLE 225: USB 2.0 DOWNSTREAM PORT 5 VARISENSE REGISTER

HS_P5_SENSE (74CCh)			USB 2.0 Downstream Physical Port 5 VariSense Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE		USB 2.0 AFE HS Disconnect Tune – Revision C silicon only Allows the HS disconnect threshold to be increased. Recommended to only be used when PHYBoost is also set. 0 = Nominal 575 mV trip point 1 = Increase by 50 mV 2 = Increase by 100 mV 3 = Increase by 125 mV
5:3	Reserved	R	Reserved
2:0	HS_SENSE	R/W	HS VariSense Tune (Squelch Tune) 000b = Nominal (100 mV trip point) 001b = Decrease by 12.5 mV 00b = Decrease by 25 mV 011b = Decrease by 37.5 mV 100b = Decrease by 50 mV 101b = Decrease by 62.5 mV 110b = Increase by 25 mV 111b = Increase by 12.5 mV

TABLE 226: USB3 PORT 5 LTSSM STATE

SS_P5_LTSSM_STATE (75C0h)			USB3 Physical Port 5 LTSSM State Default = Depends on device operation state
Bit	**Name**	**R/W**	**Description**
7:4	LTSSM_STATE	R	Physical Port 5 LTSSM state. 0000b = U0 (no sub-states) 0001b = U1 (no sub-states) 0010b = U2 (no sub-states) 0011b = U3 (no sub-states) 0100b = SIS.Disabled (See sub-state below.) 0101b = Rx.Detect (See sub-state below.) 0110b = SS.Inactive (See sub-state below.) 0111b = Polling (See sub-state below.) 1000b = Recovery (See sub-state below.) 1001b = HotReset (See sub-state below.) 1010b = Compliance (no sub-states) 1011b = Loopback (no sub-states)
3	Reserved	R	Always ‘0’

TABLE 226: USB3 PORT 5 LTSSM STATE

SS_P5_LTSSM_STATE (75C0h)			USB3 Physical Port 5 LTSSM State Default = Depends on device operation state
Bit	**Name**	**R/W**	**Description**
2:0	LTSSM_SUB_STATE	R	Physical Port 5 LTSSM sub-state. Undefined values are invalid. SIS.Disabled sub-states: 000b = SSD.Power3 001b = SSD.Power3A 010b = SSD.Main Rx.Detect sub-states: 000b = Rx.Detect.Init 001b = Rx.Detect.Power2 010b = Rx.Detect.Reset 011b = Rx.Detect.Reset_T 100b = Rx.Detect.Active0 101b = Rx.Detect.Active1 110b = Rx.Detect.Quiet SS.Inactive sub-states: 000b = SS.Inactive.Reset 001b = SS.Inactive.Power2 010b = SS.Inactive.Quite0 011b = SS.Inactive.Quiet1 100b = SS.Inactive.Disconnect.Detect0 100b = SS.Inactive.Disconnect.Detect1 Polling sub-states: 000b = Polling.Reset 001b = Polling.Power0 010b = Polling.LFPS 011b = Polling.RxEQ 100b = Polling.Active 101b = Polling.Configuration 110b = Polling.Idle Recovery sub-states: 000b = Recovery.Reset 001b = Recovery.Power0 010b = Recovery.Active 011b = Recovery.Cofiguration 100b = Recovery.Idle HotReset sub-states: 000b = HotReset.Reset 001b = HotReset.Go 010b = HotReset.Active1 011b = HotReset.Active2 100b = HotReset.Exit

TABLE 227: USB3 PORT 5 DC TEST REGISTER

SS_P5_TEST_PIPE_DC (7DC1h)			USB3 Physical Port 5 DC Test Register Default = 00h
Bit	**Name**	**R/W**	**Description**
7	PIPE_TX_DE-TR_LPBK	R/W	Transmit Detect Receiver and Loopback Mode. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. Used to tell the PHY to begin receiver loopback or to signal LFPS during polling.
6	PIPE_RX_TERMINA-TION	R/W	Receiver Termination Control. This signal is asynchronous. Controls presence of receiver terminations. ‘0’ = Terminations removed ‘1’ = Terminations present
5:4	PIPE_TX_DEEMPH	R/W	Transmit De-Emphasis Level Control. This signal is synchronous. 00 = –6.0 dB de-emphasis (Normal mode) 01 = –3.5 dB 10 = None 11 = Reserved
3	PIPE_TX_SWING	R/W	Transmit Swing Control. This signal is asynchronous. ‘0’ = Full Swing ‘1’ = Low Swing
2	PIPE_TX-C_DRIVE_HI GH	R/W	Set the DC State of the TX Output. 0: TXP = 0, TXN = 1 1: TXP = 1, TXN = 0
1	PIPE_TXDC_EN ABLE	R/W	Enable Transmitter DC Drive mode.
0	PIPE_TX_ELEC_I-DLE	R/W	Transmit Electrical Idle. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. This signal is used in conjunction with pow-er_down[1:0] and tx_detrx_lpbk to set the state of the transmitter (either Normal Transmit mode, Electrical Idle, LFPS Transmission, or Receiver Detection).

TABLE 228: USB3 PORT 5 TX TEST PATTERN REGISTER

SS_P5_TEST_PIPE_TX_PAT (75C3h)			USB3 Physical Port 5 TX Pattern Register Default = 00h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always ‘0’
4	PIPE_TX_CGEN_EN	R/W	Internal Transmit Pattern Generator Enable. This signal is asynchronous. ‘0’ = Disable pattern generator (Normal mode. Transmit data driven over the tx_data interface) ‘1’ = Enable pattern generator

TABLE 228: USB3 PORT 5 TX TEST PATTERN REGISTER (CONTINUED)

SS_P5_TEST_PIPE_TX_PAT (75C3h)			USB3 Physical Port 5 TX Pattern Register Default = 00h
Bit	**Name**	**R/W**	**Description**
3:0	PIPE_TX_CPGEN_-SEL	R/W	Internal Transmit Pattern Generator Select. This signal is asynchronous. 0 = CP0 (D0.0, scrambled, no SKP) 1 = CP1 (D10.2, Nyquist frequency) 2 =CP2 (D24.3, Nyquist/2 frequency) 3 = CP3 (K28.5, COM pattern) 4 = CP4 (LFPS) 5 = CP5 (K28.7, with de-emphasis) 6 = CP5 (K28.7, without de-emphasis) 7 = CP7 (50-250 1's and 0's, with de-emphasis) 8 = CP8 (50-250 1's and 0's, no de-emphasis) 9 = TSEQ 10 = TS1 11 = TS2 12 = Logical Idles (D0.0) 13 to 15 = Reserved

TABLE 229: USB3 PORT 5 TX_MARGIN

SS_P5_TEST_PIPE_CTL_0 (75D0h)			USB3 Physical Port 5 TX Margin Default = 00h
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always ‘0’. Do not modify.
6:4	Length	R/W	Physical port 5 transmitter biasing and amplitude adjust 000 = 0% change (default) 001 = +11% 010 = +21% 011 = +33% 100 = –67% 101 = –64% 110 = –61% 111 = –57%
3:0	Reserved	R	Always ‘0’. Do not modify.

TABLE 230: USB3 PORT 6 TX PRE-DRIVER

SS_P6_AFE_TEST_IN4 (7886h)			USB3 Physical Port 6 TX Pre-Driver Default = 00h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved. Do not modify.
2:1	Length	R/W	Physical port 6 transmitter pre-driver current adjust 00 = 100 µA (default biasing) 01 = 125 µA 10 = 87.5 µA 11 = 112.5 µA
0	Reserved	R	Reserved. Do not modify.

TABLE 231: USB 2.0 DOWNSTREAM PORT 6 RISE-AND-FALL ADJUSTMENT REGISTER

P6_RISE_FALL_ADJ (78C8h)			USB 2.0 Downstream Physical Port 6 Rise-and-Fall Adjust Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3:2	HS_TX_RISEFALL_ADJUST	R/W	High-Speed TX Rise/Fall adjust 00 = Default 01 = +18% 10 = –18% 11 = –12%
1:0	LS_TX_RISEFALL_ADJUST	R/W	Low-Speed/Full-Speed TX Rise/Fall adjust 00 =Default 01 = +100% 10 = –30% 11 = –50%

TABLE 232: USB 2.0 DOWNSTREAM PORT 6 PHYBOOST REGISTER

HS_P6_BOOST (78CAh)			USB 2.0 Downstream Physical Port 6 PHYBoost Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2:0	HS_BOOST	R/W	HS output current adjustment 000b = Nominal 001b = Decrease by 5% 00b = Increase by 10% 011b = Increase by 5% 100b = Increase by 20% 101b = Increase by 15% 110b = Increase by 30% 111b = Increase by 25%

TABLE 233: USB 2.0 DOWNSTREAM PORT 6 VARISENSE REGISTER

HS_P6_SENSE (78CCh)			USB 2.0 Downstream Physical Port 6 VariSense Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE		USB 2.0 AFE HS Disconnect Tune - Revision C silicon only Allows the HS disconnect threshold to be increased. Recommended to only be used when PHYBoost is also set. 0 = Nominal 575 mV trip point 1 = Increase by 50 mV 2 = Increase by 100 mV 3 = Increase by 125 mV
5:3	Reserved	R	Reserved

TABLE 233: USB 2.0 DOWNSTREAM PORT 6 VARISENSE REGISTER

HS_P6_SENSE (78CCh)			USB 2.0 Downstream Physical Port 6 VariSense Register Default = 00h
BIT	**Name**	**R/W**	**Description**
2:0	HS_SENSE	R/W	HS VariSense Tune (Squelch Tune) 000b = Nominal (100 mV Trip Point) 001b = Decrease by 12.5 mV 00b =Decrease by 25 mV 011b = Decrease by 37.5 mV 100b = Decrease by 50 mV 101b = Decrease by 62.5 mV 110b = Increase by 25 mV 111b = Increase by 12.5 mV

TABLE 234: USB3 PORT 6 LTSSM STATE

SS_P6_LTSSM_State (79C0h)			USB3 Physical Port 6 LTSSM State Default = Depends on device operation state
Bit	**Name**	**R/W**	**Description**
7:4	LTSSM_STATE	R	Physical Port 6 LTSSM state 0000b = U0 (no sub-states) 0001b = U1 (no sub-states) 0010b = U2 (no sub-states) 0011b = U3 (no sub-states) 0100b = SIS.Disabled (See sub-state below.) 0101b = Rx.Detect (See sub-state below.) 0110b = SS.Inactive (See sub-state below.) 0111b = Polling (See sub-state below.) 1000b = Recovery (See sub-state below.) 1001b = HotReset (See sub-state below.) 1010b = Compliance (no sub-states) 1011b = Loopback (no sub-states)
3	Reserved	R	Always ‘0’

TABLE 234: USB3 PORT 6 LTSSM STATE

SS_P6_LTSSM_State (79C0h)			USB3 Physical Port 6 LTSSM State Default = Depends on device operation state
Bit	**Name**	**R/W**	**Description**
2:0	LTSSM_SUB_STATE	R	Physical Port 6 LTSSM sub-state. Undefined values are invalid. SIS.Disabled sub-states: 000b = SSD.Power3 001b = SSD.Power3A 010b = SSD.Main Rx.Detect sub-states: 000b = Rx.Detect.Init 001b = Rx.Detect.Power2 010b = Rx.Detect.Reset 011b = Rx.Detect.Reset_T 100b = Rx.Detect.Active0 101b = Rx.Detect.Active1 110b = Rx.Detect.Quiet SS.Inactive sub-states: 000b = SS.Inactive.Reset 001b = SS.Inactive.Power2 010b = SS.Inactive.Quite0 011b = SS.Inactive.Quiet1 100b = SS.Inactive.Disconnect.Detect0 100b = SS.Inactive.Disconnect.Detect1 Polling sub-states: 000b = Polling.Reset 001b = Polling.Power0 010b = Polling.LFPS 011b = Polling.RxEQ 100b = Polling.Active 101b = Polling.Configuration 110b = Polling.Idle Recovery sub-states: 000b = Recovery.Reset 001b = Recovery.Power0 010b = Recovery.Active 011b = Recovery.Cofiguration 100b = Recovery.Idle HotReset sub-states: 000b = HotReset.Reset 001b = HotReset.Go 010b = HotReset.Active1 011b = HotReset.Active2 100b = HotReset.Exit

TABLE 235: USB3 PORT 6 DC TEST REGISTER

SS_P6_TEST_PIPE_DC (79C1h)			USB3 Physical Port 6 DC Test Register Default = 00h
Bit	**Name**	**R/W**	**Description**
7	PIPE_TX_DE-TR_LPBK	R/W	Transmit Detect Receiver and Loopback Mode. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. Used to tell the PHY to begin receiver loopback or to signal LFPS during polling.
6	PIPE_RX_TERMINA-TION	R/W	Receiver Termination Control. This signal is asynchronous. Controls presence of receiver terminations. ‘0’ = Terminations removed ‘1’ = Terminations present
5:4	PIPE_TX_DEEMPH	R/W	Transmit De-Emphasis Level Control. This signal is synchronous. 00 = –6.0 dB de-emphasis (Normal mode) 01 = – 3.5 dB 10 = None 11 = Reserved
3	PIPE_TX_SWING	R/W	Transmit Swing Control. This signal is asynchronous. ‘0’ = Full Swing ‘1’ = Low Swing
2	PIPE_TX-C_DRIVE_HI GH	R/W	Set the DC State of the TX Output. 0: TXP = 0, TXN = 1 1: TXP = 1, TXN = 0
1	PIPE_TXDC_EN ABLE	R/W	Enable Transmitter DC Drive Mode.
0	PIPE_TX_ELEC_I-DLE	R/W	Transmit Electrical Idle. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. This signal is used in conjunction with pow-er_down[1:0] and tx_detrx_lpbk to set the state of the transmitter (either Normal Transmit mode, Electrical idle, LFPS Transmission, or Receiver Detection).

TABLE 236: USB3 PORT 6 TX TEST PATTERN REGISTER

SS_P6_TEST_PIPE_TX_PAT (79C3h)			USB3 Physical Port 6 TX Pattern Register Default = 00h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always ‘0’
4	PIPE_TX_CGEN_EN	R/W	Internal Transmit Pattern Generator Enable. This signal is asynchronous. 0 = Disable pattern generator (normal mode. Transmit data driven over the tx_data interface) 1 = Enable pattern generator
3:0	PIPE_TX_CPGEN_-SEL	R/W	Internal Transmit Pattern Generator Select. This signal is asynchronous. 0 = CP0 (D0.0, scrambled, no SKP) 1 = CP1 (D10.2, Nyquist frequency) 2 = CP2 (D24.3, Nyquist/2 frequency) 3 = CP3 (K28.5, COM pattern) 4 = CP4 (LFPS) 5 = CP5 (K28.7, with de-emphasis) 6 = CP5 (K28.7, without de-emphasis) 7 = CP7 (50-250 1's and 0's, with de-emphasis) 8 = CP8 (50-250 1's and 0's, no de-emphasis) 9 = TSEQ 10 = TS1 11 =TS2 12 = Logical Idles (D0.0) 13 to 15 = Reserved

TABLE 237: USB3 PORT 6 TX_MARGIN

SS_P6_TEST_PIPE_CTL_0 (79D0h)			USB3 Physical Port 6 TX Margin Default = 00h
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always ‘0’ (Do not modify.)
6:4	Length	R/W	Physical port 6 transmitter biasing and amplitude adjust 000 = 0% change (default) 001 = +11% 010 = +21% 011 = +33% 100 = –67% 101 = –64% 110 = –61% 111 = –57%
3:0	Reserved	R	Always ‘0’ (Do not modify.)

TABLE 238: USB3 PORT 7 TX PRE-DRIVER

SS_P7_AFE_TEST_IN4 (7C86h)			USB3 Physical Port 7 TX Pre-Driver Default = 00h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved. Do not modify.
2:1	Length	R/W	Physical port 7 transmitter pre-driver current adjust 00 = 100 µA (default biasing) 01 = 125 µA 10 = 87.5 µA 11 = 112.5 µA
0	Reserved	R	Reserved. Do not modify.

TABLE 239: USB 2.0 DOWNSTREAM PORT 7 RISE-AND-FALL ADJUSTMENT REGISTER

P7_RISE_FALL_ADJ (7CC8h)			USB 2.0 Downstream Physical Port 7 Rise-and-Fall Adjust Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3:2	HS_TX_RISEFALL_ADJUST	R/W	High-Speed TX Rise/Fall adjust 00 = Default 01 = +18% 10 = –18% 11 = –12%
1:0	LS_TX_RISEFALL_ADJUST	R/W	Low-Speed/Full-Speed TX Rise/Fall adjust 00 = Default 01 = +100% 10 = –30% 11 = –50%

TABLE 240: USB 2.0 DOWNSTREAM PORT 7 PHYBOOST REGISTER

HS_P7_BOOST (7CCAh)			USB 2.0 Downstream Physical Port 7 PHYBoost Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2:0	HS_BOOST	R/W	HS output current adjustment 000b = Nominal 001b = Decrease by 5% 00b = Increase by 10% 011b = Increase by 5% 100b = Increase by 20% 101b = Increase by 15% 110b = Increase by 30% 111b = Increase by 25%

TABLE 241: USB 2.0 DOWNSTREAM PORT 7 VARISENSE REGISTER

HS_P7_SENSE (7CCCh)			USB 2.0 Downstream Physical Port 7 VariSense Register Default = 00h
BIT	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE		USB 2.0 AFE HS Disconnect Tune – Revision C silicon only Allows the HS disconnect threshold to be increased. Recommended to only be used when PHYBoost is also set. 0 = Nominal 575 mV trip point 1 = Increase by 50 mV 2 = Increase by 100 mV 3 = Increase by 125 mV
5:3	Reserved	R	Reserved
2:0	HS_SENSE	R/W	HS VariSense Tune (Squelch Tune) 000b = Nominal (100 mV trip point) 001b = Decrease by 12.5 mV 00b = Decrease by 25 mV 011b = Decrease by 37.5 mV 100b = Decrease by 50 mV 101b = Decrease by 62.5 mV 110b = Increase by 25 mV 111b = Increase by 12.5 mV

TABLE 242: USB3 PORT 7 LTSSM STATE

SS_P7_LTSSM_State (7DC0h)			USB3 Physical Port 7 LTSSM State Default = Depends on device operation state
Bit	**Name**	**R/W**	**Description**
7:4	LTSSM_STATE	R	Physical Port 7 LTSSM state 0000b = U0 (no sub-states) 0001b = U1 (no sub-states) 0010b = U2 (no sub-states) 0011b = U3 (no sub-states) 0100b = SIS.Disabled (See sub-state below.) 0101b = Rx.Detect (See sub-state below.) 0110b = SS.Inactive (See sub-state below.) 0111b = Polling (See sub-state below.) 1000b = Recovery (See sub-state below.) 1001b = HotReset (See sub-state below.) 1010b = Compliance (no sub-states) 1011b = Loopback (no sub-states)
3	Reserved	R	Always ‘0’

TABLE 242: USB3 PORT 7 LTSSM STATE (CONTINUED)

SS_P7_LTSSM_State (7DC0h)			USB3 Physical Port 7 LTSSM State Default = Depends on device operation state
Bit	**Name**	**R/W**	**Description**
2:0	LTSSM_SUB_STATE	R	Physical Port 7 LTSSM sub-state. Undefined values are invalid. SIS.Disabled sub-states: 000b = SSD.Power3 001b = SSD.Power3A 010b = SSD.Main Rx.Detect sub-states: 000b = Rx.Detect.Init 001b = Rx.Detect.Power2 010b = Rx.Detect.Reset 011b = Rx.Detect.Reset_T 100b = Rx.Detect.Active0 101b = Rx.Detect.Active1 110b = Rx.Detect.Quiet SS.Inactive sub-states: 000b = SS.Inactive.Reset 001b = SS.Inactive.Power2 010b = SS.Inactive.Quite0 011b = SS.Inactive.Quiet1 100b = SS.Inactive.Disconnect.Detect0 100b = SS.Inactive.Disconnect.Detect1 Polling sub-states: 000b = Polling.Reset 001b = Polling.Power0 010b = Polling.LFPS 011b = Polling.RxEQ 100b = Polling.Active 101b = Polling.Configuration 110b = Polling.Idle Recovery sub-states: 000b = Recovery.Reset 001b = Recovery.Power0 010b = Recovery.Active 011b = Recovery.Cofiguration 100b = Recovery.Idle HotReset sub-states: 000b = HotReset.Reset 001b = HotReset.Go 010b = HotReset.Active1 011b = HotReset.Active2 100b = HotReset.Exit

TABLE 243: USB3 PORT 7 DC TEST REGISTER

SS_P7_TEST_PIPE_DC (7DC1h)			USB3 Physical Port 7 DC Test Register Default = 00h
Bit	**Name**	**R/W**	**Description**
7	PIPE_TX_DE-TR_LPBK	R/W	Transmit Detect Receiver and Loopback Mode. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. Used to tell the PHY to begin receiver loopback or to signal LFPS during polling.
6	PIPE_RX_TERMINA-TION	R/W	Receiver Termination Control. This signal is asynchronous. Controls presence of receiver terminations. ‘0’ = Terminations removed ‘1’ = Terminations present
5:4	PIPE_TX_DEEMPH	R/W	Transmit De-Emphasis Level Control. This signal is synchronous. 00 = –6.0 dB de-emphasis (Normal mode) 01 = –3.5 dB 10 = None 11 = Reserved
3	PIPE_TX_SWING	R/W	Transmit Swing Control. This signal is asynchronous. ‘0’ = Full Swing ‘1’ = Low Swing
2	PIPE_TX-C_DRIVE_HI GH	R/W	Set the DC State of the TX Output. 0: TXP = 0, TXN = 1 1: TXP = 1, TXN = 0
1	PIPE_TXDC_EN ABLE	R/W	Enable Transmitter DC Drive mode
0	PIPE_TX_ELEC_I-DLE	R/W	Transmit Electrical Idle. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. This signal is used in conjunction with pow-er_down[1:0] and tx_detrx_lpbk to set the state of the transmitter (either Normal Transmit mode, Electrical Idle, LFPS Transmission, or Receiver Detection).

TABLE 244: USB3 PORT 7 TX TEST PATTERN REGISTER

SS_P7_TEST_PIPE_TX_PAT (7DC3h)			USB3 Physical Port 7 TX Pattern Register Default = 00h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always ‘0’
4	PIPE_TX_CGEN_EN	R/W	Internal Transmit Pattern Generator Enable. This signal is asynchronous. ‘0’ = Disable pattern generator (Normal mode. Transmit data driven over the tx_data interface) ‘1’ = Enable pattern generator
3:0	PIPE_TX_CPGEN_-SEL	R/W	Internal Transmit Pattern Generator Select. This signal is asynchronous. 0 = CP0 (D0.0, scrambled, no SKP) 1 = CP1 (D10.2, Nyquist frequency) 2 = CP2 (D24.3, Nyquist/2 frequency) 3 = CP3 (K28.5, COM pattern) 4 = CP4 (LFPS) 5 = CP5 (K28.7, with de-emphasis) 6 = CP5 (K28.7, without de-emphasis) 7 = CP7 (50-250 1's and 0's, with de-emphasis) 8 = CP8 (50-250 1's and 0's, no de-emphasis) 9 = TSEQ 10 = TS1 11 = TS2 12 = Logical Idles (D0.0) 13 to 15 = Reserved

TABLE 245: USB3 PORT 7 TX_MARGIN

SS_P7_TEST_PIPE_CTL_0 (7DD0h)			USB3 Physical Port 7 TX Margin Default = 00h
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always ‘0’ (Do not modify.)
6:4	Length	R/W	Physical port 7 transmitter biasing and amplitude adjust 000 = 0% change (default) 001 = +11% 010 = +21% 011 = +33% 100 = –67% 101 = –64% 110 = –61% 111 = –57%
3:0	Reserved	R	Always ‘0’ (Do not modify.)

3.0 CONFIGURATION VIA SMBUS

3.1 SMBus Protocol

The SMBus protocol is a flexible, 2-pin serial protocol used for low-speed communication between integrated circuits. The protocol consists of a SMBCLK pin generated by the SMBus Master and a bidirectional SMBDATA pin that can be driven by a master or a slave. To function, the bus requires a pull-up resistor on both SMBCLK and SMBDATA. The hub configures the pins as open/drain buffers where the driver will either tristate the pin or drive the pin to GND. SOCs operating and 3.3V to 2.5V are supported. The input high level threshold is 1.5V. Refer to the System Management Bus Specification for more details on the timing specifications of the bus.

3.2 SOC Configuration Stage

The SOC Configuration Stage is the first stage of activity on the SMBus interface. In this stage, the SOC may modify any of the configuration settings to customize the Hub to specific applications. The SOC may configure the hub as Full-Speed only, or have the hub report a port as non-removable. The SOC can also disable a port entirely to conserve power. During the SOC Configuration stage the hub is addressed at 2Dh.

3.3 Runtime

The hub can also be configured during runtime after enumeration. During runtime, the hub is addressed at 2Dh. The special 'AAh 56h 00h' command is required to enter runtime with the SMBus slave interface active. To ensure that the runtime SMBus slave interface always remains active during runtime, XTAL_SUSP_DIS of CLOCK_CTL register (0x0804) must be set to “= 1.” If this bit is not set, the SMBus slave interface will not be active while the hub is in the USB Suspend state.

3.4 SMBus Block Write

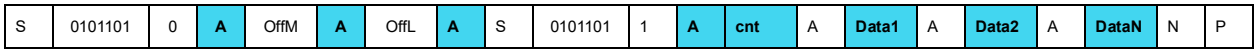
The SMBus block write consists of an Address+Direction(0) byte followed by the 16-bit memory address, split into two bytes. The address is used for special commands as well as a pointer to the hubs internal memory. After the address, the next byte of data is the count of data bytes that will follow, up to 128 bytes in a block. Finally, a write of 00h is used to terminate the write operation followed by the SMBus stop signal. See Figure 1.

FIGURE 1: SMBUS BLOCK WRITE

3.5 SMBus Block Read

The SMBus block read consists of an Address+Direction(0) byte with the 16-bit memory address followed by a repeat Start signal and an Address+Direction(1) byte. The hub will then start to output the count (128 bytes) and the contents of the internal registers starting at the 16-bit address specified. See Figure 2

FIGURE 2: SMBUS BLOCK READ



3.6 Special Commands

There are special commands that can be sent in the place of the 16-bit address bytes. These commands are used to enumerate the hub, access the configuration registers, or simply reset the device. The commands consist of the 16-bit command followed by a 00h byte to terminate the command. See Table 246.

TABLE 246: SPECIAL SMBUS COMMANDS

Operation	Opcode	Description
Reboot	9936h	Reset device
USB Attach	AA55h	Exit configuration stage and begin enumeration

TABLE 246: SPECIAL SMBUS COMMANDS (CONTINUED)

Operation	Opcode	Description
USB Attach with SMBus Slave Active	AA56h	Exit configuration stage and begin enumeration while leaving SMBus slave interface active
Configuration Register Access Command	9937h	Read and Write Configuration registers
OTP Write Command	9933h	Write OTP commands to the OTP memory space
OTP Read Command	9934h	Read the contents of the OTP memory space

3.7 Accessing Configuration Registers

The Configuration Register Access command allows the SMBus Master to read or write to the internal registers of the hub. When the Configuration Register Access command is sent, the hub will interpret the memory starting at offset 00h as shown in Table 247.

TABLE 247: MEMORY FORMAT FOR CONFIGURATION REGISTER ACCESS

Ram Address	Description	Notes
0000h	Direction	'0' = Register Write, '1' = Register Read
0001h	N	Number of bytes to read/write when executing the command
0002h	Configuration Address MSB	The upper byte of the 16-bit configuration register address
0003h	Configuration Address LSB	The lower byte of the 16-bit configuration register address
0004h	Data1	The first byte of data to write to or read from the configuration address
...	...	...
0004h+[N-1]	DataN	The Nth byte of data to write to or read from the configuration address, N is equal to the data length.

3.8 Configuration Register Write Example

The following example shows how the SMBus messages will be formatted to set the VID of the hub to a custom value, 1234h. See Table 248 to Table 249.

1. Write data to the memory of the hub:

TABLE 248: EXAMPLE SMBUS WRITE COMMAND

Byte	Value	Comment
0	5Ah	Address plus write bit
1	00h	Memory address **00**00h
2	00h	Memory address 00**00**h
3	06h	Number of bytes to write to memory
4	00h	Write configuration register
5	02h	Writing two data bytes
6	30h	VID is in register **30**00h.
7	00h	VID is in register 30**00**h.
8	34h	LSB of Vendor ID 12**34**h
9	12h	MSB of Vendor ID is **12**34h

2. Execute the Configuration Register Access command:

TABLE 249: CONFIGURATION REGISTER ACCESS COMMAND

Byte	Value	Comment
0	5Ah	Address plus write bit
1	99h	Command **99**37h
2	37h	Command 99**37**h
3	00h	Command completion

3.9 Configuration Register Read Example

The following example shows how to read the USB 2.0 Hub Status register (318Dh) to determine what type of charger the hub has connected to. See Table 250 to Table 252.

1. Write data to the memory of the hub:

TABLE 250: EXAMPLE SMBUS WRITE COMMAND

Byte	Value	Comment
0	5Ah	Address plus write bit
1	00h	Memory address **00**00h
2	00h	Memory address 00**00**h
3	06h	Number of bytes to write to memory
4	00h	Read configuration register
5	02h	Reading one data byte
6	31h	BC Detect is in register **31**8Dh.
7	8Dh	BC Detect is in register 31**8D**h.

2. Execute the Configuration Register Access command:

TABLE 251: CONFIGURATION REGISTER ACCESS COMMAND

Byte	Value	Comment
0	5Ah	Address plus write bit
1	99h	Command **99**37h
2	37h	Command 99**37**h
3	00h	Command completion

3. Read back the data starting at memory offset 04h, which is where the Data byte starts:

TABLE 252: EXAMPLE SMBUS READ COMMAND

Byte	Value	Comment
0	5Ah	Address plus write bit
1	00h	Memory address **00**04h
2	04h	Memory address 00**04**h
3	59h	Address plus read bit
4	80h	Device sends 128 bytes of data.
5	56h	Charging downstream port detect

Note: Although the device can send out 128 bytes of memory data, it isn't necessary to read the entire set. The SMBus Master can send a stop at any time.

4.0 CONFIGURATION VIA OTP

4.1 Writing to OTP via MPLAB® Connect Configurator Software

The simplest method to program to the USB58xx/USB59xx hub's OTP is through the MPLAB® Connect Configurator software package. This software pacakage is available from the USB58xx/USB59xx product page.

This tool can be used to generate a configuration file (".cfg"), then program that configuration file permanently to the hub's OTP memory space.

Alternatively, the ".cfg" file can be constructed manually using a binary/hex editor. Follow the formatting instructions shown in Section 4.3, "OTP Configuration Commands", and see the example in Section 4.4, "OTP Configuration File Example".

4.2 Writing to OTP via SMBus Overview

The OTP memory can be programmed through the SMBus interface in the SOC_CONFIG stage (during start-up). The OTP memory is configured as a series of commands that manipulate the configuration registers. The USB5734 and USB5744 hubs have a total of 8 kB of OTP memory space, and each byte of OTP memory may be written to only once. The OTP memory space can be successively written to (each programming instance appends the new command to the bottom of the OTP memory space) until the space is completely filled.

During the HUB_CONFIG stage, temporary OTP configuration registers are written to. The contents in the OTP configuration registers are then permanently loaded to the OTP memory space after sending special OTP program command. These registers will permanently change the default behavior of the hub during normal operation. These commands are stored into the OTP memory as shown in Figure 3. See Table 253.

4.3 OTP Configuration Commands

TABLE 253: OTP STORAGE COMMANDS

Command	OPCODE	Length	Description
NULL	00h	N/A	No action. Advance memory counter by 1 and move to the next instruction.
MODIFY_BYTES	01h–7Fh	OPCODE	Modifies the following bytes starting at the current memory address for length = OPCODE. The previously used SET_MODE command is used for selecting the bit operation. The default MODE is WRITE_BYTES if there is no preceding SET_MODE command.
SET_MEMORY ADDRESS	80h XXh XXh XXh XXh	N/A	Load the MEMORY_ADDRESS register with the four XXh XXh XXh XXh bytes. Example: 80h BFh 80h 30h 00h sets the memory address to BF80_3000h.
SKIP_MEMORY_WRITE	81h-FDh	OPCODE [6:0]	Skip the length number of bytes starting at the location of the MEMORY_ADDRESS register. At the end of the operation, the MEMORY_ADDRESS register is incremented by length = OPCODE[6:0].
SET_MODE_WRITE_BYTE	FEh 00	N/A	If the byte following SET_MODE = 00h, all writes replace the memory value at that location.
SET_MODE_SET_BITS	FEh 01h	N/A	If the byte following SET_MODE = 01h, all writes are OR'ed in. This is a mechanism to set the selected bits in a register without changing the others. Set the bits to be set.

TABLE 253: OTP STORAGE COMMANDS (CONTINUED)

Command	OPCODE	Length	Description
SET_MODE_CLEAR_BITS	FEh 02h	N/A	If the byte following SET_MODE = 02h, all writes are NAND'ed in. This is a mechanism to clear the selected bits in a register without changing the others. Set the bits to be cleared.
STOP	FFh	N/A	Once the storage commands are complete, this indicates the termination of the command sequence.

4.4 OTP Configuration File Example

If it was desired to have the hub started up in the Flexed state, the user would want to modify configuration register 318Eh. Refer to the command sequence in Table 254.

TABLE 254: EXAMPLE OTP CONFIGURATION BIT_COMMAND SEQUENCE

Byte	Value	Comment
1	80h	SET_ADDRESS command
2	31h	Setting address MSB to 31h (target register **31**8Eh)
3	80h	Setting address LSB to 8Eh (target register 31**8E**h)
4	FEh	BIT command
5	01h	SET_BIT command, only the selected bits will be set
6	01h	DATA_LENGTH of 1 byte
7	01	Only set the FLEXCONNECT bit in this register
8	FFh	STOP command (Omit the byte if another command follows)

TABLE 255: EXAMPLE OTP CONFIGURATION SIMPLE_WRITE SEQUENCE

Byte	Value	Comment
1	80h	SET_ADDRESS command
2	30h	Setting address MSB to 30h (target register **30**02h)
3	02h	Setting address LSB to 8Eh (target register 30**02**h)
4	02h	SIMPLE_DATA_LENGTH of 2 bytes
5	21h	Data Payload to be written to register 3002h (USB 2.0 hub PIDL register)
6	43h	Data Payload to be written to register 3003h (USB 2.0 hub PIDL register)
7	FFh	STOP command (Omit the byte if another command follows)

4.5 Writing OTP Data via SMBus

To program the configuration commands to the OTP memory space, the following steps must be followed:

1. Write **C1h** to register **0860h** to enable the Hub Feature Controller. See Example 1.

EXAMPLE 1:

```
5A 00 00 05 00 01 08 60 C1

5A 99 37 00
```

2. Write **01h** to register **0A00h** to resume internal code execution.See Example 2.

EXAMPLE 2:

```
5A 00 00 05 00 01 0A 00 01

5A 99 37 00
```

3. Write **Config Data Payload** starting at register **8000h.** Where: ***DL*** = Total Data Payload Length, ***DP*** = Total Data Payload Length + 4, ***D1- d(n)*** = data payload. See Example 3.

EXAMPLE 3:

```
5A 00 00 DP 00 DL 80 00 d1 d2 d3 … d(n-2) d(n-1) d(n) FF

5A 99 37 00
```

Note: The maximum data payload of a single SMBus write command is limited by the ***DP*** = FFh. This means that FFh is the maximum DL (256 Bytes). OTP patches that exceed 256 Bytes in length must be broken up into 256 Byte chunks and this step must be repeated at register offsets 4900h, 5000h, 5100h, 5200h, and so on as needed.

4. To write 30 02 02 34 12 FF to change hub's USB 2.0 PID to 1234h (See Example 4.), Write **03h** to register **4800h** to instruct the hub to load new OTP data payload to next available memory space. (See Example 5.)

EXAMPLE 4:

```
5A 00 00 0B 00 07 80 00 80 30 02 02 34 12 FF

5A 99 37 00
```

EXAMPLE 5:

```
5A 00 00 05 00 01 48 00 03

5A 99 37 00
```

5. Write **Total OTP Patch Length** to register **4803:4h** to instruct the hub to load new OTP data payload to next available memory space. (Note that 4803h is MSB, and 4804h is LSB.) Where: ***TL*** = Total OTP Patch Length. (See Example 6.)

EXAMPLE 6:

```
5A 00 00 06 00 02 48 03 TL(msb) TL(lsb)

5A 99 37 00
```

See Example 7 if the patch length is 6 bytes:

EXAMPLE 7:

```
5A 00 00 06 00 02 48 03 00 07

5A 99 37 00
```

6. Send the OTP Program Command **99 33 00**. See Example 8

EXAMPLE 8:

```
5A 99 33 00
```

7. Read register **414Ch** to confirm that the OTP programming was successful. If the returned value is 0, then the patch was programmed with no errors. Please do this before sending the attach command (`AA 55 00`). Where: ***XX*** = *Returned Value.* See Example 9.

EXAMPLE 9:

```
5A 00 00 04 01 01 41 4C

5A 99 37 00

5A 00 04

5B 80 XX

5A AA 55 00
```

4.6 OTP Memory Structure

The hub OTP Memory Structure is represented in the Hexadecimal table shown in Figure 3.

FIGURE 3: OTP MEMORY STRUCTURE

	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
0000	Part Number Indicator				Prog. Count			UUID USB 3.1 Hub								
0010	UUID USB 3.1 Hub											UUID USB 2.0 Hub				
0020	UUID USB 2.0 Hub															FF
0030																
0040						Configuration Commands										
0050																
0060								00h	00h	00h	00h	00h	00h	00h	00h	00h
0070	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
0080	00h	00h	00h	00h	00h	00h	Blank Memory							00h	00h	00h
0090	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
...																
1FC0	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
1FD0	00h	00h	00h	00h	00h	00h	00h									
1FE0									Configuration Signatures							
1FF0																

4.6.1 PART NUMBER INDICATOR (BYTES 00H – 03H)

The first four bytes in the OTP space contain the part number indicator.

- **USB5806:** 8Fh 00h 00h 00h
- **USB5816:** AFh 00h 00h 00h
- **USB5826:** EFh 00h 00h 00h
- **USB5906:** 9Fh 00h 00h 00h
- **USB5916:** BFh 00h 00h 00h
- **USB5926:** FFh 00h 00h 00h

4.6.2 MPLAB CONNECT CONFIGURATOR PROGRAMMING TRACKER (BYTES 04H - 06H)

The next three bytes are utilized by the MPLAB Connect Configurator tool to track the number of times the part has been programmed. The contents of these bytes are updated each time the hub is programmed. Since each bit in a byte may only be set once, up to 24 separate programs of the hub OTP may be record.

00h 00h 01h = Hub has been programmed once.

00h 00h 03h = Hub has been programmed twice.

...

FFh FFh FFh = Hub has been programmed 24 times.

4.6.3 UUID (BYTES 07H – 2FH)

Every part has a unique identification number programmed to the USB 2.0 and USB 3.1 Gen1 hub descriptors. This UUID is used by the OS to accelerate repeat enumerations of the hub and fast-track loading of drivers.This section ends with FFh at offset 2Fh.

4.6.4 CONFIGURATION COMMAND SECTION

This section grows from the start of the OTP data. These are the commands that are appended every time a Program OTP command is sent through SMBus and can vary in length depending on how many configuration registers have been manipulated.

4.6.5 BLANK MEMORY

This will cycle between 00h and FFh to show that it has not been written yet.

4.6.6 CONFIGURATION SIGNATURE

The Configuration Signature is automatically generated when the OTP data is programmed. This signature is always 8 bytes per OTP program and is appended to the back of the OTP memory space every time the Program OTP command is sent. This signature contains a checksum to confirm whether the configuration command was written correctly. It also checks the information on the location of the configuration commands within the OTP memory space and their total length.

The signatures format is shown in Table 256.

TABLE 256: CONFIGURATION SIGNATURE FORMAT

BYTE	0	1	2	3	4	5	6	
Description	I (49h)	D (44h)	X (58h)	CheckSum (CheckSum8 Xor)	Length MSB	Length LSB	OTP Memory Address Offset MSB	OTP Memory Address Offset LSB

4.7 OTP Configuration via USB

The following are the steps to configure OTP via USB:

1. Read OTP Setup Transaction
2. Set OTP Program Code
3. Program OTP Transaction to Program OTP Configuration Data to OTP
4. Get Status OTP Transaction

4.7.1 READ OTP SETUP TRANSACTION

To program OTP via USB, the entire OTP memory contents must be read to obtain the correct memory offset location for the OTP configuration block and the signature. Refer to the Section 4.6, "OTP Memory Structure" for the OTP memory organization.

The new configuration block should be programmed to the next byte following the end of the most recently programmed configuration block. (Configuration command blocks work forward from the beginning of the OTP memory space.) The new Configuration Index signature should begin 8 bytes before the start of the most recently programmed Configuration Index signature. (Signatures are added backwards from the end of the memory space.)

Note:	Two to four Bytes at the very beginning of the OTP memory are left intentionally blank at the time of production. The MPLAB Connect Configurator tool uses these bytes to keep track of the number of times the tool has been used to update the OTP memory. When programming OTP via USB manually, these bits may be optionally used to keep track of the number of additional times the hub OTP memory has been programmed. The hub FW does not use these bytes for any purpose.

Issue the command in Table 257 to read the OTP memory.

TABLE 257: OTP READ SETUP PACKET

Setup Packet	Value	Description
bmRequestType	0xC1	Device-to-host to data transfer, using vendor-specific command, targeting interface
bRequest	0x01	CMD_OTP_READ
wValue	OTP_ADRESS	Address of the OTP ROM to be read
wIndex	0x00	Reserved
wLength	Data Length	Length of data to be read

TABLE 257: OTP READ SETUP PACKET (CONTINUED)

Setup Packet	Value	Description
Command phase: Receives the setup packet with the parameters specified above. **Data phase:** Sends the data bytes of length wLength from address wValue. **Status phase:** • STALL - on read error • ACK - on successful completion of command		

4.7.2 SET OTP PROGRAM CODE

The OTP memory can be programmed by either the Program command or the PROGRAMVERIFY command. CMD_OTP_SET_PROGRAM_MODE selects the internal command that the ROM will issue to the OTP during subsequent CMD_OTP_PROGRAM commands.

The default mode in the ROM is PROGRAMVERIFY (without requiring the Set OTP Program Mode command to be issued always). See Table 258.

TABLE 258: SET OTP PROGRAM MODE SETUP PACKET

Setup Pkt	Value	Description
bmRequestType	0x41	Host-to-device to data transfer, using vendor-specific command, targeting interface
bRequest	0xF1	CMD_OTP_SET_PROGRAM_MODE
wValue	Programming Option	Indicates if the future CMD_OTP_PROGRAM commands will issue the PROGRAMVERIFY or PROGRAM command • 0x01 – PGMVFY • 0x02 – PROGRAM
wIndex	0x0000	Reserved
wLength	Data Length	No Data command
Command phase: Receives the setup packet as specified in the table. **Status phase:** • ACK - On successful completion of the command		

4.7.3 PROGRAM OTP TRANSACTION TO PROGRAM OTP CONFIGURATION DATA TO OTP

4.7.3.1 Method 1: Program the entire 8 kB in a single step.

This method allows the OTP to be updated with a signal program command, but requires transferring 8 kB to the hub before sending the program command.

To simplify the update process, it is recommended to first read back the entire 8 kB OTP memory space, insert the new Configuration data block and index signature to the read back file, and transfer the entire amended 8 kB back to the hub. Overwriting previously written to bytes with the same redundant data is supported and will have no negative effect.

With this method, OTP_ADDRESS is always 0x000, and wLength is always 0x1FFF.

4.7.3.2 Method 2: Program only the new configuration data block and signature index in two separate programming steps.

This method allows the hub OTP to be updated with the minimum amount of data transfer possible, but requires two separate program commands to achieve.

An alternate method is to perform an OTP memory dump, locate the offset of the configuration data block, and program only the new configuration block to the proper memory offset. Then, in a separate programming step, add the new configuration index signature to the correct memory offset.

An optional read-back step can be performed to ensure the data is correctly stored. (See Table 259.)

TABLE 259: OTP PROGRAM SETUP PACKET

Setup Packet	Value	Description
bmRequestType	0x41	Host-to-device data transfer, using vendor-specific command, targeting interface
bRequest	0x00	CMD_OTP_PROGRAM
wValue	OTP_ADDRESS	Address of the OTP memory for the Configuration Data block to be written
wIndex	0x00	Reserved
wLength	Data Length	Length of data to be written
Command phase: Receives the setup packet with the parameters specified above. **Data phase:** Receives the data bytes of length wLength and programs the OTP accordingly. **Status phase:** • STALL - on programming error • ACK - on successful completion of programming		

Use CMD_OTP_GET_STATUS to get the status.

Note:	Programming OTP via USB requires that a valid signature at the end of OTP is also manually generated and programmed to the correct memory location. There is no automated signature generation option when programming OTP via USB. For a configuration block to be loaded by the hub FW, steps 5 and 6 must also be followed correctly.

4.7.4 GET STATUS OTP TRANSACTION

To ensure the previous Configuration block was programmed to OTP successfully, issue the command in Table 260 to get the OTP status.

TABLE 260: OTP GET STATUS SETUP PACKET

Setup Pkt	Value	Description
bmRequestType	0xC1	Device-to-host to data transfer, using vendor-specific command, targeting interface
bRequest	0x02	CMD_OTP_GET_STATUS
wValue	0x0000	Address of the OTP ROM to be read
wIndex	0x0000	Reserved
wLength	0x01	One byte status to be returned
Command phase: Receives the setup packet with the parameters specified above. **Data phase:** Sends the status byte. **Status phase:** • STALL - on read error • ACK - on successful completion of command		

The status code returned is shown in Table 261.

TABLE 261: OTP STATUS CODES

Status Code	Description
0x00	Command successful completion
0x01	Generic error

4.8 OTP Programming Example

An OTP patch is generated to change the value of register 0x3000 = 0x34 and 0x3001 = 0x12, such that the VID is changed to 0x1234. The OTP contents for this patch is indicated in Example 10.

EXAMPLE 10:

```
80 BF 80 30 00 FE 00 02 34 12 FF
```

1. **Step 1:** An OTP memory read-back is performed, and the data in Figure 4 is returned.

FIGURE 4: EXAMPLE RETURNED OTP READ

	0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh	Eh	Fh
0000h	SKU				Prog Count			USB3 Hub UUID								
0010h	USB3 Hub UUID											USB2 Hub UUID				
0020h	USB2 Hub UUID															FFh
0030h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
0040h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
0050h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
	00h	00h	00h	00h	00h	Blank Memory							00h	00h	00h	00h
...	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
1FC0h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
1FD0h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
1FE0h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h

2. **Step 2:** The Configuration Data should be placed as shown in orange in Figure 5 at memory offset 0030h – 0038h. The Configuration Index signature should be placed in the next available signature location as also shown in orange in Figure 5 at memory offset 1FF0h-1FF7h.

FIGURE 5: OTP MEMORY WITH NEW CONFIGURATION DATA INSERTED

	0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh
0000h	SKU				Prog Count			USB3 Hub UUID						
0010h	USB3 Hub UUID												USB2 Hub U	
0020h	USB2 Hub UUID													
0030h	80h	30h	00h	FEh	00h	02h	34h	12h	FFh	00h	00h	00h	00h	00h
0040h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
0050h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
	00h	00h	00h	00h	00h	Blank Memory							00h	00h
...	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
1FC0h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
1FD0h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h

The signature data is generated based upon the data contents, a checksum, the location that it is placed within the OTP memory, and the length. Hence, the signature for this example is shown in Figure 6.

FIGURE 6: EXAMPLE CONFIGURATION INDEX

BYTE	1	2	3	4	5	6	7	8
Description	Signature			Checksum	CFG ADDRESS		CFG LENGTH	
Contents	I (49h)	D (44h)	X (58h)	AAh	00h	30h	00h	09h

3. **Step 3:** Send the CMD_OTP_PROGRAM command with the 8 kB of amended OTP data as the data payload for the USB transaction.
4. **Step 4:** Verify that programming was successful by sending CMD_OTP_GET_STATUS and check if the returned payload is 0x00.
5. **Step 5:** Perform another OTP memory read to confirm programming was successful.

5.0 CONFIGURATION VIA SPI ROM

5.1 Writing to SPI ROM configuration space via MPLAB Connect Configurator Software

Before attempting to write to SPI ROM configuration space, two files are needed:

1. **USB58xx/USB59xx Base Firmware File.** When using a SPI ROM, the hub executes all of its firmware directly from the SPI ROM. Thus, a complete hub base firmware file is required. A base firmware file which replicates the default internal ROM is available. Other custom base firmware files created for special applications may also be available. See product page for available firmware files.
2. **Configuration File(s) (".cfg").** This follows the same format as a standard OTP configuration file. ProTouch2 software can be used to generate a configuration file, or a file can be created manually following the instructions shown in **Section 4.3 "OTP Configuration Commands"** and **Section 4.4 "OTP Configuration File Example"**.

Once both files are obtained, use the MPLAB Connect Configurator software to program the base firmware file to the attached SPI ROM. Then, program the configuration file to the SPI ROM "pseudo-OTP" space (a space in the SPI ROM which emulates the hub's internal OTP memory).

The combined "Base Firmware File" and "Configuration File" can then be read back from the SPI ROM using the MPLAB Connect Memory Dump feature. This combined file can be used to pre-program SPI ROMs for mass production.

6.0 CONFIGURATION VIA USB COMMAND TO INTERNAL HUB FEATURE CONTROLLER DEVICE

The USB5806, USB5816, USB5826, USB5906, USB5916, and USB5926 devices all have an internal WinUSB device connected to the last USB 2.0 port. This device is called the Hub Feature Controller. Hub configuration can be achieved via the USB connection to the hub by communicating to the Hub Feature Controller WinUSB device using standard Windows® or Linux® drivers.

6.1 Writing to OTP via USB Command

ProTouch2 software can be used to generate a configuration file, or a file can be created manually following the instructions shown in **Section 4.3 "OTP Configuration Commands"** and **Section 4.4 "OTP Configuration File Example"**.

Once the proper ".cfg" is created, the ProTouch2 tool can be used to permanently program the configuration to the hub's internal 8kB One-Time Programmable memory space. Download the ProTouch2 tool package from the hub product page and follow the included User's Manual for additional info.

6.2 Writing to Configuration Registers during Runtime via USB Command

Any of the registers can be manipulated via USB command during runtime. Note that not all registers should be modified during runtime, and some may require a hub reset in order to take effect.

The ProTouch2 software package contains a DLL library to aid in software development on Windows and Linux operating systems.

For applications which utilize an OS not supported by the ProTouch2 DLL library, the details of the USB commands are shown below.

6.3 Configuration Write

This command can be used to update any of the register addresses 0x0000-0xFFFF. To ensure predictable operation, only configuration writes must be limited to registers documented within this document. Furthermore, Reserved bits should never been changed. Failure to follow these requirements may result in unpredictable behavior. See Table 262.

6.3.1 CONFIGURATION WRITE SETUP PACKET DETAILS

TABLE 262: CONFIGURATION WRITE SETUP PACKET DETAILS

Setup Parameters	Value	Description
bmRequestType	0x41	Host-to-device, vendor class, targeted to interface
bRequest	0x03	CMD_CFG_WRITE
wValue	Configuration Address	Valid Address Range 0x0000-0xFFFF
wIndex	0x0000	Reserved
wLength	Data Length	Length of data bytes to write

6.3.2 CONFIGURATION WRITE TRANSACTION SEQUENCE

Command Phase: Host must send the following Setup packet initiate the configuration register write command.

Data Phase: Host must send the data bytes to be written of length wLength specified in Setup packet.

Status Phase: Hub will ACK upon completion of a configuration write.

6.4 Configuration Read

This command can be used to read any of the register addresses 0x0000-0xFFFF. See Table 263.

6.4.1 CONFIGURATION READ SETUP PACKET DETAILS

TABLE 263: CONFIGURATION READ SETUP PACKET DETAIL

Setup Parameters	Value	Description
bmRequestType	0xC1	Device-to-host, vendor class, targeted to interface
bRequest	0x04	CMD_CFG_READ
wValue	Configuration Address	Valid Address Range 0x0000-0xFFFF
wIndex	0x0000	Reserved
wLength	Data Length	Length of data bytes to read

6.4.2 CONFIGURATION READ TRANSACTION SEQUENCE

Command Phase: Host must send the following Setup packet initiate the configuration register read command.

Data Phase: Hub will send the data bytes of length wLength from the address specified in the Setup packet.

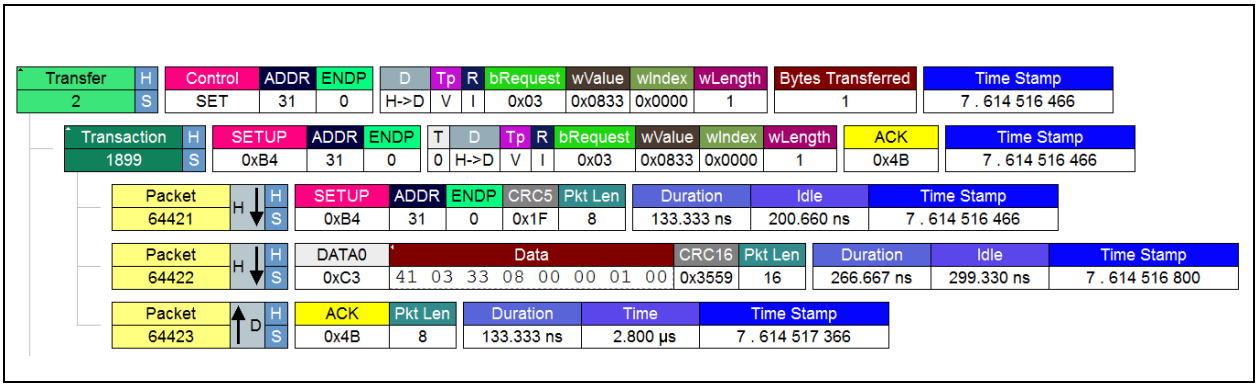
6.5 Configuration Write Example

1. **Command Phase (SETUP Transaction):** Send the following Setup Register Write command to Endpoint 0 of the USB58xx/USB59xx Hub Feature Controller to write the contents of registers 0x833 which contain the direction control settings for GPIOs 1 to 7. In this example, GPIOs 4 and 5 will be set as outputs, all other GPIOS will remain at the default Input state. See Table 264 and Figure 7.

TABLE 264: REGISTER WRITE SETUP COMMAND EXAMPLE

Setup Parameter	Value	Description
bmRequestType	0x41	—
bRequest	0x03	—
wValue	0x0833	First register in a series of consecutive registers to write from.
wIndex	0x0000	—
wLength	0x0001	1 register is to be read.

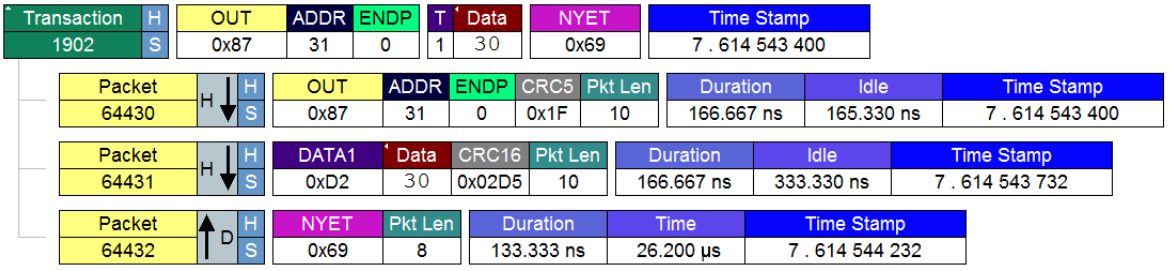
FIGURE 7: REGISTER WRITE SETUP TRANSACTION EXAMPLE



2. **Data Phase (OUT Transaction):** Host sends the one data bytes to set 0x833 = 0x30 after sending the OUT

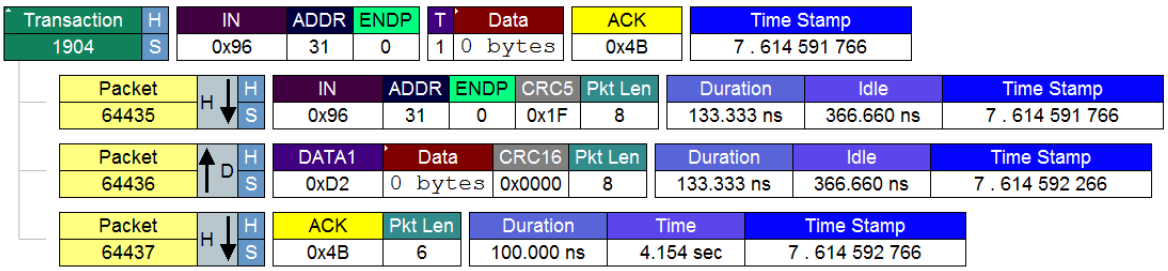
packet. See Figure 8.

FIGURE 8: REGISTER WRITE OUT TRANSACTION EXAMPLE



3. **Status Phase (OUT Transaction):** Host sends an IN packet to complete the USB Transfer. Hub Feature Controller responds with a zero length data packet.See Figure 9.

FIGURE 9: REGISTER WRITE IN TRANSACTION EXAMPLE



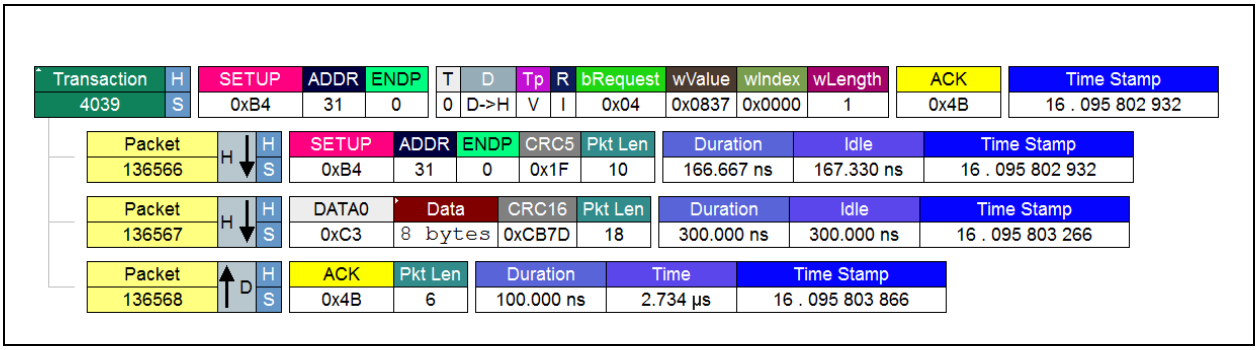
6.6 Configuration Read Example

1. **Command Phase (SETUP Transaction):** Send the following Setup Register Read command to Endpoint 0 of the USB58xx/USB59xx Hub Feature Controller to read the contents of registers 0x833 which contain the direction control settings for GPIOs 1 to 7. See Table 265 and Figure 10.

TABLE 265: REGISTER READ SETUP COMMAND EXAMPLE

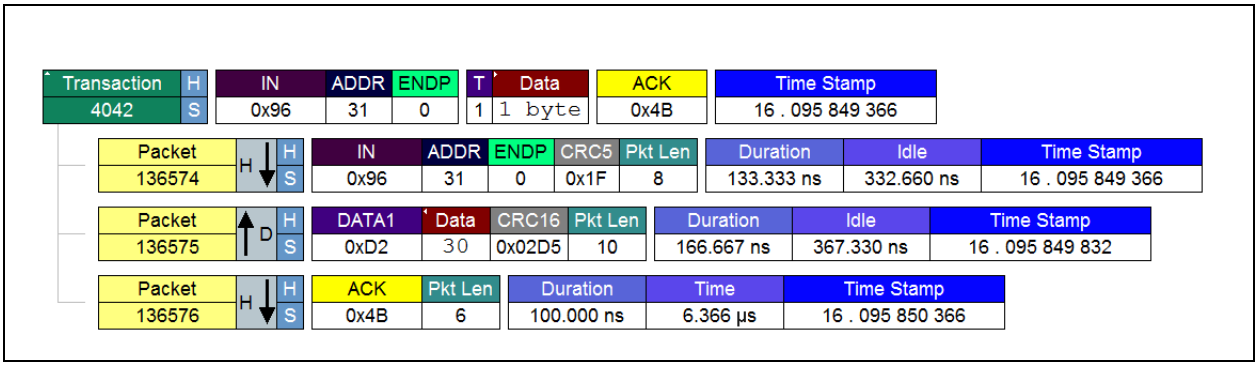
Setup Parameter	Value	Description
bmRequestType	0xC1	—
bRequest	0x04	—
wValue	0x0833	First register in a series of consecutive registers to read from.
wIndex	0x0000	—
wLength	0x0001	4 consecutive registers are to be read.

FIGURE 10: REGISTER READ SETUP TRANSACTION EXAMPLE



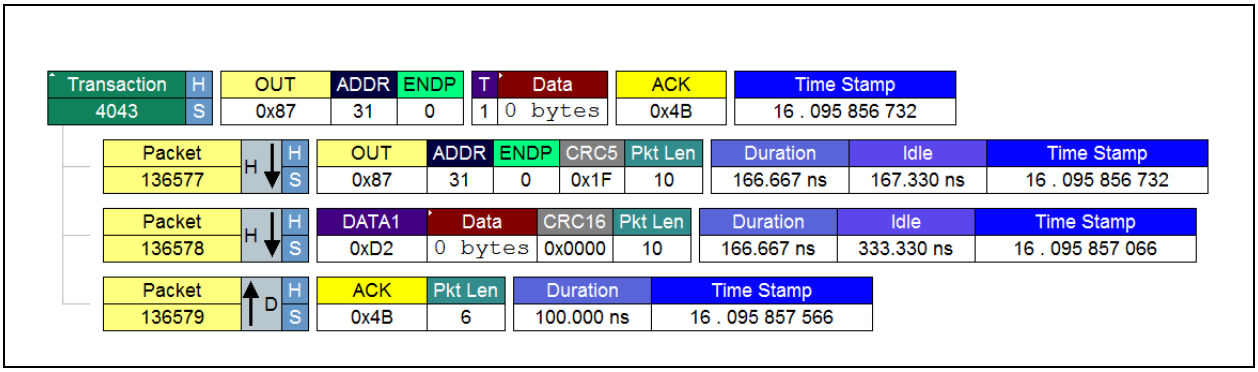
2. **Data Phase (IN Transaction):** Hub Feature Controller sends the data bytes of length wLength starting from the specified address after receiving an IN packet. See Figure 11.

FIGURE 11: REGISTER READ IN TRANSACTION EXAMPLE



3. **Status Phase (OUT Transaction):** Host sends an OUT packet to complete the USB Transfer. Hub Feature Controller responds with a zero-length data packet. See Figure 12.

FIGURE 12: REGISTER READ OUT TRANSACTION EXAMPLE



7.0 CONFIGURATION VIA VSM USB COMMAND TO HUB CONTROLLER

The USB5807 device does not include a Hub Feature Controller device, but basic register Read/Write commands can still be issued to the hub controller endpoints using VSM commands. Many major operating systems restrict issuing VSM commands from applications with standard permissions, so this method is primarily included for advanced users who have low-level access to USB control (such as in embedded processors) and may not be practical for many use-cases.

All VSM Commands are issued to the USB2 hub endpoint. The hub supports either register write or register read VSM commands. See Table 266.

TABLE 266: VSM COMMAND PARAMETERS

bmRequestType	bRequest	wValue	wIndex	wLength	Data
0x40	0x02	0x0000	REG_ADDR	WRITE_LEN	Byte 0 = 0x03 Bytes(s) 1 to N = REG_VALUE
0xC0	0x01	0x0000	REG_ADDR	READ_LEN	Data array of length = READ_LENGTH

The following are the input parameters for the VSM command:

- REG_ADDR = Any valid hub register address
- WRITE_LEN = Length of the REG_VALUE array **+ 1**
- REG_VALUE = Value(s) to be written to memory starting at the target register address
- READ_LEN = Length data be read starting at the target register address

8.0 STRING DESCRIPTORS

String descriptors allow human readable product text to be displayed when a device enumerates to a PC. It is common to include customized string data for consumer products.

Microchip USB58xx/USB59xx allows the following strings to be independently customized for the USB2 Hub, USB Hub, and internal Hub Feature Controller:

- Language ID – List published and maintained by USB-IF as (LANGIDs)
- Product description string
- Manufacturer string
- Serial string

String data is encoded in UTC16 unicode format in Little Endian. Two bytes are necessary for each character.

8.1 USB2 Hub String Descriptors

The USB2 Hub String Descriptor Data is contained within the registers defined in Table 267. The maximum combined number of unicode string characters for all strings is 90 characters.

TABLE 267: USB2 HUB STRING DESCRIPTOR REGISTERS

Register Address Start	Size	Name	Description
3013h	1	USB2_iManufacturer	Index value assigned to manufacturer string. Can be 01h, 02h, or 03h. Use 00h if unused.
3014h	1	USB2_iProduct	Index value assigned to product string. Can be 01h, 02h, or 03h. Use 00h if unused.
3015h	1	USB2_iSerialNumber	Index value assigned to serial string. Can be 01h, 02h, or 03h. Use 00h if unused.
4267h	1	USB2_byDeviceType0	Device type. Do not change. 01h = USB20_HUB
4268h	1	USB2_byDescType0	Descriptor type. Do not change. This descriptor shall always be the Language ID. 06h = STRING0_DESC
4269h	2	USB2_wLength0	[Big Endian] – Language ID shall always have a length of 0004h.
426Bh	2	USB2_wOffset0	[Big Endian] – Language ID shall always be placed in register 4325h.
426Dh	1	USB2_byDeviceType1	[Big Endian] – Device Type. Do not change. 01h = USB20_HUB
426Eh	1	USB2_byDescType1	[Big Endian] - Descriptor Type. Do not change. This descriptor shall always be the Language ID. 07h = STRING1_DESC
426Fh	2	USB2_wLength1	Length of String Descriptor 1
4271h	2	USB2_wOffset1	Starting Register location of String Descriptor 1. String data must be contained within 4329h – 43E3h
4273h	1	USB2_byDeviceType2	Device type. Do not change. 01h = USB20_HUB

TABLE 267: USB2 HUB STRING DESCRIPTOR REGISTERS

Register Address Start	Size	Name	Description
4274h	1	USB2_byDescType2	Descriptor type. Do not change. This descriptor shall always be the Language ID. 08h = STRING2_DESC
4275h	2	USB2_wLength2	[Big Endian] – Length of String Descriptor 2
4277h	2	USB2_wOffset2	[Big Endian] – Starting Register location of String Descriptor 1. String data must be contained within 4329h – 43E3h.
4279h	1	USB2_byDeviceType3	Device type. Do not change 01h = USB20_HUB
427Ah	1	USB2_byDescType3	Descriptor type. Do not change. This descriptor shall always be the Language ID. 09h = STRING2_DESC
427Bh	2	USB2_wLength3	[Big Endian] – Length of String Descriptor 2
427Dh	2	USB2_wOffset3	[Big Endian] – Starting Register location of String Descriptor 1. String data must be contained within 4329h – 43E3h
4325h	4	USB2_bLangID[32:0]	Contains the Language ID. By default the Language ID is set to 0409h for United States – English. Byte[0] = Combined Length (Always 04h) Byte[1] = Descriptor Type (Always 03h for String) Byte[3] = Language ID LSB Byte[4] = Language ID MSB
4329h	186	USB2_bString[1447:0]	String Data Container for all customized String Data.

8.1.1 USB2 HUB STRING CONFIGURATION EXAMPLE

In this example, the strings are to be programmed such that the USB2 Hub appears as shown in Table 268. Note that the index is selected by the user, any string can be assigned any index, but users cannot skip an index if two or fewer strings are used. The language ID is not modified in this example.

TABLE 268: USB2 HUB STRING DESCRIPTORS EXAMPLE

String Descriptor	Text	UTF-16 Length	Index	Combined Length	Descriptor Type	UTF-16 String Data (Little Endian)
Manufacturer	John's Engineering Co.	32 Bytes	1	2Eh	03h (String)	4A 00 6F 00 68 00 6E 00 19 20 73 00 20 00 45 00 6E 00 67 00 69 00 6E 00 65 00 65 00 72 00 69 00 6E 00 67 00 20 00 43 00 6F 00 2E 00
Product	USB2 Super Gizmo	44 Bytes	2	22h	03h (String)	55 00 53 00 42 00 32 00 20 00 53 00 75 00 70 00 65 00 72 00 20 00 47 00 69 00 7a 00 6D 00 6F 00
Serial	13243546	16 Bytes	3	12h	03h (String)	31 00 33 00 32 00 34 00 33 00 35 00 34 00 36 00

Note 1: The combined length is the UTF-16 String Data + 2

The raw binary data of Combined Length + Descriptor Type + String Data from each row is then concatenated together in the order of the previously defined Index. See Example 11.

EXAMPLE 11:

```
2E 03 4A 00 6F 00 68 00 6E 00 19 20 73 00 20 00 45 00 6E 00 67 00 69 00 6E 00 65 00 65
00 72 00 69 00 6E 00 67 00 20 00 43 00 6F 00 2E 00 22 03 55 00 53 00 42 00 32 00 20 00
53 00 75 00 70 00 65 00 72 00 20 00 47 00 69 00 7a 00 6D 00 6F 00 12 03 31 00 33 00 32
00 34 00 33 00 35 00 34 00 36 00
```

This concatenated data is then programmed into **USB2_bString[1447:0]** register beginning at **4329h**

Final Register Settings for this example:

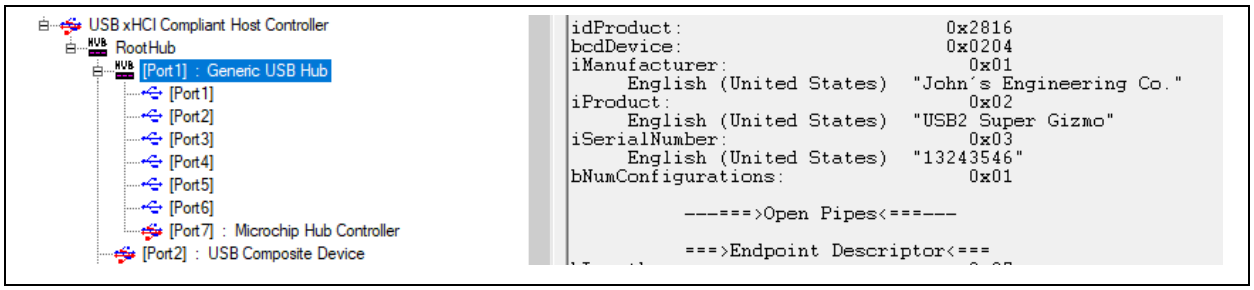
1. Set STRING_EN bit in HUB_CFG_3 to ensure string functionality is enabled. (Default value should be 09h, so this step may not be necessary.) **3008h** = 09
2. Program the Manufacturer Index Number to **USB2_iManufacturer: 3013h** = 01
3. Program the Product Index Number to **USB2_iProduct: 3014h** = 02
4. Program the Serial Index Number to **USB2_iSerialNumber: 3015h** = 03
5. Program **USB2_byDeviceType3** to 01h to indicate USB20_HUB: **426Dh =** 01
6. Program **USB2_byDescType1** to 07h to indicate STRING1_DESC: **426Eh =** 07
7. Program **USB2_wLength1** with the String Descriptor Index 1 Combined Length [Big Endian]: **426Fh =** 00 2E
8. Program **USB2_wOffset1** the String Descriptor Index 1 Register Location [Big Endian]:**4271h =** 43 29
9. Program **USB2_byDeviceType3** to 01h to indicate USB20_HUB: **4273h =** 01
10. Program **USB2_byDescType1** to 08h to indicate STRING2_DESC: **4274h =** 08
11. Program **USB2_wLength2** the String Descriptor Index 2 Combined Length [Big Endian]: **4275h =** 00 22
12. Program **USB2_wOffset2** the String Descriptor Index 2 Register Location [Big Endian]: **4277h =** 43 57
13. Program **USB2_byDeviceType3** to 01h to indicate USB20_HUB: **4279h =** 01
14. Program **USB2_byDescType3** to 09h to indicate STRING3_DESC: **427Ah =** 07
15. Program **USB2_wLength3** the String Descriptor Index 3 Combined Length [Big Endian]: **427Bh =** 00 12
16. Program **USB2_wOffset3** the String Descriptor Index 3 Register Location [Big Endian]: **427Dh** = 43 79
17. Program the Raw String Data to the String Container Registers. See Example 12.

EXAMPLE 12:

```
4329h = 2E 03 4A 00 6F 00 68 00 6E 00 19 20 73 00 20 00 45 00 6E 00 67 00 69 00 6E 00
65 00 65 00 72 00 69 00 6E 00 67 00 20 00 43 00 6F 00 2E 00 22 03 55 00 53 00 42 00 32
00 20 00 53 00 75 00 70 00 65 00 72 00 20 00 47 00 69 00 7a 00 6D 00 6F 00 12 03 31 00
33 00 32 00 34 00 33 00 35 00 34 00 36 00
```

After making these modifications, the changes to the string descriptors will appear to a USB host as illustrated in Figure 13.

FIGURE 13: USB3 HUB CUSTOM STRING EXAMPLE APPEARANCE IN USB VIEW



The raw data for an OTP patch in Example 13 can be applied to the hub to achieve the results for the example.

EXAMPLE 13:

```
80 30 08 FE 00 01 09 80 30 13 03 01 02 03 80 42 6D 12 01 07 00 2E 43 29 01 08 00 22 43
57 01 09 00 12 43 79 80 43 29 62 2E 03 4A 00 6F 00 68 00 6E 00 19 20 73 00 20 00 45 00
6E 00 67 00 69 00 6E 00 65 00 65 00 72 00 69 00 6E 00 67 00 20 00 43 00 6F 00 2E 00 22
03 55 00 53 00 42 00 32 00 20 00 53 00 75 00 70 00 65 00 72 00 20 00 47 00 69 00 7A 00
6D 00 6F 00 12 03 31 00 33 00 32 00 34 00 33 00 35 00 34 00 36 00 FF
```

8.2 USB3 Hub String Descriptors

The USB3 Hub String Descriptor Data is contained within the registers defined in the table below. The maximum combined number of unicode string characters for all strings is 90. See Table 269.

TABLE 269: USB3 HUB STRING DESCRIPTOR REGISTERS

Register Address Start	Size	Name	Description
4410h	2	USB3_StringDescriptor-0Size[15:0]	[Little Endian] Combined Length of String 0 Data **(Note 1)**
4412h	2	USB3_StringDescriptor-0Offset[15:0]	[Little Endian] Offset from base address 4400h where the String Descriptor 0 data begins **(Note 2)**
4414h	2	USB3_StringDescriptor-1Size[15:0]	[Little Endian] Combined Length of String 1 Data
4416h	2	USB3_StringDescriptor-1Offset[15:0]	[Little Endian] Offset from base address 4400h where the String Descriptor 1 data begins
4418h	2	USB3_StringDescriptor-2Size[15:0]	[Little Endian] Combined Length of String 2 Data
441Ah	2	USB3_StringDescriptor-2Offset[15:0]	[Little Endian] Offset from base address 4400h where the String Descriptor 2 data begins
441Ch	2	USB3_StringDescriptor-3Size[15:0]	[Little Endian] Combined Length of String 3 Data
441Eh	2	USB3_StringDescriptor-3Offset[15:0]	[Little Endian] Offset from base address 4400h where the String Descriptor 1 data begins
444Eh	1	USB3_iManufacturer	Index value assigned to Manufacturer String. Can be 01h, 02h, or 03h. Use 00h if unused
444Fh	1	USB3_iProduct	Index value assigned to Manufacturer String. Can be 01h, 02h, or 03h. Use 00h if unused.
4450h	1	USB3_iSerialNumber	Index value assigned to Manufacturer String. Can be 01h, 02h, or 03h. Use 00h if unused.
44ACh	4	USB3_bLangID[32:0]	Contains the Language ID. By default the Language ID is set to 0409h for the United States. Byte[0] = Combined Length (Always 04h) Byte[1] = Index (Always 03h) Byte[3] = Language ID LSB Byte[4] = Language ID MSB
44B0h	186	USB3_bString[1447:0]	String Data Container for all customized String Data.

Note 1: String Descriptor 0 should always be used for Language ID, and hence this length always shall be 0004h.
2: String Descriptor 0 should always be used for Language ID, and hence the offset shall always be 00ACh.

8.2.1 USB3 HUB STRING CONFIGURATION EXAMPLE

In this example, the strings are to be programmed such that the USB3 hub appears as shown in Table 270. The string indices are reversed from the USB2 example to show that the Index is selected by the system integrator. Any string can be assigned any index, but you cannot skip an index if two or fewer strings are used. The language ID is not modified in this example.

TABLE 270: USB3 HUB STRING DESCRIPTORS EXAMPLE

String Descriptor	Text	UTF-16 Length	Index	Combined Length	Descriptor Type	UTF-16 String Data (Little Endian)
Manufacturer	ACME	8 Bytes	3	0Ah	03h (String)	41 00 43 00 4d 00 45 00
Product	UltraFastUSBHub	30 Bytes	2	20h	03h (String)	55 00 6C 00 74 00 72 00 61 00 46 00 61 00 73 00 74 00 55 00 53 00 42 00 48 00 75 00 62 00
Serial	A-00001	14 Bytes	1	10h	03h (String)	41 00 2D 00 30 00 30 00 30 00 30 00 31 00
Note 1: The Combined Length is the UTF-16 String Data + 2						

The raw binary data from each row is then concatenated together in the order of the previously defined Index. See Example 14.

EXAMPLE 14:

```
10 03 41 00 2D 00 30 00 30 00 30 00 30 00 31 00 20 03 55 00 6C 00 74 00 72 00 61 00 46
00 61 00 73 00 74 00 55 00 53 00 42 00 48 00 75 00 62 00 0A 03 41 00 43 00 4d 00 45 00
```

This concatenated data is then programmed into **USB3_bString[1447:0]** register beginning at **44B0h**

Final Register Settings for this example:

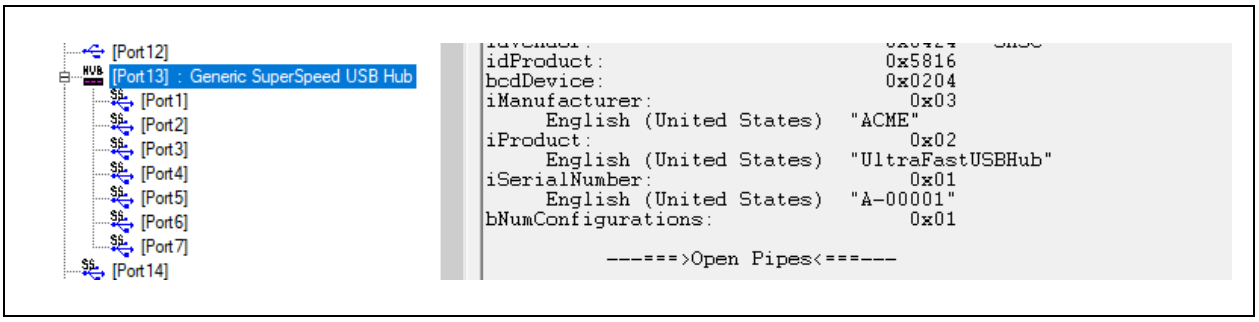
1. Program the String Descriptor Index 1 Combined Length [Little Endian]: **4414h =** 10 00
2. Program the String Descriptor Index 1 Offset (From base address 4400h) [Little Endian]: **4416h =** B0 00
3. Program the String Descriptor Index 2 Combined Length [Little Endian]: **4418h =** 20 00
4. Program the String Descriptor Index 2 Memory Offset (From base address 4400h) [Little Endian]: **441Ah =** C0 00
5. Program the String Descriptor Index 3 Combined Length [Little Endian]: **441Ch =** 0A 00
6. Program the String Descriptor Index 3 Memory Offset (From base address 4400h) [Little Endian]: **441Eh** = E0 00
7. Program the Manufacturer Index Number to **USB3_iManufacturer**: **444Eh** = 03
8. Program the Product Index Number to **USB3_iProduct**: **444Fh** = 02
9. Program the Serial Index Number to **USB3_iSerialNumber**: **4450h** = 01
10. Program the Raw String Data to **USB3_bString**. See Example 15.

EXAMPLE 15:

```
44B0h = 10 03 41 00 2D 00 30 00 30 00 30 00 30 00 31 00 20 03 55 00 6C 00 74 00 72 00
61 00 46 00 61 00 73 00 74 00 55 00 53 00 42 00 48 00 75 00 62 00 0A 03 41 00 43 00 4d
00 45 00
```

After making these modifications, the changes to the string descriptors will appear to a USB host as indicated in Figure 14.

FIGURE 14: USB3 HUB CUSTOM STRING EXAMPLE APPEARANCE IN USB VIEW



The follow is the raw data for an OTP patch which can be applied to the hub to achieve the results in Example 16.

EXAMPLE 16:

```
80 44 14 FE 00 0C 10 00 B0 00 20 00 C0 00 0A 00 E0 00 80 44 4E 03 03 02 01 80 44 B0 3A
10 03 41 00 2D 00 30 00 30 00 30 00 30 00 31 00 20 03 55 00 6C 00 74 00 72 00 61 00 46
00 61 00 73 00 74 00 55 00 53 00 42 00 48 00 75 00 62 00 0A 03 41 00 43 00 4D 00 45 00
FF
```

8.3 Hub Feature Controller (UDC) String Descriptors

The USB2 Hub Feature Controller String Descriptor Data is contained within the registers defined in the table below. The maximum combined number of unicode string characters for all strings is 60. The HFC is limited to only two simultaneous strings. See Table 271.

TABLE 271: USB3 HUB STRING DESCRIPTORS EXAMPLE

Register Address Start	Size	Name	Description
4194h	4	HFC_bLangID[32:0]	Contains the Language ID. By default the Language ID is set to 0409h for United States - English. Byte[0] = Combined Length (Always 04h) Byte[1] = Descriptor Type (Always 03h for String) Byte[3] = Language ID LSB Byte[4] = Language ID MSB
4198h	124	HFC_bString[991:0]	String Data Container for all customized String Data.
42DCh	1	HFC_iManufacturer	Index value assigned to Manufacturer String. Can be 01h, 02h, or 03h. Use 00h if unused.
42DDh	1	HFC_iProduct	Index value assigned to Product String. Can be 01h, 02h, or 03h. Use 00h if unused.
42DEh	1	HFC_iSerialNumber	Index value assigned to Serial String. Can be 01h, 02h, or 03h. Use 00h if unused.

8.3.1 USB2 HUB STRING CONFIGURATION EXAMPLE

In this example, the strings are to be programmed such that the USB2 Hub Feature Controller device appears as shown in Table 272. As the HFC device is limited to two strings, only a Product and Serial is specified.

The language ID is in this example is modified to Spanish, 2C0Ah.

TABLE 272: USB2 HUB FEATURE CONTROLLER STRING DESCRIPTORS EXAMPLE

String Descriptor	Text	UTF-16 Length	Index	Combined Length	Descriptor Type	UTF-16 String Data (Little Endian)
Manufacturer	n/a	—	—	—	—	—
Product	USB Compañero	44 Bytes	1	1Ch	03h (String)	55 00 53 00 42 00 20 00 43 00 6F 00 6D 00 70 00 61 00 F1 00 65 00 72 00 6F 00
Serial	01-01-2010-apara-to3052	46 Bytes	2	2Eh	03h (String)	30 00 31 00 2D 00 30 00 31 00 2D 00 32 00 30 00 31 00 30 00 2D 00 61 00 70 00 61 00 72 00 61 00 74 00 6F 00 33 00 30 00 35 00 32 00
Note 1: The Combined Length is the UTF-16 String Data + 2						

The raw binary data of Combined Length + Descriptor Type + String Data from each row is then concatenated together in the order of the previously defined Index. See Example 17.

EXAMPLE 17:

```
1C 03 55 00 53 00 42 00 20 00 43 00 6F 00 6D 00 70 00 61 00 F1 00 65 00 72 00 6F 00 2E
03 30 00 31 00 2D 00 30 00 31 00 2D 00 32 00 30 00 31 00 30 00 2D 00 61 00 70 00 61 00
72 00 61 00 74 00 6F 00 33 00 30 00 35 00 32 00
```

This concatenated data is then programmed into **HFC_bString[991:0]** register beginning at **4198h.**

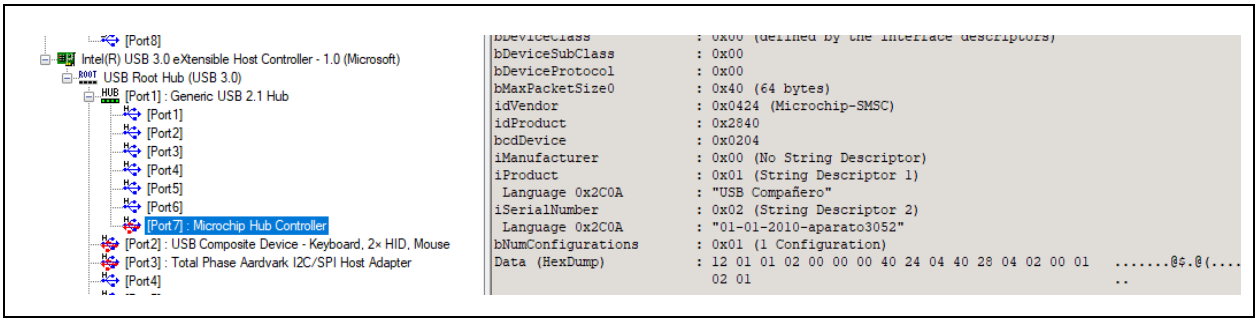
Final Register Settings for this example:

1. Program **HFC_bLangID** to indicate Spanish (LANGID = 2C0Ah): **4194h =** 04 03 0A 2C
2. Program the Raw String Data to **HFC_bString**:

   4198h = 1C 03 55 00 53 00 42 00 20 00 43 00 6F 00 6D 00 70 00 61 00 F1 00 65 00 72 00 6F 00 2E 03 30 00 31 00 2D 00 30 00 31 00 2D 00 32 00 30 00 31 00 30 00 2D 00 61 00 70 00 61 00 72 00 61 00 74 00 6F 00 33 00 30 00 35 00 32 00
3. Program the Manufacturer Index Number to **HFC_iManufacturer: 42DCh** = 00
4. Program the Product Index Number to **HFC_iProduct: 42DEh** = 01
5. Program the Serial Index Number **HFC_iSerialNumber: 42DDh** = 02

After making these modifications, the changes to the string descriptors will appear to a USB host as shown in Figure 15.

FIGURE 15: USB3 HFC CUSTOM STRING EXAMPLE APPEARANCE IN USB VIEW



The following is the raw data for an OTP patch which can be applied to the hub to achieve the results in Example 18.

EXAMPLE 18:

```
80 41 94 4E 04 03 0A 2C 1C 03 55 00 53 00 42 00 20 00 43 00 6F 00 6D 00 70 00 61 00 F1
00 65 00 72 00 6F 00 2E 03 30 00 31 00 2D 00 30 00 31 00 2D 00 32 00 30 00 31 00 30 00
2D 00 61 00 70 00 61 00 72 00 61 00 74 00 6F 00 33 00 30 00 35 00 32 00 80 42 DC 03 00
01 02 FF
```

9.0 HUB PRODUCT IDS

9.1 Hub Feature Controller (UDC)

The Hub Feature Controller (UDC) is enabled by default, thus reported as a non-removable device. The Hub Feature Controller exposes different USB interfaces depending on the state of the configuration straps (CONFIG_STRAPx pins), enabling the features relevant to the selected PFx pins.

9.2 Hub PID Selection

Table 273 shows the USB2 Hub, USB3 Hub, and UDC PIDs based on part number.

TABLE 273: PID SELECTION OPTIONS

Device	Package	USB2 HUB PID	USB3 HUB PID	UDC PID
USB5807	QFN100	2807h	5807h	2840h
USB5806	QFN100	2806h	5806h	2840h
USB5816	QFN100	2816h	5816h	2840h
USB5826	QFN100	2826h	5826h	2840h
USB5906	QFN100	2906h	5906h	2840h
USB5916	QFN100	2916h	5916h	2840h
USB5926	QFN100	2926h	5926h	2840h

9.3 Automatic PID Adjustment Based on Port Disable Straps

If USB ports are disabled via the Port Disable strap options (achieved by pulling D+ and D– pins of to 3.3V on the PCB) the PID of the hub is automatically adjusted to reflect the change. The PID will be decreased by 01h for every port that is disabled.

Some examples:

- USB5806 with 1 port disabled via strap
  - USB2 Hub PID = 2805h
  - USB3 Hub PID = 5805h
- USB5926 with 2 ports disabled via strap
  - USB2 Hub PID = 2924h
  - USB3 Hub PID = 5924h
- USB5807 with 3 ports disabled via strap
  - USB2 Hub PID = 2804h
  - USB3 Hub PID = 5804h

10.0 BILLBOARD DEVICE DESCRIPTOR

The Billboard (BB) is a device which is attached to the Hub Feature Controller (UDC) endpoint when enabled. The purpose of the Billboard device is to prompt the user that the alternate mode negotiation through Type-C lines has failed.

A Billboard device must be controlled from an external USB Power Delivery controller within the USB system that the USB58xx/USB59xx is designed in.

10.1 Billboard Enumeration Sequence

The Billboard is not a permanent device. It will be enumerated only when the negotiation fails in the following order:

1. Normal Hub enumeration happens.
2. The PF pin to be used for BB is written in the OTP.
3. When the PF pin detects a high to low edge, an interrupt is triggered for BB enumeration sequence.
4. The Hub Feature Controller device is detached.
5. The Billboard device attaches to the port where Hub Feature Controller was previously connected.
6. Timer A (1s timeout) is configured and started.
7. As soon as the host asks for the string descriptor, Timer B (100 ms) is configured.
8. Once either of these timers expire, the BB is detached and UDC will now attach as the Hub Feature Controller device.

10.2 Billboard Descriptor Addresses

The Billboard descriptors can be customized following the formatting described within the USB Billboard class device specification. See Table 274 and Table 275.

TABLE 274: BILLBOARD DESCRIPTORS

Descriptor Type	Size (Bytes)	Start Address	End Address	Default (hex)
BOS Descriptor	5	4C00h	4C04h	05 0f 49 00 02
Container ID	20	4C05h	4C18h	14 10 04 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10
Billboard Capability	48	4C19h	4C49h	See Billboard Capability Descriptors.
String Descriptors	128	4C51h	4CD0h	04 03 09 04 14 03 4D 00 69 00 63 00 72 00 6F 00 63 00 68 00 69 00 70 00 2E 03 48 00 75 00 62 00 20 00 46 00 65 00 61 00 74 00 75 00 72 00 65 00 20 00 43 00 6F 00 6E 00 74 00 72 00 6F 00 6C 00 6C 00 65 00 72 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Configuration Descriptor: Config	9	4CD1h	4CD9h	09 02 12 00 01 01 00 C0 00

TABLE 274: BILLBOARD DESCRIPTORS (CONTINUED)

Descriptor Type	Size (Bytes)	Start Address	End Address	Default (hex)
Configuration Descriptor: Interface	9	4CDAh	4CE2h	09 04 00 00 00 11 00 00 00
Device Descriptor	12	4CE3h	4CEEh	12 01 01 02 11 00 00 40 24 04 40 28

TABLE 275: BILLBOARD CAPABILITY DESCRIPTORS

Descriptor Type	Size (Bytes)	Start Address	End Address	Default (hex)
bLength	1	4C19h	—	30
bDescriptorType	1	4C1Ah	—	10
bDevCapabilityType	1	4C1Bh	—	0D
iAdditionalInfoURL	1	4C1Ch	—	01
bNumberofAlternateModes	1	4C1Dh	—	01
bPreferredAlternateMode	1	4C1Eh	—	00
VCONN Power	2	4C1Fh	4C20h	00 80
bmConfigured	32	4C21h	4C41h	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
bcdVersion	2	4C42h	4C43h	01 00
bAdditonalFailureInfo	1	4C44h	—	00
bReserved	1	4C45h	—	00
wSVID[0]	2	4C46h	4C47h	FF 00
bAlternateMode[0]	1	4C48h	—	01
iAlternateModeString[0]	1	4C49h	—	00

11.0 PHYSICAL AND LOGICAL PORT MAPPING

USB58xx/USB59xx family of devices are based upon a common architecture, but all have different port settings and mapping to achieve the various device configurations.

The base chip is composed of a total of 8 USB3 PHYs and 8 USB2 PHYs. These PHYs are physically arranged on the chip in a certain way, which is what is referred to as the physical port mapping.

The actual port numbering may be remapped by default in different ways on each product. This changes the way that the ports are numbered from the USB host's perspective. This is referred to as logical mapping.

The various configuration options available for these devices may at times be with respect to physical mapping or logical mapping. Each individual configuration option which has a physical or logical dependency is declared as such within the register description.

Physical versus logical mapping is described within each device's respective data sheet, and is also abbreviated in Table 276 to Table 282.

Note: The device data sheets also include visual aids for describing the logical vs. physical mapping.

A system design in schematics and layout is generally performed using the pinout from the device data sheet, which is assigned by the default logical mapping. Hence it is necessary to cross reference the physical vs. logical lookup tables when determining the hub configuration.

Note: The MPLAB Connect Configurator tool makes configuration simple. The settings can be selected by the user with respect to the logical port numbering. The tool handles the necessary linking to the physical port settings.

TABLE 276: USB5807 PHYSICAL VS. LOGICAL PORT MAPPING

Device Pin	Pin Name (as in data sheet)	LOGICAL PORT NUMBER								PHYSICAL PORT NUMBER							
		0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
6	USB2DN_DP1		X								X						
7	USB2DN_DM1		X								X						
8	USB3DN_TXDP1		X								X						
9	USB3DN_TXDM1		X								X						
11	USB3DN_RXDP1		X								X						
12	USB3DN_RXDM1		X								X						
13	USB2DN_DP2			X								X					
14	USB2DN_DM2			X								X					
15	USB3DN_TXDP2			X								X					
16	USB3DN_TXDM2			X								X					
18	USB3DN_RXDP2			X								X					
19	USB3DN_RXDM2			X								X					
28	USB2DN_DP3				X								X				
29	USB2DN_DM3				X								X				
30	USB3DN_TXDP3				X								X				
31	USB3DN_TXDM3				X								X				
33	USB3DN_RXDP3				X								X				
34	USB3DN_RXDM3				X								X				
35	USB2DN_DP4					X								X			
36	USB2DN_DM4					X								X			

TABLE 276: USB5807 PHYSICAL VS. LOGICAL PORT MAPPING (CONTINUED)

Device Pin	Pin Name (as in data sheet)	LOGICAL PORT NUMBER								PHYSICAL PORT NUMBER							
		0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
37	USB3DN_TXDP4					X								X			
38	USB3DN_TXDM4					X								X			
40	USB3DN_RXDP4					X								X			
41	USB3DN_RXDM4					X								X			
43	USB2DN_DP5						X								X		
44	USB2DN_DM5						X								X		
45	USB3DN_TXDP5						X								X		
46	USB3DN_TXDM5						X								X		
48	USB3DN_RXDP5						X								X		
49	USB3DN_RXDM5						X								X		
79	USB2DN_DP7								X								X
80	USB2DN_DM7								X								X
81	USB3DN_TXDP7								X								X
82	USB3DN_TXDM7								X								X
84	USB3DN_RXDP7								X								X
85	USB3DN_RXDM7								X								X
86	USB2DN_DP6							X								X	
87	USB2DN_DM6							X								X	
88	USB3DN_TXDP6							X								X	
89	USB3DN_TXDM6							X								X	
91	USB3DN_RXDP6							X								X	
92	USB3DN_RXDM6							X								X	
94	USB2UP_DP	X								X							
95	USB2UP_DM	X								X							
96	USB3UP_TXDP	X								X							
97	USB3UP_TXDM	X								X							
99	USB3UP_RXDP	X								X							
100	USB3UP_RXDM	X								X							

TABLE 277: USB5806 PHYSICAL VS. LOGICAL PORT MAPPING

Device Pin	Pin Name (as in datasheet)	LOGICAL PORT NUMBER								PHYSICAL PORT NUMBER							
		0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
6	USB2DN_DP1		X								X						
7	USB2DN_DM1		X								X						
8	USB3DN_TXDP1		X								X						
9	USB3DN_TXDM1		X								X						
11	USB3DN_RXDP1		X								X						
12	USB3DN_RXDM1		X								X						
13	USB2DN_DP2			X								X					
14	USB2DN_DM2			X								X					
15	USB3DN_TXDP2			X								X					
16	USB3DN_TXDM2			X								X					
18	USB3DN_RXDP2			X								X					

TABLE 277: USB5806 PHYSICAL VS. LOGICAL PORT MAPPING (CONTINUED)

Device Pin	Pin Name (as in datasheet)	LOGICAL PORT NUMBER								PHYSICAL PORT NUMBER							
		0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
19	USB3DN_RXDM2			X								X					
28	USB2DN_DP3				X								X				
29	USB2DN_DM3				X								X				
30	USB3DN_TXDP3				X								X				
31	USB3DN_TXDM3				X								X				
33	USB3DN_RXDP3				X								X				
34	USB3DN_RXDM3				X								X				
35	USB2DN_DP4					X								X			
36	USB2DN_DM4					X								X			
37	USB3DN_TXDP4					X								X			
38	USB3DN_TXDM4					X								X			
40	USB3DN_RXDP4					X								X			
41	USB3DN_RXDM4					X								X			
43	USB2DN_DP5						X								X		
44	USB2DN_DM5						X								X		
45	USB3DN_TXDP5						X								X		
46	USB3DN_TXDM5						X								X		
48	USB3DN_RXDP5						X								X		
49	USB3DN_RXDM5						X								X		
86	USB2DN_DP6							X								X	
87	USB2DN_DM6							X								X	
88	USB3DN_TXDP6							X								X	
89	USB3DN_TXDM6							X								X	
91	USB3DN_RXDP6							X								X	
92	USB3DN_RXDM6							X								X	
94	USB2UP_DP	X								X							
95	USB2UP_DM	X								X							
96	USB3UP_TXDP	X								X							
97	USB3UP_TXDM	X								X							
99	USB3UP_RXDP	X								X							
100	USB3UP_RXDM	X								X							

TABLE 278: USB5816 PHYSICAL VS. LOGICAL PORT MAPPING

Device Pin	Pin Name (as in datasheet)	LOGICAL PORT NUMBER								PHYSICAL PORT NUMBER							
		0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
6	USB2DN_DP1		X								X						
7	USB2DN_DM1		X								X						
8	USB3DN_TXDP1A		X								X						
9	USB3DN_TXDM1A		X								X						
11	USB3DN_RXDP1A		X								X						
12	USB3DN_RXDM1A		X								X						
13	USB2DN_DP6							X				X					
14	USB2DN_DM6							X				X					

TABLE 278: USB5816 PHYSICAL VS. LOGICAL PORT MAPPING (CONTINUED)

Device Pin	Pin Name (as in datasheet)	LOGICAL PORT NUMBER								PHYSICAL PORT NUMBER							
		0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
15	USB3DN_TXDP1B		X									X					
16	USB3DN_TXDM1B		X									X					
18	USB3DN_RXDP1B		X									X					
19	USB3DN_RXDM1B		X									X					
28	USB2DN_DP2			X									X				
29	USB2DN_DM2			X									X				
30	USB3DN_TXDP2			X									X				
31	USB3DN_TXDM2			X									X				
33	USB3DN_RXDP2			X									X				
34	USB3DN_RXDM2			X									X				
35	USB2DN_DP3				X									X			
36	USB2DN_DM3				X									X			
37	USB3DN_TXDP3				X									X			
38	USB3DN_TXDM3				X									X			
40	USB3DN_RXDP3				X									X			
41	USB3DN_RXDM3				X									X			
43	USB2DN_DP4					X									X		
44	USB2DN_DM4					X									X		
45	USB3DN_TXDP4					X									X		
46	USB3DN_TXDM4					X									X		
48	USB3DN_RXDP4					X									X		
49	USB3DN_RXDM4					X									X		
86	USB2DN_DP5						X									X	
87	USB2DN_DM5						X									X	
88	USB3DN_TXDP5						X									X	
89	USB3DN_TXDM5						X									X	
91	USB3DN_RXDP5						X									X	
92	USB3DN_RXDM5						X									X	
94	USB2UP_DP	X								X							
95	USB2UP_DM	X								X							
96	USB3UP_TXDP	X								X							
97	USB3UP_TXDM	X								X							
99	USB3UP_RXDP	X								X							
100	USB3UP_RXDM	X								X							

TABLE 279: USB5826 PHYSICAL VS. LOGICAL PORT MAPPING

Device Pin	Pin Name (as in datasheet)	LOGICAL PORT NUMBER								PHYSICAL PORT NUMBER							
		0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
6	USB2DN_DP1		X								X						
7	USB2DN_DM1		X								X						
8	USB3DN_TXDP1A		X								X						
9	USB3DN_TXDM1A		X								X						
11	USB3DN_RXDP1A		X								X						

TABLE 279: USB5826 PHYSICAL VS. LOGICAL PORT MAPPING

Device Pin	Pin Name (as in datasheet)	LOGICAL PORT NUMBER								PHYSICAL PORT NUMBER							
		0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
12	USB3DN_RXDM1A		X								X						
13	USB2DN_DP5						X					X					
14	USB2DN_DM5						X					X					
15	USB3DN_TXDP1B		X									X					
16	USB3DN_TXDM1B		X									X					
18	USB3DN_RXDP1B		X									X					
19	USB3DN_RXDM1B		X									X					
28	USB2DN_DP2			X									X				
29	USB2DN_DM2			X									X				
30	USB3DN_TXDP2A			X									X				
31	USB3DN_TXDM2A			X									X				
33	USB3DN_RXDP2A			X									X				
34	USB3DN_RXDM2A			X									X				
35	USB2DN_DP6							X						X			
36	USB2DN_DM6							X						X			
37	USB3DN_TXDP2B			X										X			
38	USB3DN_TXDM2B			X										X			
40	USB3DN_RXDP2B			X										X			
41	USB3DN_RXDM2B			X										X			
43	USB2DN_DP3				X										X		
44	USB2DN_DM3				X										X		
45	USB3DN_TXDP3				X										X		
46	USB3DN_TXDM3				X										X		
48	USB3DN_RXDP3				X										X		
49	USB3DN_RXDM3				X										X		
86	USB2DN_DP4					X										X	
87	USB2DN_DM4					X										X	
88	USB3DN_TXDP4					X										X	
89	USB3DN_TXDM4					X										X	
91	USB3DN_RXDP4					X										X	
92	USB3DN_RXDM4					X										X	
94	USB2UP_DP	X								X							
95	USB2UP_DM	X								X							
96	USB3UP_TXDP	X								X							
97	USB3UP_TXDM	X								X							
99	USB3UP_RXDP	X								X							
100	USB3UP_RXDM	X								X							

TABLE 280: USB5906 PHYSICAL VS. LOGICAL PORT MAPPING

Device Pin	Pin Name (as in Data Sheet)	LOGICAL PORT NUMBER								PHYSICAL PORT NUMBER							
		0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
6	USB2DN_DP1		X								X						
7	USB2DN_DM1		X								X						

TABLE 280: USB5906 PHYSICAL VS. LOGICAL PORT MAPPING (CONTINUED)

Device Pin	Pin Name (as in Data Sheet)	LOGICAL PORT NUMBER								PHYSICAL PORT NUMBER							
		0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
8	USB3DN_TXDP1		X								X						
9	USB3DN_TXDM1		X								X						
11	USB3DN_RXDP1		X								X						
12	USB3DN_RXDM1		X								X						
13	USB2DN_DP2			X								X					
14	USB2DN_DM2			X								X					
15	USB3DN_TXDP2			X								X					
16	USB3DN_TXDM2			X								X					
18	USB3DN_RXDP2			X								X					
19	USB3DN_RXDM2			X								X					
28	USB2DN_DP3				X								X				
29	USB2DN_DM3				X								X				
30	USB3DN_TXDP3				X								X				
31	USB3DN_TXDM3				X								X				
33	USB3DN_RXDP3				X								X				
34	USB3DN_RXDM3				X								X				
35	USB2DN_DP4					X								X			
36	USB2DN_DM4					X								X			
37	USB3DN_TXDP4					X								X			
38	USB3DN_TXDM4					X								X			
40	USB3DN_RXDP4					X								X			
41	USB3DN_RXDM4					X								X			
43	USB2DN_DP5						X								X		
44	USB2DN_DM5						X								X		
45	USB3DN_TXDP5						X								X		
46	USB3DN_TXDM5						X								X		
48	USB3DN_RXDP5						X								X		
49	USB3DN_RXDM5						X								X		
81	USB3UP_TXDPB	X															X
82	USB3UP_TXDMB	X															X
84	USB3UP_RXDPB	X															X
85	USB3UP_RXDMB	X															X
86	USB2DN_DP6							X								X	
87	USB2DN_DM6							X								X	
88	USB3DN_TXDP6							X								X	
89	USB3DN_TXDM6							X								X	
91	USB3DN_RXDP6							X								X	
92	USB3DN_RXDM6							X								X	
94	USB2UP_DP	X								X							
95	USB2UP_DM	X								X							
96	USB3UP_TXDPA	X								X							
97	USB3UP_TXDMA	X								X							
99	USB3UP_RXDPA	X								X							

TABLE 280: USB5906 PHYSICAL VS. LOGICAL PORT MAPPING (CONTINUED)

Device Pin	Pin Name (as in Data Sheet)	LOGICAL PORT NUMBER								PHYSICAL PORT NUMBER							
		0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
100	USB3UP_RXDMA	X								X							

TABLE 281: USB5916 PHYSICAL VS. LOGICAL PORT MAPPING

Device Pin	Pin Name (as in Data Sheet)	LOGICAL PORT NUMBER								PHYSICAL PORT NUMBER							
		0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
6	USB2DN_DP1		X								X						
7	USB2DN_DM1		X								X						
8	USB3DN_TXDP1A		X								X						
9	USB3DN_TXDM1A		X								X						
11	USB3DN_RXDP1A		X								X						
12	USB3DN_RXDM1A		X								X						
13	USB2DN_DP6							X				X					
14	USB2DN_DM6							X				X					
15	USB3DN_TXDP1B		X									X					
16	USB3DN_TXDM1B		X									X					
18	USB3DN_RXDP1B		X									X					
19	USB3DN_RXDM1B		X									X					
28	USB2DN_DP2			X									X				
29	USB2DN_DM2			X									X				
30	USB3DN_TXDP2			X									X				
31	USB3DN_TXDM2			X									X				
33	USB3DN_RXDP2			X									X				
34	USB3DN_RXDM2			X									X				
35	USB2DN_DP3				X									X			
36	USB2DN_DM3				X									X			
37	USB3DN_TXDP3				X									X			
38	USB3DN_TXDM3				X									X			
40	USB3DN_RXDP3				X									X			
41	USB3DN_RXDM3				X									X			
43	USB2DN_DP4					X									X		
44	USB2DN_DM4					X									X		
45	USB3DN_TXDP4					X									X		
46	USB3DN_TXDM4					X									X		
48	USB3DN_RXDP4					X									X		
49	USB3DN_RXDM4					X									X		
81	USB3UP_TXDPB	X															X
82	USB3UP_TXDMB	X															X
84	USB3UP_RXDPB	X															X
85	USB3UP_RXDMB	X															X
86	USB2DN_DP5						X									X	
87	USB2DN_DM5						X									X	
88	USB3DN_TXDP5						X									X	
89	USB3DN_TXDM5						X									X	

TABLE 281: USB5916 PHYSICAL VS. LOGICAL PORT MAPPING (CONTINUED)

Device Pin	Pin Name (as in Data Sheet)	LOGICAL PORT NUMBER								PHYSICAL PORT NUMBER							
		0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
91	USB3DN_RXDP5						X									X	
92	USB3DN_RXDM5						X									X	
94	USB2UP_DP	X								X							
95	USB2UP_DM	X								X							
96	USB3UP_TXDP	X								X							
97	USB3UP_TXDM	X								X							
99	USB3UP_RXDP	X								X							
100	USB3UP_RXDM	X								X							

TABLE 282: USB5826 PHYSICAL VS. LOGICAL PORT MAPPING

Device Pin	Pin Name (as in Data Sheet)	LOGICAL PORT NUMBER								PHYSICAL PORT NUMBER							
		0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
6	USB2DN_DP1		X								X						
7	USB2DN_DM1		X								X						
8	USB3DN_TXDP1A		X								X						
9	USB3DN_TXDM1A		X								X						
11	USB3DN_RXDP1A		X								X						
12	USB3DN_RXDM1A		X								X						
13	USB2DN_DP5						X					X					
14	USB2DN_DM5						X					X					
15	USB3DN_TXDP1B		X									X					
16	USB3DN_TXDM1B		X									X					
18	USB3DN_RXDP1B		X									X					
19	USB3DN_RXDM1B		X									X					
28	USB2DN_DP2			X									X				
29	USB2DN_DM2			X									X				
30	USB3DN_TXDP2A			X									X				
31	USB3DN_TXDM2A			X									X				
33	USB3DN_RXDP2A			X									X				
34	USB3DN_RXDM2A			X									X				
35	USB2DN_DP6							X						X			
36	USB2DN_DM6							X						X			
37	USB3DN_TXDP2B			X										X			
38	USB3DN_TXDM2B			X										X			
40	USB3DN_RXDP2B			X										X			
41	USB3DN_RXDM2B			X										X			
43	USB2DN_DP3				X										X		
44	USB2DN_DM3				X										X		
45	USB3DN_TXDP3				X										X		
46	USB3DN_TXDM3				X										X		
48	USB3DN_RXDP3				X										X		
49	USB3DN_RXDM3				X										X		
81	USB3UP_TXDPB	X															X

TABLE 282: USB5826 PHYSICAL VS. LOGICAL PORT MAPPING (CONTINUED)

Device Pin	Pin Name (as in Data Sheet)	LOGICAL PORT NUMBER								PHYSICAL PORT NUMBER							
		0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
82	USB3UP_TXDMB	X															X
84	USB3UP_RXDPB	X															X
85	USB3UP_RXDMB	X															X
86	USB2DN_DP4					X										X	
87	USB2DN_DM4					X										X	
88	USB3DN_TXDP4					X										X	
89	USB3DN_TXDM4					X										X	
91	USB3DN_RXDP4					X										X	
92	USB3DN_RXDM4					X										X	
94	USB2UP_DP	X								X							
95	USB2UP_DM	X								X							
96	USB3UP_TXDP	X								X							
97	USB3UP_TXDM	X								X							
99	USB3UP_RXDP	X								X							
100	USB3UP_RXDM	X								X							

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00002316B (04-30-2020)	Section 2.0, "Configuration Register Map"	Added registers: • 0800h: DEV_REV • 0801h: DEV_ID • 0804h: CLOCK_CTL • 080Ah: UTIL_CONFIG1 • 080Bh: CLOCK_DETECT • 0A10h - 0A20h: PF0_CTL to PF16_CTL • 3101h: USB2_LINK_STATE2 • 3840h: USB3_HUB_CTL • 3841h: USB3_HUB_CTL2 • 3842h: USB3_HUB_CTL3 • 3843h: USB3_VBUS_DEB_PERIOD • 3844h: USB3_HUB_CTL4 • 3849h: USB3_HUB_CTL5 • 3851h: USB30_HUB_STAT • 3878h-3879h: PENDING_HP_MAX_VALUE • 387Ah: PM_ENTRY_AND_U1_RESIDENCY_-TIME • 387Bh-387Ch: U1_LFPS_EXIT • 387Dh-387Eh: PM_LC_TIME_IN_US • 3C48h: USB3_PORT_SPLIT_EN • 411Eh USB2_DEFAULT_PIDM • 411Fh USB2_DEFAULT_PIDL • 4120h USB3_DEFAULT_PIDM • 4121h USB3_DEFAULT_PIDL • 4134h RUNTIME_FLAGS • 4135h BC_VBUS_DIS_TIME • 416Ah PRTPWR1_USB3_SPLIT • 416Bh PRTPWR2_USB3_SPLIT • 416Ch PRTPWR3_USB3_SPLIT • 416Bh PRTPWR4_USB3_SPLIT • 416Fh PRTPWR6_USB3_SPLIT • 4170h PRTPWR7_USB3_SPLIT • 4175h BC_CDP_2_SDP_VBUS_DIS • 42D0h UDC_BCD_USB_LSB • 42D1h UDC_BCD_USB_MSB • 42D6h UDC_VID_MSB • 42D7h UDC_VID_MSB • 42D8h UDC_PID_MSB • 42D9h UDC_PID_MSB • 42DAh UDC_DID_MSB • 42DBh UDC_DID_MSB • 44A4h: USB3_HUB_CHAR2 • 44A5h: USB3_BPWRON2PWRGOOD

TABLE A-1: REVISION HISTORY (CONTINUED)

Revision Level & Date	Section/Figure/Entry	Correction
	Section 2.0, "Configuration Register Map", Table 1	• 6086h: SS_P0_AFE_TEST_IN4 • 60C8h: UP_RISE_FALL_ADJ • 61C0h: SS_P0_LTSSM_STATE • 61C1h: SS_P0_TEST_PIPE_DC • 61C3h: SS_P0_TEST_PIPE_TX_PAT • 61D0h: SS_P0_TEST_PIPE_PIPE_CTL_0 • 6486h: SS_P1_AFE_TEST_IN4 • 64C8h: P1_RISE_FALL_ADJ • 65C0h: SS_P1_LTSSM_STATE • 65C1h: SS_P1_TEST_PIPE_DC • 65C3h: SS_P1_TEST_PIPE_TX_PAT • 65D0h: SS_P1_TEST_PIPE_PIPE_CTL_0 • 6886h: SS_P2_AFE_TEST_IN4 • 68C8h: P2_RISE_FALL_ADJ • 69C0h: SS_P2_LTSSM_STATE • 69C1h: SS_P2_TEST_PIPE_DC • 69C3h: SS_P2_TEST_PIPE_TX_PAT • 69D0h: SS_P2_TEST_PIPE_PIPE_CTL_0 • 6C86h: SS_P3_AFE_TEST_IN4 • 6CC8h: P3_RISE_FALL_ADJ • 6DC1h: SS_P3_TEST_PIPE_DC • 6DC3h: SS_P3_TEST_PIPE_TX_PAT • 6DD0h: SS_P3_TEST_PIPE_PIPE_CTL_0 • 7086h: SS_P4_AFE_TEST_IN4 • 70C8h: P4_RISE_FALL_ADJ • 71C0h: SS_P4_LTSSM_STATE • 71C1h: SS_P4_TEST_PIPE_DC • 71C3h: SS_P4_TEST_PIPE_TX_PAT • 71D0h: SS_P4_TEST_PIPE_PIPE_CTL_0 • 7486h: SS_P5_AFE_TEST_IN4 • 74C8h: P5_RISE_FALL_ADJ • 75C0h: SS_P5_LTSSM_STATE • 75C1h: SS_P5_TEST_PIPE_DC • 75C3h: SS_P5_TEST_PIPE_TX_PAT • 75D0h: SS_P5_TEST_PIPE_PIPE_CTL_0 • 7886h: SS_P6_AFE_TEST_IN4 • 78C8h: P6_RISE_FALL_ADJ • 79C0h: SS_P6_LTSSM_STATE • 79C1h: SS_P6_TEST_PIPE_DC • 79C3h: SS_P6_TEST_PIPE_TX_PAT • 79D0h: SS_P6_TEST_PIPE_PIPE_CTL_0 • 7C86h: SS_P7_AFE_TEST_IN4 • 7DC0h: SS_P7_LTSSM_STATE • 7DC1h: SS_P7_TEST_PIPE_DC • 7DC3h: SS_P7_TEST_PIPE_TX_PAT • 7DD0h: SS_P7_TEST_PIPE_PIPE_CTL_0
	Section 2.0, "Configuration Register Map"	Added default value information to each register table

TABLE A-1: REVISION HISTORY (CONTINUED)

Revision Level & Date	Section/Figure/Entry	Correction
	Section 2.0, "Configuration Register Map"	Added USB2_HS_DISC_TUNE settings to HS_P0_-SENSE through HS_P7_SENSE Registers
	Section 2.0, "Configuration Register Map"	Added more content to HUB_CFG_1 Register (3006h)
	Section 2.0, "Configuration Register Map"	Fixed incorrect description in OCS_INACTIVE_TIMER (30EBh) Register
	Section 2.0, "Configuration Register Map"	Updated USB3_PRT_CFG_SEL1 (3C00h) - USB3_PRT_CFG_SEL7 (3C18h)
	Section 4.0, "Configuration via OTP"	Replaced Section 4.3, "OTP Configuration Commands" to improve clarity Added Section 4.7, "OTP Configuration via USB"
	Section 6.0, "Configuration via USB Command to Internal Hub Feature Controller Device"	Changed name of section for clarity
	Section 7.0, "Configuration via VSM USB Command to Hub Controller"	New Section
	Section 8.0, "String Descrip-tors"	New Section
	Section 9.0, "Hub Product IDs"	New Section
	Section 10.0, "Billboard Device Descriptor"	New Section
	Section 11.0, "Physical and Logical Port Mapping"	New Section
	Entire document	Made textual edits and formatting changes through-out document.
DS00002316A (12-07-16)	Initial release.	

NOTES:

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