VSC7513/14

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip VSC7513/14. These checklist items should be followed when utilizing the VSC7513/14 in a new design. A summary of these items is provided in Section 13.0, "Hardware Checklist Summary," on page 19. Detailed information on these subjects can be found in the corresponding section:

- Section 2.0, "General Considerations"
- Section 3.0, "Power"
- Section 4.0, "Reference Clock"
- Section 5.0, "CPU System"
- Section 6.0, "Port Configurations"
- Section 7.0, "Internal Copper PHY Ports"
- Section 8.0, "SerDes Interfaces"
- Section 9.0, "Serial GPIO Controller"
- Section 10.0, "Other Interfaces"
- Section 11.0, "System Reset"
- Section 12.0, "SyncE and PTP"

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The VSC7513/14 implementor should have the following documents on hand:

- *VSC7513 Data Sheet*
- *VSC7514 Data Sheet*
- *Microsemi VSC7514EV Ocelot Managed Hardware Manual*

2.2 Pin Check

- Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.
- If the customer plans to use Microchip turnkey software package, Microchip recommends to use one of its reference design schematics as a basis and retain the reference design's use of GPIO (parallel as well as serial) whenever possible to minimize software changes. Keep a log of the major changes (for example, port numbering, PHY addresses, GPIO, and SGPIO) and provide this log when there is design review or when starting software customization.

2.3 Strapping Pins

Some of the GPIO pins used are strapping pins at power-up for configuring PLL reference clock frequency and for selecting CPU start-up modes. See Figure 2-1 and Table 2-1 for the description of the strapping pins and the corresponding configurations and modes. 1K-4.7K resistors are recommended for pulling the strapping high or low accordingly.

FIGURE 2-1: STRAPPING PINS OVERLAID WITH GPIO PINS

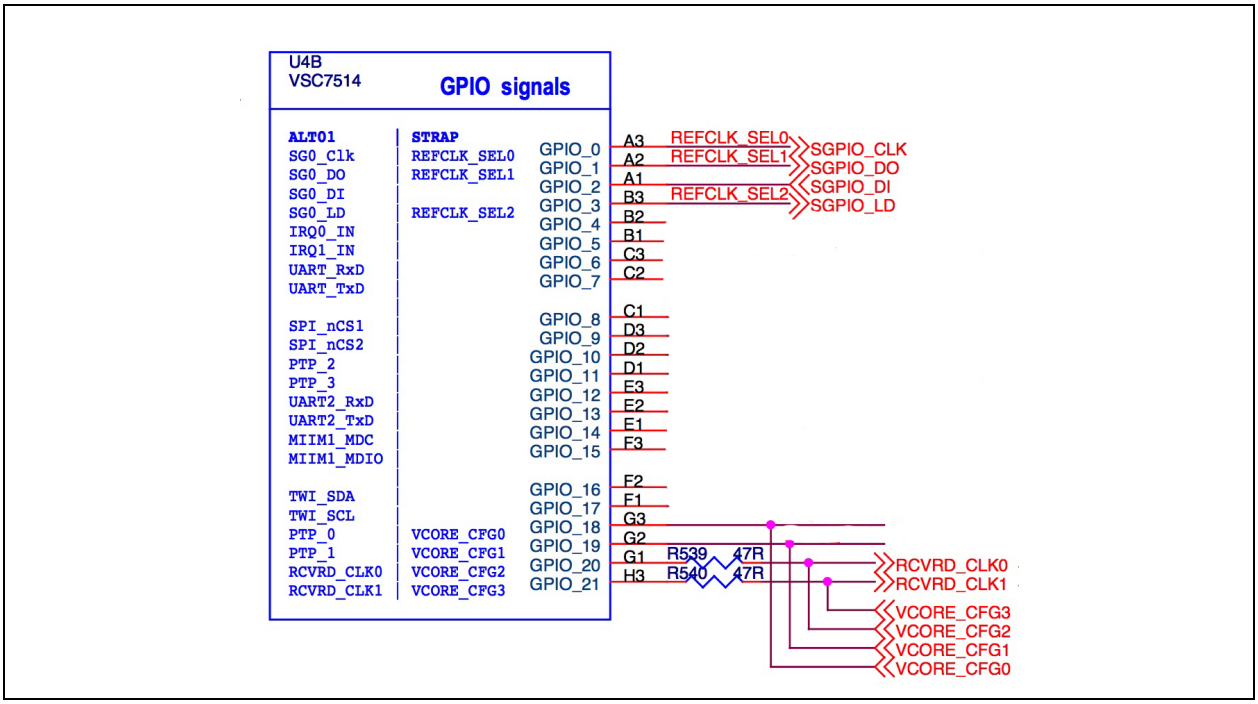


TABLE 2-1: VSC7513/14 STRAPPING PIN DESCRIPTIONS

Pin	Description
REFCLK_CONF[2:0]	Configuration of reference clock frequency for PLL 000: 125 MHz 001: 156.25 MHz 010: 250 MHz 100: 25 MHz Other values are reserved and must not be used.
VCORE_CFG[3:0]	Configuration of VCore system start-up conditions 0000: VCore-III CPU is enabled (Little Endian mode) and boots from SI (the slave is disabled). 1001: PCIe 1.x endpoint is enabled. Automatic boot of VCore-III CPU is disabled, and SI slave is enabled. 1010: MIIM slave is enabled with MIIM address 0 (MIIM slave points are overlaid on GPIOs). Automatic boot of VCore-III CPU is disabled, and SI slave is enabled. 1011: MIIM slave is enabled with MIIM address 31 (MIIM slave pins are overlaid on GPIOs). Automatic boot of VCore-III CPU is disabled, and SI slave is enabled. 1100: VCore-III CPU is enabled (Big Endian mode) and boots from SI (the SI slave is disabled). 1111: Automatic boot of VCore-III CPU is disabled, and SI slave is enabled. Other values are reserved and must not be used.

2.4 Ground

- Create at least one unbroken ground plane (GND).
- **GND** is also the main path for removing heat from the VSC7513/14. It is therefore important that there are enough vias under the VSC7513/14 connecting it to the ground and that those vias are evenly distributed.

3.0 POWER

3.1 Power Supply

- VSC7513/14 requires power at:
  - 2.5V for I/O circuits on **VDD_IO** pins.
  - 2.5V for internal copper PHY analog circuits on **VDD_AH** pins.
  - 1.0V for internal copper PHY analog circuits on **VDD_AL** pins.
  - 1.0V for internal core on **VDD** pins.
  - 1.0V for internal analog circuits on **VDD_A** pins.
  - 1.0V or 1.2V for all the Serializer/Deserializer (SerDes) interfaces on **VDD_VS** pins.
  - 1.35V or 1.5V supply for the double data rate (DDR) interface on **VDD_IODDR** pins. (Note that 1.5V DDR supply should be used when covering I-temp applications.)
- Each power supply voltage should have both bulk and high-frequency decoupling capacitors. Recommended bulk decoupling capacitors are 10 µF, but 47 µF should be used for VDD_A due to initial load during power-up. High-frequency decoupling capacitors that are 0.1 µF are also recommended. Surface mount decoupling capacitors should be placed as close to the power supply pins as possible.
- Analog supplies must be isolated from the remaining board supplies using ferrite beads.

3.2 Power Supply Sequencing

- During power-on and power-off, **VDD_A** and **VDD_VS** must never be more than 300 mV above **VDD**.
- **VDD_VS** must be powered even if the associated interfaces are not used. These power supplies must not remain at ground or left floating.
- A maximum delay of 100 ms from **VDD_IODDR** to **VDD** is recommended. There is no requirement from **VDD** to **VDD_IODDR**.

4.0 REFERENCE CLOCK

The device reference clock can be a 25 MHz, 125 MHz, 156.25 MHz, or 250 MHz clock signal. The frequency is selected through REFCLK_CONF[2:0] described in Table 2-1.

The reference clock can be either a differential reference clock or a single-ended clock. Note of the device data sheet's requirements for maximum clock jitter, which must be accounted for in board design when selecting clock source (oscillator) and clock distribution (buffer) components.

4.1 Differential Clock

When the differential clock is used, the input is best compatible with low voltage differential signaling (LVDS) signal. Each P/N pin of the clock input has an internal 50R termination to 0.7V that results in a 100R differential termination from P to N, inherently biased to 2/3 VDD. AC coupling is recommended to meet the reference clock input specification on common-mode voltage using the internal termination as biasing.

The data sheet prescribes an upper voltage limit on the P/N signals of 1200 mV. This is due to the ESD clamp diodes on the inputs. Because of the termination or biasing to 2/3 VDD (typically the common-mode voltage), this imposes a limit on the single-ended swing for P or N of 2*(1200 mV-700 mV) = 1000 mV. Some low voltage positive emitter-couple logic (LVPECL) might have a larger differential swing than 400 mV, so it should be attenuated using resistor dividers to meet the input specification for voltage swing.

To meet the QSGMII requirements, a differential reference clock of minimum 125 MHz is recommended.

4.2 Single-Ended REFCLK Input

Although the VSC7514 reference clock input is differential, it is also possible to use a single-ended clock source. This can be done by setting one differential input to a common-mode voltage and shaping the single-ended signal driving the other differential input, so that it toggles around this common-mode voltage with a voltage swing comparable to LVDS. The reference clock differential input buffer sees this as a valid differential signal. An external resistor network is required to do so. The resistor network limits the amplitude and adjusts the center of the swing. Figure 4-1 and Figure 4-2 show the resistor network and the recommended values for the resistors for 3.3V and 2.5V CMOS single-ended clock signals.

FIGURE 4-1: RESISTOR NETWORK FOR 3.3V CMOS SINGLE-ENDED CLOCK

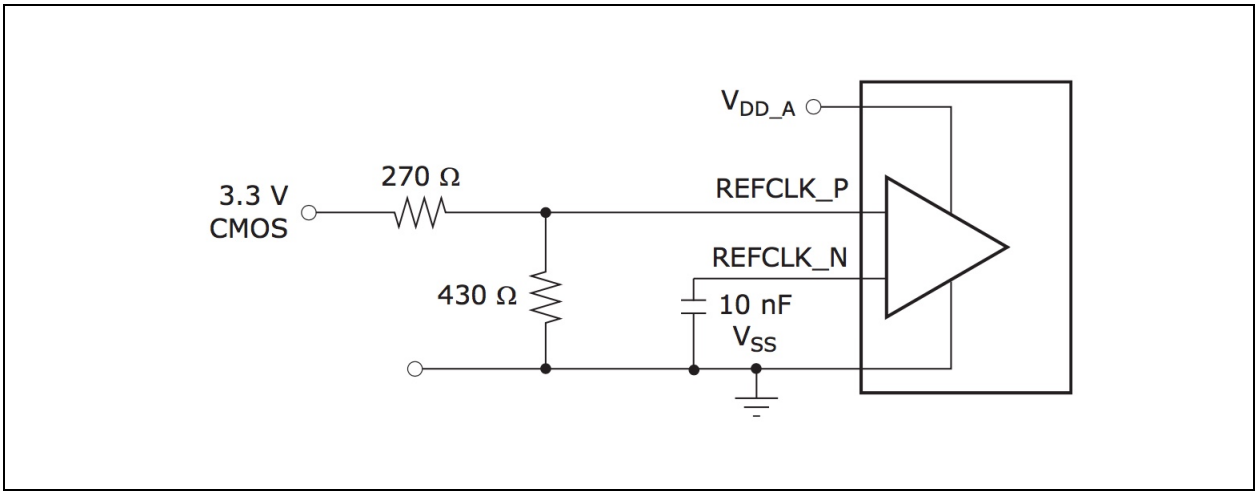
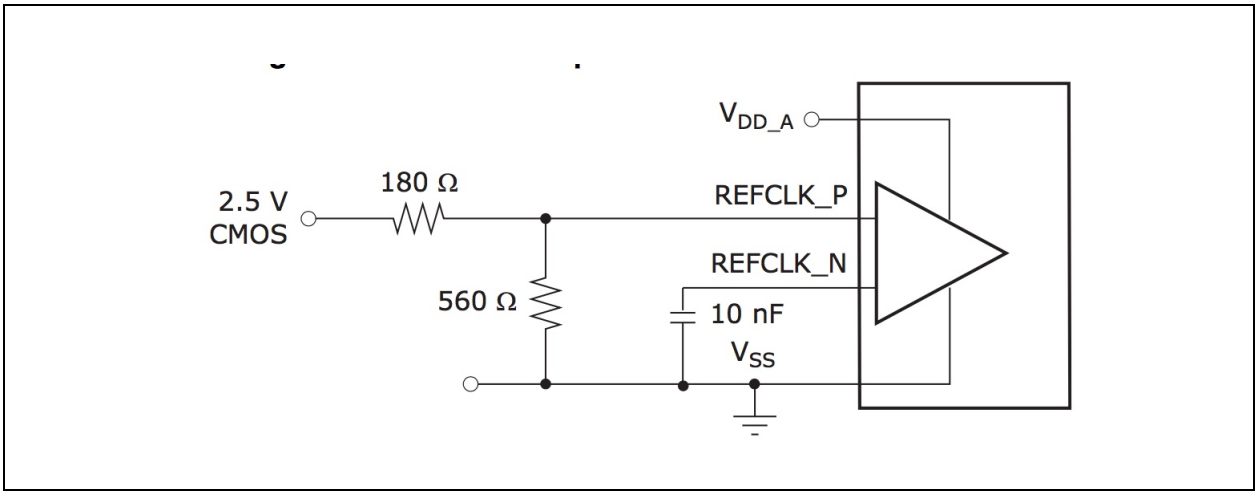


FIGURE 4-2: RESISTOR NETWORK FOR 2.5V SINGLE-ENDED CLOCK



5.0 CPU SYSTEM

VSC7513/14 can be managed by either the internal VCore-III MIPS CPU or an external CPU. The selection between internal or external CPU is based on VCORE_CFG[3:0] strapping pins described in **Section 2.3 "Strapping Pins"**.

5.1 Internal CPU Mode

The internal CPU is enabled and boots from the SPI Flash when VCore-CFG[3:0] strapping is configured to be 0000 or 1100. The internal VCore-III CPU system is based on a powerful MIPS24KEc-compatible microprocessor with 16-entry MMU, 32 KB instruction, and 32 KB data caches. The VCore-III CPU system includes an SPI boot controller and a DDR3 Memory controller. When automatic booting is enabled through the strapping pins, the VCore-III CPU automatically starts to execute the code from the SPI Flash at byte address 0. Below is the typical automatic boot sequence:

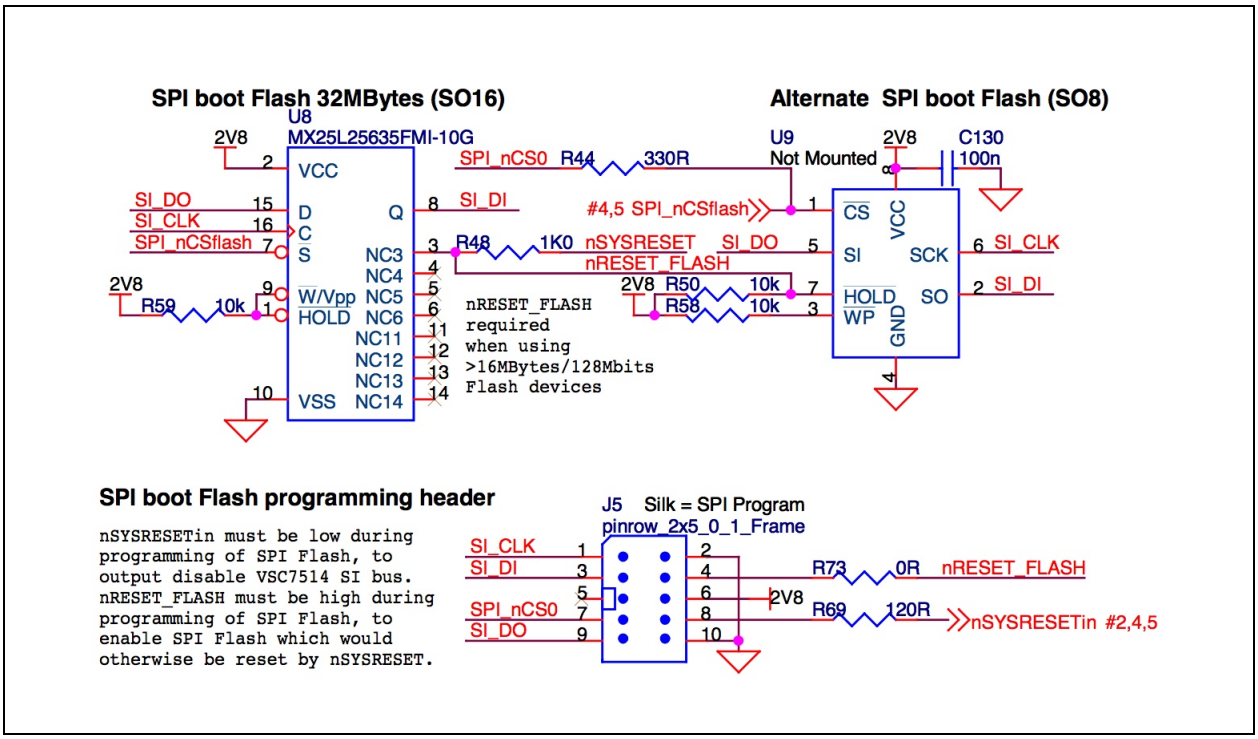
1. Speed up the SPI boot interface and execute the code in the Flash memory.
2. Initialize the DDR3/DDR3L controller.
3. Copy the code-image from the Flash to the DDR3/DDR3L memory.
4. Change the memory map from Boot mode to Normal mode and execute the code in the DDR3 memory.

SPI Flash and DDR3 are always required when internal CPU mode is enabled.

5.1.1 FLASH MEMORY

The switch supports four SPI chip-select pins. Both Nor Flash or NAND Flash can be supported on any of the four chip-select pins, but the boot controller only supports Nor Flash on SI_nCS0. By default, the SPI boot controller operates in 24-bit address mode. In that mode, 16 MB Flash memory can be addressed. Most Flash memories use an extended address register (EAR) to select a 16 MB page inside the Flash to support a Flash size larger than 16 MB, which is generally recommended for VSC7513/14 managed solution. To make sure page 0 is always selected by EAR after power-up (hardware reset button), connecting the board reset signal (nSYSREST) to the reset input of the Flash is recommended as shown in Figure 5-1.

FIGURE 5-1: SPI BOOT FLASH AND PROGRAMMING HEADER



A Flash programming header in Microchip reference design is available to support on-PCB Flash programming. Pin 8 of the Flash programmer header is nSYSRESETin in Figure 5-1. It is an input to the reset generator. The purpose of this signal is to make nSYSRESET output low during Flash programming so that VSC7513/14 is held in reset and does not drive the SPI signals. Otherwise, both VSC7514 and the Flash programmer drive the SPI signals that cause Flash programming failure.

The boot controller on SI_nCS0 only support Nor Flash, but after the CPU boots up, the software is going to run in the DDR memory, and it is possible to enable less expensive SPI NAND Flash on SI_nCS1-SI_nCS3.

SPI_nCSx and SPI_CLK signals are recommended to be pulled up, so the two signals will be high when the switch is not driving them.

Note: VSC7513/14 is 2.5V I/O device and the output high voltage (Voh) from the switch can be as low as 1.7V at worst cases. This might not meet the Vih requirement of a SPI Flash with 3.3V power supply. It is recommended to use a Flash with lower power supply voltage, or to put a buffer with voltage translation on the SPI bus between VSC7513/14 and the Flash memories.

5.1.2 DDR3

A DDR3 memory is required when the internal CPU is enabled to manage the switch. At least 128 MB, 16-bit DDR3 or DDR3L memory is recommended.

It is recommended to use a shared voltage reference between the reference voltage of the device and the DDR3 memory. Generate the DDR_Vref from the VDD-ioddr supply using a resistor divider with value of 1 KΩ and accuracy of 1% or better. Use a decoupling capacitance of at least 0.1 µF on the supply in a manner similar to VDD_IODDR and VSS to ensure tracking of supply variations; however, the time constant of the resistor divider and decoupling capacitance should not exceed the nRESET assertion time after power on. VDD-ioddr pins must not share vias. Use at least one via for each VDD_ioddr pin. The extra inductance from sharing vias may cause bit errors in the DDR interface.

It is recommended to connect one of the GPIO pins (GPIO_19 is used in the reference design) to the reset input of the DDR3 memory so that the DDR3 memory can be software reset. Note of the I/O voltage difference between the switch (2.5V) and the DDR3 (1.5V or 1.35V) so a resistor network is required to divide the voltage. (Note that 1.5V should be used in I-temp applications.)

5.1.2.1 Routing Recommendations

Because reflections are absorbed by the devices, keep the physical distance of all the SDRAM interface signals as low as possible. Omit external discrete termination on the address, command, control, and clock lines.

- DDR_CK/DDR_CKn must be routed as a differential pair with a 100Ω differential characteristic impedance.
- DDR_xDQS/DDR_xDQSn must be routed as a differential pair with a 100Ω differential characteristic impedance.
- To minimize crosstalk, the characteristic impedance of the single-ended signals should be determined predominantly by the distance to the reference plane and not the distance to the neighboring traces.
- The crosstalk should be below –20 dB.
- When routing the DDR interface, attention must be paid to the skew lists in table *"Recommended Skew Budget"* of *VSC7513/14 Data Sheet*.

When the switch is managed by an external CPU, the DDR3 memory is not needed. The VDD_IODDR supply can remain at ground or left floating in that case. If VDD_IODDR is grounded, DDR_Vref must also be grounded.

5.2 External CPU Mode

Some of the VCORE_CFG strapping options (see Table 2-1) disable the internal CPU and allow an external CPU to control the switch through either the SPI slave interface, the MIIM slave interface, or the PCIe interface.

5.2.1 SPI SLAVE INTERFACE

The SPI slave interface shares the same pins as the SPI boot controller interface. Among the chip selection signals, only SI_nCS0 supports Slave mode.

When the external CPU uses the SPI slave interface to read switch registers, VSC7513/14 needs to prepare read data after receiving the last address bit. The access time of the register that is read must be satisfied before shifting out the first bit of read data, so there must be a delay between the last address bit and the first data bit. The following are some ways to satisfy the needed delay:

- Use SI_CLK with a period of minimum twice the access time for the register target. For example, for normal switch core targets (single master): 1/(2 × 1 µs) = 500 kHz (maximum).

- Pause the SI_CLK between shifting of serial address bit 0 and the first data bit with enough time to satisfy the access time for the register target.
- Configure the device to send out padding bytes before transmitting the read data to satisfy the access time for the register target. For example, 1 dummy byte allows enough read time for the SI clock to run up to 6 MHz in a single master system.

5.2.2 MIIM SLAVE INTERFACE

The MIIM slave pins on the device are overlaid functions on the GPIO interface. MIIM Slave mode is enabled by configuring the appropriate VCore_CFG strapping pins. The MIIM slave can be configured to answer one of two different PHY addresses using ICPU_CFG::GENERAL_CTRL.IF_MIIM_SLV_ADDR_SEL or the VCore_CFG strapping pins (see Table 2-1).

MIIM_SLV_MDIO is recommended to be pulled high through the 1.5K resistor.

Note: The bandwidth of the MIIM slave interface is much lower than the SPI and PCIe interfaces because all accesses go through two address registers and two data registers in order to make conversion between MIIM using 16-bit wide access and switch core register interface of 32 bits wide.

5.2.3 PCIE INTERFACE

The PCIe interface can also be used for an external CPU to read/write switch registers and to send/receive Ethernet frames to/from the switch. AC coupling is recommended on the PCIe link between the switch and the external CPU.

To ensure correct operation of the clock PLL, a PLL restart might be needed after the switch is powered up, and PLL restart must occur without using the PCIe interface because the restart disconnects the PCIe interface. So it is recommended to have either the SPI slave or the MIIM slave interface between the switch and the external CPU when the PCIe interface is used. The SPI slave or the MIIM slave interface can be used by the external CPU to restart the PLL when needed. Refer to *AN1272 - Using the PCIe Endpoint Controller* for more detail.

6.0 PORT CONFIGURATIONS

6.1 VSC7514 Port Configuration

VSC7514 has up to four internal copper PHY ports and nine SerDes (six 1G SerDes and three 6G SerDes) interfaces. Not all of those copper PHY and SerDes interfaces can be enabled to work as an independent switch port at the same time. Internally, VSC7514 is an 11-port switch. The copper PHY and SerDes interfaces are mapped to the 11 switch ports and a PCIe interface through the port MUX. The configuration of the port MUX is done through the MACRO_CTRL::HW_CFG register. Table 6-1 lists the definition of that register.

TABLE 6-1: REGISTER DESCRIPTION OF HW_CFG FOR VSC7514

Bit	Name	Access	Description	Default
6	DEV2G5_10_MODE	R/W	Configure mode of device DEV2G5_10. This can be connected to SerDes1G_5 or SerDes6G_2. Setting PCIE_ENA prevents DEV2G5_10 to be connected to SerDes6G_2. 0: DEV2G5_10 is connected to SerDes6G_2. 1: DEV2G5_10 is connected to SerDes1G_5.	0x0
5	DEV1G_9_MODE	R/W	Configure mode of device DEV1G_9. This can be connected to SerDes1G_4 or be disconnected. 0: DEV1G_9 is disconnected. 1: DEV1G_9 is connected to SerDes1G_4.	0x0
4	DEV1G_6_MODE	R/W	Configure mode of device DEV1G_6. This can be connected to SerDes1G_3 or SerDes6G_0 when QSGMII mode is enabled. Setting HW_CFG.QSGMII_ENA forces QSGMII mode, and ignores the DEV1G_6_MODE setting. 0: DEV1G_6 is disconnected. 1: DEV1G_6 is connected to SerDes1G_3.	0x0
3	DEV1G_5_MODE	R/W	Configure mode of device DEV1G_5. This can be connected to SerDes1G_5, SerDes1G_1, or SerDes6G_0 when QSGMII mode is enabled. Setting HW_CFG.QSGMII_ENA forces QSGMII mode, and ignores the DEV1G_5_MODE setting. 0: DEV1G_5 is connected to SerDes1G_5. 1: DEV1G_5 is connected to SerDes1G_1.	0x0
2	DEV1G_4_MODE	R/W	Configure mode of device DEV1G_4. This can be connected to SerDes1G_4, SerDes1G_2, or SerDes6G_0 when QSGMII mode is enabled. Setting HW_CFG.QSGMII_ENA forces QSGMII mode, and ignores the DEV1G_4_MODE setting. 0: DEV1G_4 is connected to SerDes1G_4. 1: DEV1G_4 is connected to SerDes1G_2.	0x0
1	PCIE_ENA	R/W	Set to enable PCIe mode for SerDes6G_2. 0: Disable PCIE 1: Enable PCIE	0x0
0	QSGMII_ENA	R/W	Set bit 0 to enable QSGMII mode for devices DEV1G_4, DEV1G_5, DEV1G_6, and DEV1G_7 via SerDes6G_0. 0: Disable QSGMII 1: Enable QSGMII	0x0

Some of the typical configurations of the switch are shown in the table below.

TABLE 6-2: VSC7514 TYPICAL PORT CONFIGURATION

SerDes/CuPHY No SerDes Type			0 Cu	1 Cu	2 Cu	3 Cu	0 1G	1 1G	2 1G	3 1G	4 1G	5 1G	6 6G	7 6G	8 6G	Max BW Incl NPI
Configuration	**VSC7514**	**D0-D10**														
2	8 + NPI	4 x dual + 2 x 1G SGMII + 2 x 2.5G SGMII + 2.5G NPI	D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D7	D8	D10	13.5
b	8 + PCIe	4 x dual + 2 x 1G SGMII + 2 x 2.5G SGMII + PCIe	D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D7	D8	PCIe	11
0	10 + NPI	4 x dual + 1 x 1G SGMII + 1 x QSGMII + 1 x 2.5G SGMII + 2.5G NPI	D0	D1	D2	D3	D0	D1	D2	D3	D9		Q0	D8	D10	14
c	11 + PCIe	4 x dual + 2 x 1G SGMII + 1 x QSGMII + 1 x 2.5G SGMII + PCIe	D0	D1	D2	D3	D0	D1	D2	D3	D9	D10	Q0	D8	PCIe	12.5
d	11 + PCIe	1 x dual + 3 x CUPHY + 5 x 1G SGMII + 2 x 2.5G SGMII + PCIe	D0	D1	D2	D3	D0	D5	D4	D6	D9	D10	D7	D8	PCIe	14
e	10 + NPI	2 x dual + 2 x CUPHY + 4 x 1G SGMII + 2 x 2.5G SGMII + 2.5G NPI	D0	D1	D2	D3	D0	D1	D4	D6	D9	D5	D7	D8	D10	15.5

- Config 2 in Table 6-2 represents a 4-combo + 5-SerDes switch. This is the default configuration (HW_CFG = 0x0) of the switch, where:
  - the QSGMII and the PCIe are disabled.
  - the first four switch ports connect to both an internal copper PHY (Cu0-Cu3) and a SerDes interface (S0-S3). Examples are Cu0 and S0.
  - Cu0 and S0 map to D0 (switch port 0) and only one of the media can work at the same time. This is called a combo port.
  - SerDes S4-S8 map to switch ports D4, D5, D7, D8, and D10.
- Config b is enabled by setting only HW_CFG = 0x2 to enable PCIe. When the PCIe is enabled, it overrules bit 6 of HW_CFG. The PCIe interface can only be enabled on SerDes s8.
- Config 0 is a 4-combo + 3-SerDes + 1-QSGMII switch. This configuration is enabled by enabling the QSGMII interface (HW_CFG = 0x21). The QSGMII interface can only be enabled on s6. When the QSGMII is enabled, it is always mapped to switch ports D4, D5, D6, and D7, and bit 2, 3, and 4 of HW_CFG are overruled by the QSGMII interface. It is recommended to enable TX for all four ports in the QSGMII even when not all of them are actually connected to the external PHY for timing consideration.
- Config c is enabled by setting HW_CFG to 0x63.
- Config d is a 1-combo + 3-Cu + 7-SerDes + 1* PCIe switch. It is enabled by setting HW_CFG to 0x7e.
- Config e is a 2-combo + 2-Cu + 7-SerDes switch. It is enabled by setting HW_CFG to 0x74.

6.2 VSC7513 Port Configuration

VSC7513 has up to four internal copper PHY ports and 8 SerDes (6*1G SerDes and 2*6G SerDes) interfaces. S6 can only be used as QSGMII interface; S7 is only available on VSC7514. Not all of the copper PHY and SerDes interfaces can be enabled to work as an independent switch port at the same time. Internally, VSC7513 is a 9-port switch. The copper PHY and SerDes interfaces are mapped to the nine switch ports and a PCIe interface through the port MUX. The configuration of the port MUX is done through register MACRO_CTRL::HW_CFG. Table 6-3 shows the definition of that register.

TABLE 6-3: REGISTER DESCRIPTION OF HW_CFG FOR VSC7513

Bit	Name	Access	Description	Default
6	DEV2G5_10_MODE	R/W	Configure mode of device DEV2G5_10. This can be connected to SerDes1G_5 or SerDes6G_2. Setting PCIE_ENA prevents DEV2G5_10 to be connected to SerDes6G_2. 0: DEV2G5_10 is connected to SerDes6G_2. 1: DEV2G5_10 is connected to SerDes1G_5.	0x0
5	RESERVED	R/W	Configure mode of device set to its default	0x0
4	DEV1G_6_MODE	R/W	Configure mode of device DEV1G_6. This can be connected to SerDes1G_3 or SerDes6G_0 when QSGMII mode is enabled. Setting HW_CFG.QSGMII_ENA forces QSGMII mode and ignores the DEV1G_6_MODE setting. 0: DEV1G_6 is disconnected. 1: DEV1G_6 is connected to SerDes1G_3.	0x0
3	DEV1G_5_MODE	R/W	Configure mode of device DEV1G_5. This can be connected to SerDes1G_5, SerDes1G_1, or SerDes6G_0 when QSGMII mode is enabled. Setting HW_CFG.QSGMII_ENA forces QSGMII mode and ignores the DEV1G_5_MODE setting. 0: DEV1G_5 is connected to SerDes1G_5. 1: DEV1G_5 is connected to SerDes1G_1.	0x0
2	DEV1G_4_MODE	R/W	Configure mode of device DEV1G_4. This can be connected to SerDes1G_4, SerDes1G_2, or SerDes6G_0 when QSGMII mode is enabled. Setting HW_CFG.QSGMII_ENA forces QSGMII mode and ignores the DEV1G_4_MODE setting. 0: DEV1G_4 is connected to SerDes1G_4. 1: DEV1G_4 is connected to SerDes1G_2.	0x0
1	PCIE_ENA	R/W	Set to enable PCIe mode for SerDes6G_2. 0: Disable PCIE 1: Enable PCIE	0x0
0	QSGMII_ENA	R/W	Set bit 0 to enable QSGMII mode for devices DEV1G_4, DEV1G_5, DEV1G_6, and DEV1G_7 via SerDes6G_0. 0: Disable QSGMII 1: Enable QSGMII	0x0

Some of the typical configurations of the switch are shown in Table 6-4.

TABLE 6-4: VSC7513 TYPICAL PORT CONFIGURATION

SerDes/CuPHY No SerDes Type			0 Cu	1 Cu	2 Cu	3 Cu	0 1G	1 1G	2 1G	3 1G	4 1G	5 1G	6 6G	7 6G	8 6G	Max BW Incl NPI
Configuration	**VSC7513**	**D0-D10**														
2	6 + NPI	4 x dual + 2 x 1G SGMII + 2.5G SGMII + 2.5G NPI	D0	D1	D2	D3	D0	D1	D2	D3	D4	D5			D10	8.5
b	6 + PCIe	4 x dual + 2 x 1G SGMII + PCIe + PCIe	D0	D1	D2	D3	D0	D1	D2	D3	D4	D5			PCIe	6
0	8 + NPI	4 x dual + 1 x QSGMII + 2.5G NPI	D0	D1	D2	D3	D0	D1	D2	D3			Q0		D10	10.5
c	9 + PCIe	4 x dual + 1G SGMII + 1 x QSGMII + PCIe	D0	D1	D2	D3	D0	D1	D2	D3		D10	Q0		PCIe	9
d	8 + PCIe	1 x dual + 3 x CUPHY + 4 x 1G SGMII + PCIe	D0	D1	D2	D3	D0	D5	D4	D6		D10			PCIe	8
e	7 + NPI	2 x dual + 2 x CUPHY + 3 x 1G SGMII + 2.5G NPI	D0	D1	D2	D3	D0	D1	D4	D6		D5			D10	9.5

- Config 2 in Table 6-4 represents a 4-combo + 3-SerDes switch. This is the default configuration (HW_CFG = 0x0) of the switch, where:
  - the QSGMII and the PCIe are disabled.
  - the first four switch ports connect to both an internal copper PHY (Cu0-Cu3) and a SerDes interface (S0-S3). Examples are Cu0 and S0.
  - Cu0 and S0 map to D0 (switch port 0) and only one of the media can work at the same time. This is called a combo port.
  - SerDes S4, S5, and S8 map to switch ports D4, D5, and D10.
- Config b is enabled by setting only HW_CFG = 0x2 to enable PCIe. When the PCIe is enabled, it overrules bit 6 of HW_CFG. The PCIe interface can only be enabled on SerDes s8.
- Config 0 is a 4-combo + 1-SerDes + 1-QSGMII switch. This configuration is enabled by enabling the QSGMII interface (HW_CFG = 0x1). The QSGMII interface can only be enabled on s6. When the QSGMII is enabled, it is always mapped to switch ports D4, D5, D6, and D7 and bit 2, 3, and 4 of HW_CFG are overruled by the QSGMII interface. It is recommended to enable TX for all four ports in the QSGMII even when not all of them are actually connected to the external PHY for timing consideration.
- Config c is enabled by setting HW_CFG to 0x43.
- Config d is a 1-combo + 3-Cu + 4-SerDes + 1-PCIe switch. It is enabled by setting HW_CFG to 0x5e.
- Config e is a 2-combo + 2-Cu + 4-SerDes switch. It is enabled by setting HW_CFG to 0x54.

7.0 INTERNAL COPPER PHY PORTS

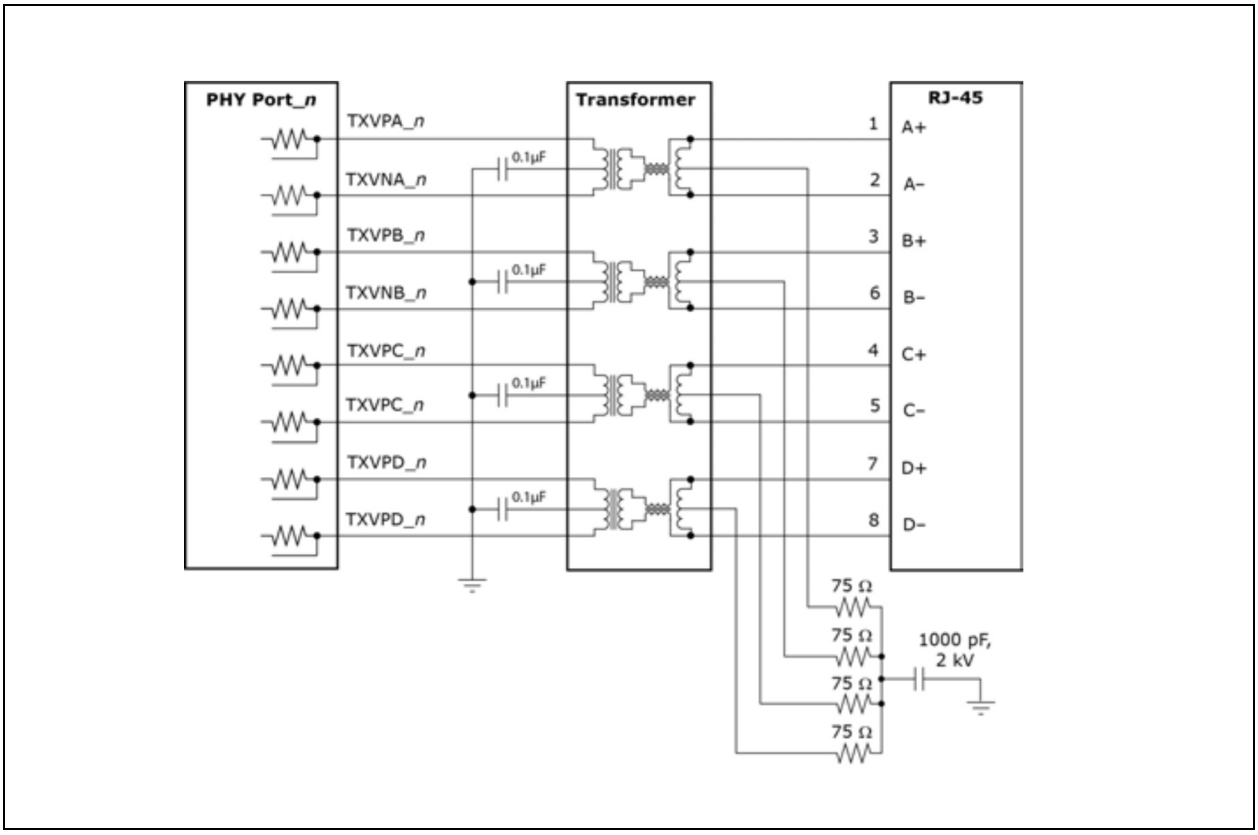
Four internal copper Gigabit (GbE) PHYs are available in VSC7513/14. More external PHY can be supported on the QSGMII interface or SGMII interfaces.

7.1 Copper PHY MDI Interface

Figure 7-1 shows the recommended connection from the internal copper PHY to the transformer. The internal copper PHY uses voltage mode line drive technology so no center tap voltage is required at the transformer. Each of the four center taps are recommended to be connected to GND through a separate 0.1 µF capacitor because the common-mode voltage on each pair might be different. The PHY has integrated termination resistors so no external terminations are needed.

Note: The PHY has integrated termination resistors so no external terminations are needed. It is recommended to use minimum 8-core magnetics with common mode choke (CMC) at the RJ45/cable side.

FIGURE 7-1: TRANSFORMER CONNECTIONS FOR INTERNAL COPPER PHY PORTS



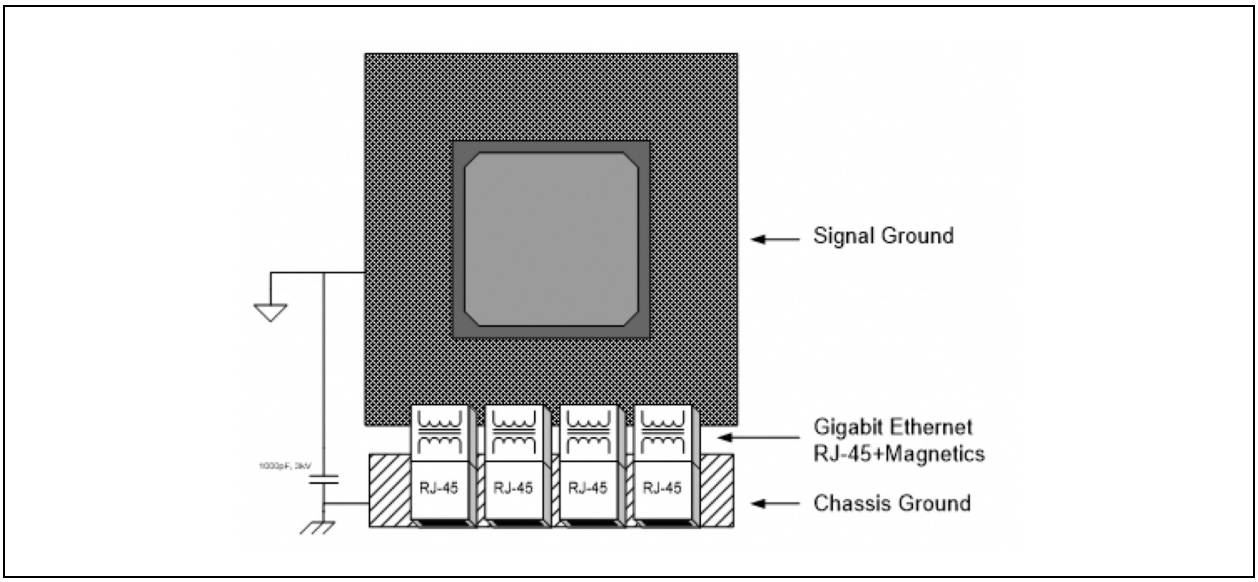
The MDI interface is organized into four differential pairs (A, B, C, and D) for each PHY port. Pairs C and D are only used in Gigabit speed. When routing these pairs on a PCB, the characteristics must match one of the following:

- Route each single-ended trace with a characteristic impedance of 50Ω referenced to ground.
- Route each positive and negative trace on each port as differential pairs with 100Ω characteristic differential impedance.

7.2 Chassis Ground

To isolate the board from ESD events and to prevent a common-mode noise ground path, a separate chassis ground region should be allocated. This separate chassis ground, as shown in Figure 7-2, should be electrically connected to the external chassis and to the shield ground of the RJ-45 connectors.

FIGURE 7-2: RECOMMENDED SEPARATE CHASSIS GROUND



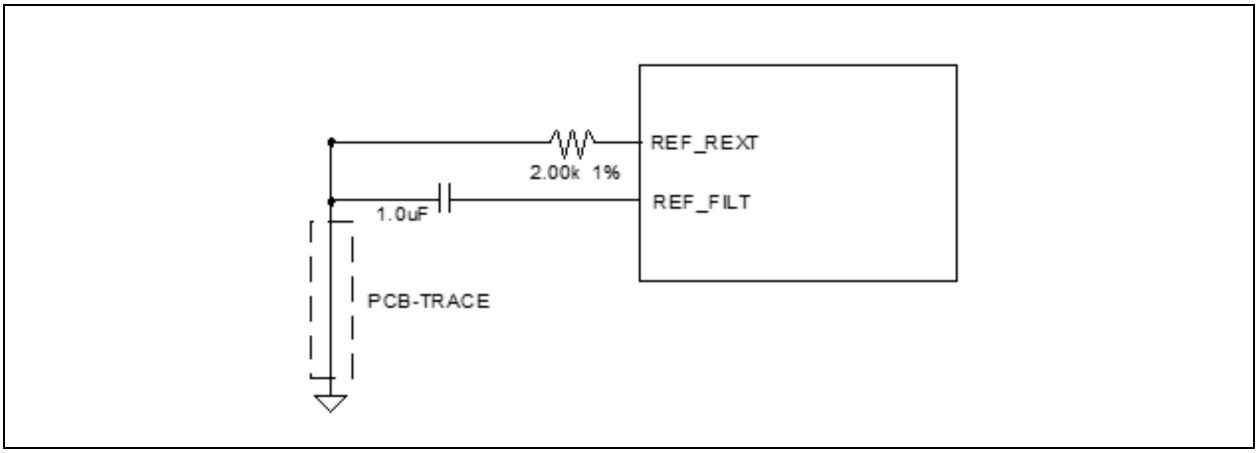
7.3 Voltage Reference Pins

For proper operation of the internal copper PHY, the switch must generate an on-chip band gap reference voltage at the REF_FILT pin. To generate that reference voltage, the following components are required for each VSC7513/14 in the system.

- 2.0 kΩ reference resistor, 1% tolerance, minimum 1/16 W connected to REF_REXT pin
- 1 µF capacitor, 10% tolerance or better connected to REF_FILT pin

For best performance, special consideration of the ground connection of the voltage reference circuit is necessary to prevent bus drops that would cause reference voltage inaccuracy. The ground connections of the resistor and the capacitor should each be connected to a shared PCB signal trace (rather than being connected individually to a common ground plane), as shown in Figure 7-3. This PCB signal trace should then be connected to a ground plane at a single point. In addition, the reference capacitor and resistor should be placed as close as possible to VSC7513/14.

FIGURE 7-3: VOLTAGE REFERENCE CIRCUIT



8.0 SERDES INTERFACES

As shown in Table 6-1 and Table 6-2, six 1G SerDes interfaces and three 6G SerDes interfaces are supported by VSC7514, and four 1G SerDes and three 6G SerDes are supported by VSC7513. All of the SerDes interfaces can connect small form-factor pluggable (SFP) modules directly to support 100FX, 1000BX, and 2.5G fiber optical ports. They can also be configured as SGMII to connect to the external PHY. One of the 6G SerDes (S6) can be configured as QSGMII to support QSGMII PHY. The 1G and 6G SerDes can also support MAC-to-MAC and backplane connection.

A bias resistor of 620Ω ±1% between SerDes_Rext_[1:0] is always needed even if none of the above SerDes interfaces are enabled in the design.

8.1 SFP Port

Since there are internal AC-coupling capacitors in the SFP modules, the connection from a VSC7513/14 SerDes to the SFP modules can be DC coupling.

SFP control signals can be supported by the GPIO pins on the switch. RX_LOS signal from the modules should be connected to one of the six SFPx_SD inputs to support hardware-based signal detection for the physical coding sub-layer (PCS) module of those SFP ports. The SFPx_SD inputs pins are overlaid on GPIO pins.

Alternatively, the SFP I/O control signals can all be supported by the serial GPIO controller through the four SGPIO pins (overlaid on GPIO_0-GPIO_3). There are rules to map RX_LOS signals to the SGPIO bits. See **Section 9.0 "Serial GPIO Controller"** on the SGPIO controller.

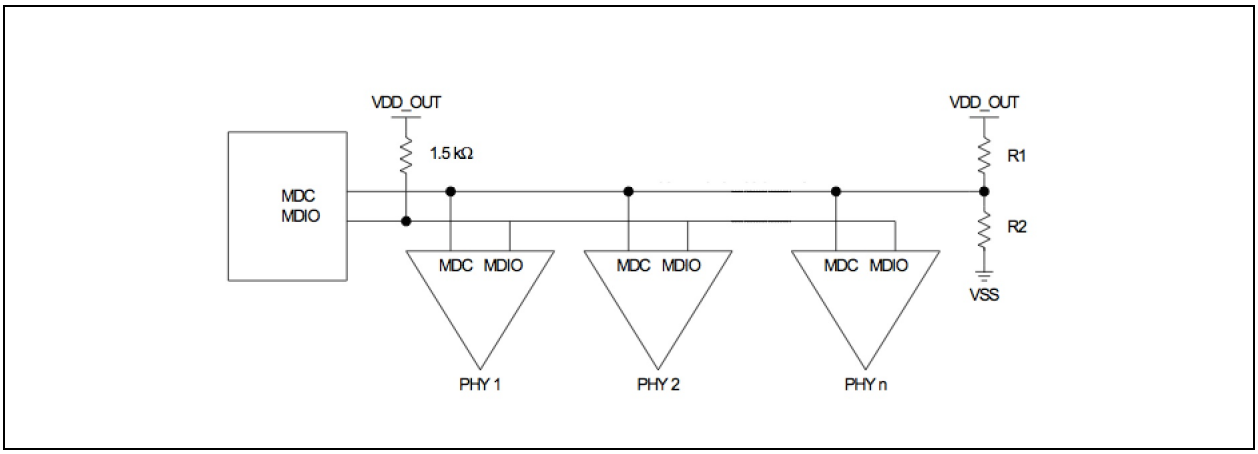
8.2 External PHY

When the SerDes interfaces are used to connect to the external PHY, then AC coupling is recommended between the switch and the external PHY. Take caution in naming the RX and TX pairs on the switch and PHY. Normally, RX is the output pair and TX is the input pair on a PHY. This is different from how they are named on a switch. Make sure that the output pair from the switch is connected to the input pair of the PHY and vice versa.

In order for the software to access the external PHY registers, a MIIM interface should be connected from VSC7513/14 to the external PHY. VSC7513/14 supports two MIIM interfaces: MIIM0 and MIIM1. MIIM0 is an internal bus to access the internal PHY only. MIIM1 should be used to access the external PHY.

Because MDIO is an open drain output, MDIO should be pulled high with the resistor around 1.5 KΩ. When connecting MDC/MDIO to multiple PHYs, the layout scheme in Figure 8-1 with end termination is recommended. The MIIM controller uses PHY address to select one of the external PHY, so the PHY addresses must be configured differently for each PHY on the same MIIM bus.

FIGURE 8-1: CONNECTING MDC/MDIO TO MULTIPLE PHYS



8.3 MAC-to-MAC Connection

AC coupling is recommended on the MAC-to-MAC connection especially when the receiving end is a non-Microchip device. VSC7513/14 has internal 100R termination and biasing. Check if termination and biasing are required if the receiving end is a non-Microchip device. Make sure that the signal direction and polarity are correct. It is recommended to simulate the high-speed signals like the QSGMII interface.

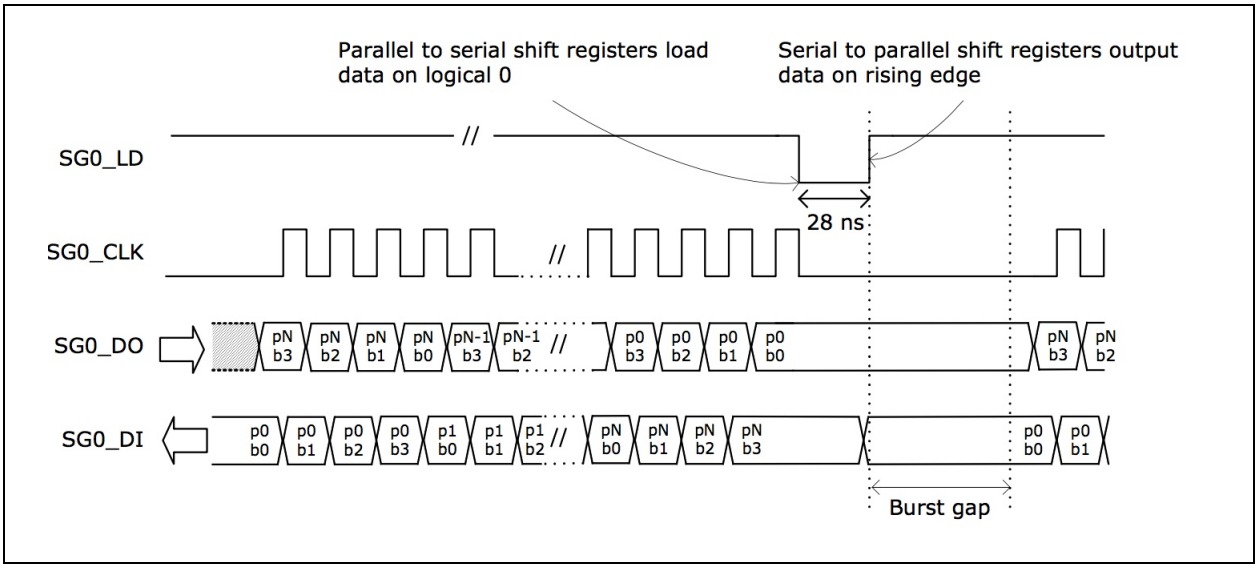
Signal detection can be omitted since MAC-to-MAC or backplane connection is always connected.

Unused SerDes interfaces can be left floating.

9.0 SERIAL GPIO CONTROLLER

The serial GPIO controller uses a 4-pin serial interface to extend the number of available general purpose I/O pins. The four SGPIO pins are overlaid on GPIO_0-GPIO_3. Figure 9-1 shows the I/O timing of the serial GPIO controller. Serial data are output on the SG_DO pin clocked by SG_CLK in bursts. After each burst, there is an assertion of the SG_LD signal. At the same time as shifting out serial outputs on SG_DO, the serial GPIO controller also samples the SG_DI input. The values sampled on SG_DI are made available to the software.

FIGURE 9-1: SGPIO TIMING



The maximum length of a burst is 128 bits data cycles organized by 32 ports with 4-bit port width. However, each SGPIO port can be enabled or disabled individually, and the port width (number of bits per port) is also centrally configurable. All enabled ports will have the same port width. The configuration of port enabling and port width applies to both serial input and output.

SG_LD can be used to ensure that outputs are stable when serial data is being shifted through the shift registers (for example, the TX_DIS output signals for the SFP modules). This can be done by using the SG_LD signal to load the serial data onto the parallel output pins after the burst has completed. 74HC595 is one of the shift registers that supports load input. If the serial GPIO controller is used for serial LED output, then SG_LD is optional because it is usually not detected when serial data are updated (shift through the chain). In that case, 74HC164 can also be used, which does not have the load input.

When a serial output bit is configured to support link/activity LED, it needs to know which switch port status to display on which SGPIO bit. This mapping is not completely software-programmable. The SGPIO controller uses a 1:1 mapping that means SGPIO port 0 can only display link/activity for switch port 0, SGPIO port 1 can only display link/activity for switch port 1, and so on.

The serial input function of the SGPIO controller can automatically route Signal detection (RX_LOS) to the internal PCS block of a certain port. The signal detection function also uses 1:1 mapping between the switch port number and the SGPIO port number. And only bit 0 of each SGPIO port can be enabled for signal detection the RX_LOS input.

There might be more serial output bits than serial input bits in a typical design especially when serial LED is supported. Since the port enabling and port width configuration are shared by the SGPIO output and input, the same number of serial bits in the output and input streams is present, which means the same number of external shift registers is required for both output and input chain. Hence, some shift registers are wasted on the serial input chain. To save the shift registers for the unused SGPIO input bits, the serial input bits can be looped – the SG_DI input signal is also connected to the serial input pins of the last shift register to create a loop so that the bits in that loop can be duplicated and the length of the whole serial stream is expanded. Check the Microchip reference design and application note on the SGPIO for more details.

10.0 OTHER INTERFACES

10.1 UART

VSC7513/14 supports two UART interfaces. The first UART is overlaid on GPIO_6 and GPIO_7, and is used by the software to upload images and also used as the command line interface to control and monitor the switch. It must be made available through an RS-232 interface. The second UART (UART2) is overlaid on GPIO_12 and GPIO_13. This interface can be used to send or receive time of day (ToD) frames with precision time protocol (PTP) applications.

10.2 I^2C

The two-wire serial interface (TWI) is compatible with I^2C. It uses two pins that are overlaid on GPIO_16 and GPIO_17. The two pins are recommended to be pulled high. VSC7513/14 has built-in support for connecting to multiple I^2C devices that use the same address (for example, SFP modules). This is done using the multiplexed clock outputs (TWI_SCL_Mn) rather than TWI_SCL. Depending on which device it needs to communicate, the software can enable or disable the various clocks. TWI_SCL_Mn are overlaid pins on GPIO_6-GPIO_15 and GPIO_17-GPIO_21.

11.0 SYSTEM RESET

The nRESET and JTAG_nTRST inputs must be held low until all power supply voltages have reached their recommended operating condition values. When the JTAG interface is not used, JTAG_nTRST is recommended to be pulled low. nRESET (active low) must be deasserted no less than 20 ms after the power supplies and the reference clock are valid. For this reason, a reset generator with power on reset (POR)/delay circuit must be used on the nRESET pin. It is also recommended to use a reset generator with a manual input so that the switch can be put into reset during on-PCB Flash programming. See **Section 5.1.1 “Flash Memory”** for more detail. While the reset signal resets the VSC7514 switch, it also resets the Flash, external PHY, shift registers for SGPIO, and other parts that must be put in known state. It is recommended to use one of the GPIO pins (GPIO_19 is used in the reference design) to reset the DDR memory so that the software can have extra control of the DDR memory.

12.0 SYNCE AND PTP

VSC7513/14 supports SyncE clock recovery from either the four internal copper PHY ports or any of the SerDes interfaces. The recovered clocks share the two recovered clock output pins overlaid on GPIO_20 and GPIO_21. For SyncE application, the two recovered clock output pins are connected to the inputs of an external digital phase locked loop (DPLL). The DPLL output is looped to the reference clock input of VSC7513/14. Make sure the DPLL outputs the correct clock signal for VSC7513/14 to boot after power-up.

VSC7513/14 also supports PTP application. GPIO_18 and GPIO_19 can be configured as PTP 1PPS input or output. They can also be configured to output a programmable clock signal. UART2 can be used to send or receive ToD frames.

Normally, for E2E or P2P transparent clock-only devices, no external components are needed, but for high-accuracy OC master or slave devices with frequency synchronization application, an external DPLL is recommended. Microchip ZL30363 series SyncE+PTP DPLL is supported by the current software. Please contact Microchip for the latest recommended software and hardware solutions.

13.0 HARDWARE CHECKLIST SUMMARY

TABLE 13-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet and retain the reference design's use of GPIO as much as possible to minimize software efforts.		
	Section 2.3, "Strapping Pins"	Check VCORE_CFG[3:0] to match the booting mode and REFCLKSEL[2:0] to match the reference clock frequency.		
Section 3.0, "Power"	Section 3.0, "Power"	Each power rail should have bulk and high-frequency decoupling capacitors.		
		Analog supplies should be isolated from digital supplies through ferrite beads.		
		Check power sequencing.		
Section 4.0, "Reference Clock"	Section 4.1, "Differential Clock"	Check that differential clock is compatible with LDVS. See the data sheet specification for reference clock input voltage range.		
	Section 4.2, "Single-Ended REFCLK Input"	Check the resistor values of the resistor network.		
Section 5.0, "CPU System"	Section 5.1, "Internal CPU Mode"	Check the VCORE_CFG[3:0] strapping.		
		Check SPI Flash memory. Voltage translation buffer might be needed.		
		Check DDR3. Check DDR_REXT.		
	Section 5.2, "External CPU Mode"	Check the VCORE_CFG[3:0] strapping.		
		Check SPI slave, MIIM slave, or PCIe interface used as management interface from the external CPU to VSC7513/14.		
		Check DDR_REXT, external DDR calibration. Connect the pin to ground through 240Ω ±1%.		
Section 6.0, "Port Configurations"	Section 6.0, "Port Configurations"	Make sure the selected copper PHY ports plus SerDes ports combination can be supported by VSC7513/14.		

TABLE 13-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 7.0, "Internal Copper PHY Ports"	Section 7.1, "Copper PHY MDI Interface"	Check the magnetic connection. No center tap voltage is allowed, and external termination resistors are not needed.		
	Section 7.2, "Chassis Ground"	Chassis ground is recommended.		
	Section 7.3, "Voltage Reference Pins"	Use 2.0 kΩ, 1% resistor for REF_REXT and 1 µF capacitor for REF_FILT. Use single-point grounding for REF_FILT and REF_REXT.		
Section 8.0, "SerDes Interfaces"	Section 8.0, "SerDes Interfaces"	Connect an external 620Ω ±1% resistor between SerDes_Rext_0 and SerDes_Rext_1 for analog bias calibration.		
	Section 8.1, "SFP Port"	Make sure SerDes polarity is correct. Check the SFP control signals. RX_LOS is recommended to be connected to the switch (SFPx_SD inputs or SGPIO).		
		All SFP control signals are recommended to be pulled high.		
	Section 8.2, "External PHY"	AC coupling is recommended. Check the signal directions. Check the MIIM connection and topology.		
	Section 8.3, "MAC-to-MAC Connection"	AC coupling is recommended. Check the signal directions.		
Section 9.0, "Serial GPIO Controller"	Section 9.0, "Serial GPIO Controller"	Check the switch port to SGPIO port mapping for the link/active LED output and RX_LOS signal input.		
Section 10.0, "Other Interfaces"	Section 10.1, "UART"	Make UART available for image loading and CLI.		
	Section 10.2, "I^2C"	Pull high is required. Use the multiplexed clockout for I^2C slave devices with the same addresses (like SFP modules).		
Section 11.0, "System Reset"	Section 11.0, "System Reset"	Check that all the devices and the board are reset by the system reset output — switch, PHY, Flash, SGPIO shift registers, and so on. Put the switch into reset when the PCB Flash programming is performed. DDR3 software reset is recommended.		
Section 12.0, "SyncE and PTP"	Section 12.0, "SyncE and PTP"	Check if an external DPLL is needed. Find the recommended ZL30xxx DPLL.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003199A (08-23-19)	Initial release	

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