Atmel AVR32837: AVR UC3 D Schematic Checklist

Features

- **Power circuit**
- **Reset circuit**
- **USB connection**
- **aWire and JTAG debug ports**
- **Clocks and crystal oscillators**
- **Capacitive Touch (CAT) module**
- **Patents and trademarks:**
  - **Atmel® QTouch® (patented charge-transfer method)**

1 Introduction

A good hardware design comes from a proper schematic. Since Atmel 32-bit AVR® UC3 D devices have a fair number of pins and functions, the schematic for these devices can be large and quite complex.

This application note describes a common checklist which should be used when starting and reviewing the schematics for a 32-bit AVR UC3 D design.

32-bit Atmel Microcontrollers

Application Note

Rev. 32171A-AVR-08/11

2 Power circuit

2.1 Single 3.3 volt power supply

Figure 2-1. Single 3.3 volt power example schematic.

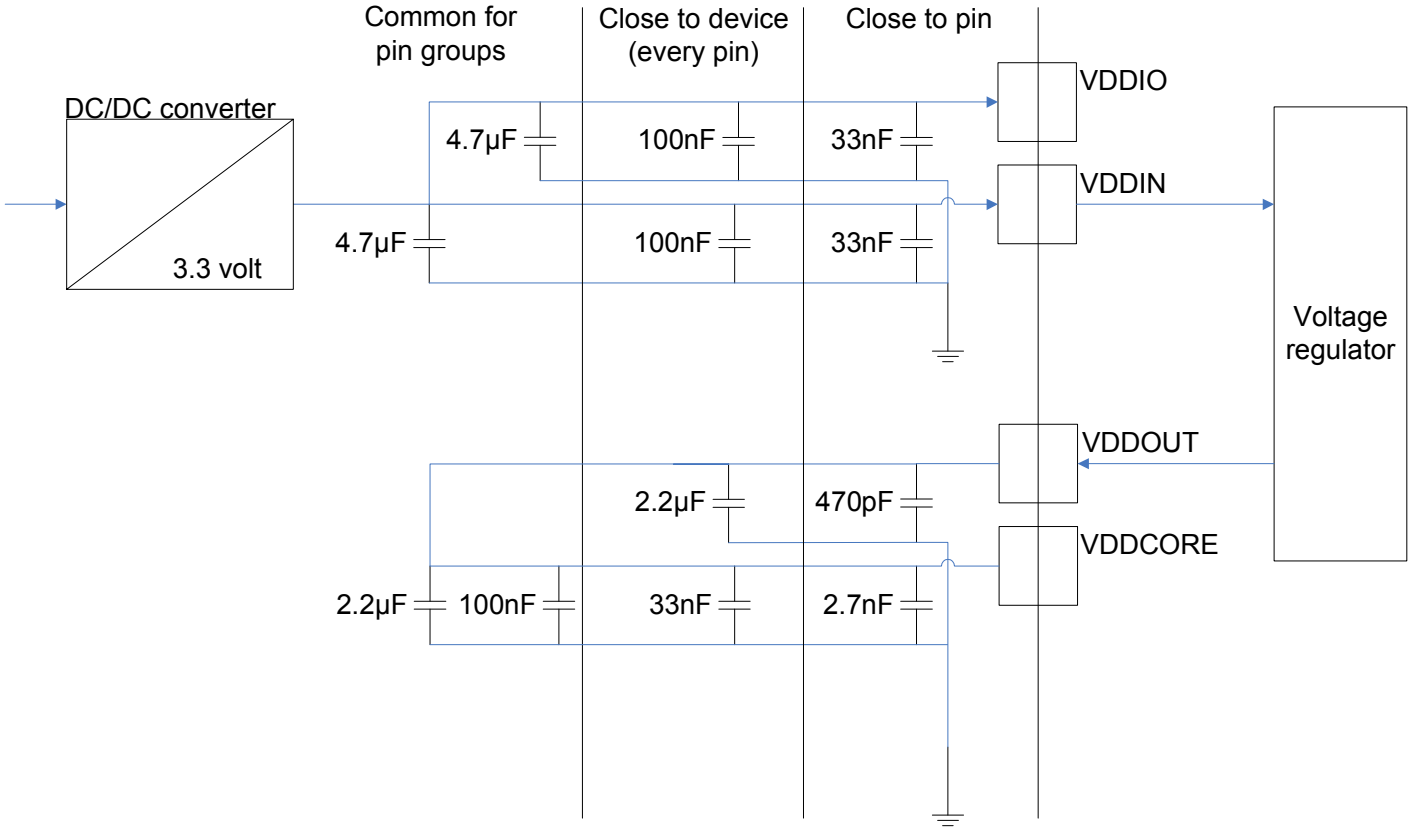


Table 2-1. Single 3.3 volt power supply checklist.

☑	Signal name	Recommended pin connection	Description
	VDDIO	3.0V to 3.6V Decoupling/filtering capacitors 33nF(1)(2), 100nF(1)(3), and 4.7µF(1)	Powers I/O lines and USB transceiver Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop
	VDDIN	3.0V to 3.6V Decoupling/filtering capacitors 33nF(1)(2), 100nF(1)(3), and 4.7µF(1)	Powers on-chip voltage regulator Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop
	VDDOUT	Decoupling/filtering capacitors 470pF(1)(2) and 4.7µF(1)	Output of the on-chip 1.8V voltage regulator Decoupling/filtering capacitors must be added to guarantee 1.8V stability
	VDDCORE	1.65V to 1.95V Connected to VDDOUT Decoupling/filtering capacitors 2.7nF(1)(2), 33nF(1)(3), 100nF(1), and 4.7µF(1)	Powers device, flash logic and on-chip RC Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop

Notes:
1. These values are given only as a typical example.
2. Decoupling capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.
3. Decoupling capacitor should be placed close to the device for each pin in the signal group.

2.2 Dual 3.3 volt and 1.8 volt power supply

Figure 2-2. Dual 3.3 volt and 1.8 volt power example schematic.

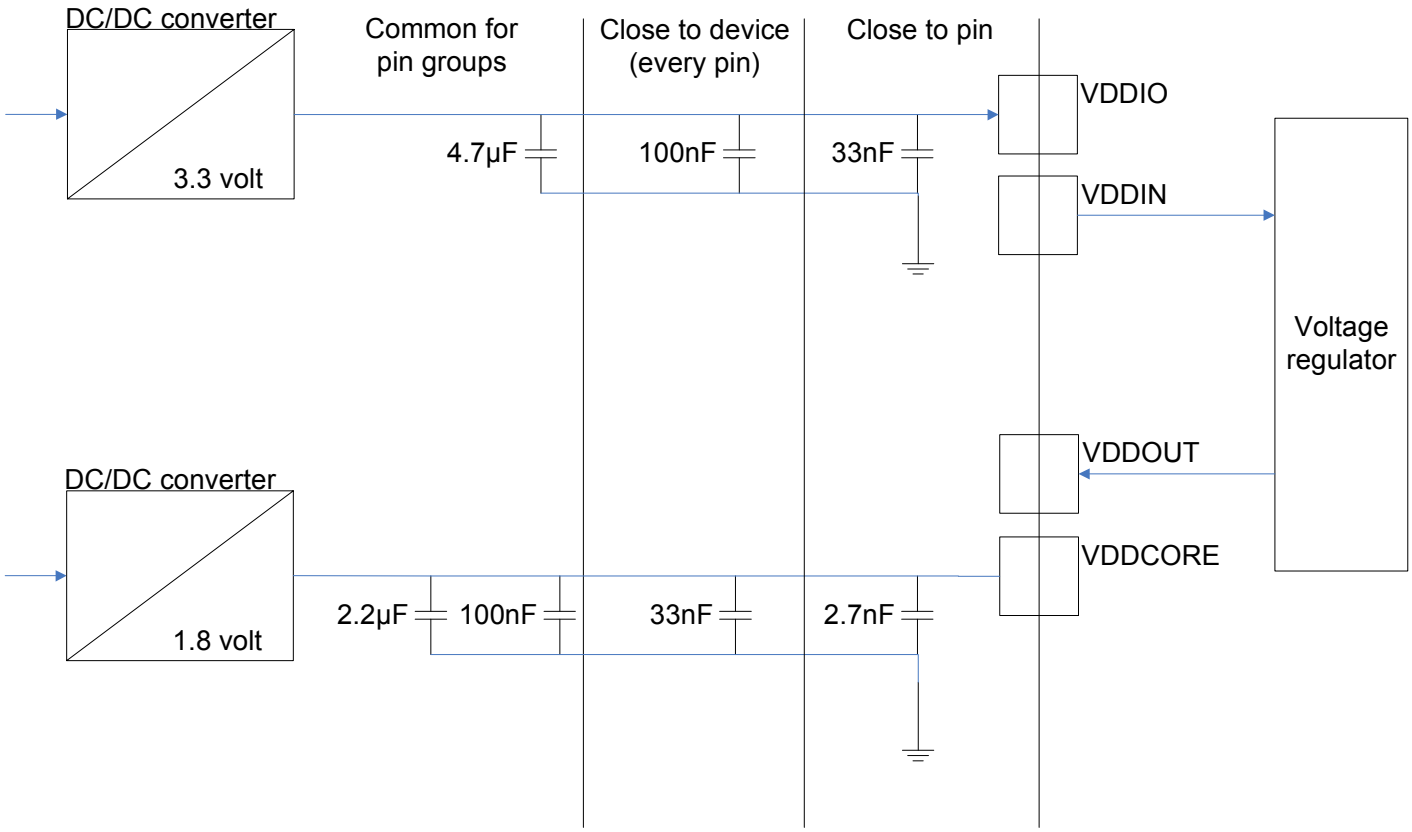


Table 2-2. Dual 3.3 volt and 1.8 volt power supply checklist.

☑	Signal name	Recommended pin connection	Description
	VDDIO	3.0V to 3.6V Decoupling/filtering capacitors 33nF(1)(2), 100nF(1)(3), and 4.7µF(1)	Powers I/O lines and USB transceiver Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop
	VDDIN	Connected to ground	On-chip voltage regulator not in use
	VDDOUT	Connected to ground	On-chip voltage regulator not in use
	VDDCORE	1.65V to 1.95V Decoupling/filtering capacitors 2.7nF(1)(2), 33nF(1)(3), 100nF(1), and 2.2µF(1)	Powers device, flash logic and on-chip RC Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop

Notes:
1. These values are given only as a typical example.
2. Decoupling capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.
3. Decoupling capacitor should be placed close to the device for each pin in the signal group.

2.3 ADC reference power supply

The following schematic checklist is only necessary if the design is using the internal analog to digital converter.

Figure 2-3. ADC reference power supply example schematic.

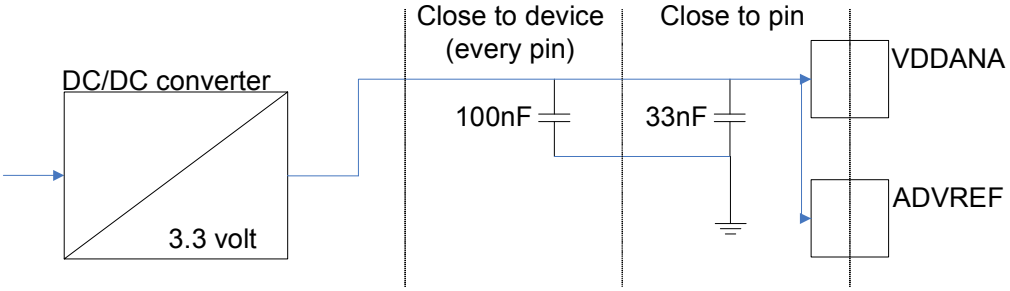


Table 2-3. ADC reference power supply checklist.

☑	Signal name	Recommended pin connection	Description
	VDDANA	3.0V to 3.6V Decoupling/filtering capacitors 33nF(1)(2) and 100nF(1)(3)	Powers on-chip ADC Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop
	ADVREF	2.6V to VDDANA Connect with VDDANA	ADVREF is a pure analog input

Notes:
1. These values are given only as a typical example.
2. Decoupling capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.
3. Decoupling capacitor should be placed close to the device for each pin in the signal group.

2.4 No ADC power supply

The following schematic checklist is only necessary if the design is not using the internal analog to digital converter.

Figure 2-4. No ADC power supply example schematic.

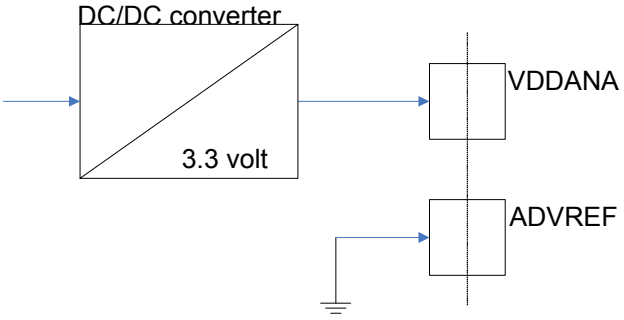


Table 2-4. No ADC power supply checklist.

☑	Signal name	Recommended pin connection	Description
	VDDANA	3.0V to 3.6V	
	ADVREF	Connected to ground	

3 Reset circuit

Figure 3-1. Reset circuit example schematic.

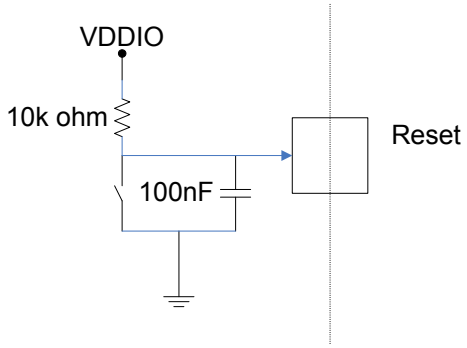


Table 3-1. Reset circuit checklist.

☑	Signal name	Recommended pin connection	Description
	RESET	Can be left unconnected in case no reset from the system needs to be applied to the product	The RESET_N pin is a Schmitt input and integrates a permanent pull-up resistor to VDDIO

4 Clocks and crystal oscillators

4.1 External clock source

Figure 4-1. External clock source schematic.

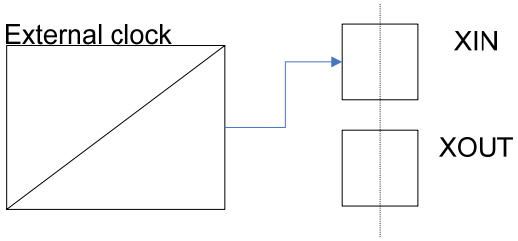


Table 4-1. External clock source checklist.

☑	Signal name	Recommended pin connection	Description
	XIN	Connected to clock output from external clock source	Up to VDDIO volt square wave signal up to 50MHz
	XOUT	Can be left unconnected or used as GPIO	

4.2 Crystal oscillator

Figure 4-2. Crystal oscillator example schematic.

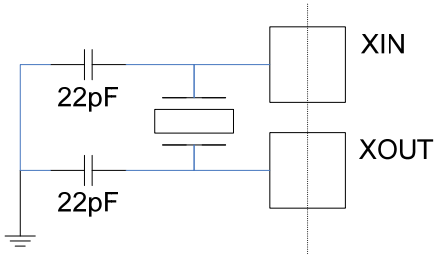


Table 4-2. Crystal oscillator checklist.

☑	Signal name	Recommended pin connection	Description
	XIN	Biasing capacitor 22pF[(1)(2)]	External crystal between 450kHz and 16MHz
	XOUT	Biasing capacitor 22pF[(1)(2)]	

Notes:
1. These values are given only as a typical example. The capacitance C of the biasing capacitors can be computed based on the crystal load capacitance CL and the internal capacitance Ci of the MCU as follows:

   C = 2 (CL – Ci)

   The value of CL can be found in the crystal datasheet and the value of Ci can be found in the MCU datasheet.
2. Decoupling capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.

5 USB connection

5.1 Not used

When the USB interface is not used, D+ and D- should be connected to ground.

5.2 Device mode, powered from bus connection

Figure 5-1. USB in device mode, bus powered connection example schematic.

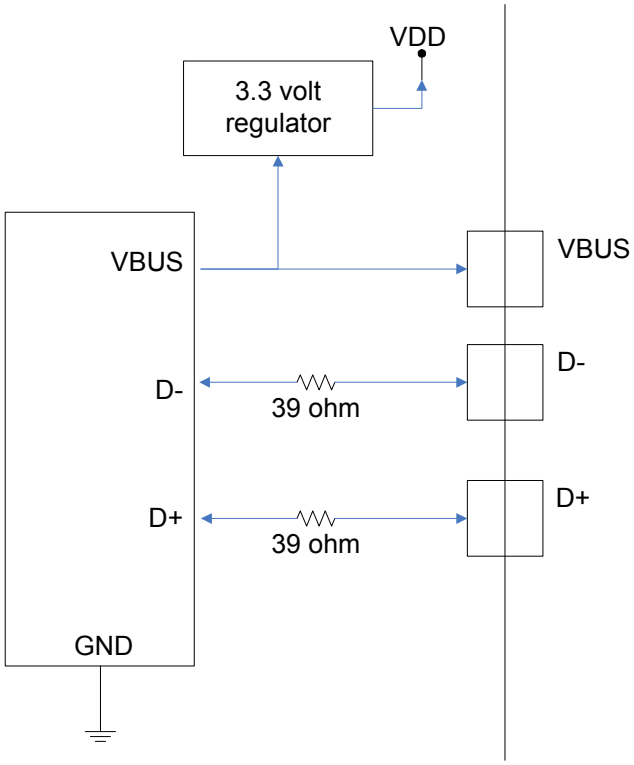


Table 5-1. USB bus powered connection checklist.

☑	Signal name	Recommended pin connection	Description
	VBUS	Directly to connector	USB power measurement pin
	D-	39 ohm series resistor Placed as close as possible to pin	Negative differential data line
	D+	39 ohm series resistor Placed as close as possible to pin	Positive differential data line

5.3 Device mode, self powered connection

Figure 5-2. USB in device mode, self powered connection example schematic.

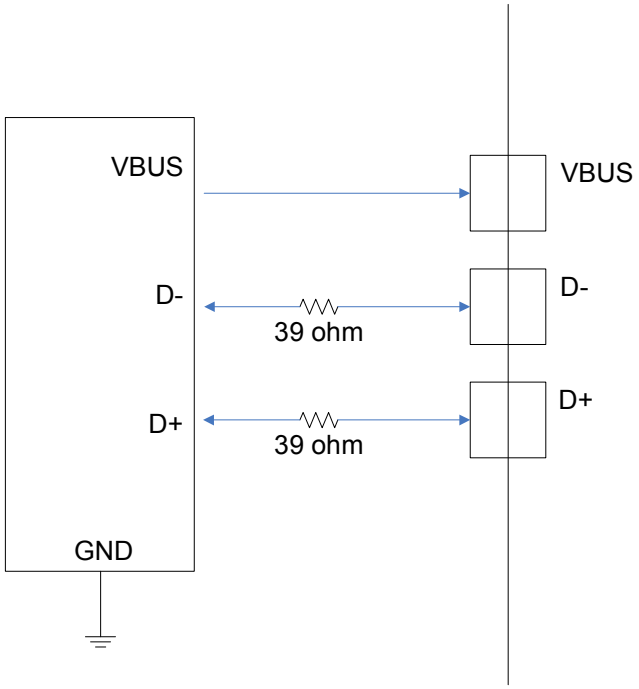


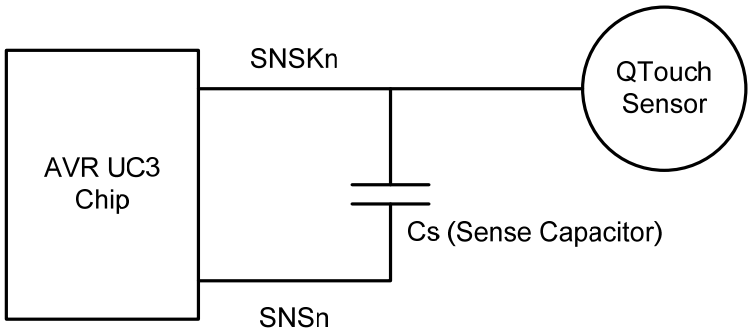
Table 5-2. USB self powered connection checklist.

☑	Signal name	Recommended pin connection	Description
	VBUS	Directly to connector	USB power measurement pin
	D-	39 ohm series resistor Placed as close as possible to pin	Negative differential data line
	D+	39 ohm series resistor Placed as close as possible to pin	Positive differential data line

6 Capacitive Touch (CAT) Module

6.1 QTouch

Figure 6-1. QTouch typical connection.



Refer to the Atmel AVR UC3 D datasheet; section CAT, section I/O lines for the pin selection guide.

7 aWire and JTAG debug ports

7.1 aWire port interface

Figure 7-1. aWire port interface example schematic.

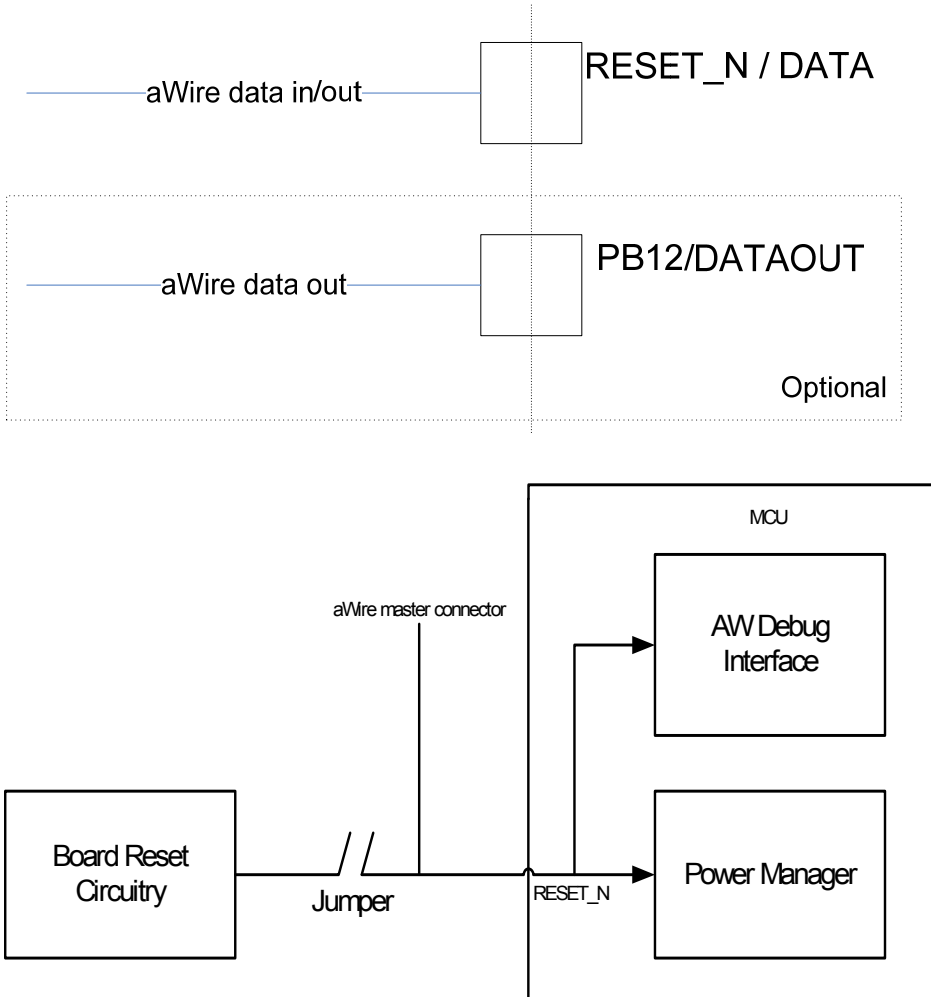


Table 7-1. aWire port interface checklist.

☑	Signal name	Recommended pin connection	Description
	DATA	Connect to aWire DATA signal on external tool	Device external reset line used for data input and output. Reset circuitry should be disabled as shown above when the RESET_N pin is used during aWire operation
	DATAOUT	Optional, connect to aWire DATAOUT signal on external tool	Data output is optional and only needed for aWire full duplex mode

Note: 1. The aWire needs an external pull-up on the RESET_N pin to ensure that the pin pulled up when the bus is not driven.

7.2 JTAG port interface

Figure 7-2. JTAG port interface example schematic.

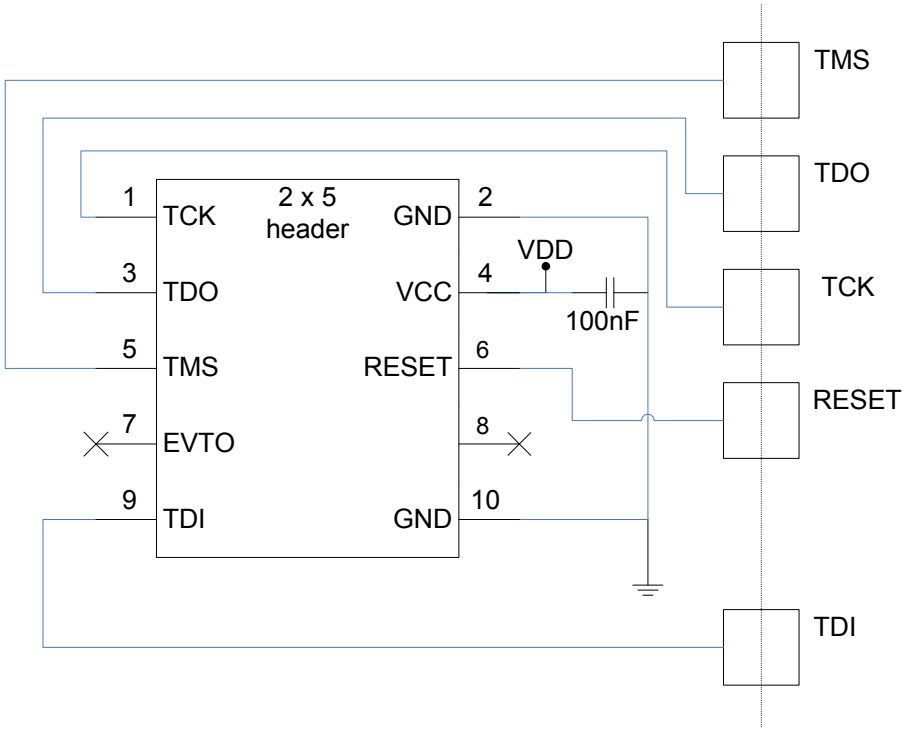


Table 7-2. JTAG port interface checklist.

☑	Signal name	Recommended pin connection	Description
	TMS	PA02	Test mode select, sampled on rising TCK
	TDO	PA01	Test data output, driven on falling TCK
	TCK	PB12	Test clock, fully asynchronous to system clock frequency
	RESET	RESET	Device external reset line
	TDI	PA00	Test data input, sampled on rising TCK
	EVTO		Event output, not used

8 Miscellaneous topics

8.1 I/O line considerations

The device datasheet contains subsection “I/O Line Considerations” under section “Package and Pinout”.

8.2 Boot loader pin

If a pin is used to enter in the boot loader mode provided by the default boot loader programmed on all chips, that pin should be pulled-up or pulled-low depending on the chosen boot loader pin configuration.

9 Suggested reading

9.1 Device datasheet

The device datasheet contains block diagrams of the peripherals and details about implementing firmware for the device. The datasheet is available on http://www.atmel.com/dyn/products/documents.asp?category_id=163&family_id=607&subfamily_id=2138 in the *Datasheets* section.

9.2 Touch design documents

Touch design documents contain the principles required for designing with buttons, sliders and wheels. They are available on, http://www.atmel.com/dyn/products/documents.asp?category_id=170&family_id=702&subfamily_id=2259.

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Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: (+1)(408) 441-0311
Fax: (+1)(408) 487-2600
www.atmel.com

Atmel Asia Limited
Unit 01-5 & 16, 19F
BEA Tower, Milennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
HONG KONG
Tel: (+852) 2245-6100
Fax: (+852) 2722-1369

Atmel Munich GmbH
Business Campus
Parkring 4
D-85748 Garching b. Munich
GERMANY
Tel: (+49) 89-31970-0
Fax: (+49) 89-3194621

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chou-ku, Tokyo 104-0033
JAPAN
Tel: (+81) 3523-3551
Fax: (+81) 3523-7581

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