



USB2244/USB2244I

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip USB2244/USB2244I. These checklist items should be followed when utilizing the USB2244/USB2244I in a new design. A summary of these items is provided in [Section 9.0, "Hardware Checklist Summary," on page 12](#). Detailed information on these subjects can be found in the corresponding section:

- [Section 2.0, "General Considerations"](#)
- [Section 3.0, "Power"](#)
- [Section 4.0, "USB Signals"](#)
- [Section 5.0, "Card Reader Interface"](#)
- [Section 6.0, "Clock Circuit"](#)
- [Section 7.0, "Power and Startup"](#)
- [Section 8.0, "Configuration Options"](#)

2.0 GENERAL CONSIDERATIONS

2.1 Pin Check

Check the pinout of the part against the data sheet. Ensure all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.2 Ground

- The ground pins, **GND**, should be connected to the solid ground plane on the board.
- It is recommended that all ground connections be tied together to the same ground plane. Separate ground planes are not recommended.

2.3 USB-IF-Compliant USB Connector

- USB-IF-certified USB Connector with a valid Test ID (TID) is required for all USB products to be compliant and pass USB-IF product certification.

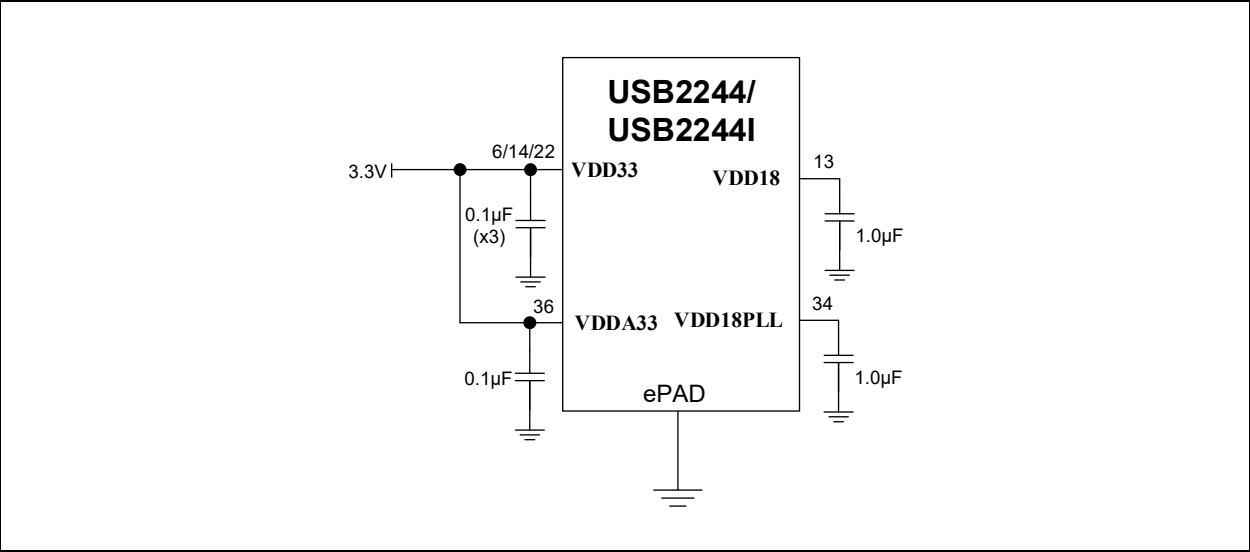
3.0 POWER

- The 3.3V supplies (**VDD33** and **VDDA33**) are located on pins 6, 14, 22, and 36. These pins all require a connection to a regulated 3.3V power plane.
- The **VDD33/VDDA33** pins each should include 0.1 μ F capacitors to decouple the device. The capacitor size should be SMD_0603 or smaller.
- **VDD18** (pin 13) is a core regulator output and should connect to an external filter capacitor. A 1.0 μ F capacitor, $\pm 20\%$, ESR $< 0.1\Omega$ is recommended. Do not power external circuitry from this regulator output.
- **VDD18PLL** (pin 34) is a PLL regulator output and should connect to an external filter capacitor. A 1.0 μ F capacitor, $\pm 20\%$, ESR $< 0.1\Omega$ is recommended. Do not power external circuitry from this regulator output.

The power and ground connections are shown in [Figure 3-1](#).

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FIGURE 3-1: POWER AND GROUND CONNECTIONS



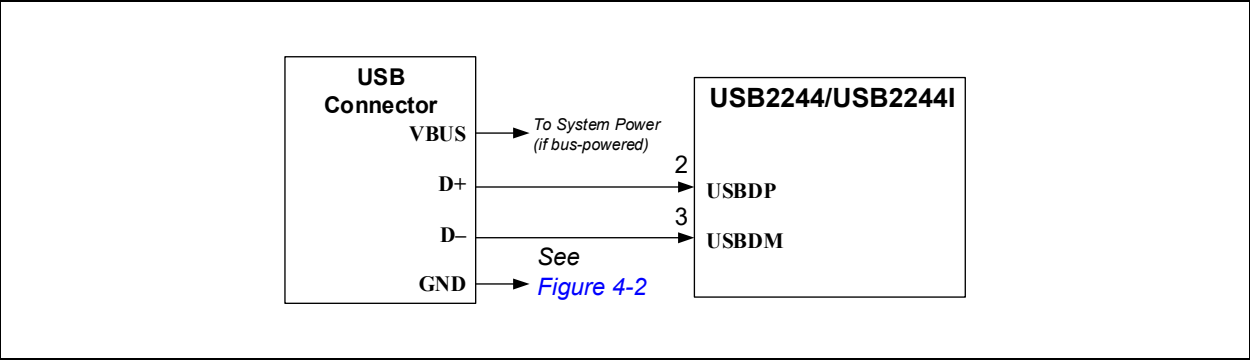
4.0 USB SIGNALS

4.1 USB PHY Interface

- **USBDP** (pin 2): This pin is the positive (+) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included internal the IC. This pin can connect directly to the D+/DP pin of a USB Connector or an embedded USB Host.
- **USBDM** (pin 3): This pin is the negative (–) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included internal the IC. This pin can connect directly to the D–/DM pin of a USB Connector or an embedded USB Host.

For details of USB connections, refer to [Figure 4-1](#).

FIGURE 4-1: USB DATA SIGNAL CONNECTIONS



4.2 USB Protection

The use of external protection circuitry may be required to provide additional ESD protection beyond what is included in the hub IC. These generally are grouped into three categories:

- TVS protection diodes
 - ESD protection for IEC-61000-4-2 system-level tests
- Application-targeted protection ICs or galvanic isolation devices
 - DC-overvoltage protection for short-to-battery protection
- Common-mode chokes
 - For EMI reduction

The USB2244/USB2244I can be used in conjunction with these types of devices, but it is important to understand the negative effect on USB signal integrity that these devices may have and to select components accordingly and follow the implementation guidelines from the manufacturer of these devices.

The following general guidelines may also be used for implementing these devices:

- Select only devices that are designed specifically for high-speed applications. Per the USB specification, a total of 5 pF is budgeted for connector, PCB traces, and protection circuitry.
- Place these devices as close as possible to the USB connector.
- Never branch the USB signals to reach protection devices. Always place the protection devices directly on top of the USB differential traces.
- The effectiveness of TVS devices depends heavily on effective grounding. Always ensure a very low impedance path to a large ground plane.
- Place TVS diodes on the same layer as the USB signal trace. Avoid vias or place vias behind the TVS device if possible.

4.3 GND and EARTH Recommendations

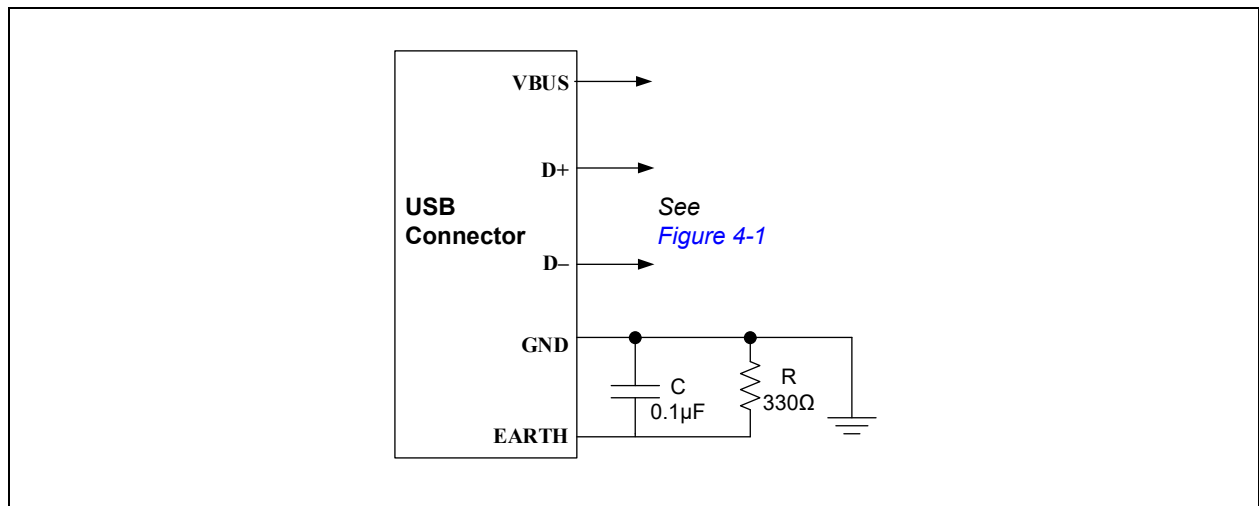
The GND pins of the USB connector must be connected to the PCB with a low impedance path directly to a large GND plane.

The EARTH pins of the USB connector may be connected in one of two ways:

- (Recommended) To GND through a resistor and capacitor in parallel. An RC filter can help to decouple and minimize EMI between a PCB and a USB cable.
- Directly to the GND plane.

The recommended implementation is shown in [Figure 4-2](#).

FIGURE 4-2: RECOMMENDED USB CONNECTOR GND AND EARTH CONNECTIONS



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5.0 CARD READER INTERFACE

5.1 Secure Digital/MultiMediaCard™ Slot

USB2244/USB2244I supports Secure Digital (SD) 2.0 including HS-SD, SDXC, and SDHC media. Newer media and small form factor SD media (that is, microSD) are also supported due to backwards compatibility requirements on all compliant SD media, though newer features and performance cannot be taken advantage of.

1-/4-/8-bit MultiMediaCard™ (MMC) 4.2 is also supported on the same interface and card slot. Newer MMC media and eMMC media are also supported due to backwards compatibility requirements on all compliant MMC media, though newer features and performance can not be taken advantage of.

If designing with a standard SD/MMC card slot, refer to [Figure 5-1](#). If designing with an embedded eMMC memory, refer to [Figure 5-2](#). If designing with a microSD card slot, refer to [Figure 5-3](#).

FIGURE 5-1: SD/MMC MEDIA SLOT

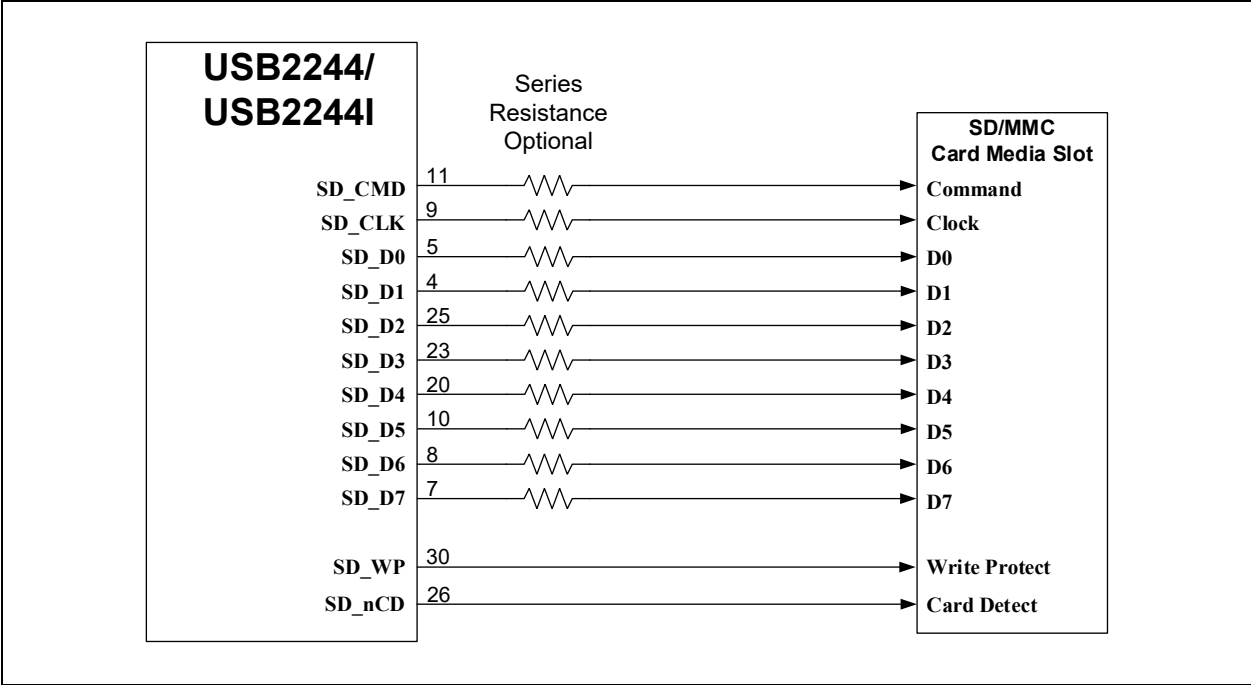
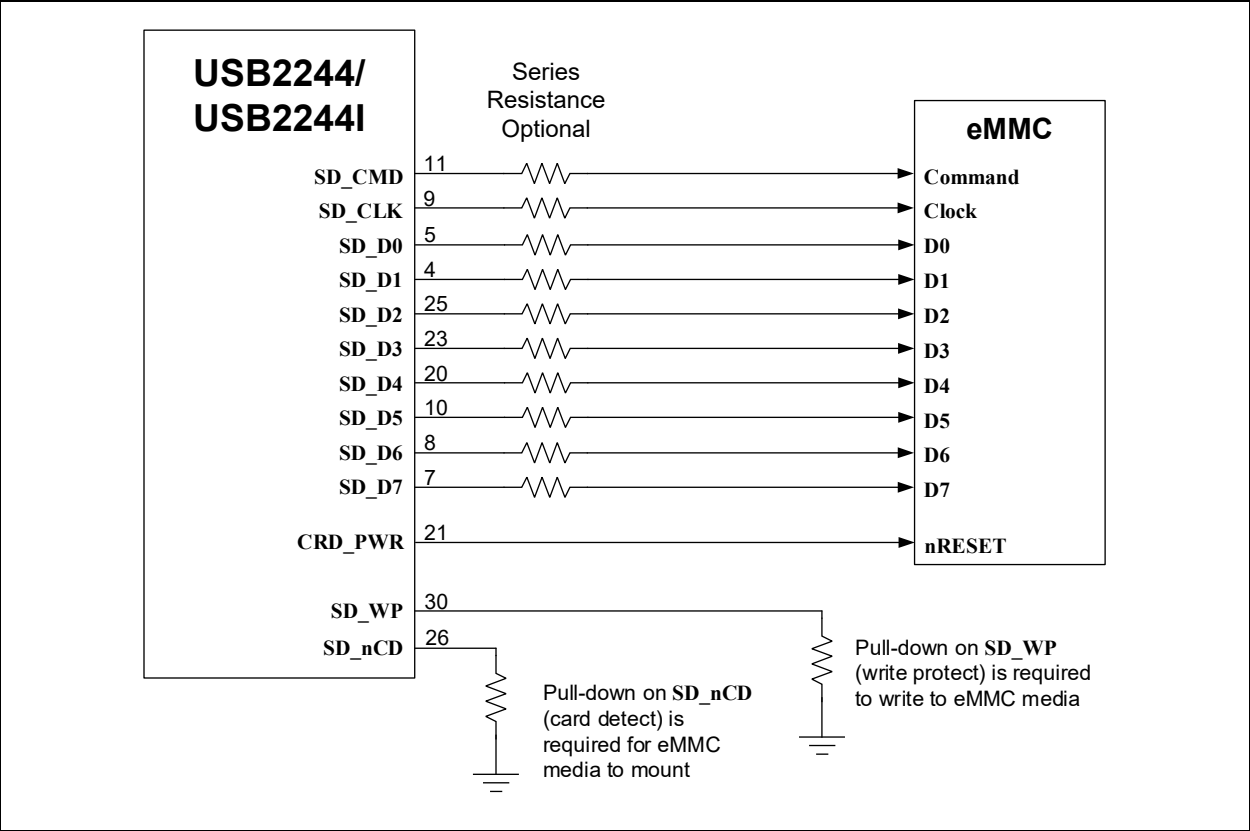
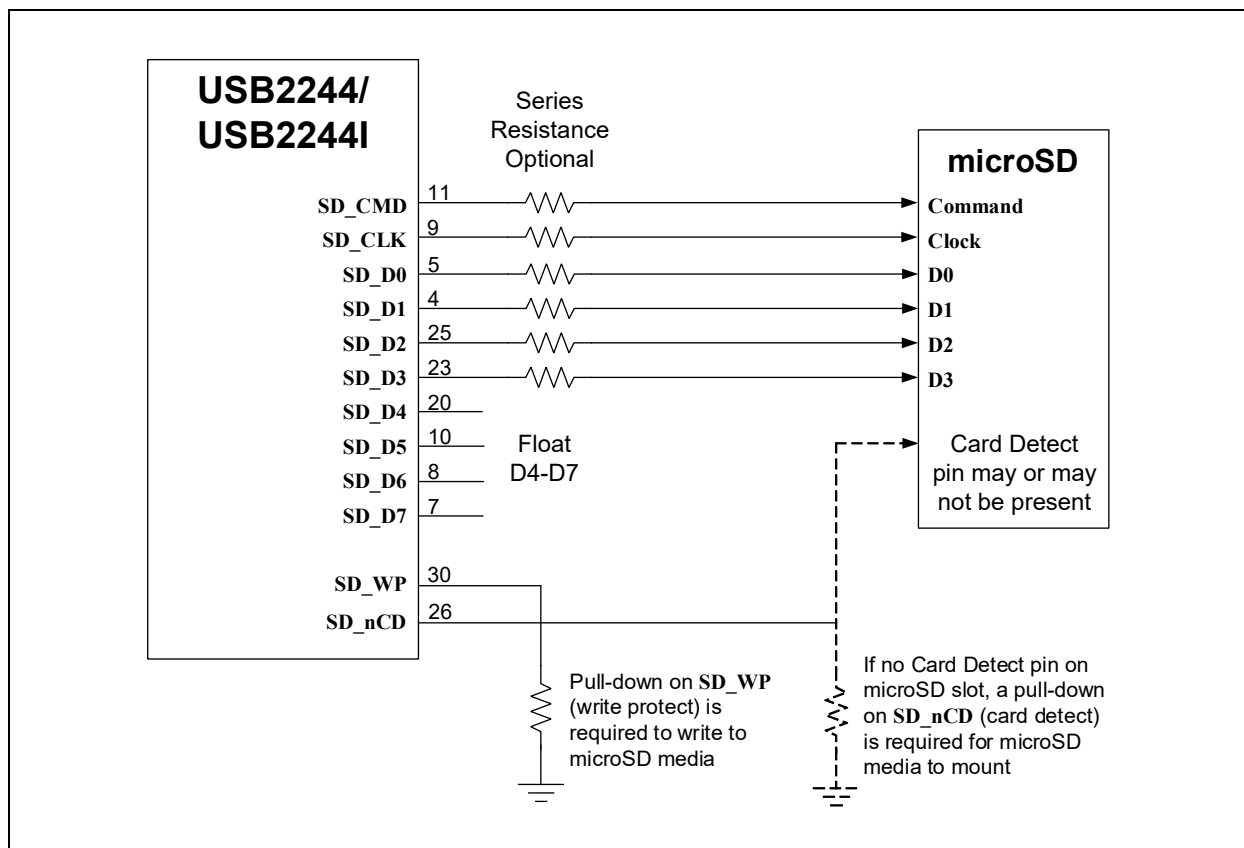


FIGURE 5-2: eMMC MEMORY CONNECTIONS



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FIGURE 5-3: MICROSD CARD SLOT CONNECTIONS



5.2 Card Power Switch

USB2244/USB2244I includes an internal 3.3V power switch capable of supplying up to 200 mA continuously to the attached media. The card power switch includes fault protection and will automatically shut off the output if current draw exceeds the 200 mA maximum.

Note: The default setting for card power current limit is 200 mA. It may be optionally set to 100 mA via EEPROM configuration if desired.

The card power output should include some bulk capacitance to maintain voltage stability during card use. A 4.7 μ F ceramic capacitor is sufficient for most use-cases. Certain high power media may require more. Smaller capacitances can also be added to filter out high frequency noise, if present in the system.

A LED may be optionally connected directly to the card power output to give visual indication of card power.

FIGURE 5-4: CRD_PWR CARD MEDIA POWER SUPPLY SWITCH

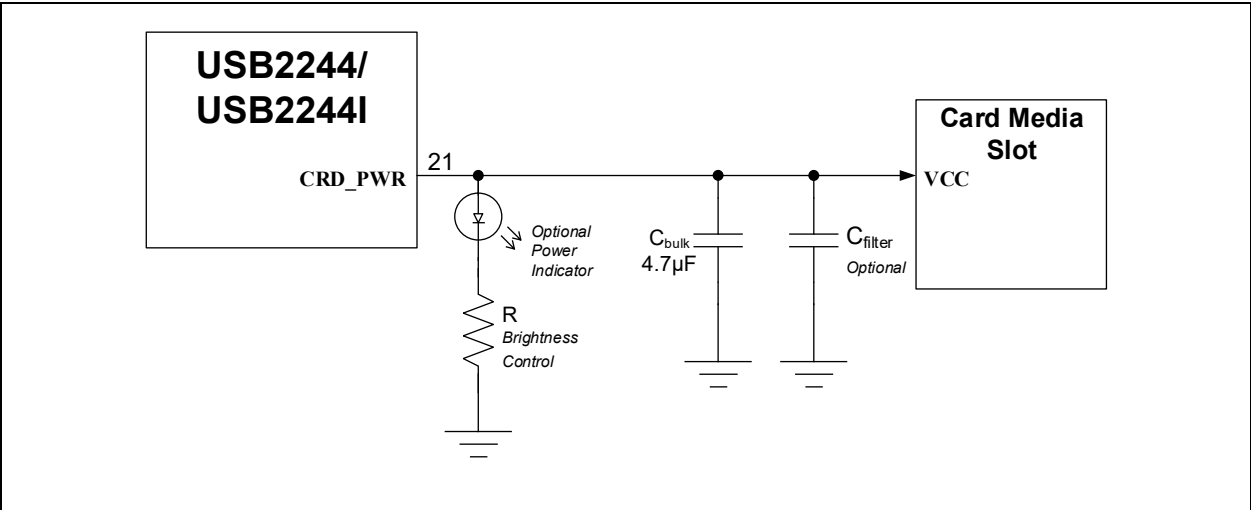
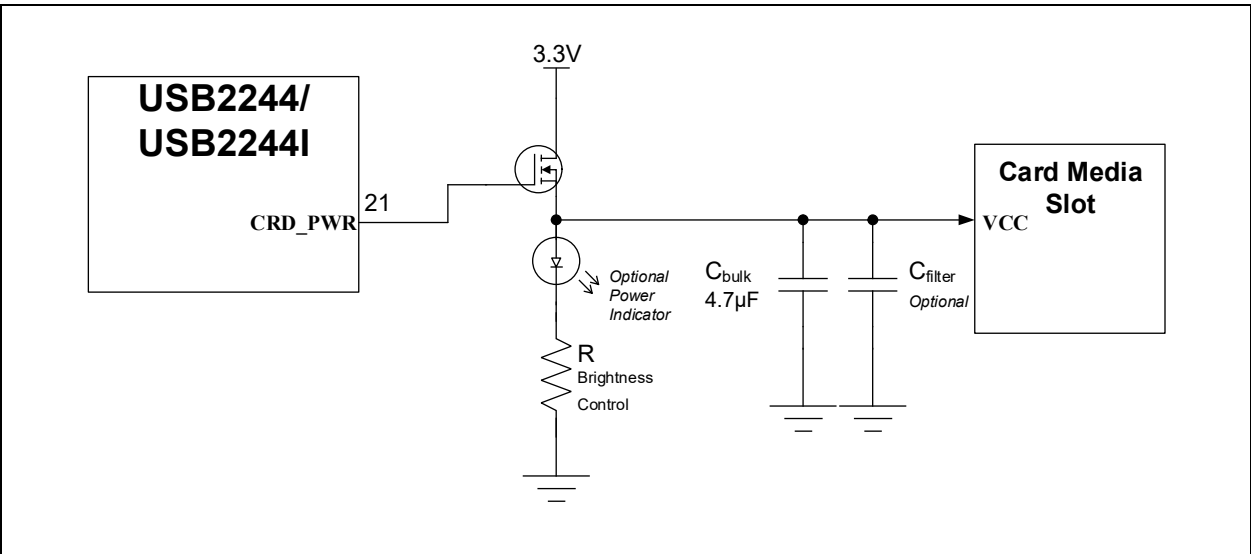


FIGURE 5-5: CRD_PWR CONTROLLED POWER SUPPLY FOR CARDS REQUIRING MORE THAN 200 MA



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6.0 CLOCK CIRCUIT

6.1 Crystal and External Clock Connection

A 24.000 MHz (± 350 ppm) reference clock is the source for the USB interface and for all other functions of the device. For exact specifications and tolerances, refer to the latest revision of the *USB2244/USB2244I Data Sheet*.

- **XTAL1** (pin 33) is the clock circuit input for the USB2244/USB2244I. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- **XTAL2** (pin 32) is the clock circuit output for the USB2244/USB2244I. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- A 1 megohm resistor ($1\text{ M}\Omega$) is required to be connected across the **XTAL1** and **XTAL2** pins.
- The crystal loading capacitor values are system-dependent, based on the total C_L specification of the crystal and the stray capacitance value. The PCB design, crystal, and layout all contribute to the characteristics of this circuit. A commonly-used formula for calculating the appropriate physical C_1 and C_2 capacitor values is:

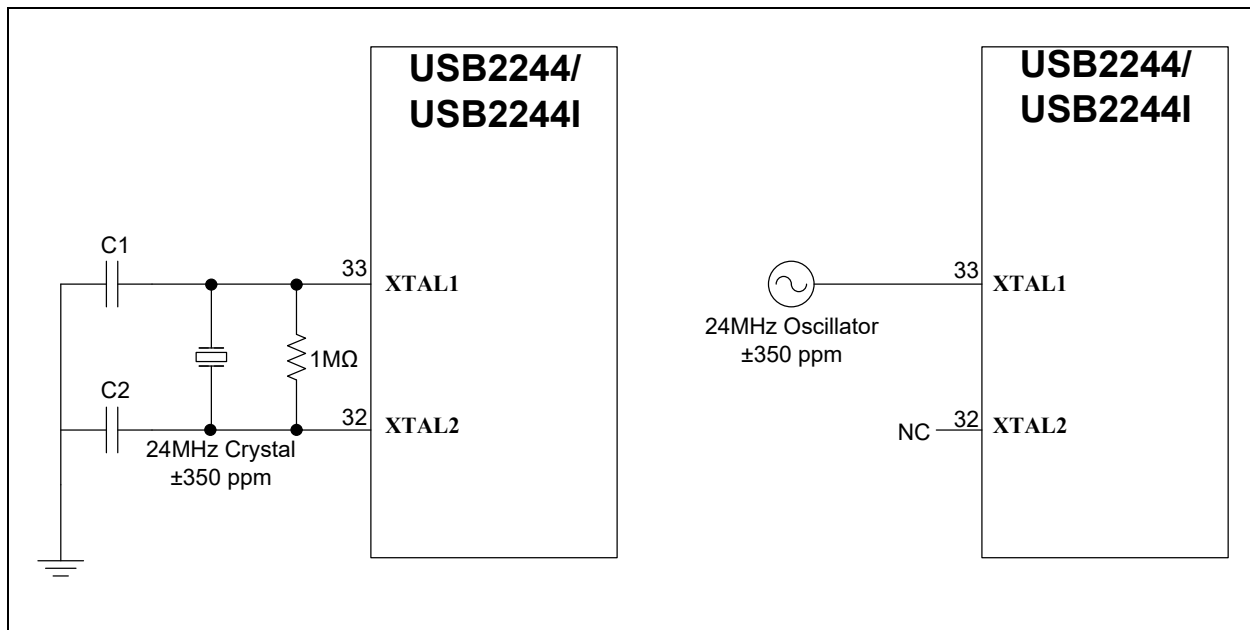
$$C_L = ((C_{X1})(C_{X2}) / (C_{X1} + C_{X2}))$$

Where: C_L is the spec from the crystal data sheet, $C_{X1} = C_{\text{stray}} + C_1$, $C_{X2} = C_{\text{stray}} + C_2$

Note: C_{stray} is the stray/parasitic capacitance due to PCB layout. It can be assumed to be very small, in the 1-2 pF range, and then verified by physical experiments in the lab if PCB simulation tools are not available.

- Alternately, a 24.000 MHz, 1.2V-3.3V clock oscillator may be used to provide the clock source for the USB2244/USB2244I. When using a single-ended clock source, **XTALOUT** (pin 21) should be left floating as a No Connect (NC).

FIGURE 6-1: CRYSTAL AND OSCILLATOR CONNECTIONS



7.0 POWER AND STARTUP

7.1 RBIAS Resistor

RBIAS (pin 35) on the USB2244/USB2244I must connect to ground through a 12 k Ω resistor with a tolerance of 1.0%. This is used to set up critical bias currents for the internal circuitry. This should be placed as close as possible to the IC pin, and be given a dedicated, low-impedance path to a ground plane.

7.2 Board Power Supplies

7.2.1 POWER RISE TIME

The power rail voltage and rise time should adhere to the supply rise time specification as defined in the *USB2244/USB2244I Data Sheet*.

If a monotonic/fast power rail rise cannot be assured, then the **RESET_N** signal should be controlled by a reset supervisor and only released when the power rail has reached a stable level.

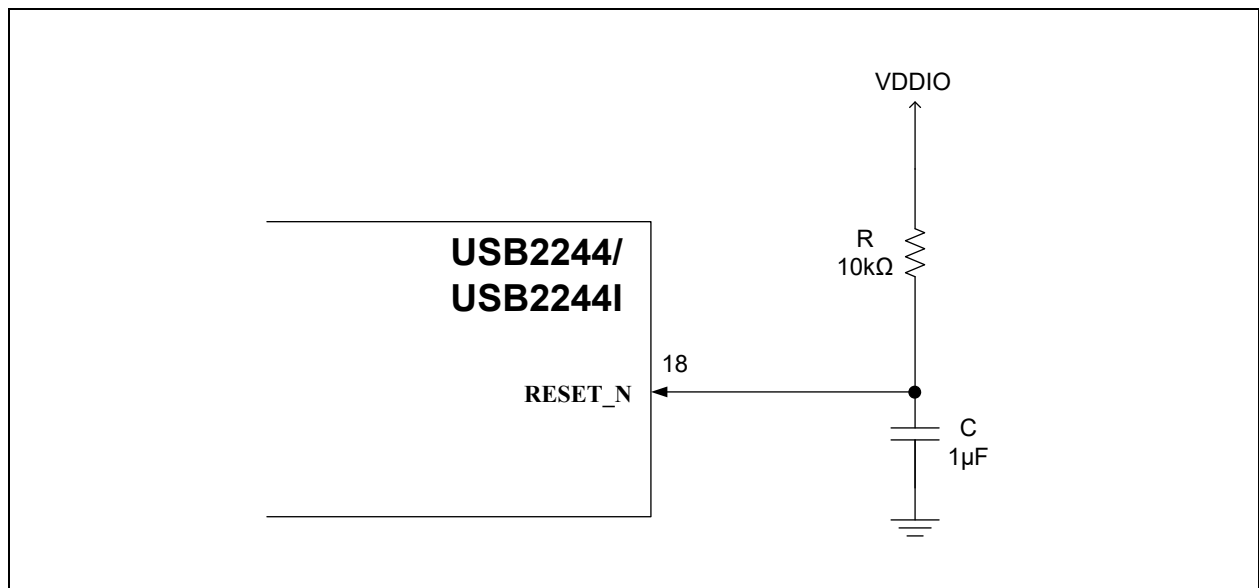
7.2.2 CURRENT CAPABILITY

It is important to size the 3.3V power rails appropriately. The 3.3V power supply must be capable of supplying sufficient power for the USB2244/USB2244I (up to 165 mA at 3.3V) as well as the card media supported (up to 200 mA if using the internal card power supply output on **CRD_PWR**).

7.3 Reset Circuit

RESET_N (pin 18) is an active-low reset input. This signal resets all logic and registers within the USB2244/USB2244I. A hardware reset (**RESET_N** assertion) is not required following power-up. Please refer to the latest copy of the *USB2244/USB2244I Data Sheet* for reset timing requirements. [Figure 7-1](#) shows a recommended reset circuit for powering up the USB2244/USB2244I when reset is triggered by the power supply. The values for the “R” resistor and “C” capacitor are not critical and may be adjusted per individual system needs or preferences.

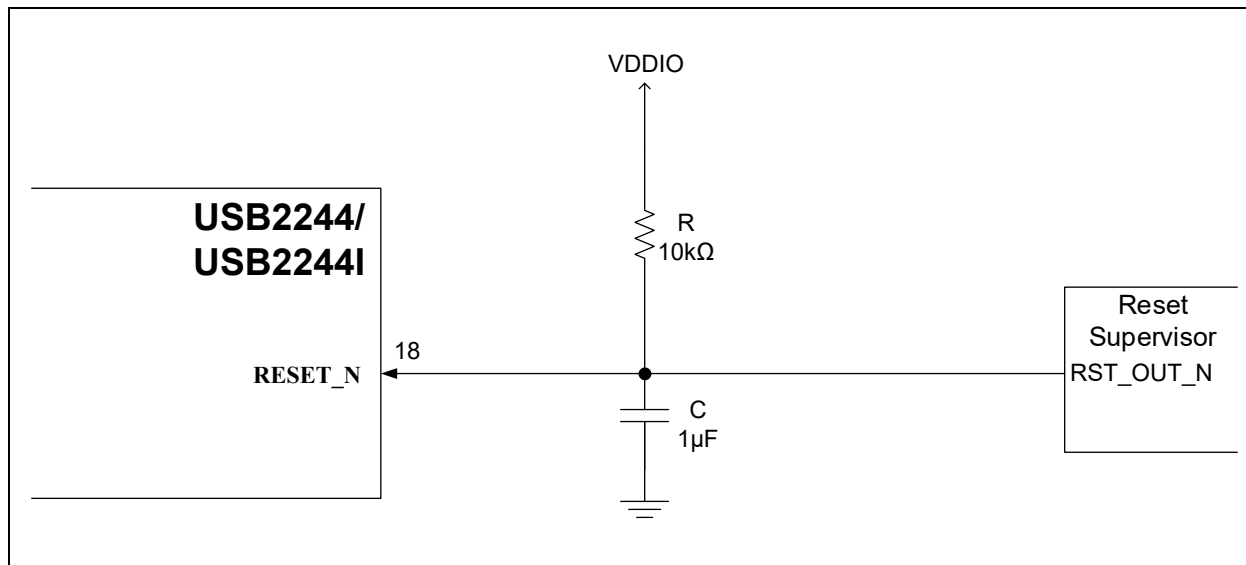
FIGURE 7-1: RESET TRIGGERED BY POWER SUPPLY



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Figure 7-2 details the recommended reset circuit for applications where reset is driven by an external CPU/MCU. The reset out pin (**RST_OUT_N**) from the CPU/MCU provides the warm reset after power-up. The values for the “R” resistor and “C” capacitor are not critical and may be adjusted per individual system needs or preferences.

FIGURE 7-2: RESET CIRCUIT INTERFACE WITH CPU/MCU RESET OUTPUT

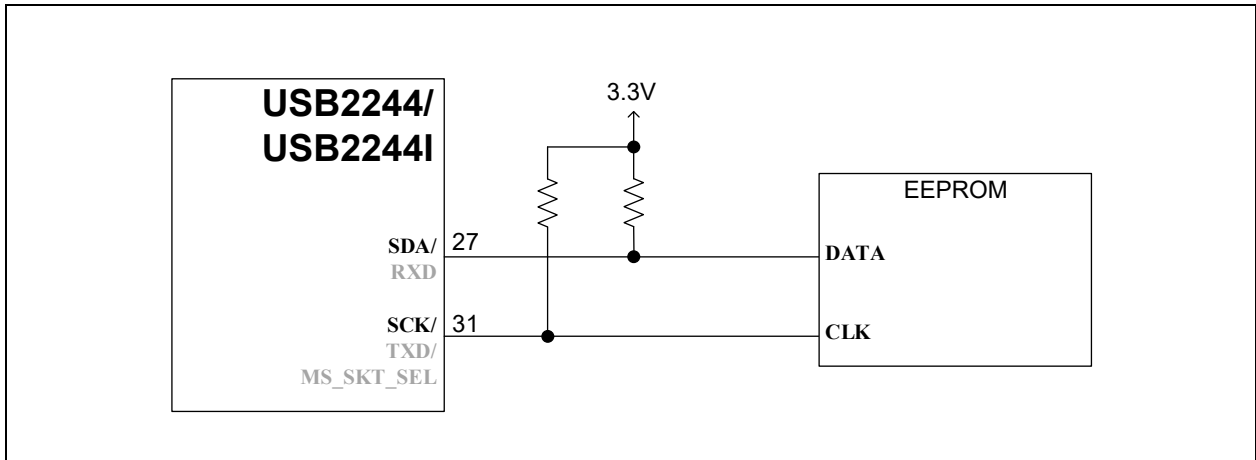


8.0 CONFIGURATION OPTIONS

The USB2244/USB2244I can be configured via an external I²C 512 byte (512x8) EEPROM memory device to allow for customizable vendor, product, and device IDs, serial number, product string descriptors, and so on.

An external EEPROM is not required for USB2244/USB2244I operation—internal defaults may be used for many applications. If the external EEPROM is not detected upon boot, internal defaults will be loaded.

FIGURE 8-1: EEPROM CONNECTIONS



9.0 HARDWARE CHECKLIST SUMMARY

TABLE 9-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	✓	Notes
Section 2.0, "General Considerations"	Section 2.1, "Pin Check"	Verify that the pins match the data sheet.		
	Section 2.2, "Ground"	Verify that the grounds are tied together.		
	Section 2.3, "USB-IF-Compliant USB Connector"	If present, verify that a USB-IF-compliant USB connector with an assigned TID is used in the design (if USB compliance is required for the design).		
Section 3.0, "Power"	Section 3.0, "Power"	- Ensure VDD33/VDDA33 is in the range 3.0V to 3.6V, 0.1 μF capacitors are connected to pins 6, 14, 22, and 36. - Ensure VDD18 (pin 13) has a 1.0 μF capacitor to GND. - Ensure VDD18PLL (pin 34) has a 1.0 μF capacitor to GND.		
Section 4.0, "USB Signals"	Section 4.1, "USB PHY Interface"	Verify that the USB data pins are correctly routed to the USB connectors. Pay special attention to the polarity of the USB2.0 D+ and D– data lines.		
	Section 4.2, "USB Protection"	Verify that ESD/EMI protection devices are designed specifically for high-speed data applications and that the combined parasitic capacitance of protection devices, USB traces, and USB connector do not exceed 5 pF on each USB trace.		
Section 5.0, "Card Reader Interface"	Section 5.1, "Secure Digital/MultiMediaCard™ Slot"	Verify that connections to a standard SD/MMC card slot, embedded eMMC memory, or microSD card slot are correct and refer to Figure 5-1 , Figure 5-2 , or Figure 5-3 .		
	Section 5.2, "Card Power Switch"	Verify that either CRD_PWR connects directly to the card media or card media slot supply power, or CRD_PWR enables an external supply switch if the internal card power switch is not used directly.		
Section 6.0, "Clock Circuit"	Section 6.1, "Crystal and External Clock Connection"	Confirm the crystal or clock is 24.000 MHz ($\pm$350 ppm). If a single-ended clock is used, ensure it is connected to XTAL1 while leaving XTAL2 floating. If a crystal is used, ensure that the loading capacitors are appropriately sized for the crystal loading requirement.		

TABLE 9-1: **HARDWARE DESIGN CHECKLIST (CONTINUED)**

Section	Check	Explanation	√	Notes
Section 7.0, "Power and Startup"	Section 7.1, "RBIAS Resistor"	Confirm that a 12.0 kΩ 1% resistor is connected between the RBIAS pin and PCB ground.		
	Section 7.2, "Board Power Supplies"	Verify that the board power supplies deliver 3.0V-3.6V to the hub power rails, and that the power-on rise time meets the requirement of the hub as defined in the data sheet. If the rise time requirement cannot be met, ensure that the RESET_N line is held low until the power regulators reach a steady state.		
	Section 7.3, "Reset Circuit"	Ensure that the RESET_N signal has an external pull-up resistor, or is otherwise properly controlled by an external SOC, MCU, or Reset supervisor device.		
Section 8.0, "Configuration Options"	Section 8.0, "Configuration Options"	Ensure that if an EEPROM device is used, it is connected properly and external pull-resistors to 3.3V are in place.		

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APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004319A (01-24-22)	Initial release	

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