# ENT-AN1276

# Application Note

# VSC8489 Device Family Bring-up and Troubleshooting

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# Contents

# 1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 1.0

Revision 1.0 was published in September 2018. It was the first publication of this document.

# 2 Bring-up and Troubleshooting

Use this information to bring up boards containing devices within the VSC8489 family (that also includes the VSC8490 and VSC8491), starting with the following checks.

- Check that the different power supplies have the correct voltage
- Check the frequency, amplitude, and jitter for the reference clocks
- Confirm that the input control pin states are stable and accurate (especially the MODE[1:0] pins)
- Confirm that the hardware reset duration is correct and that it occurs after the power supplies and reference clock inputs are stable

There are two amplitude settings for the clock inputs and each one requires a different register setting. After checking that the register accesses are correct, check line-side register 1Ex8208 (L_PLL5G_CFG4A) and host-side register 1Ex 8108 (H_PLL5G_CFG4A). Set bit 9 of both registers to 0 to select a larger reference clock swing input (from 1100 mV to 2400 mV) and set it to 1 to select a smaller swing input (from 200 mV to 1200 mV).

## 2.1 Register Access

Registers are accessible with a loosely defined clock frequency, and it is generally acceptable to configure the reference clock input amplitude register even if the starting register value and the actual clock input amplitude do not match.

Both 16-bit and 32-bit registers are accessed in the same way when using 32-bit SPI. However, if MDIO is used to access the registers, accessing 32-bit registers requires a specific sequence of 16-bit operations. In the case of a read operation, the MDIO read-increment command must be used (see Register Access Sequence).

To accommodate access to the 32-bit registers through 32-bit SPI and 16-bit MDIO, the addresses for the 32-bit registers are different when using SPI and MDIO. The API manages the differences if the management bus is ported correctly.

The global device 0x1E registers can only be accessed through the physical port 0 of the PHY. Read the chip ID through 1Ex0000, which should return 0x8489/0x8490/8491, depending on the PHY used. The version of the chip is then read back through 1Ex0001 to return the value 0x0000 for rev A/B and 0x0001 for rev C/D. To differentiate rev C and rev D die, please read the global_spare_cfg_stat.spare_rw1 register at 1Ex01d4. When the register= 1, it is revision D.

Use the registers listed in the following sections to check the status and I/O settings. The addresses given are for the 16-bit MDIO address scheme. If 32-bit SPI is used, addresses for some registers need to be adjusted.

Use the following access sequence under the given conditions for the listed registers.

**Table 1 • Register Access Sequence**

| 16-bit MDIO Read to 32-bit Register | 16-bit MDIO Write to 32-bit Register |
|---|---|
| Set up the lower 16-bit register address by MDIO ADDR | Set up the higher 16-bit register address by MDIO ADDR |
| Read the lower 16-bit register content by MDIO READ INC | Write the higher 16-bit register content by MDIO WRITE |
| The address for the higher 16-bit register will increment automatically after the read | Set up the lower 16-bit register address by MDIO ADDR |
| Read the higher 16-bit register content by regular MDIO READ | Write the lower 16-bit register content by MDIO WRITE |

## 2.2 PLL Lock Status

When the PHY is powered up but does not pass traffic, use the following checks to ensure the different PLLs are up and running.

**Table 2 • PLL Status Check**

| PLL | Check |
|---|---|
| LineLCPLL | 1Ex8211.3:1 (6= locked, all others= unlocked) |
| HostLCPLL | 1Ex810E.3:1 (6= locked, all others= unlocked) |
| Host Rx RCPLL (per channel) | 4xE634 is for channel 0. 4xE63B, 4xE642, and 4xE649 are for channel 1, 2, and 3, respectively.<br><br>Bit 12: Calibration. 0= Not complete, 1= Complete.<br><br>Bit 11: Calibration result. 0= Good, 1= Error.<br><br>Bit 10: PLL range. 0= Good, 1= Error.<br><br>A properly configured lane should read back bits 15:08 as 0x10. |
| Line Rx RCPLL (per channel) | 1xF268.3:0 being 0xd means locked, all others mean unlocked.<br><br>For 32-bit SPI, 1xF134.3:0 |
| Line Tx RCPLL (per channel) | 1xF2C8.3:0 (13= locked, all others= unlocked).<br><br>For 32-bit SPI, 1xF164.3:0 |

When the PLLs are functional, program the RXCLKOUT or TXCLKOUT to generate a line rate/64 clock (161 MHz) and use a scope to measure if the frequency is correct.

**Table 3 • PLL Accuracy Check**

| RXCLKOUT | TXCLKOUT |
|---|---|
| Set 1xA000 to 0x0009 to generate a recovered clock from 10G data input in 161 MHz | Set 1xA001 to 0x000b to generate a recovered clock from 10G data input in 161 MHz |
| Set 1xA000 to 0x000b to generate a 161 MHz clock from the 10G Tx transmit clock, which is based on the internal PLL derived from the XREFCLK input | Set 1xA000 to 0x0009 to generate a 161 MHz clock from the 10G Tx transmit clock, which is based on the internal PLL derived from the XREFCLK input |

## 2.3 General Status Settings

If the PLLs are working correctly but the link is still down or there are CRC errors registered in the link partner, check the following PCS block and XAUI block registers to determine if the problem is at the PMA side or the XAUI side.

### Table 4 • PCS Block Status for 10G Rx Input

| Value | Status |
|---|---|
| 3x0008 | Bit 11 indicates Tx fault and bit 10 indicates Rx fault.<br><br>These two bits are latched bits. In order to get the current status, they should be read twice as the first read will clear the residual value and the second read will provide the current value. When these bits are high, it means there is a fault.<br><br>This bit is affected by register 3xE600.<br><br>When 3xE600= 1, Rx fault depends on block lock (= 1) or high BER (= 1).<br><br>When 3xE600= 0, Rx fault depends on block lock= 1 only. |
| 3x0021 | Bit 15 indicates block lock.<br>Bit 14 indicates high BER is reported.<br>Bit 13:8 is the BER counter.<br>Bit 7:0 are counts for error blocks (read to clear). |
| 3x8010 | PCS_TX_Sequencing_Error_Count (read to clear) |
| 3x8011 | PCS_RX_Sequencing_Error_Count (read to clear) |
| 3x8012 | PCS_TX_Block_Encode_Error_Count (read to clear) |
| 3x8013 | PCS_RX_Block_Decode_Error_Count (read to clear) |
| 3x8014 | PCS_TX_Char_Encode_Error_Count (read to clear) |
| 3x8015 | PCS_RX_Char_Decode_Error_Count (read to clear) |

### Table 5 • XAUI Block Status for XAUI Input Data

| Value | Status |
|---|---|
| 4x0008 | Bit 11 indicates Tx fault, which most likely is caused by the XAUI input.<br><br>Bit 10 reflects similar information as in 3x0008.10 (latched bit, so read twice). |
| 4xF020 | Bit 12 indicates the current alignment status.<br><br>Bit 3:0 indicates the current sync status of lane 3, lane 2, lane 1, and lane 0, respectively. |
| 4xF021 | Bit 4 indicates the current link status.<br><br>Bit 3:0 indicates the current signal detection status of lane 3, lane 3, lane 1, and lane 0, respectively. |
| 4xF022 | This is a sticky register. Write 0xFFFF to clear the bits first.<br><br>Bit 15:12 indicates sticky bit for local fault status for lane 3–lane 0.<br><br>Bit 3:0 indicates change was detected on sync status change for lane 3–lane 0.<br><br>Other bit definitions are listed in the register descriptions that follow. |
| 4xF023 | This is a sticky register. Write 0xFFFF to clear the bits first.<br><br>Bit 4 indicates sticky bit for alignment lost for lane 3–lane 0.<br><br>Bit 3:0 indicates change was detected on sync lost status for lane 3–lane 0.<br><br>Other bit definitions are listed in register descriptions that follow. |
| 4xF026 | This register is read if 4xF023 bit 6 is 1 because this register being 1 means remote fault and 0 means local fault. |
| 4xF042 | In normal mode, Rx FIFO overflow error counter for the rate adaptation FIFO from 10G recovered clock domain to local XAUI Tx clock domain. |
| 4xF043 | In normal mode, Rx FIFO underflow error counter for the rate adaptation FIFO from 10G recovered clock domain to local XAUI Tx clock domain. |

If the problem is on the line-side PMA input, check the APC at the 10G input data path and the KR output (d_filter register) settings that control the 10G Tx output.

### 2.3.1 10G I/O Settings per Channel

Adjust the KR output setting to compensate for line-side output channel loss on the PCB. The error detection is assumed at the link partner Rx status. So, by adjusting the KR output of the local VSC8489 family PHY, the link partner Rx status should be monitored to see if the CRC error count drops down to zero.

Attached is the spreadsheet for converting C-1, C0, and C+1 into a hex value put into the d-filter register controlling the 10G output. The address of the KR output setting (d_filter register) is at 1xF225/1xF224 (bit 23:0) [1xF112 for SPI 32-bit address].

### 2.3.2 Line-Side 10G Input Registers for APC

Use the following tips to troubleshoot line-side 10G issues.

- If 1xF001.19:16 is not at 0x8 and 1xF001.2:0 is not at 0x2, then the APC is not initialized properly. Either the input reference clock is bad or there is some register programming issue (such as the wait state not implementing correctly) that results in insufficient wait. Check the PLL status to make sure the PLLs are locked.
- If there is no block lock or lots of block errors and bit errors, it could be a signal integrity issue and the APC parameters need to be checked thoroughly. Also, check if the Rx_LOS is asserted. If any of the APC parameters do not seem correct, try resetting the APC by toggling 1xF001.11 (32-bit SPI address—MDIO address is 1xF002 bit 11) from 0x0 to 0x1 and back to 0x0 while 1xF001.10= 0 and 1xF001.9= 1.
- If there is no block lock at all, the link might be physically broken. Again, also check the Rx_LOS from the optical transceiver.
- If there is block lock but lots of block errors only (that is, 3x0021 being 0x80FF), the link connection should be fine but the link partner is sending out traffic with error blocks. Check the link partner.
- If APC parameters are not in a good range and stay the same after executing APC_reset, there could be a cable problem or layout issue.
- If APC parameters are in a good range but still have BER error or block lock issues, check if the polarity of the signal is inverted.

**Table 6 • Line-Side 10G Input Registers**

| Control | Setting |
|---|---|
| Common config register | 1xF003/1xF002 (bit 19:16 is expected to be 0x8, bit 11 to be 0, and 2:0 to be 2).<br>[1xF001 for SPI 32-bit address] |
| L of input equalizer | 1xF031/1xF030 (bit 25:16 is expected to have a ratio AGC:L:C to be 8:2:1 if media_type_SC is not used).<br>[1xF016 for SPI 32-bit address] |
| Offset of input equalizer | 1xF025/1xF024 (bit 25:16 is expected to be around 0x200).<br>[1xF010 for SPI 32-bit address] |
| C of input equalizer | 1xF02B/1xF02A (bit 25:16 is expected to have a ratio AGC:L:C to be 8:2:1 if media_type_SC is not used).<br>[1xF013 for SPI 32-bit address] |
| AGC of input equalizer | 1xF037/1xF036 (bit 25:16 is expected to have a ratio AGC:L:C to be 8:2:1 if media _type_SC is not used).<br>[1xF019 for SPI 32-bit address] |
| Gain of input equalizer | 1xF019/1xF018 (bit 15:6—the actual gain is expected to be less than 0x2xx; bit 5:0 level detect set).<br>[1xF00C for SPI 32-bit address] |
| DFE1 of input equalizer | 1xF03D/1xF03C (bit 25:16 is expected to be around 0x40).<br>[1xF01E for SPI 32-bit address] |

| Control | Setting |
|---|---|
| DFE2 of input equalizer | 1xF043/1xF042 (bit 25:16 is expected to be around 0x20). [1xF021 for SPI 32-bit address] |
| DFE3 of input equalizer | 1xF049/1xF048 (bit 25:16 is expected to be around 0x10). [1xF024 for SPI 32-bit address] |
| DFE4 of input equalizer | 1xF04F/1xF04E (bit 25:16 is expected to be around 0x10). [1xF027 for SPI 32-bit address] |

### 2.3.3 XAUI/RXAUI I/O Settings Per Channel

Use the following tips to troubleshoot XAUI/RXAUI I/O settings issues.

- If no amplitude signal is detected when 4xF021 is read back, there might not be signals coming from the MAC chip to the PHY.
- If there is no sync or no link but amplitude is detected when 4xF020 and 4xF021 are read back, there might be a signal integrity issue and the registers for the host PLL at 4xE634, 4xE63B, 4xE642, and 4xE649 should be checked. The polarity of the signal should be checked. The status of the high-pass gain, mid-pass gain, low-pass gain, and offset should be checked.
- Adjust the 4xE61A.9:8 among 00, 01, 10, 11 to see if there is any improvement on bit error rate. The preset 0x0 for bit 9:8 is for regular trace length (within ~24" FR4 material). A higher value could be used for longer trace length.
- If there is sync and link up but traffic cannot be passed through, then check if local fault or remote fault is received by checking the fault status at 4xF023 bit 6 is 1. If there is a fault, then read 4xF026 to see if it is 0x1 (remote fault) or 0x0 (local fault).
- Check the FIFO overflow/underflow at 4xF042/4xF043.
- If the error is seen at the MAC chip's Rx input, then try to adjust the pre-cursor, post-cursor, amplitude, slew rate, and so on of the XAUI/RXAUI output buffer to see if the bit error registered at MAC chip's Rx input is eliminated.

The host input buffer calibrated parameter status values should fall between the minimum and maximum values configured through the following registers.

**Table 7 • Input Buffer Min/Max Values**

| | High-Pass Gain | Mid-Pass Gain | Low-Pass Gain | Offset |
|---|---|---|---|---|
| **Min.** | 4xE623.13:8 | 4xE623.5:0 | 4xE624.13:8 | 4xE623.5:0 |
| **Max.** | 4xE621.13:8 | 4xE621.5:0 | 4xE622.13:8 | 4xE622.5:0 |

4xE61A.9:8 sets the pattern detection for offset. In general, 0 is good for all lengths (particularly for short trace). If longer trace is needed, set it to 2.

**Table 8 • Host Input Buffer Calibrated Parameter Status**

| Calibration | Input Buffer High-Pass Gain | Input Buffer Mid-Pass Gain | Input Buffer Low-Pass Gain | Input Buffer Offset |
|---|---|---|---|---|
| 4xE630.8= 1 Lane 0 | 4xE631.13:8 | 4xE631.5:0 | 4xE632.13:8 | 4xE632.5:0 |
| 4xE637.8= 1 Lane 1 | 4xE638.13:8 | 4xE638.5:0 | 4xE639.13:8 | 4xE639.5:0 |
| 4xE63E.8= 1 Lane 2 | 4xE63F.13:8 | 4xE63F.5:0 | 4xE640.13:8 | 4xE640.5:0 |
| 4xE645.8= 1 Lane 3 | 4xE646.13:8 | 4xE646.5:0 | 4xE647.13:8 | 4xE647.5:0 |

**Table 9 • Host Output Buffer Calibrated Parameter Status**

| Setting | Description |
|---|---|
| 4xE625.15= 1 | Squelch the XAUI/RXAUI outputs on all four lanes |
| 4xE625.13= 1 | Invert the XAUI/RXAUI outputs' polarity on all four lanes |
| 4xE625.12:7 | Pre-cursor |
| 4xE625.6:2 | Post-cursor |
| 4xE626.15:11 | Second post-cursor |
| 4xE626.8= 0 | Slew rate <60 ps |
| 4xE626.8= 1 | Slew rate >60 ps |
| 4xE626.7:4 | If 4xE626.8= 0: fine adjustment of slew with 30 ps to 60 ps<br>If 4xE626.8= 1, 60 ps to 140 ps |
| 4xE627.5:0 | Defines the XAUI/RXAUI output amplitude (with 0 being lowest and 63 being highest) |

## 2.3.4 1G Debugging

**Table 10 • 1G Host-Side Debugging**

| Register | Description |
|---|---|
| 3xE002 | Bit 8: 1= Signal detection enable<br>Bit 4: 1= Signal-detect pin is used to determine if a signal is detected |
| 3xE003 | Bit 0: 1= Auto-negotiation enabled<br>Auto-negotiation should be disabled for host side. |
| 3xE00D | Bit 8: Signal detect<br>Bit 4: Link status<br>Bit 0: Sync status<br>**Note:** For a good link, these three bits should all be 1. |

**Table 11 • 1G Line-Side Debugging**

| Register | Description |
|---|---|
| 3xE102 | Bit 8: 1= Signal detection enable<br>Bit 4: 1= Signal-detect pin is used to determine if a signal is detected |
| 3xE103 | Bit 0: 1= Auto-negotiation enabled |
| 3xE104 | Bit 5:4 has to be set to 0x2 if auto-negotiation is enabled.<br>For debugging simplicity, disable auto-negotiation at the PHY and at the module. When it works with autoneg, then try to add back the autoneg and retest. |
| 3xE10D | Bit 8: Signal detect<br>Bit 4: Link status<br>Bit 0: Sync status<br>**Note:** For a good link, these three bits should all be 1. |

## 2.4 Related Registers

The following tables list the related registers.

### 2.4.1 10G Line Side

Read this register twice to get the latest status.

**Table 12 • 3x0008.11:10**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 11 | Transmit_fault | R/O | This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read.<br><br>0: No fault condition on transmit path<br>1: Fault condition on transmit path | 0x0 |
| 10 | Receive_fault | R/O | This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read.<br><br>0: No fault condition on receive path<br>1: Fault condition on receive path | 0x0 |

**Table 13 • 3x0020**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 12 | is_10GBASE_R_receive_lock_status | R/O | 0: 10GBASE-R PCS receive link down BLOCK_LOCK (3x0020.0)= 0 or BER_HI (3x0020.1)= 1<br>1: 10GBASE-R PCS receive link up BLOCK_LOCK (3x0020.0)= 1 and BER_HI (3x0020.1)= 0 | 0x0 |
| 1 | is_10GBASE_R_PCS_high_BER | R/O | 0: 10GBASE-R PCS not reporting a high BER<br>1: 10GBASE-R PCS reporting a high BER | 0x0 |
| 0 | is_10GBASE_R_PCS_block_lock | R/O | 0: 10GBASE-R PCS is not locked to receive blocks<br>1: 10GBASE-R PCS is locked to receive blocks | 0x0 |

**Table 14 • 3x0021**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15 | BLOCK_LOCK | R/O | This is a sticky bit that latches the low state. The latch-low bit is cleared when the register is read.<br><br>0: 10GBASE-R PCS does not have block lock<br>1: 10GBASE-R PCS has block lock | 0x1 |
| 14 | PCS_HIGHBER | R/O | This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read.<br><br>0: 10GBASE-R PCS has not reported a high BER<br>1: 10GBASE-R PCS has reported a high BER | 0x0 |
| 13:8 | BER | R/O | BER counter. The counter saturates when the maximum value is exceeded. The counter is cleared when the register is read. | 0x00 |
| 7:0 | PCS_ERRORED_BLOCKS | R/O | Errored blocks counter. The counter saturates when the maximum value is exceeded. The counter is cleared when the register is read. | 0x00 |

### 2.4.2 1G Line Side

**Table 15 • 3xE100**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 4 | LINK_STATUS_TYPE | R/W | Set type of link_status indication at CPU system.<br>0: Sync_status (from PCS synchronization state machine)<br>1: Bit 15 of PCS1G_ANEG_STATUS.lp_adv_ability (Link up/down) | 0x0 |
| 1 | Reserved | R/W | Factory use | 0x0 |
| 0 | PCS_ENA | R/W | PCS enable.<br>0: Disable PCS<br>1: Enable PCS | 0x0 |

**Table 16 • 3xE101**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 4 | UNIDIR_MODE_ENA | R/W | Unidirectional mode enable.<br><br>Implementation of 802.3, Clause 66. When asserted, this enables MAC to transmit data independent of the state of the receive link.<br>0: Unidirectional mode disabled<br>1: Unidirectional mode enabled | 0x0 |
| 0 | SGMII_MODE_ENA | R/w | Selection of PCS operation.<br>0: PCS is used in SerDes mode<br>1: PCS is used in SGMII mode. Configuration bit PCS1G_ANEG_CFG.SW_RESOLVE_ENA must be set additionally. | 0x1 |

**Table 17 • 3xE102**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 8 | SD_SEL | R/W | Signal-detect selection (select input for internal signal_detect line).<br><br>0: Select signal_detect line from hard macro<br>1: Select external signal_detect line | 0x0 |
| 4 | SD_POL | R/W | Signal-detect polarity.<br><br>The signal level on signal_detect input pin must be equal to SD_POL to indicate signal detection (SD_ENA must be set)<br><br>0: The signal-detect input pin must be "0" to indicate a signal detection<br>1: The signal-detect input pin must be "1" to indicate a signal detection | 0x1 |
| 0 | SD_ENA | R/W | Signal-detect enable.<br><br>0: The signal-detect input pin is ignored. The PCS assumes an active signal detect at all times.<br>1: The signal-detect input pin is used to determine if a signal is detected | 0x1 |

### Table 18 • 3xE103

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 8 | SW_RESOLVE_ENA | R/W | Software resolve abilities.<br><br>0: If auto-negotiation fails (no matching HD or FD capabilities), the link is disabled<br>1: The result of an auto-negotiation is ignored (the link can be set up through software). This bit must be set in SGMII mode. | 0x0 |
| 1 | ANEG_RESTART_ONE_SHOT | One-shot | Auto-negotiation restart.<br><br>0: No action<br>1: Restart auto-negotiation | 0x0 |
| 0 | ANEG_ENA | R/W | Auto-negotiation enable.<br><br>0: Auto-negotiation disabled<br>1: Auto-negotiation enabled | 0x0 |

### Table 19 • 3xE104

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | ADV_ABILITY | R/W | Advertised ability register.<br><br>Holds the capabilities of the device as described IEEE 802.3, Clause 37.<br><br>If SGMII mode is selected (PCS1G_MODE_CFG.SGMII_MODE_ENA= 1), SW_RESOLVE_ENA must be set. | 0x0000 |

### Table 20 • 3xE10D

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 8 | SIGNAL_DETECT | R/O | Indicates whether or not the selected signal detect input line is asserted.<br><br>0: No signal detected<br>1: Signal detected | 0x0 |
| 4 | LINK_STATUS | R/O | Indicates whether the link is up or down (a link is up when ANEG state machine is in state LINK_OK or AN_DISABLE_LINK_OK).<br><br>0: Link down<br>1: Link up | 0x0 |
| 0 | SYNC_STATUS | R/O | Indicates if PCS has successfully synchronized.<br><br>0: PCS is out of sync<br>1: PCS has synchronized | 0x0 |

### Table 21 • 3xE10E

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 7:0 | LINK_DOWN_CNT | R/W | Link down counter.<br><br>A counter that counts the number of times a link has been down. The counter does not saturate at 255 and is only cleared when writing 0 to the register. | 0x00 |

**Table 22 • 3xE00F**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 4 | LINK_DOWN_STICKY | Sticky | The sticky bit is set when the link has been down (that is, if the ANEG state machine has not been in the AN_DISABLE_LINK_OK or LINK_OK state for one or more clock cycles). This occurs if, for example, ANEG is restarted or if signal-detect or synchronization has been lost for more than 10 ms (1.6 ms in SGMII mode).<br><br>0: Link is up<br>1: Link has been down<br><br>Bit is cleared by writing a 1 to this position. | 0x0 |
| 0 | OUT_OF_SYNC_STICKY | Sticky | Sticky bit indicating if PCS synchronization has been lost.<br><br>0: Synchronization has not been lost at any time<br>1: Synchronization has been lost for one or more clock cycles<br><br>Bit is cleared by writing a 1 to this position. | 0x0 |

## 2.4.3 10G Host Side

**Table 23 • 4xF020**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 12 | ALIGNMENT_STATUS | R/O | Status of lane alignment.<br><br>0= No alignment reached<br>1= All lanes are aligned | 0x0 |
| 3:0 | SYNC_STATUS | R/O | Status of code group alignment (lane independent), one bit for each lane.<br><br>The order of the bits is:<br><lane_3><lane_2><lane_1><lane_0>.<br><br>1111: All lanes in sync<br>0001: Lane 0 is in sync<br>... | 0x0 |

**Table 24 • 4xF021**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 4 | LINK_STATE | R/O | Status of the link.<br><br>0= Link is not in LINK_OK state<br>1= Link is in LINK_OK state | 0x0 |
| 3:0 | SIGNAL_DETECT | R/O | Current status of selected signal_detect input lines. For each lane, the bit will be "1" if a valid signal is detected.<br><br>The order of the bits is:<br><lane_3><lane_2><lane_1><lane_0>.<br><br>0= No valid signal detected<br>1= Valid signal detected | 0x0 |

**Table 25 • 4xF022**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:12 | LOCAL_FAULT_STICKY | Sticky | Local fault status (one or more sync/align/fifo_of /fifo_uf/8b10b error), one bit for each lane.<br><br>The order of the bits is:<br><lane_3><lane_2><lane_1><lane_0>.<br><br>1= A fault occurred<br>0= No fault detected<br><br>Bit is cleared by writing a 1 to this position. | 0x0 |
| 11 | RX_OSET_FIFO_FULL_STICKY | Sticky | Interrupt indicating that the ordered set FIFO is full.<br><br>0= Overhead FIFO not full<br>1= Overhead FIFO full | 0x0 |
| 10 | RX_OSET_STICKY | Sticky | Interrupt indicating that an ordered set was received and captured in the FIFO.<br><br>0= No ordered set captured<br>1= Ordered set captured in FIFO | 0x0 |
| 9 | LINK_CHANGE_STICKY | Sticky | This bit is asserted when the PCS enters or leaves the LINK_OK state.<br><br>0= No change<br>1= Link has changed into or out of the LINK_OK state | 0x0 |
| 8 | ALIGNMENT_CHANGE_STICKY | Sticky | A change was detected in ALIGNMENT_STATUS.<br><br>0= No change<br>1= A change was detected (rising or falling) | 0x0 |
| 7:4 | SIGNAL_DETECT_CHANGE_STICKY | Sticky | A change was detected in the SIGNAL_DETECT status.<br><br>One bit per lane:<br><lane_3><lane_2><lane_1><lane_0>.<br><br>0= No change<br>1= A change was detected (rising or falling) | 0x0 |
| 3:0 | SYNC_CHANGE_STICKY | Sticky | A change was detected in SYNC_STATUS.<br><br>One bit is asserted per lane:<br><lane_3><lane_2><lane_1><lane_0>.<br><br>0= No change<br>1= A change was detected (rising or falling) | 0x0 |

Write 0xFFFF and read it back. Expect it to be 0x0, meaning no sticky bit interrupts.

**Table 26 • 4xF023**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 9 | RX_FSET_FIFO_FULL_STICKY | Sticky | Interrupt indicating that the signal ordered set FIFO is full.<br><br>0= Overhead FIFO not full<br>1= Overhead FIFO full | 0x0 |

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 8 | RX_FSET_STICKY | Sticky | Interrupt indicating that an signal ordered set was received and captured in the FIFO.<br><br>0= No signal ordered set captured<br>1= Signal ordered set captured in FIFO | 0x0 |
| 7 | RX_FSIG_CHANGED_STICKY | Sticky | Received \|\|Fsig\|\| code changed.<br><br>1= New \|\|Fsig\|\| has been received<br>0= No new \|\|Fsig\|\| since last read<br><br>Bit is cleared by writing a 1 to this position. | 0x0 |
| 6 | RX_Q_CHANGED_STICKY | Sticky | Received \|\|Q\|\| code changed.<br><br>1= New \|\|Q\|\| has been received<br>0= No new \|\|Q\|\| since last read<br><br>Bit is cleared by writing a 1 to this position. | 0x0 |
| 5 | C8B10B_ERR_STICKY | Sticky | Coding error detected in received 8B/10B encoded data.<br><br>0= No error found<br>1= Coding error detected<br><br>Bit is cleared by writing a 1 to this position. | 0x0 |
| 4 | ALIGNMENT_LOST_STICKY | Sticky | Alignment lost in de-skew logic.<br><br>0= No misalignment occurred<br>1= A (temporary) misalignment has been detected<br><br>Bit is cleared by writing a 1 to this position. | 0x0 |
| 3:0 | SYNC_LOST_STICKY | Sticky | Synchronization lost in lane *i* (i= 0...3, one bit per lane).<br><br>The order of the bits is:<br><lane_3><lane_2><lane_1><lane_0>.<br><br>0= No sync lost occurred<br>1= Synchronization lost in lane *i* (temporarily)<br><br>Bit is cleared by writing a 1 to this position. | 0x0 |

Write 0xFFFF and read it back. Expect it to be 0x0, meaning no sticky bit interrupts.

### Table 27 • 4xF026

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | RX_Q | R/O | Received \|\|Q\|\| code (sequence information, that is, the lower 24 bits of a sequence) | 0x0000 |

### Table 28 • 4xF042

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | ERR_CNT_FIFO_OF_L0 | R/W | Number of detected FIFO overflow errors/number of errors in lane 0.<br><br>This counter will saturate at 0xffff. | 0x0000 |

### Table 29 • 4xF043

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | ERR_CNT_FIFO_UF_L1 | R/W | Number of detected FIFO underflow errors/number of errors in lane 1.<br><br>This counter will saturate at 0xffff. | 0x0000 |

### Table 30 • 4xE625 XAUI/RXAUI Output CFG0

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15 | OB_IDLE | R/W | 1: Force to 0 V differential<br>0: Normal mode | 0x0 |
| 14 | Reserved | R/W | Factory use | 0x1 |
| 13 | OB_POL | R/W | Polarity of output signal.<br><br>0: Normal<br>1: Inverted | 0x1 |
| 12:7 | OB_POST0 | R/W | Coefficients for first post-cursor (MSB is sign) | 0x00 |
| 6:2 | OB_PREC | R/W | Coefficients for pre-cursor (MSB is sign) | 0x00 |
| 1 | Reserved | R/W | Factory use | 0x0 |
| 0 | Reserved | R/W | Factory use | 0x0 |

### Table 31 • 4xE626 XAUI/RXAUI Output CFG1

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:11 | OB_POST1 | R/W | Coefficients for second post-cursor (MSB is sign) | 0x00 |
| 10 | Reserved | R/W | Factory use | 0x0 |
| 9 | Reserved | R/W | Factory use | 0x0 |
| 8 | OB_SR_H | R/W | Half the pre-driver speed, use for slew rate control.<br><br>0: Disable—slew rate < 60 ps<br>1: Enable—slew rate > 60 ps | 0x1 |
| 7:4 | OB_SR | R/W | Driver speed, fine adjustment of slew rate.<br><br>If OB_SR_H= 0: 30 ps–60 ps<br>If OB_SR_H= 1: 60 ps–140 ps | 0x7 |
| 3:0 | Reserved | R/W | Factory use | 0x1 |

### Table 32 • 4xE627 XAUI/RXAUI Output CFG2

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 8:6 | OB_ENA_CAS | R/W | Output skew, used for skew adjustment in SGMII mode | 0x1 |
| 5:0 | OB_LEV | R/W | Level of output amplitude.<br><br>0: Lowest level<br>63: Highest level | 0x30 |

### 2.4.4 1G Host Side

**Table 33 • 3xE000**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 4 | LINK_STATUS_TYPE | R/W | Set type of link_status indication at CPU system.<br>0: Sync_status (from PCS synchronization state machine)<br>1: Bit 15 of PCS1G_ANEG_STATUS.lp_adv_ability (link up/down) | 0x0 |
| 1 | Reserved | R/W | Factory use | 0x0 |
| 0 | PCS_ENA | R/W | PCS enable.<br>0: Disable PCS<br>1: Enable PCS | 0x0 |

**Table 34 • 3xE001**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 4 | UNIDIR_MODE_ENA | R/W | Unidirectional mode enable.<br><br>Implementation of 802.3, Clause 66. When asserted, this enables the MAC to transmit data independent of the state of the receive link.<br>0: Unidirectional mode disabled<br>1: Unidirectional mode enabled | 0x0 |
| 0 | SGMII_MODE_ENA | R/W | Selection of PCS operation.<br>0: PCS is used in SerDes mode<br>1: PCS is used in SGMII mode. Configuration bit PCS1G_ANEG_CFG.SW_RESOLVE_ENA must be set additionally. | 0x1 |

**Table 35 • 3xE002**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 8 | SD_SEL | R/W | Signal detect selection (select input for internal signal_detect line).<br><br>0: Select signal_detect line from hard macro<br>1: Select external signal_detect line | 0x0 |
| 4 | SD_POL | R/W | Signal detect polarity.<br><br>The signal level on signal_detect input pin must be equal to SD_POL to indicate signal detection (SD_ENA must be set).<br><br>0: Signal detect input pin must be "0" to indicate a signal detection<br>1: Signal detect input pin must be "1" to indicate a signal detection | 0x1 |
| 0 | SD_ENA | R/W | Signal detect enable.<br><br>0: The signal detect input pin is ignored (the PCS assumes an active signal detect at all times)<br>1: The signal detect input pin is used to determine if a signal is detected | 0x1 |

### Table 36 • 3xE003

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 8 | SW_RESOLVE_ENA | R/W | Software resolve abilities.<br><br>0: If auto-negotiation fails (no matching HD or FD capabilities), the link is disabled<br>1: The result of an auto-negotiation is ignored (the link can be set up through software)<br><br>This bit must be set in SGMII mode. | 0x0 |
| 1 | ANEG_RESTART_ONE_SHOT | One-shot | Auto-negotiation restart.<br><br>0: No action<br>1: Restart auto-negotiation | 0x0 |
| 0 | ANEG_ENA | R/W | Auto-negotiation enable.<br><br>0: Auto-negotiation disabled<br>1: Auto-negotiation enabled | 0x0 |

### Table 37 • 3xE00D

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 8 | SIGNAL_DETECT | R/O | Indicates whether or not the selected signal detect input line is asserted.<br><br>0: No signal detected<br>1: Signal detected | 0x0 |
| 4 | LINK_STATUS | R/O | Indicates whether the link is up or down. A link is up when ANEG state machine is in state LINK_OK or AN_DISABLE_LINK_OK.<br><br>0: Link down<br>1: Link up | 0x0 |
| 0 | SYNC_STATUS | R/O | Indicates if PCS has successfully synchronized.<br><br>0: PCS is out of sync<br>1: PCS has synchronized | 0x0 |

### Table 38 • 3xE00E

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 7:0 | LINK_DOWN_CNT | R/W | Link down counter.<br><br>A counter that counts the number of times a link has been down. The counter does not saturate at 255 and is only cleared when writing 0 to the register. | 0x00 |

**Table 39 • 3xE00F**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 4 | LINK_DOWN_STICKY | Sticky | The sticky bit is set when the link has been down (that is, if the ANEG state machine has not been in the AN_DISABLE_LINK_OK or LINK_OK state for one or more clock cycles). This occurs if, for example, ANEG is restarted or if signal-detect or synchronization has been lost for more than 10 ms (1.6 ms in SGMII mode).<br><br>0: Link is up<br>1: Link has been down<br><br>Bit is cleared by writing a 1 to this position. | 0x0 |
| 0 | OUT_OF_SYNC_STICKY | Sticky | Sticky bit indicating if PCS synchronization has been lost.<br><br>0: Synchronization has not been lost at any time<br>1: Synchronization has been lost for one or more clock cycles<br><br>Bit is cleared by writing a 1 to this position. | 0x0 |

### 2.4.5 Miscellaneous

The following table lists the host mode register information for operation mode.

**Table 40 • 4xE806.2:0**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 2:0 | OP_MODE | R/O | Current operation mode.<br><br>0: XAUI<br>1: RXAUI<br>2: SGMII on lane 0<br>3: SGMII on lane 3<br>4–7: Reserved | 0x0 |

The following table lists the sync control configuration register information.

**Table 41 • 1xB700**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 4 | CLR_SYNC_STAT | R/W | Clear sync control status register.<br><br>0: Idle<br>1: Clear | 0x0 |
| 1:0 | LANE_SYNC_SRC | R/W | Source selection for lane synchronization.<br><br>0: Select DES_0<br>1: Select DES_1<br>2: Select F to delta F<br>3: Synchronization disabled | 0x3 |

## 2.5 Tracing Faults

Debugging can sometimes be difficult because of the interactions between the local MAC/PHY and link partner MAC/PHY.

When the cable is unplugged, the local PHY will detect no data or just noise coming in at 10G Rx input. When this happens, the PHY will generate a local fault to the MAC chip at the host side. When host-side MAC receives a local fault, it will respond with a remote fault. If only the optical cable of Rx is unplugged but the Tx cable is still on, then this remote fault will be sent from the local PHY to the link partner's PHY, which will pass the frame to the link partner's MAC chip. When the link partner's MAC chip receives a remote fault, it will respond with IDLEs back to the PHY to the non-terminated cable.

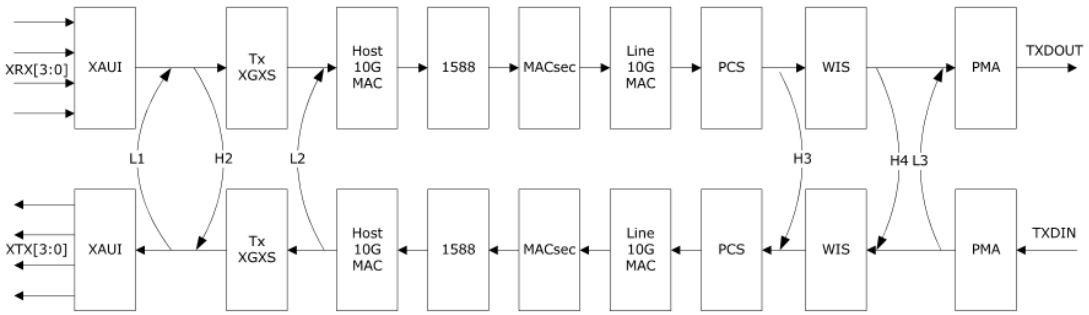
The described state remains until the Rx cable is re-plugged to the local PHY. When this happens, the local PHY passes the IDLE instead of a local fault to the local PHY at host side. The MAC chip at the host side will respond by removing the generation of the remote fault and start sending IDLE or traffic to the link partner. When these IDLEs or traffic reach the link partner MAC, the link partner MAC chip will respond with data packets and so the link will come up and pass traffic between the two sides.

In debugging, if faults are seen in both MAC chips, try to find out where the local fault originates. The readings in 4xF022/4xF023/4xF026 may be useful in determining the flow of local fault versus remote fault.

## 2.6 Loopbacks

Loopbacks are very useful in narrowing down the problematic area. There are three facility (line) loopbacks and three (host) equipment loopbacks.

**Figure 1 • Loopbacks**




### 2.6.1 Facility Loopbacks

Loopback L3 uses the recovered clock of the line-side Rx input to be the transmit clock for the line-side Tx output. The input and output data is totally synchronous and does not pass through the PCS block of the PHY.

It is enabled by the following steps if done by direct registers access. MDIO is used in this example.

1. WM_1E_01_A003_0001
2. WM_1E_01_B700_0000
3. WM_1E_01_F285_07C1
4. WM_1E_01_F284_3608
5. WM_1E_01_F2A1_1DDE
6. WM_1E_01_F2A0_0D07
7. WM_1E_01_F285_0FC1
8. WM_1E_01_F284_3608

[where WM is the write MDIO command, 1E is the port number, 01 is the device number, followed by the address offset, and the value to be written into the register.]

To disable loopback L3:

1. WM_1E_01_F2A1_1DDE
2. WM_1E_01_F2A0_0C07
3. WM_1E_01_B700_0003
4. WM_1E_01_A003_0000

Loopback L2 will have the line-side Rx input data pass through the PCS block and the rate adaptation FIFO, then loop back to the PCS block and out from the PHY to the link partner. The clock used for the transmit data at the line side is based on the internal high-speed clock synchronous to the XREFCLK.

- To enable loopback L2: WM_1E_04_EA20_0001
- To disable loopback L2: WM_1E_04_EA20_0000

Loopback L1 will have the line-side Rx input data to pass through the PCS block, the rate adaptation FIFO, the XGXS block (including 8b/10 endec), then loop back to the XGXS block to PCS block and out from the PHY to the link partner. The clock used for the transmit data at the line side is based on the internal high-speed clock synchronous to the XREFCLK.

- To enable loopback L1: WM_1E_03_E107_0001
- To disable loopback L3: WM_1E_04_E62A_0090

### 2.6.2 Equipment Loopbacks

Loopback H2 uses the recovered clock of the host-side Rx input to be the transmit clock for the host-side Tx output. The data of input and output is totally synchronous and the output data does not even go through the 8b/10 endec of the PHY.

- To enable loopback H2: WM_1E_04_E62A_0490
- To disable loopback H2: WM_1E_04_E62A_0090

Loopback H3 will have the host-side Rx input data pass through the rate adaptation FIFO and then PCS block, then loop back to the PCS block and out from the PHY to the MAC chip. The clock used for the transmit data at the host side is based on the internal high-speed clock synchronous to the XREFCLK.

- To enable loopback H3: WM_1E_03_0000_6040
- To disable loopback H3: WM_1E_03_0000_2040

Loopback H4 will have the host-side Rx input data pass through the rate adaptation FIFO, the PCS block, and the WIS block, then loop back to the WIS block, the PCS block, and out from the PHY to the MAC chip. The clock used for the transmit data at the host side is based on the internal high-speed clock synchronous to the XREFCLK.

- To enable loopback H4: WM_1E_02_0000_6040
- To disable loopback H4: WM_1E_02_0000_2040

**Note:** In this section, direct register access is used to set up the loopbacks. These loopbacks could be also be set up by API calls, which is recommended over direct register access unless direct register access is the only option in that particular debug stage (for example, if the API is not yet implemented successfully and there is an urgent need to get the hardware tested).

## 2.7 BIST

There are two types of BIST: packet BIST and non-packet BIST.

Packet BIST can pass through the PCS block, but non-packet BIST will fail the PCS block because there are no delimiter/frame boundaries in the non-packet pattern. As a result, the packet BIST traffic can be passed all the way to the MAC chip at the host side of either the local MAC chip or the link partner's host-side MAC chip.

Non-packet BIST is usually PRBSn pattern, but is not limited to such. For example, an 8b/10b coded pattern could be a non-packet BIST pattern. PRBS31 and PRBS9 patterns are usually used for PMA to PMA point-to-point connection signal integrity checks. At the host side for XAUI, RXAUI, or SGMII, a pattern of 8b/10b coded or PRBSn could also be used for a signal integrity check.

### 2.7.1 Packet BIST

This BIST engine resides in between the XGXS block and L2 loopback.

The following steps turn on the packet BIST generator.

1. Set 4xE903 to 0x0003 (set up the BIST generated packet size)
2. Set 4xE900 to 0x3001 (enable the BIST generator)
3. Set 4xEA20 to 0x0100 (set up the data path to use BIST generator facing the line side)

**Note:** To set up the data path to use the BIST generator facing the host side, set 4xEA20 for the VSC8489 family to 0x0080.

The following steps turn on the packet BIST checker.

1. Set 4xE940 to 0x0001 (enable the BIST checker)
2. Set 4xE950 to 0x001F (reset the counters)
3. Set 4xE901 to 0x0001 (update the read-back registers)

To read the counters, reset the counters at the beginning and then update the read-back registers before reading the following registers.

- 4xE960/4xE961 (Good CRC)
- 4xE970/4xE971 (Bad CRC)
- 4xE980/E981 (Fragments)
- 4xE990/E991 (Local Fault)

When using the BIST checker for the host side of revision A/B, enable loopback H3 (set 3x0000 from 0x2040 to 0x0640) or loopback H4 (set 2x0000 from 0x2040 to 0x6040) to route the data back to the BIST checker. For revision C/D, the setting of 4xEA21 to 0x0001 will also take care of this loopback.

#### 2.7.1.1 Registers

The following tables list the related register information.

##### 2.7.1.1.1 GEN_PKTLEN

**Table 42 • 4xE902**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 7:0 | PKTLEN | R/W | Packet length: packet bytes= header + pktlen*64 + (8-lenofs) | 0x17 |

##### 2.7.1.1.2 GEN_IPGLEN

**Table 43 • 4xE903**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | IPGLEN | R/W | IPG length: /I/ bytes= lenofs + ipglen*4 | 0x0001 |

##### 2.7.1.1.3 GEN_TIME

**Table 44 • 4xE904**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | PTPTIME | R/W | PTP timestamp to generate: [15:8] is seconds, [7:0] is ns | 0x0000 |

#### 2.7.1.1.4 GEN_ETYPE

**Table 45 • 4xE905**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | ETYPE | R/W | Etype field for standard frames | 0x0000 |

#### 2.7.1.1.5 GEN_SA0

**Table 46 • 4xE910**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | SA0 | R/W | Generated source address [15:0] | 0x0000 |

#### 2.7.1.1.6 GEN_SA1

**Table 47 • 4xE911**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | SA1 | R/W | Generated source address [31:16] | 0x0000 |

#### 2.7.1.1.7 GEN_SA2

**Table 48 • 4xE912**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | SA2 | R/W | Generated source address [47:32] | 0x0000 |

#### 2.7.1.1.8 GEN_DA0

**Table 49 • 4xE920**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | DA0 | R/W | Generated destination address [15:0] | 0x0000 |

#### 2.7.1.1.9 GEN_DA1

**Table 50 • 4xE921**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | DA1 | R/W | Generated destination address [31:16] | 0x0000 |

#### 2.7.1.1.10 GEN_DA2

**Table 51 • 4xE922**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | DA2 | R/W | Generated destination address [47:32] | 0x0000 |

#### 2.7.1.1.11 GEN_SENT_LSW

**Table 52 • 4xE930**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | SENT_LSW | R/O | LSW of number of packets generated | 0x0000 |

#### 2.7.1.1.12 GEN_SENT_MSW

**Table 53 • 4xE931**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | SENT_MSW | R/O | MSW of number of packets generated | 0x0000 |

#### 2.7.1.1.13 MON_CFG

**Table 54 • 4xE940**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 0 | ENABLE | R/W | Enable packet monitor.<br><br>0: Monitor is disabled<br>1: Monitor is enabled | 0x0 |

#### 2.7.1.1.14 MON_RST

**Table 55 • 4xE950**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 4 | BER_RST | One-shot | Reset BER counter.<br><br>0: Normal operation<br>1: Reset | 0x0 |
| 3 | LFAULT_RST | One-shot | Reset Local_Fault counter.<br><br>0: Normal operation<br>1: Reset | 0x0 |
| 2 | FRAG_RST | One-shot | Reset Packet_Fragment counter.<br><br>0: Normal operation<br>1: Reset | 0x0 |
| 1 | BAD_RST | One-shot | Reset Bad_CRC counter.<br><br>0: Normal operation<br>1: Reset | 0x0 |
| 0 | GOOD_REST | One-shot | Reset Good_CRC counter.<br><br>0: Normal operation<br>1: Reset | 0x0 |

#### 2.7.1.1.15 UPDATE

**Table 56 • 4xE901**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 0 | UPDATE | One-shot | Freeze all generator and monitor counters for read back | 0x0 |

#### 2.7.1.1.16 MON_GOOD_LSW

**Table 57 • 4xE960**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | GOOD_LSW | R/O | LSW of Good_CRC counter | 0x0000 |

#### 2.7.1.1.17 MON_BAD_LSW

**Table 58 • 4xE970**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | BAD_LSW | R/O | LSW of Bad_CRC counter | 0x0000 |

#### 2.7.1.1.18 MON_BAD_MSW

**Table 59 • 4xE971**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | BAD_MSW | R/O | MSW of Bad_CRC counter | 0x0000 |

#### 2.7.1.1.19 MON_FRAG_LSW

**Table 60 • 4xE980**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | FRAG_LSW | R/O | LSW of Packet_Fragment counter | 0x0000 |

#### 2.7.1.1.20 MON_FRAG_MSW

**Table 61 • 4xE980**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | FRAG_MSW | R/O | MSW of Packet_Fragment counter | 0x0000 |

#### 2.7.1.1.21 MON_LFAULT_LSW

**Table 62 • 4xE990**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | LFAULT_LSW | R/O | LSW of Local_Fault counter | 0x0000 |

#### 2.7.1.1.22 MON_LFAULT_MSW

**Table 63 • 4xE991**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | LFAULT_MSW | R/O | MSW of Local_Fault counter | 0x0000 |

#### 2.7.1.1.23 Datapath Control

**Table 64 • 4xEA20**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 8 | EGR_XGMII_PG_SEL | R/W | Selects source of data transmitted from PG_MUXA.<br><br>0: Data from client-side PCS1G (1G mode)/XGXS (10G mode)<br>1: Data from pattern generator | 0x0 |
| 7 | IGR_XGMII_PG_SEL | R/W | Selects source of data transmitted from PG_MUXB.<br><br>0: Data from PG_MUXC in the ingress data path<br>1: Data from pattern generator | 0x0 |

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 6 | IGR_XGMII_PG_SEL2 | R/W | Selects source of data transmitted from PG_MUXC.<br><br>0: Data is from the ingress data path<br>1: Data is from PG_MUXA in the egress data path | 0x0 |
| 0 | LOOP_L2_ENA | R/W | Line-side/network Loopback L2 enable.<br><br>0: Disabled<br>1: Enabled | 0x0 |

**Note:** EGR_XGMII_PG_SEL and IGR_XGMII_PG_SEL may not be set to 1 simultaneously.

#### 2.7.1.1.24 Datapath Control

**Table 65 • 4xEA21**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 0 | IGR_XGMII_PG_SEL2 | R/W | Selects source of data transmitted from PG_MUXC.<br><br>This mux is intended to be used to route data to the packet BIST monitor and may not be used as a host-side loopback (that is, XAUI /RXAUI data input looped back to XAUI/RXAUI data output).<br><br>0: Data from ingress data path<br>1: Data from PG_MUXA in the egress data path | 0x0 |

## 2.7.2 Non-Packet BIST

There are two PRBSn BIST engines facing the line interface: one is inside the PMA block and one is at the PCS block, as defined by IEEE 802.3ae. In addition, there is another non-packet BIST engine facing the host interface that can generate PRBSn patterns and 8b/10b coded patterns.

### 2.7.2.1 PRBSn at PCS Block (Facing the Line Interface)

To enable this BIST generator, set 3x002A.4 to 1.

To enable this BIST checker, set 3x002A.5 to 1.

Check the 16-bit version error counter at 3x002B, which is read to clear.

Check the 32-bit version error counter at 3x8008/3x8007—3x8008 should be read first and then 3x8007, because reading 3x8007 will clear this counter.

**Note:** When there is no link, the error counter is at 0. When the link is up and no error observed, the error counter is also 0. A customer might want to make sure the link is up first by reading 3x0021 until a value of 0x8000 is obtained (indicating that the link is up) and then run the PRBS BIST. Because 3x0021 is a PCS block-lock check register, it will indicate no block lock and a high value of error counts if it is read when PRBSn BIST is on.

#### 2.7.2.1.1 Registers

The following tables list the related register information.

##### *2.7.2.1.1.1 Eth_10GBASE-R PCS Test-Pattern Control*

**Table 66 • 3x002A**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 5 | PCS_PRBS31_ANA | R/W | 0: Disable PRBS31 test pattern mode on the receive path<br><br>1: Enable PRBS31 test pattern mode on the receive path | 0x0 |

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 4 | PCS_PRBS31_GEN | R/W | 0: Disable PRBS31 test pattern mode on the transmit path<br>1: Enable PRBS31 test pattern mode on the transmit path | 0x0 |
| 3 | PCS_TSTPAT_GEN | R/W | 0: Disable transmit test pattern<br>1: Enable transmit test pattern | 0x0 |
| 2 | PCS_TSTPAT_ENA | R/W | 0: Disable receive test pattern<br>1: Enable receive test pattern | 0x0 |
| 1 | PCS_TSTPAT_SEL | R/W | 0: Pseudo random test pattern<br>1: Square wave test pattern | 0x0 |
| 0 | PCS_TSTDAT_SEL | R/W | 0: LF data pettern<br>1: Zero data pattern | 0x0 |

#### 2.7.2.1.1.2 Eth_10GBASE-R PCS Test-Pattern Counter

**Table 67 • 3x002B**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | PCS_ERR_CNT | R/O | Error counter (clear on read).<br>This is the 16-bit test pattern error counter defined by IEEE. The counter is cleared upon read of this register.<br>There is a 32-bit version of this counter in the Test_Error_Counter_0 and Test_Error_Counter_1 registers. If reading the 32-bit version, read Test_Error_Counter_1, followed by Test_Error_Counter_0. A read of the Test_Error_Counter_0 or Eth_10GBASE_R_PCS_test_pattern_counter registers will clear the 32-bit error counter. | 0x0000 |

#### 2.7.2.1.1.3 Test Error Counter 0

**Table 68 • 3x8007**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | PCS_VSERR_CNT_0 | R/O | Lower 16 bits of 32-bit version of PCS_ERR_CNT (Eth_10GBASE_R_PCS_test_pattern_counter)—clear on read.<br>This register should only be read directly after reading Test_Error_Counter_1. Upon read of this register or Eth_10GBASE_R_PCS_test_pattern_counter, the 32-bit error counter is cleared. | 0x0000 |

#### 2.7.2.1.1.4 Test Error Counter 1

**Table 69 • 3x8008**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | PCS_VSERR_CNT_1 | R/O | Clear on read.<br><br>Upper 16 bits of 32-bit version of PCS_ERR_CNT (Eth_10GBASE_R_PCS_test_pattern_counter).<br><br>This register should be read, followed immediately by Test_Error_Counter_0. Upon read of Test_Error_Counter_0 or Eth_10GBASE_R_PCS_test_pattern_counter, the 32-bit error counter is cleared. | 0x0000 |

### 2.7.2.2 Enable PMA BIST Engine

For the following code (using MDIO):

- WM is the register write operand.
- The first byte followed means the channel used is of port address 1E.
- The second byte is the device number.
- The next 2 bytes are the offset address.
- The last 2 bytes are the data to be written.

```
WM_1E_01_B114_192; configure DFT-Tx
WM_1E_01_B114_1921; enable DFT-Tx
WM_1E_01_B101_25C1; configure DFT-Rx
WM_1E_01_B106_000A; configure DFT-Rx
WM_1E_01_B10D_000A; configure DFT-Rx
WM_1E_01_B108_0014; configure DFT-Rx
WM_1E_01_B109_000A; configure DFT-Rx
WM_1E_01_B10B_03E7; configure DFT-Rx
WM_1E_01_B107_7A11; configure DFT-Rx
WM_1E_01_B100_0044; configure DFT-Rx
WM_1E_01_B101_25C1; configure DFT-Rx
WM_1E_01_B101_25C7; enable DFT-Rx
RM_1E_01_B113; read status of the checker
RM_1E_01_B113; read status of the checker
RM_1E_01_B113; read status of the checker
RM_1E_01_B113; read status of the checker
RM_1E_01_B113; read status of the checker
RM_1E_01_B113; read status of the checker
RM_1E_01_B113; read status of the checker
RM_1E_01_B113; read status of the checker
RM_1E_01_B113; read status of the checker
RM_1E_01_B113; read status of the checker;
               should be 0x1 now indicating good status before moving on
WM_1E_01_B100_0244; enable data capture
RM_1E_01_B10E; read msb of error count
RM_1E_01_B10F; read lsb of error count
WM_1E_01_B100_0044; disable data capture
WM_1E_01_B101_25E7; write 1 to bit 5 to reset error counter if needed
```

#### 2.7.2.2.1 Registers

The following tables list the related register information.

#### 2.7.2.2.1.1 SD10G65 DFT Main Configuration Register 1

**Table 70 • DFT_RX_CFG_1 (1xB100)**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 12 | Reserved | R/W | Factory use | 0x1 |
| 11 | Reserved | R/W | Factory use | 0x0 |
| 10 | Reserved | R/W | Factory use | 0x0 |
| 9 | ERR_CNT_CAPT_CFG | R/W | Captures data from error counter to allow reading of stable data | 0x0 |
| 8:7 | RX_DATA_SRC_SEL | R/W | Data source selection.<br><br>0: Main path<br>1: Reserved<br>2: Reserved | 0x0 |
| 6:5 | BIST_CNT_CFG | R/W | States in which error counting is enabled.<br><br>3: All but IDLE<br>2: Check<br>1: Stable + check<br>0: Wait_stable + stable + check | 0x0 |
| 4 | FREEZE_PATTERN_CFG | R/W | Disable change of stored patterns (for instance, to avoid changes during read-out) | 0x0 |
| 3 | CHK_MODE_CFG | R/W | Selects pattern to check.<br><br>0: PRBS pattern<br>1: Constant pattern | 0x0 |
| 2:0 | RX_WID_SEL_CFG | R/W | Selects DES interface width.<br><br>0:8<br>1:10<br>2:16<br>3:20<br>4:32<br>5:40 (default) | 0x4 |

#### 2.7.2.2.1.2 SD10G65 DFT Main Configuration Register 2

**Table 71 • DFT_RX_CFG_2 (1xB101)**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 14 | RX_WORD_MODE_CFG | R/W | Pattern generator.<br><br>0: Bytes mode<br>1: 10-bit word mode | 0x0 |
| 13:11 | RX_PRBS_SEL_CFG | R/W | Selects PRBS check.<br><br>0: PRBS7<br>1: PRBS15<br>2: PRBS23<br>3: PRBS11<br>4: PRBS31 (default)<br>5: PRBS9 | 0x4 |
| 10 | INV_ENA_CFG | R/W | Enables PRBS checker input inversion | 0x0 |
| 9 | Reserved | R/W | Factory use | 0x0 |
| 8:6 | Reserved | R/W | Factory use | 0x0 |

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 5 | CNT_RST | R/W | Software reset of error counter (rising edge activates reset) | 0x0 |
| 4:3 | CNT_CFG | R/W | Selects modes in which error counter is active.<br><br>0: Learn and compare mode<br>1: Transition between modes<br>2: Learn mode<br>3: Compare mode | 0x0 |
| 2:1 | BIST_MODE_CFG | R/W | BIST mode.<br><br>0: Off<br>1: BIST<br>2: BER<br>3: CONT (infinite mode) | 0x3 |
| 0 | DFT_RX_ENA | R/W | Enable RX DFT capability.<br><br>0: Disable DFT<br>1: Enable DFT | 0x0 |

#### 2.7.2.2.1.3 SD10G65 DFT BIST Configuration Register A

BIST configuration register A for SD10G65 DFT controlling "check and wait-stable" mode.

**Table 72 • DFT_BIST_CFG0A (1xB106)**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | WAKEUP_DLY_CFG | R/W | BIST FSM: threshold to leave DOZE state | 0x0000 |

#### 2.7.2.2.1.4 SD10G65 DFT BIST Configuration Register B

BIST configuration register B for SD10G65 DFT controlling "check and wait-stable" mode.

**Table 73 • DFT_BIST_CFG0B (1xB107)**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | MAX_BIST_FRAMES_CFG | R/W | BIST FSM: threshold to enter FINISHED state | 0x0000 |

#### 2.7.2.2.1.5 SD10G65 DFT BIST Configuration Register A

BIST configuration register A for SD10G65 DFT controlling "stable" mode.

**Table 74 • DFT_BIST_CFG1A (1xB108)**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | MAX_UNSTABLE_CYC_CFG | R/W | BIST FSM: threshold to iterate counter for max_stable_attempts | 0x0000 |

#### 2.7.2.2.1.6 SD10G65 DFT BIST Configuration Register B

BIST configuration register B for SD10G65 DFT controlling "stable" mode.

**Table 75 • DFT_BIST_CFG1B (1xB109)**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | STABLE_THRES_CFG | R/W | BIST FSM: threshold to enter CHECK state | 0x0000 |

#### 2.7.2.2.1.7 SD10G65 DFT BIST Configuration Register A

BIST configuration register A for SD10G65 DFT controlling frame length in "check" mode.

**Table 76 • DFT_BIST_CFG2A (1xB10A)**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | FRAME_LEN_CFG_MSB | R/W | BIST FSM: threshold to iterate counter for max_bist_frames [31:16] | 0x0000 |

#### 2.7.2.2.1.8 SD10G65 DFT BIST Configuration Register B

BIST configuration register B for SD10G65 DFT controlling frame length in "check" mode.

**Table 77 • DFT_BIST_CFG2B (1xB10B)**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | FRAME_LEN_CFG_LSB | R/W | BIST FSM: threshold to iterate counter for max_bist_frames [15:0] | 0x0000 |

#### 2.7.2.2.1.9 SD10G65 DFT BIST Configuration Register B

BIST configuration register B for SD10G65 DFT controlling stable attempts in "wait-stable" mode.

**Table 78 • DFT_BIST_CFG3B (1xB10D)**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | MAX_STABLE_ATTEMPTS_CFG_LSB | R/W | BIST FSM: threshold to enter SYNC_ERR state [15:0] | 0x0000 |

#### 2.7.2.2.1.10 SD10G65 DFT Error Status Register 1

Status register 1 for SD10G65 DFT containing the error counter value.

**Table 79 • DFT_ERR_STAT_1 (1xB10E)**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | ERR_CNT_MSB | R/O | Counter output depending on cnt_cfg [31:16] | 0x0000 |

#### 2.7.2.2.1.11 SD10G65 DFT Error Status Register 2

Status register B2 for SD10G65 DFT containing the error counter value.

**Table 80 • DFT_ERR_STAT_2 (1xB10F)**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 15:0 | ERR_CNT_LSB | R/O | Counter output depending on cnt_cfg [15:0] | 0x0000 |

#### 2.7.2.2.1.12 SD10G65 DFT Miscellaneous Status Register 2

Status register 2 for SD10G65 DFT.

**Table 81 • DFT_MAIN_STAT_2 (1xB113)**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 5 | STUCK_AT_PAR | R/O | Data input is unchanged for all 40 parallel bits for at least 7 clock cycles (defined by c_STCK_CNT_THRES) | 0x0 |

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 4 | STUCK_AT_01 | R/O | Data input is constantly 0 or constantly 1 for all 40 parallel bits for at least 7 clock cycles (defined by c_STCK_CNT_THRES) | 0x0 |
| 3 | NO_SYNC | R/O | BIST: no sync found since BIST enabled | 0x0 |
| 2 | INSTABLE | R/O | BIST: input data not stable | 0x0 |
| 1 | INCOMPLETE | R/O | BIST not complete (that is, not reached stable state or following) | 0x0 |
| 0 | ACTIVE | R/O | BIST is active (that is, left DOZE but did not enter a final state) | 0x0 |

#### *2.7.2.2.1.13 SD10G65 DFT Main Configuration Register*

Main configuration register for SD10G65 DFT.

**Table 82 • DFT_TX_CFG (1xB114)**

| Bit | Name | Access | Description | Default |
|---|---|---|---|---|
| 12 | Reserved | R/W | Factory use | 0x1 |
| 11:9 | TX_WID_SEL_CFG | R/W | Selects SER interface width.<br><br>0:8<br>1:10<br>2:16<br>3:20<br>4:32<br>5:40 (default) | 0x4 |
| 8:6 | TX_PRBS_SEL_CFG | R/W | Selects PRBS generator.<br><br>0: PRBS7<br>1: PRBS15<br>2: PRBS23<br>3: PRBS11<br>4: PRBS (default)<br>5: PRBS9 | 0x4 |
| 5 | SCRAM_INV_CFG | R/W | Inverts the scrambler output | 0x0 |
| 4 | IPATH_CFG | R/W | Selects PRBS generator input.<br><br>0: Pattern generator<br>1: Core | 0x0 |
| 3:2 | OPATH_CFG | R/W | Selects DFT-TX output.<br><br>0: PRBS/scrambler (default)<br>1: Bypass | 0x0 |
| 1 | TX_WORD_MODE_CFG | R/W | Word width of constant pattern generator.<br><br>0: Bytes mode<br>1: 10-bits word mode | 0x0 |
| 0 | DFT_TX_ENA | R/W | Enable TX DFT capability.<br><br>0: Disable DFT<br>1: Enable DFT | 0x0 |

## 2.8 VScope

VScope™ is a feature that provides an estimation of the 10G input data eye healthiness. It is not easy to measure the input data eye with a bench scope in customer's system, as there is no SMA connector installed, and high-impedance probes for 10G are not always available.

There are two types of VScope provided in the VSC8489 family devices: the fast eye scan and the full VScope scan. With FAST_SCAN/QUICK_SCAN, you get the number of error free x and y values along with the amplitude range. With FULL_SCAN, you get the complete error matrix for each x, y (phase, amplitude) point measured for a configured bit error rate (BER).

The CLI function displays the VScope scan result as an ASCII plot where "X" represents pixels without error during the measurement and "." represents pixels with one or more error during the measurement. That is, the region filled with "X" represents the inner eye.

The full VScope scan gathers the error rate information for a two-dimensional array of pixels. There are 128 tics on the x-axis and 63 tics on the y-axis (for an area of 128 × 63 tics). To reduce the time for the scan, it is possible to reduce the number of measured pixels. With the X_start value, you select the first pixel on the x-axis. The X_incr value determines the distance to the next column. The x_count value determines the number of columns to scan. The Y_start/incr/count values determine the same for the y-axis. The BER argument is a pointer to a two-dimensional array that holds the result: the error numbers for the respective pixel. The error number is the number of samples where the main sampler (sampling at the center of the eye) and the auxiliary sampler (scanning the eye) are sampling different values for a defined number of samples.

For the x-axis, we would suggest using x-start= 0, x-incr= 0, and x-count= 127. This utilizes the full range with maximum resolution. For the y-axis, it is reasonable to leave out outer regions for this kind of scan, because we "only" get the inner eye. So, we suggest staying with y-start= 20, y-incr= 0, and y-count= 25.

The BER parameter determines the number of samples taken for the measurement of a single pixel. The number of samples is 2**(ber+1). A BER of 10**–15 is not feasible. The VScope hardware implements 32-bit counters that allow for BER of ~10**-9, but even that would take a lot of time.

The error-threshold parameter is only used during preparation of the measurement. The result of a test measurement is compared against this value to determine the phase of the auxiliary samplers, because there is an ambiguity of 180° in VScope mode. For the actual plot, the threshold is zero.

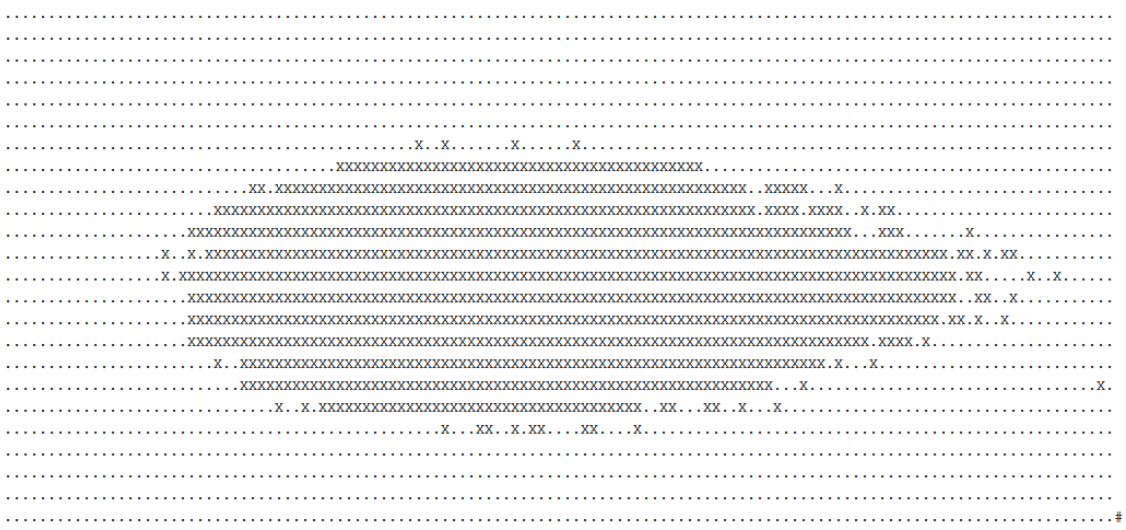
The following scan configuration values are recommended when using the full scan for getting the proper inner eye.

- x_start: 0
- y_start: 20
- x_incr: 0
- y_incr: 0
- x_count: 127

**Example:**

# $x-count 127 y-count 25 x-incr 0 y-incr 0 ber 5 error-threshold 3 VScope= successfully configured.

The error counter values for the full scan are as follows:



Both types of VScope are approximates only, but the fast eye is less accurate than the eye captured by the full VScope. However, it is quick and simple. In general, “two limits” are suggested as an indication for the healthiness of the eye. Typically, 50% or above means everything is fine and there is no need for action, while 25% or below indicates poor quality where errors are likely. Everything in between these two values means the link may be acceptable but could be better.

The following scan configuration values are recommended for a fast eye status report.

- error_free_x: 75
- error_free_y: 11
- amp_range: 17
- amp_percent: 64%
- phase_percent: 58%
- eye_open_percent: 37%

**Note:** For the fast eye report, the phase percent calculation is based on 128 units, the amplitude percent calculation is based on the amp_range (17 units), and the eye opening percent calculation is based on phase percent multiplied by amplitude percent.

The following API and structures get the eye capture scan.

```
/**\brief VSCOPE scan configuration */
typedef struct{
        BOOL line;      /**<selects line or host side, 1 for line */
        u32 x_start;    /**<start value for x (0-127)*/
        u32 y_start;    /**<start value for y (0-63)*/
```

```
        u32 x_incr;     /**<increment value for x during the scan */
        u32 y_incr;     /**<increment value for y during the scan */
        u32 x_count;    /**<max value for x ( up to which scan is to be performed) */
        u32 y_count;    /**<max value for y ( up to which scan is to be performed) */
        u32 ber;        /**<bit error rate */
} vtss_phy_10g_vscope_scan_conf_t;
#define PHASE_POINTS 128 /**<phase points range from 0-127 */
#define AMPLITUDE_POINTS 64 /**<amplitude points range from 0-63 */
/**\ brief Vscope eye scan status*/
typedef struct {
        vtss_phy_10g_vscope_scan_conf_t scan_conf; /**<scan configuration data */
        i32 error_free_x;       /**<error free x values in case of fast eye scan */
        i32 error_free_y;       /**<error free y values in case of fast eye scan */
        i32 amp_range;          /**<amp range in case of fast eye scan */
        u32 errors[PHASE_POINTS][AMPLITUDE_POINTS];     /**<error matrix in full scan mod

} vtss_phy_10g_vscope_scan_status_t;
/** \ brief VSCOPE fast scan status *//**
* \brief set VSCOPE fast scan configuration
* \param inst    [IN]  Target instance reference.
* \param port_no [IN]  Port number
* \param conf    [IN]  VSCOPE fast scan configuration
*
* \return
*   VTSS_RC_OK on success.\n
*   VTSS_RC_ERROR on error.
**/
vtss_rc vtss_phy_10g_vscope_scan_status_get(const vtss_inst_t inst,
                const vtss_port_no_t port_no,
                vtss_phy_10g_vscope_scan_status_t *const conf);
```

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