AN2709

Low-Power Features of SAM L Series Devices

Introduction

The Microchip SMART SAM L MCUs are ultra low-power ARM® Cortex® M0+ based microcontrollers.

This application note describes the low-power optimization key features and low-power modes of the following SAM L Series devices:

- SAM L10
- SAM L11
- SAM L21
- SAM L22

The SAM L series devices have specific low-power features, such as low-power modes, ultra low-power peripherals,performance levels, and SleepWalking. The SAM L10, SAM L11 and SAM L21 series devices have additional features, such as Peripheral Power Domains and SleepWalking with Power Domain Gating.

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1. Overview

In many applications using low power is highly important. In such applications there is a need to balance responsiveness with power consumption. A standard low-power technique is to limit the amount of time a device spends in Active mode by increasing the time spent in low power Sleep modes. The features described in this application note enables the device to perform tasks, while in Active mode or in Sleep mode, with a very low power consumption.

This application note will focus on the available sleep modes, Performance Levels, Power Domains, and SleepWalking on SAM L series devices.

This application note also explains about a unique feature, such as SleepWalking with Power Domain Gating on the SAM L10, SAM L11 and SAM L21 series of devices.

2. Sleep Modes

Before introducing the new features, it is necessary to understand the various sleep modes available in SAM L series devices. In addition to Active mode, there are four sleep modes in SAM L21/SAM L22 series devices and three different sleep modes in SAM L10, SAM L11 series devices.

For the typical Sleep mode wake-up times, refer to the "Wake-up Time" section in the "Electrical Characteristics" chapter in the respective data sheet.

2.1 Idle

There is one Idle (IDLE) Sleep mode in SAM L series devices. In this mode, the CPU clock is switched off. The default state of the synchronous AHBx and APBx clocks is off but they can be enabled if requested by peripherals. For example, if the DMA receives a transfer trigger, it will request its clock signal and start to transfer. By default, the asynchronous Generic Clocks (GCLK_PERIPH) runs in IDLE. Writing the On Demand bit for a clock source to one ONDEMAND bit will override this default setting, ensuring GCLK_PERIPH only propagates to a peripheral when requested. IDLE is entered by executing the Wait For Interrupt (WFI) instruction with IDLE written to the Sleep Mode bit group in the Sleep Configuration register (SLEEPCFG.SLEEPMODE written to 0x2). The device will exit IDLE when it detects any non-masked interrupt.

2.2 Standby

In Standby (STANDBY) Sleep mode, the device is capable of switching both clocks and power domains on and off. If the device is configured to perform multiple operations in STANDBY, clocks and power domains will only be available when they are needed. This will reduce the overall power consumption.

By default all clocks except the OSCULP32K are switched off in Standby (STANDBY) Sleep mode. Peripherals can still perform tasks as long as the Run in Standby bit (RUNSTDBY) in the peripheral's control register is written, that is, Control A for the ADC module (CTRLA.RUNSTDBY written to one). This will enable the peripheral to run while in STANDBY. If in addition the clock source is set to run on demand, the oscillator will only be enabled when requested by a peripheral. STANDBY is entered by executing the WFI instruction with STANDBY written to the Sleep Mode bit group in the Sleep Configuration register (SLEEPCFG.SLEEPMODE written to 0x4). The device will exit STANDBY on any asynchronous interrupt.

In STANDBY, by default the device will switch to a low-power voltage regulator (LP VREG) to further reduce the power consumption. Refer to 3.2.2 Low Power Voltage Regulator for more details. For SAM L10, SAM L11, and SAM L21 series devices, another feature is available, that is, while in STANDBY the dynamical switching of power domains. Refer to 5.1 SleepWalking with Power Domain Gating for more details.

The SAM L10 and SAM L11 SRAM is divided into sub-blocks which can be retained in STANDBY Low-Power mode to optimize power consumption. By default, all sub-blocks are retained but it is possible to switch them off depending on SRAM memory size. This behavior can be changed by configuring the RAMPSWC bit groups in the Power Configuration register (PWCFG).

2.3 Backup

Important: Backup mode is not supported on SAM L10, SAM L11 series devices.

In Backup (BACKUP) Sleep mode only the backup domain is powered and only registers in this domain will hold their value. For more details on the backup power domain, refer to 4.1 Power Domains for SAM L21 Series Devices for SAM L21 series devices, 4.2 Power Domains for SAM L22 Series Devices for SAM L22 series devices. SRAM will also be turned off and not retain any data. This mode can be entered by executing the WFI instruction with BACKUP written to the Sleep Mode bit group in the Sleep Configuration register (SLEEPCFG.SLEEPMODE written to 0x5). Wakeup from BACKUP will be similar to a device start-up after reset. The device will start executing code in the reset handler and load data from Flash to SRAM. The difference is that the peripheral registers in the backup domain will retain their value and the Real-Time Counter (RTC) will, if enabled, continue to run. The I/O Retention bit in the Control A register (CTRLA.IORET) in the Power Manager (PM) is used to decide whether or not the I/O lines are to hold their value when exiting BACKUP. The Reset Cause (RCAUSE) register in the Reset Controller (RSTC) will indicate the reset source after a reset. If the reset is issued by a Backup reset, it is possible to alter the startup routine in the main function by first evaluating the Reset Cause register. The Reset Controller contains additional 32-bit registers for storing state information, which is useful for determining the wakeup cause and the correct execution at startup after BACKUP.

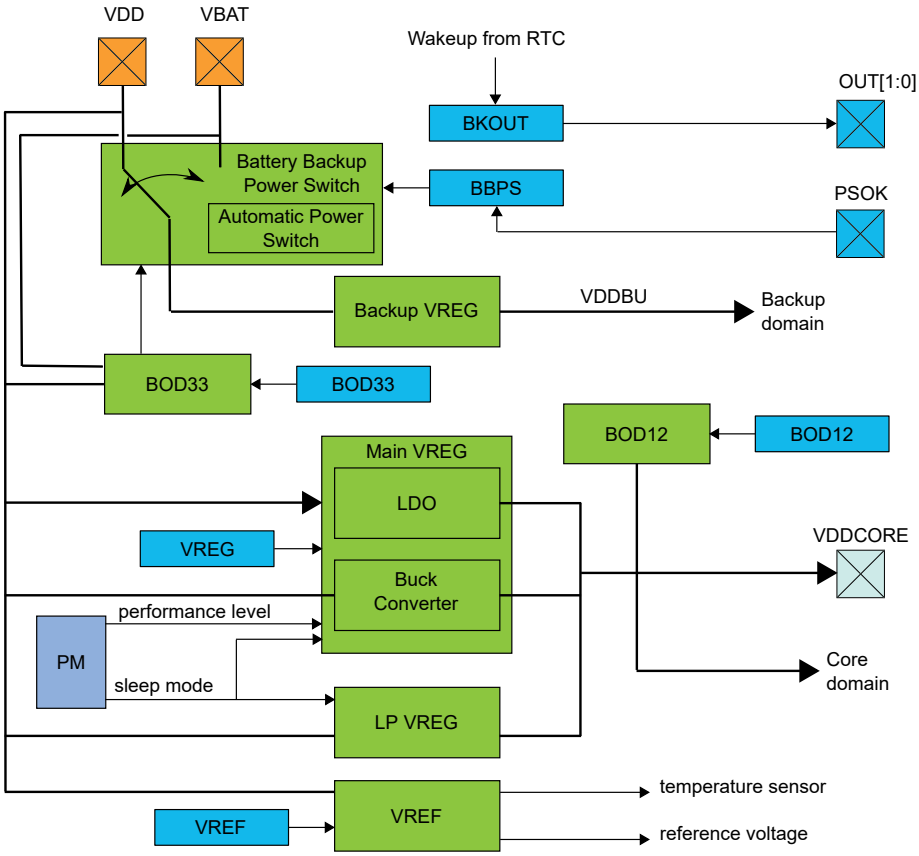
Because only the backup domain is powered, the device will consume a minimum amount of power. For SAM L21 series devices the External Wakeup pins, Real-Time Counter (RTC) interrupts or the Battery Backup Power Switch (BBPS) can be used as wake up sources. For SAM L22 series devices, the Real-Time Counter (RTC) interrupts or the Battery Backup Power Switch (BBPS) can be used as wake up sources.

For SAM L21 series devices, the BBPS can also be used to enter BACKUP. This is further investigated in 2.3.1 Battery Backup Power Switch (BBPS). For that purpose the External Wakeup pins must be configured correctly. Refer to the "External Wakeup Detector" section in the "Reset Controller" chapter in the SAM L21 data sheet for more details. The External Interrupt Controller (EIC) is not part of the backup power domain and cannot be used to wake the device from BACKUP.

2.3.1 Battery Backup Power Switch (BBPS)

The Battery Backup Power Switch (BBPS) enables the device to switch the backup domain supply (VDDBU) between main power (V_{DD}) and battery backup power (VBAT), see Figure 2-1. The BBPS can be forced to, or automatically switched between, either the V_{DD} or VBAT.

Figure 2-1. Supply Controller Block Diagram



Forced Power Switch

After any reset, the BBPS is configured with no action (BBPS.CONF written to 0x0). This backup domain is supplied by V_{DD}. The BBPS can also be forced (BBPS.CONF written to 0x2) to supply the backup domain from the V_{BAT} supply pin.

Automatic Power Switch

As mentioned, the BBPS can also be configured to automatically switch from main power to battery backup power and back to main power again. The Automatic Power Switch (BBPS.CONF written to 0x1) is the only configuration allowing switching from both ways. If V_{DD} decreases below a certain threshold level, the Automatic Power Switch switches to VBAT and the device enters in to BACKUP. If the V_{DD} is restored, the device can either stay in BACKUP or leave BACKUP, depending on the Wake Enable (BBPS.WAKEEN) configuration.

BOD33 Power Switch

BOD33 Power Switch (BBPS.CONF written to 0x3) enables automatic switching from V_{DD} to VBAT. The Threshold Level bit group in the BOD33 Control register (BOD33.BKUPLEVEL) holds the V_{DD} threshold when the device is in Backup mode, and the VBAT threshold level in Active mode. The device will enter BACKUP when V_{DD} threshold value is violated if BOD33 action is to enter Backup mode (BOD33.ACTION written to 0x3) and voltage monitor is set to monitor V_{DD} (BOD33.VMON written to zero).

Main Power Supply OK Pin Enable

Main Power Supply OK Pin Enable is a configuration enabling automatic switching from VBAT to V_{DD} using the PSOK pin (PB00). If the Automatic Power Switch is not enabled (BBPS.CONF is not 0x1) when V_{DD} is restored and Main Power Supply OK Enable is set (BBPS.PSOKEN written to one), a low-to-high transition on the PSOK pin will switch VDDBU back to V_{DD}. The device can either stay in BACKUP or leave BACKUP depending on the Wake Enable (BBPS.WAKEEN) configuration.

2.4 Off

In the Off (OFF) Sleep mode the device has no peripherals, voltage regulators or oscillators running. This mode is entered by executing the WFI instruction with OFF written to the Sleep Mode bit group in the Sleep Configuration register (SLEEPCFG.SLEEPMODE written to 0x6). The only option to wake up the device is by asserting an external reset on the Reset pin or by a Power-on-Reset (POR).

3. Performance Levels

The SAM L series devices can operate at two performance levels. When operating from the lowest level PL0, the voltage applied on the full logic area is reduced by voltage scaling. This voltage scaling technique allows to reduce the active power consumption while decreasing the maximum frequency of the device. On the highest performance level PL2 the voltage regulator supplies the highest voltage, allowing the device to run at higher clock speeds.

3.1 Changing Performance Level

Switching to a different performance level does not affect oscillators, prescalers, or GCLK generators. After changing to a higher performance level, it is necessary to wait for the Performance Level Ready bit in the Interrupt Flag Status and Clear register (INTFLAG.PLRDY) in the Power Manager (PM) to be set before changing the clock speed. When changing to a lower performance level, the clock frequency must be set to a speed below the maximum limit before reducing the performance level. It may also be necessary to change the number of read wait states, which is dependent of CPU clock speed, performance level and VDDIN voltage. Refer to the "Electrical Characteristics" chapter in the respective data sheet for more details. The number of read wait states is configured by writing to the NVM Read Wait States bit group in the Control B register (CTRLB.RWS) in the Non-Volatile Memory Controller (NVMCTRL). Increasing of the read wait states must be done before changing the performance level. Similarly, decreasing the number of wait states must be done after changing the performance level. Following are two step-by-step examples demonstrating how to change the performance level.

Changing to a lower level (PL0) when running at maximum frequency (48MHz for SAM L21 series devices, 32MHz for SAM L10, SAM L11 and SAM L22 series devices) with VDDIN = 3.3V (> 2.7V):

1. Disable/decrease clock generators above the allowed maximum frequency at 12 MHz (for SAM L21 series devices), 8MHz (for SAM L10, SAM L11 and SAM L22 series devices).
2. Choose PL0 as performance level (PLCFG.PLSEL written to 0x0).
3. If the new CPU speed is <7.5 MHz the number of read wait states can be reduced from one to zero (CTRLB.RWS written to 0x0). Refer to NVM Characteristics section in "Electrical Characteristics" chapter for more details.

Changing to a higher level (PL2) when running at 8MHz with VDDIN = 1.62V (< 2.7V):

1. If the new CPU speed is >28 MHz the number of read wait states must be increased to two for SAM L10, SAM L11 and SAM L21series devices, two or three for SAM L22 series devices (CTRLB.RWS written to 0x2 or 0x3), depending on the CPU speed.
2. Choose PL2 as performance level (PLCFG.PLSEL written to 0x2).
3. Wait for the Performance Level Ready (INTFLAG.PLRDY) bit to be set. This bit change will generate an interrupt if the Performance Level Ready interrupt is enabled (INTSET.PLRDY written to one).
4. The user can increase CPU clock speed without exceeding the maximum allowed frequency.

3.2 Voltage Regulator System

The SAM L series devices can operate from one of several internal voltage regulators. The main voltage regulator (Main VREG) supplies the core domain (VDDCORE) when the device is in Active mode or Idle Sleep mode. In Standby Sleep mode, VDDCORE is either powered by Main VREG or the low-power

voltage regulator (LP VREG). The SAM L21 and SAM L22 series devices also have VDDBU which is powered by the Backup voltage regulator (Backup VREG).

3.2.1 Main Voltage Regulator

Main VREG can be supplied by two voltage regulators: an LDO regulator and a buck switching regulator. The buck switching regulator will consume the least amount of power, having the highest efficiency of the two in Active mode. The buck switching regulator does however require an inductor to be connected to the device. Since this inductor is not guaranteed to be available in all designs, the SAM L series devices will by default start from the LDO regulator. Switching between LDO regulator and buck switching regulator is done by writing to the Voltage Regulator Selection bit in the Voltage Regulator System Control register (VREG.SEL) in the Supply Controller (SUPC).

3.2.2 Low Power Voltage Regulator

For SAM L21 series devices, the low-power voltage regulator can be used to supply VDDCORE when in Standby Sleep mode if all power domains are in retention state. If many power domains are active with no clocks requested, the device can still be powered by LP VREG as long as the V_{REG} Switching mode not set to Performance mode (STDBYCFG.VREGSMOD written to one). Setting this bit group to one, will force the device to be powered by the main voltage regulator as long as one or more power domains are active.

For SAM L10, SAM L11 and SAM L22 series devices, the low-power voltage regulator can be used to supply VDDCORE when in Standby Sleep mode, if the V_{REG} Switching mode is set to Low-Power mode (STDBYCFG.VREGSMOD written to two) or if the V_{REG} Switching mode is set to auto (STDBYCFG.VREGSMOD written to zero) without SleepWalking feature is used.

The efficiency of LP VREG can be improved by setting the Low-Power mode Efficiency bit in the VREG register (VREG.LPEFF written to one) for applications where a limited V_{DD} range (2.5V to 3.6V) is used.

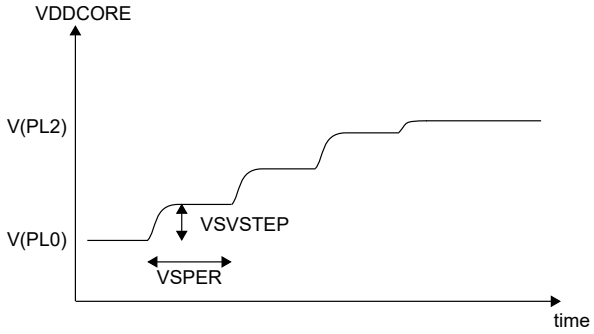
For more details, refer to Power Domains for SAM L21 Series Devices, Power Domains for SAM L22 Series Devices or Power Domains for SAM L10 SAM L11 sections.

3.2.3 Voltage Scaling Control

The VDDCORE supply will change under certain circumstances, such as switching to a different performance level, entering or exiting STANDBY, or when a SleepWalking task is started. A sudden VDDCORE increase can cause a spike in the current flow. Forcing the regulator to make a softer transition of voltage levels by writing to the Voltage Scaling Step and Voltage Scaling Frequency bit groups in the Voltage Regulator System Control register (VREG.VSSTEP and VREG.VSPER) will limit such current spike(s) but also increase the total step time. For additional information, see Figure 3-1. The transition time can be decreased by configuring a larger voltage step height since the number of steps are reduced. By default VSVSTEP is written to zero giving a step height of 5mV. The scaling frequency VSPER determines the delay between the steps. By default VSPER is written to zero giving a delay of 1µs.

In designs where the power supply is weak, and if powered by a nearly discharged battery, a softer transition may prevent the external power supply voltage level from dropping below the BOD threshold value. The current spikes only affects the external power supply and not the device as long as the external power supply manages to source the necessary current flow.

Figure 3-1. Voltage Scaling



4. Power Domains

Most of the power domains can switch between the following three states:

- **Active state:** Peripherals in the power domain are powered and ready to be used or configured.
- **Retention state:** Main voltage supply is powered off while maintaining a low-power supply to hold the state of the registers and SRAM.
- **Off state:** Peripherals in the domain are not powered and registers must be reprogrammed for a peripheral to be used.

Turning power domains off or to retention state allows the device to consume less power in STANDBY than what is achievable by only disabling clocks. Power domains are automatically switched between active and retention state but can also be forced to active state. The dynamical switching is known as Power Domain Gating. Power domain configurations are set in the Standby Configuration (STDBYCFG) register in the Power Manager (PM) module.

4.1 Power Domains for SAM L21 Series Devices

The SAM L21 series devices have five digital power domains as shown in Figure 4-1. These power domains enable power saving by limiting or powering off logic areas in the device.

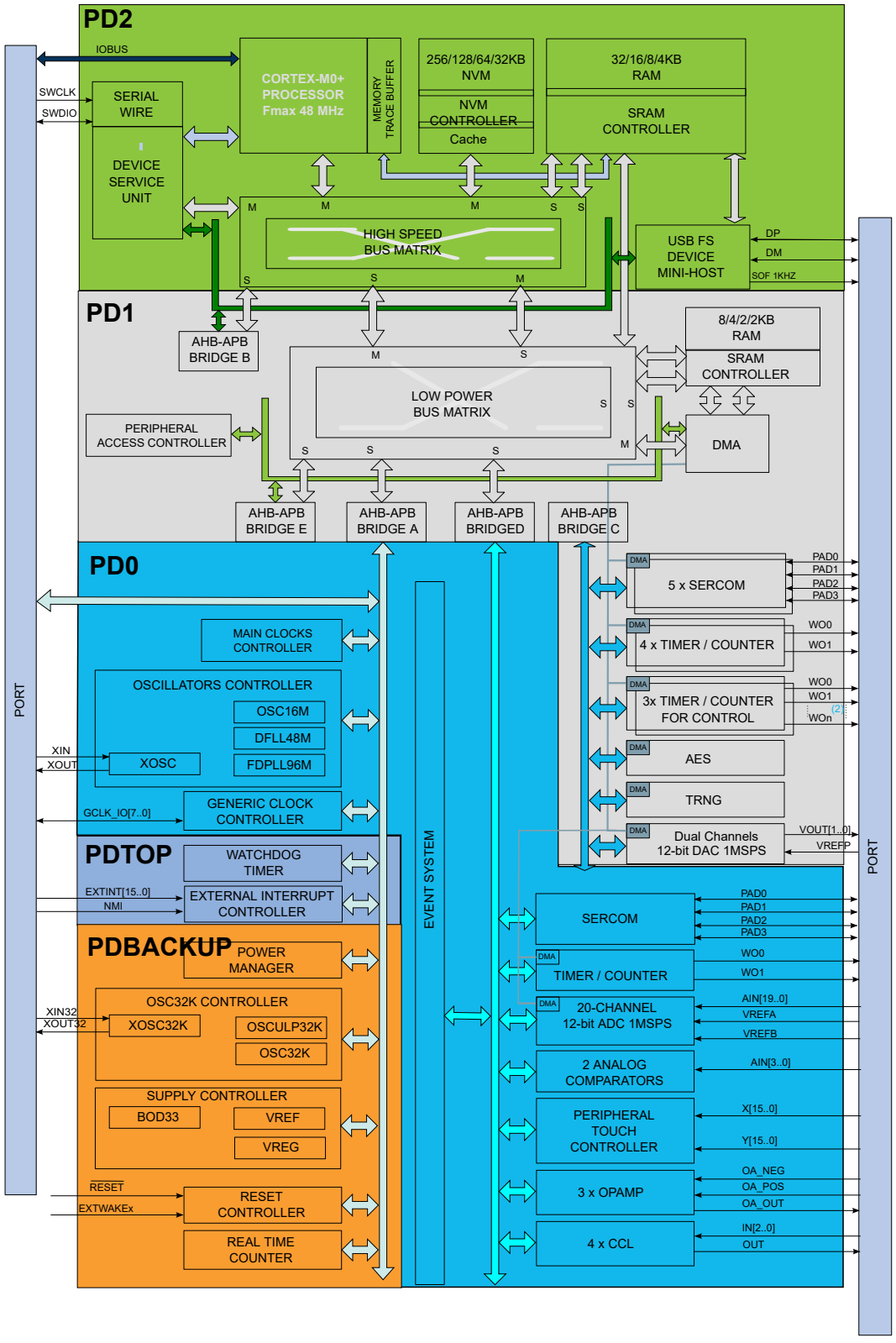
4.1.1 Power Domain Partitioning

The SAM L21 series device's peripherals are partitioned into five power domains. The power domain partitioning are provided in Table 4-1 and Figure 4-1 illustrates the power domain partitioning.

Table 4-1. Power Domain Partitioning

PDBACKUP	PDTOP	PD0	PD1	PD2
OSC32CTRL	EIC	AC	AES	CORE
PM	PORT	ADC	AHB-APB Bridges	DSU
RSTC	WDT	CCL	DAC	SRAM
RTC		EVSYS	DMAC	USB
SUPC		GCLK	I^2S	Flash
		MCLK	PAC	
		OPAMP	SERCOM	
		OSCCTRL	TC	
		PTC	TCC	
		LP TC	TRNG	
		LP SERCOM	LP SRAM	

Figure 4-1. Power Domain Partitioning



4.1.2 PDBACKUP

PDBACKUP is the lowest of the five power domains and will always be in active state, except when the device is in OFF position. When the device is in Backup Sleep mode, the backup domain is the only powered partition. The Real-Time Counter (RTC) is located in the backup domain and can be used to e.g. wakeup the device from BACKUP or to toggle a pin each time an RTC event occurs.

4.1.3 PDTOP

PDTOP is either in active or off state. The domain contains the External Interrupt Controller (EIC) and the Watchdog Timer (WDT) modules and is turned off when in BACKUP or OFF.

4.1.4 PD0, PD1, and PD2

PD0, PD1, and PD2 can be in one of the active, retention, or off states. In STANDBY with all peripherals idle, the three power domains are by default set in retention state, allowing low power consumption while retaining all the logic content. When exiting STANDBY, the domains are set back to active state. If a peripheral needs to remain active when entering STANDBY, its power domain will remain in active state. For additional information on switching of power domains, refer to 5.1 SleepWalking with Power Domain Gating. The domains are in off state when in BACKUP or OFF.

Note: If a power domain (PDn) is active, all inferior domains (<PDn) will be active.

4.1.5 Low-Power Modules

For potential power saving, both the TC and the SERCOM modules are split between PD0 and PD1. In applications where it is sufficient to use only the PD0 modules, the need for entering PD1 can be reduced, which leads to low power consumption. The low-power modules in PD0 are TC4 and SERCOM5.

Note: The features of low-power SERCOM are limited.

As shown in Figure 4-1, SRAM is located in both PD1 and PD2. The low-power SRAM (LP SRAM) block in PD1 is used for DMAC descriptors but can also be used to store data. Using the LP SRAM in PD1 will save power if PD2 is less frequently enabled. Another benefit from the LP SRAM is to enable DMAC transfers without slowing down other bus masters accessing the main SRAM when in Active mode.

4.2 Power Domains for SAM L22 Series Devices

The SAM L22 series devices have two power domains (PDTOP,PDBACKUP) which are different than the supply domains, such as VDDIO and VDDANA.

For additional information on Power Domain Partitioning, refer to the "Peripheral Configuration Summary" chapter in the SAM L22 data sheet.

4.2.1 PDBACKUP

The Backup Power Domain (PDBACKUP) is always on, except in the Off Sleep mode. The PDBACKUP contains the 32 kHz oscillator sources, Supply Controller, Reset Controller, Real Time Counter, and Power Manager.

4.2.2 PDTOP

PDTOP contains all controllers located in the core domain. It is powered when in Active mode, Idle mode, or Standby mode. When in Backup of Off mode, this domain is powered down.

4.3 Power Domains for SAM L10 SAM L11 Series Devices

The SAM L10 and SAM L11 series devices have two power domains (PDAO,PDSW) other than the supply domains, such as VDDIO and VDDANA. For Power Domain Partitioning details, refer to the "Peripheral Configuration Summary" chapter in the SAM L10/SAM L11 data sheet.

4.3.1 PDAO

The PDAO contains all controllers located in the always-on domain. It is powered when in Active mode, Idle mode, or Standby mode.

4.3.2 PDSW

The PDSW is a "switchable power domain" which contains the Event System, Generic Clock Controller, Main Clock Controller, Oscillator Controller, Non-Volatile Memory Controller, DMA Controller, Device Service Unit, and ARM core. The PDSW also contains a number of peripherals that enables the device to wake up from an interrupt: SERCOM, Timer, ADC, DAC, OPAMP, CCL, and the PTC. In Standby Sleep mode, it can be turned off to save leakage consumption according to the user configuration.

5. SleepWalking

SleepWalking feature enables the peripherals to request clocks to perform tasks without waking the CPU when in STANDBY. SleepWalking is the capability for a device to temporarily wake up clocks for a peripheral to perform a task without waking up the CPU from STANDBY Sleep mode. At the end of the sleepwalking task, the device can either be woken up by an interrupt (from a peripheral involved in SleepWalking) or enter again into STANDBY Sleep mode. The SleepWalking is supported only on GCLK clocks by using the on-demand clock principle of the clock sources.

The Sleep Walking feature is supported in SAM L10, SAM L11, SAM L21, SAM L22 series devices.

5.1 SleepWalking with Power Domain Gating

In SAM L10, SAM L11 and SAM L21 series devices, the SleepWalking feature is extended to the capability of setting a power domain from retention to active state and vice-versa. This means that a power domain will only be active when a peripheral within needs to run. To apply this feature based on events or DMA triggers the Dynamic Power Gating bits in the Standby Configuration register (STDBYCFG.DPGPD0/1 for SAM L21, STDBYCFG.DPGPDSW for SAM L10 and SAM L11) in the Power Manager (PM) must be set. When a SleepWalking task activates a power domain, this is done without waking the CPU. When the task is complete the device can either wake up, if an interrupt is issued, or return to STANDBY.

By default, a power domain is set automatically to retention state in STANDBY if no activity is required in it. Turning on a power domain is relatively time consuming, and for some applications this delay may be unacceptable. It is then possible to disable the dynamic switching of the power domains to ensure that one or more power domains always are active in STANDBY. This feature is configured with the Power Domain Configuration bit group in the Standby Configuration register (STDBYCFG.PDCFG). Another option for the SAM L21 is to enable Linked Power Domains, allowing PD1 to be activated whenever PD0 is active, PD2 to be activated whenever PD1 is active, or activate both PD1 and PD2 if PD0 is active. This will reduce the delay if a peripheral in PD0 activates a peripheral in PD1. Linking of power domains is configured in the Linked Power Domain bit group in the Standby Configuration register (STDBYCFG.LINKPD).

Note:

1. When a peripheral running in STANDBY is requesting a clock source, the performance level is determined by its state prior to entering STANDBY.
2. The SleepWalking with Power Domain Gating Feature is supported in SAM L10, SAM L11 and SAM L21 series devices only.

6. Example Project for SAM L21

In Atmel Studio perform these actions:

Go to *File* > *New* > *Example Project …* > *SAM L21 Low Power Application* > *SAM L21 Xplained Pro.*

Prerequisites:

- Atmel Studio 6.2 Service Pack 2 or later
- Atmel Software Framework 3.21.0 or later
- Atmel Data Visualizer Version 2.1.212 or later
- SAM L21 Xplained Pro Evaluation Kit with Micro-B USB cable

Note:

1. Jumper positions in the Xplained Pro kit: I/O - BYPASS position, MCU - MEASURE, VBAT SELECT - Open, VCC_MCU - Closed (VCC_I/O).
2. The example projects are available for both SAM L21 Xplained Pro (ATSAML21J18A) and SAM L21 Xplained Pro (ATSAML21J18B) kits.
3. In stand alone Advanced Software Framework, the same example projects are available for GCC and IAR compilers, which are available for download from the following location: http://www.microchip.com/avr-support/advanced-software-framework-(asf).

7. Example Project for SAM L22

In Atmel Studio perform these actions:

Go to *File* > *New* > *Example Project …* > *SAM L22 Low Power Application* >*SAM L22 Xplained Pro.*

Prerequisites:

- Atmel Studio 7.0.594 or later
- Atmel Software Framework 3.28.10 or later
- Atmel Data Visualizer Version 2.1.212 or later
- SAM L22 Xplained Pro Evaluation Kit with Micro-B USB cable

Note:

1. Jumper positions in the Xplained Pro kit: I/O - BYPASS position, MCU - MEASURE, VBAT SELECT - Open.
2. The example projects are available for both SAM L22 Xplained Pro (ATSAML22N18A with SLCD1 Xplained Pro) and SAM L22 Xplained Pro B (ATSAML22N18A with TSLCD1 Xplained Pro) kits.
3. In stand alone Advanced Software Framework, the same example projects are available for GCC and IAR compilers, which are available for download from the following location: http://www.microchip.com/avr-support/advanced-software-framework-(asf).

8. Example Project for SAM L10 and SAM L11

In Atmel START, go to BROWSE EXAMPLES and look for Low Power for SAML10/L11 example. This example demonstrates the different low-power modes of the SAM L10/L11, such as Idle mode, Standby mode, and Off mode. An RTC is used to enter or exit different modes every 5 seconds. Active mode can also be measured.

Use the following options to measure current consumptions:

1. Use Data Visualizer in Atmel Studio where power analysis window displays current power consumption, and have both Current Measurement jumpers in MEASURE position.
2. Connect an ammeter on J104, and have both Current Measurement jumpers in BYPASS position.

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- Microchip is willing to work with the customer who is concerned about the integrity of their code.

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