SmartFusion2 and IGLOO2 Power Estimator

User Guide

August 2014

Microsemi

Revision History

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8 August 2014	1	First release

Confidentiality Status

This is a non-confidential document.

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SmartFusion2 and IGLOO2 Power Estimator

Introduction

This user guide describes the SmartFusion2 and IGLOO2 Power Estimator for SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) and IGLOO®2 FPGA device families. Early power estimation helps designers to define the architecture within the power budget by applying power saving strategies. It also helps the board designers to design and select the power supplies and heat sink. The *Power Estimator* workbook enables you to estimate power consumption from early design concept to design implementation. It also provides details about thermal analysis and factors that contribute to power consumption. Device resources, Flash*Freeze settings, operating frequency, clock resources, toggle rates, and many other parameters are entered into the *Power Estimator* workbook. These parameters are then combined with the power models to estimate the power. The power models are based on simulation or characterized device data.

The accuracy of power estimation depends on the data entered into the workbook. Therefore, ensure that realistic data is entered into the design. The actual power depends greatly on actual RTL design, place-and-route, and operating conditions. The power estimator result is an early estimation of power consumption rather than measured. Use the SmartPower tool in the Libero® System-on-Chip (SoC) software for accurate and detailed power estimations for designs after place-and-route. Power must be measured during device operation.

Features

The power estimator has the following features:

- Estimation of power consumption from design concept phase to implementation.
- Integrated graphical user interface (GUI) in a worksheet to initialize the power estimator and for I/O Bank voltage settings.
- Power estimation of Active, Static, and Flash*Freeze power modes.
- Power estimation using scenarios.
- Separate worksheet for device features and also a subtotal of power consumed by each device feature.
- Junction temperature calculation and thermal input support.

Additional Documentation

Refer to the Table 1 for more information on features, resources, and I/O standard for the SmartFusion2 device.

***Table 1* • Additional Documents for SmartFusion2 Device**

Documents	Description
SmartFusion2 System-on-Chip FPGA Datasheet	This datasheet contains SmartFusion2 DC and switching characteristics.
SmartFusion2 SoC FPGA Fabric User Guide	SmartFusion2 SoC FPGA fabric architecture, memories, mathblocks, routing, and I/Os.

Table 1 • **Additional Documents for SmartFusion2 Device (continued)**

Documents	Description
SmartFusion2 Microcontroller Subsystem User Guide	SmartFusion2 devices integrate a hard microcontroller subsystem (MSS). The MSS consists of a ARM® Cortex™-M3 processor with embedded trace macrocell (ETM), instruction cache, embedded memories, DMA engines, communication peripherals, timers, real-time counter (RTC), general purpose I/Os, and FPGA fabric interfaces. This document describes the SmartFusion2 MSS and its internal peripherals.
SmartFusion2 SoC FPGA High Speed Serial and DDR Interfaces User Guide	SmartFusion2 devices integrate hard high-speed serial interfaces (PCIe, XAUI/XGXS, SERDES) for accessing external bulk memories. This document describes the SmartFusion2 high speed serial interfaces.
SmartFusion2 Clocking Resources User Guide	SmartFusion2 clocking resources include oscillators, FPGA fabric global network, and clock conditioning circuitry (CCCs) with dedicated phase-locked loops (PLLs). These clocking resources provide flexible clocking schemes to the on-chip hard IP blocks—MSS, fabric DDR (FDDR) subsystem, and high-speed serial interfaces (PCIe, XAUI/XGXS, SERDES)—and logic implemented in the FPGA fabric.
SmartFusion2 Low Power Design User Guide	In addition to low static power consumption during normal operation, SmartFusion2 devices support an ultra-low-power Static mode (Flash*Freeze mode) with power consumption less than 1 mW. Flash*Freeze mode retains all the SRAM and register data which enables fast recovery to Active mode. This document describes the SmartFusion2 Flash*Freeze mode entry and exit mechanisms.
SmartFusion2 Security and Reliability User Guide	The SmartFusion2 device family incorporates essentially all the security features that made third generation Microsemi SoC devices the gold standard for security in the PLD industry. Also included are unique design and data security features and use models new to the PLD industry. SmartFusion2 flash-based FPGA fabric has zero FIT configuration rate due to its single event upset (SEU) immunity, which is critical in reliability applications. This document describes the SmartFusion2 security features and error detection and correction (EDAC) capabilities.
SmartFusion2 Programming User Guide	Describes different programming modes supported in the SmartFusion2 devices. High level schematics of these programming methods are also provided as a reference. Important board-level considerations are discussed.

Refer to the Table 2 for more information on features, resources, and I/O standard for the IGLOO2 device.

Table 2 • **Additional Documents for IGLOO2 Device**

Documents	Description
IGLOO2 FPGA Product Brief	This product brief provides an overview of IGLOO2 family, features, and development tools.
IGLOO2 FPGA Datasheet	This datasheet contains IGLOO2 DC and switching characteristics.

Table 2 • **Additional Documents for IGLOO2 Device (continued)**

Documents	Description
IGLOO2 Pin Descriptions	This document contains IGLOO2 pin descriptions, package outline drawings, and links to pin tables in Excel format.
IGLOO2 FPGA Fabric User Guide	IGLOO2 FPGAs integrate fourth generation flash-based FPGA fabric. The FPGA fabric composed of 4-input look-up table (LUT) logic elements, includes embedded memories and mathblocks for DSP processing capabilities. This document describes the IGLOO2 FPGA fabric architecture, embedded memories, mathblocks, fabric routing, and I/Os.
IGLOO2 FPGA High Speed DDR Interfaces User Guide	IGLOO2 devices integrate hard high-speed DDR memory controllers for accessing external bulk memories. This document describes the IGLOO2 high-speed external memory interfaces.
IGLOO2 FPGA High Speed Serial Interfaces User Guide	IGLOO2 devices integrate hard high-speed serial interfaces (PCIe, XAUI/XGXS, SERDES) for accessing external bulk memories. This document describes the IGLOO2 high-speed serial interfaces.
IGLOO2 High Performance Memory Subsystem	IGLOO2 devices integrate a hard high performance memory subsystem (HPMS) that consists of embedded memories, DMA engines, and FPGA fabric interfaces. This document describes the IGLOO2 HPMS and its internal peripherals
IGLOO2 Clocking Resources User Guide	IGLOO2 clocking resources include oscillators, FPGA fabric global network, and clock conditioning circuitry (CCCs) with dedicated phase-locked loops (PLLs). These clocking resources provide flexible clocking schemes to the on-chip hard IP blocks—HPMS, fabric DDR (FDDR) subsystem, and high-speed serial interfaces (PCIe, XAUI/XGXS, SERDES)—and logic implemented in the FPGA fabric.
IGLOO2 Low Power Design User Guide	In addition to low static power consumption during normal operation, IGLOO2 devices support an ultra-low-power Static mode (Flash*Freeze mode) with power consumption less than 1 mW. Flash*Freeze mode retains all the SRAM and register data which enables fast recovery to Active mode. This document describes the IGLOO2 Flash*Freeze mode entry and exit mechanisms.
IGLOO2 Security and Reliability User Guide	The IGLOO2 device family incorporates essentially all the security features that made third generation Microsemi SoC devices the gold standard for security in the PLD industry. Also included are unique design and data security features and use models new to the PLD industry. IGLOO2 flash-based FPGA fabric has zero FIT configuration rate due to its single event upset (SEU) immunity, which is critical in reliability applications. This document describes the IGLOO2 security features and error detection and correction (EDAC) capabilities.
IGLOO2 Programming User Guide	Describes different programming modes supported in IGLOO2 devices. High level schematics of these programming methods are also provided as a reference. Important board-level considerations are discussed.

Launching Power Estimator

This section contains the following sub sections:

- System Requirement
- Downloading Power Estimator and Enabling Macros
- Minimum Input Requirements

System Requirement

1. The *Power Estimator* workbook requires Microsoft Excel. Table 3 shows the supported software.
2. Windows operating system.

Table 3 • **Supported Software**

Supported Software
Microsoft Excel 2003
Microsoft Excel 2007
Microsoft Excel 2010
Microsoft Excel 2013

Note: OpenOffice and Google Docs spreadsheet editors are not supported.

Downloading Power Estimator and Enabling Macros

The *Power Estimator* workbook for SmartFusion2 and IGLOO2 devices are available in the Microsemi *Power Calculators* web page. The latest version can be downloaded from: http://www.microsemi.com/products/fpga-soc/design-resources/power-calculator.

The *Power Estimator* workbook has many built-in macros. By default, the macro security level in Microsoft Excel software is set to High. The macros are automatically disabled if the macro security level is set to High. So, ensure that Microsoft Excel settings allow macro executions for the Power Calculator workbook to function properly.

The following sections describe how to change the macro security settings in different versions of Microsoft Excel software:

- "Microsoft Excel 2003" on page 7
- "Microsoft Excel 2007" on page 7
- "Microsoft Excel 2010 and 2013" on page 9

Microsoft Excel 2003

1. Open the *Power Calculator* Excel file and select **Tools** > **Macro** > **Security** from the main menu.

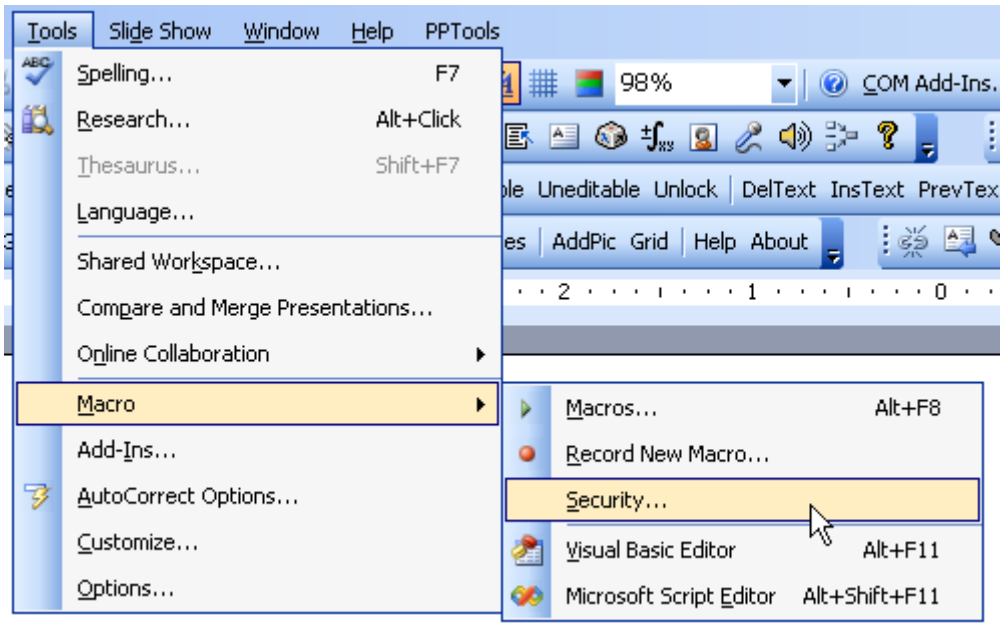

Figure 1 • **Macro Security Level Settings in Microsoft Excel 2003**

2. From the **Macro Security** dialogue box, click **Security Level** tab and then select **Medium**. Then click **OK**.
3. Close the *Power Calculator* file and reopen it.
4. Click **Enable Macros** when prompted to enable macros.

Microsoft Excel 2007

1. Open the *Power Calculator* Excel file and click the **Office** button at the upper left corner.

2. Click **Excel Options**.

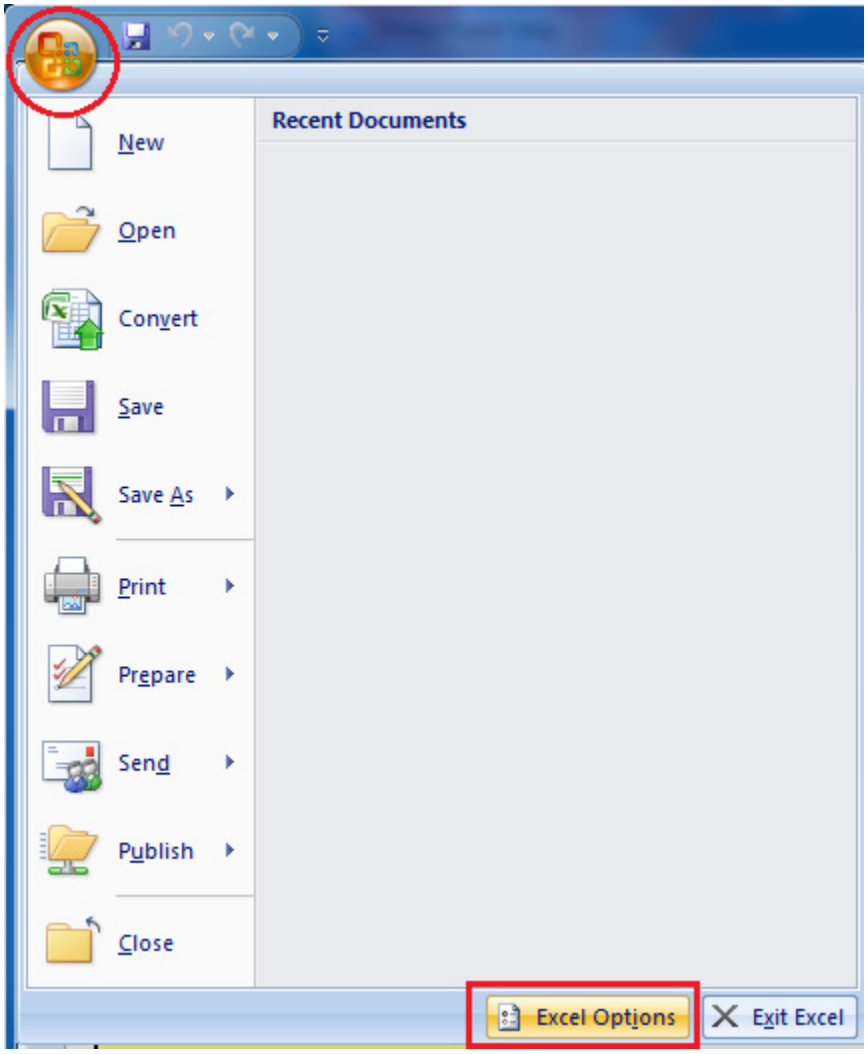

Figure 2 • **Macro Security Level Settings in Microsoft Excel 2007**

3. Click **Trust Center** from the left panel.
4. Click **Trust Center Settings...**.
5. From the **Trust Center** window, click **Macro Settings** from the left panel. Select **Disable all macros with notification** and then click **OK**.
6. Close the *Power Calculator* file and reopen it.
7. A security warning notification appears under the **Office** ribbon, click the **Options** button.
8. Choose **Enable this content** in the **Microsoft Office Security Options** window.

Microsoft Excel 2010 and 2013

1. Open the *Power Calculator* Excel file.
2. Click the **File** tab and then click **Options**.

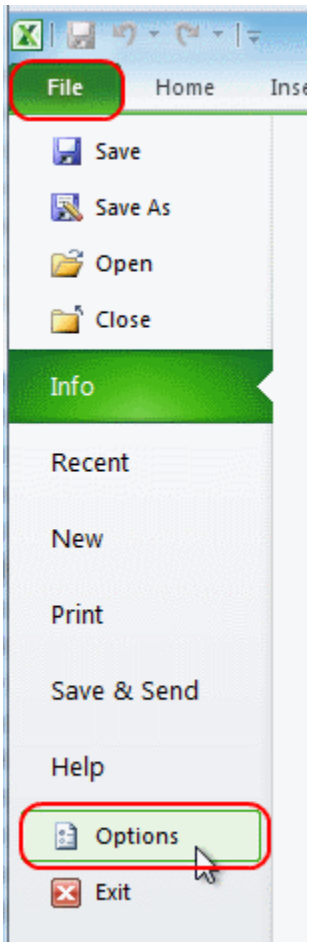

Figure 3 • **Macro Security Level Settings in Microsoft Excel 2010 and 2013**

3. Click **Trust Center** from the left panel.
4. Click **Trust Center Settings...**.
5. From the Trust Center window, click **Macro Settings** from the left panel. Select **Disable all macros with notification** and then click **OK**.
6. Close the *Power Calculator* file and reopen it.
7. A security warning notification appears under the **Office** ribbon. Click the **Options** button.
8. Choose **Enable this content** in the **Microsoft Office Security Options** window.

Minimum Input Requirements

Estimating power for SmartFusion2 SoC FPGA and IGLOO2 FPGA devices are highly dependent on the amount of logic present in the FPGA Fabric. The following are the minimum input requirements for a reasonably accurate power estimation.

- Select a proper device with suitable operating conditions
- Proper estimation of FPGA Fabric resources (For example, flip-flops, LUTs, LSRAM, uSRAM, MACC, and I/O).

- Proper estimation of MSS/HPMS peripherals.
- Proper estimation of high speed serial and DDR interfaces.
- System clock and clock domain.
- Toggle rates of logic and I/Os.

Power Estimator Excel Workbook

This section describes each worksheet of the SmartFusion2and IGLOO2 Power Estimator Excel workbook. Separate worksheets for device features are available and also a subtotal of power consumed by each device feature is available. The usage and activity details of the different resources available in the targeted SmartFusion2/IGLOO2 device can be entered (For example, flip-flops, LUTs, LSRAM, uSRAM, MACC, I/O, high speed serial and DDR interfaces, system clock and clock domain, toggle rates of logic, and I/Os). The **Power Summary** section in the *Summary* worksheet provides the total power and the power breakdown based on the power sources and rail.

This section contains the following sub sections:

- Cell Color-Coding
- Recommended Flow

Cell Color-Coding

The *Power Estimator* worksheet cells are color coded to simplify the data entry and review. Table 4 lists the cell colors and description.

Table 4 • **Cell Color Coding**

Cell color	User Action	Description
	Editable	User can enter data.
	Non Editable	User cannot enter data.
	Read-Only	Calculated values.
	Read-Only	Summary values.
	Read-Only	Error

Recommended Flow

Step - 1: Settings

Select the Device, temperature grade, operating condition and thermal inputs settings.

Step - 2: Active Mode Configuration

Set up the design specific information that is used to compute the dynamic power.

- FPGA Fabric Components:
  - Set up the FPGA fabric components and their operating frequencies.
- I/Os:
  - Set up the I/O technology and their operating frequencies.
- Built-in Blocks (MSS/HPMS, SERDES and FDDR):
  - Set up the peripherals and their operating frequencies.

Step - 3: Scenarios

Optional: Update the percentage of time the device should be in a given mode during its operational time (for instance, 50% of the time Active and 50% in Flash*Freeze).

Step - 4: Power Estimation Summary

The power summary section in the *Summary* worksheet provides the total power and its breakdown based on the power sources and rails. The total power for the scenario and the low power mode power consumption is displayed in the scenario section.

The following sections describe these steps in detail

- "Step - 1: Settings" on page 12
- "Step - 2: Active Mode Configuration" on page 15
- "Step - 3: Scenarios" on page 33
- "Step - 4: Power Estimation Summary" on page 34

Step - 1: Settings

Figure 4 shows the **Settings** section in the *Summary* worksheet.

Settings

General	
Family	SmartFusion2
Device	M2S050T
Package	896 FBGA
Range	Commercial
Core Voltage	**1.2V**
Process	Typical
Data State	**Preliminary**

Flash*Freeze Settings	
µSRAM state	Sleep
LSRAM state	Sleep
MSS StandBy Clock	32 KHz

Thermal Inputs	
○ User Entered Tj	◉ Estimated Tj
Ambient Temperature Ta (°C)	25.00
○ Custom Theta JA	◉ Estimated Theta JA
Effective Θ_{JA}	5.01
Heat Sink	15 mm - Medium Profile
Air Flow	2.5 m/s
Custom Θ_{SA} (°C/W)	3.0
Board Thermal Model	JEDEC (2s2p)

Figure 4 • **Settings Section in the Summary Worksheet**

Table 5 shows the General, Flash*Freeze, and Thermal Inputs settings in the Settings section of the Summary worksheet. Ensure that you select the device with the appropriate operating conditions.

Table 5 • **General and Flash*Freeze Settings**

Parameters	Description
General Settings	
Family	Select the device family. The following device families are available: • SmartFusion2 • IGLOO2
Device	Select the device. All SmartFusion2 and IGLOO2 devices are available.
Package	Select the package.
Range	Select the product grade The following grades are available. • Commercial • Industrial • Military Temperature grade for different ranges: • Commercial (0°C to 85°C) • Industrial (-40°C to 100°C) • Military (-55°C to 125°C)
Core Voltage	Core supply voltage (1.2 V)
Process	Select the process The following conditions are available: • Typical • Maximum Process accounts for manufacturing process variations that affect power dissipation. **Typical** uses average power dissipation factors for your design. **Maximum** uses the highest power dissipation factors. Voltage and Temperature are controlled independent of the process.
Data State	**Advanced**: Initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. **Preliminary**: Information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible. **Production**: Information that is considered to be final.
Flash*Freeze Settings	
uSRAM State	Select uSRAM state during Flash*Freeze: • Suspend • Sleep

Table 5 • **General and Flash*Freeze Settings**

Parameters	Description
LSRAM State	Select LSRAM state during Flash*Freeze: • Suspend • Sleep
MSS StandBy Clock	Select MSS StandBy Clock: • 32KHz • 1 MHz • 50 MHz MSS is always powered during Flash*Freeze mode and is clocked by the 50 MHz RC oscillator, 1 MHz RC oscillator, or the main crystal oscillator (32 KHz - 20 MHz).
Thermal Inputs	
Junction Temperature Tj (°C)	Enter the Junction Temperature of the device. This field is available only when the **User Entered T_J** option is selected. In this case, other thermal input fields are disabled. When the **Estimated T_J** option is selected, the junction temperature is calculated based on the thermal inputs entered.
Ambient Temperature Ta (°C)	Enter the temperature of the air surrounding the device. This field is available only if the **Estimated T_J** option is selected. Valid temperature ranges are: Commercial: 0° C to 85° C Industrial: -40° C to 100° C Military: -55° C to 125° C When the **Estimated Theta J_A** option is selected, this field is used to calculate the junction temperature based on the thermal resistance and the power dissipation. When the **Custom Theta J_A** option is selected, this field is used to calculate the junction temperature based on the effective θ_{JA} and the power dissipation.
Effective θ_{JA}	Effective thermal resistance: User selected device, package, airflow, heat sink and board model are used with characterization and simulation data to calculate effective thermal resistance. To enter a custom effective Theta JA select the radio button **Custom Theta JA** and enter a value, to account for conditions not covered by the available choices or where more extensive thermal modeling has been done. The following fields are disabled when **Custom Theta JA** is selected and enabled when **Estimated Theta JA** is selected: • Heat Sink • Air Flow • Custom θ_{SA} (°C/W) • Board Thermal Model

Table 5 • **General and Flash*Freeze Settings**

Parameters	Description
Heat Sink	Select one of the following options: • None • Custom • 10 mm-Low Profile • 15 mm-Medium Profile • 20 mm-High Profile This field is enabled only when the **Estimated T_J** and the **Estimated Theta JA** options are selected.
Airflow	Select an ambient airflow in meter per second (m/s): • 1.0 m/s • 2.5 m/s This field is enabled only when the **Estimated T_J** and the **Estimated Theta JA** options are selected. The junction temperature is reduced if the ambient airflow is increased.
Custom θ_{SA} (°C/W)	If a custom heat sink is selected, enter the heat sink-to-ambient thermal resistance from the heat sink datasheet. This field is enabled only when the **Estimated T_J** and the **Estimated Theta JA** options are selected.
Board Thermal Model	Select one of the following options: • None (Conservative) • JEDEC (2s2p) This field is enabled only when the **Estimated T_J** and the **Estimated Theta JA** options are selected. If **None (Conservative)** option is selected, the thermal model assumes that no heat is dissipated through the board. If **JEDEC (2s2p)** option is selected, the thermal model assumes that the characteristics is of the JEDEC 2s2p test board specified in standard JESD51-9.

Step - 2: Active Mode Configuration

In this section, enter design specific information that can be used to compute dynamic power.

It contains the following subsections:

- "Initialize Power Estimator Wizard" on page 16
- "FPGA Fabric Components" on page 17
- "I/Os" on page 24
- "Built-in Blocks" on page 27

Initialize Power Estimator Wizard

The *Summary* worksheet has an integrated power estimator wizard. Click **Initialize Power Estimator** at the top left of the worksheet to invoke the **Initialize Power Estimator** wizard. This wizard enables you to select design specific information. Upon running the wizard, it populates the power estimator spreadsheet with design specific information and estimates power for the design. Change the wizard populated entries to provide more accurate inputs to the power estimator. Figure 5 shows the **Initialize Power Estimator** wizard.

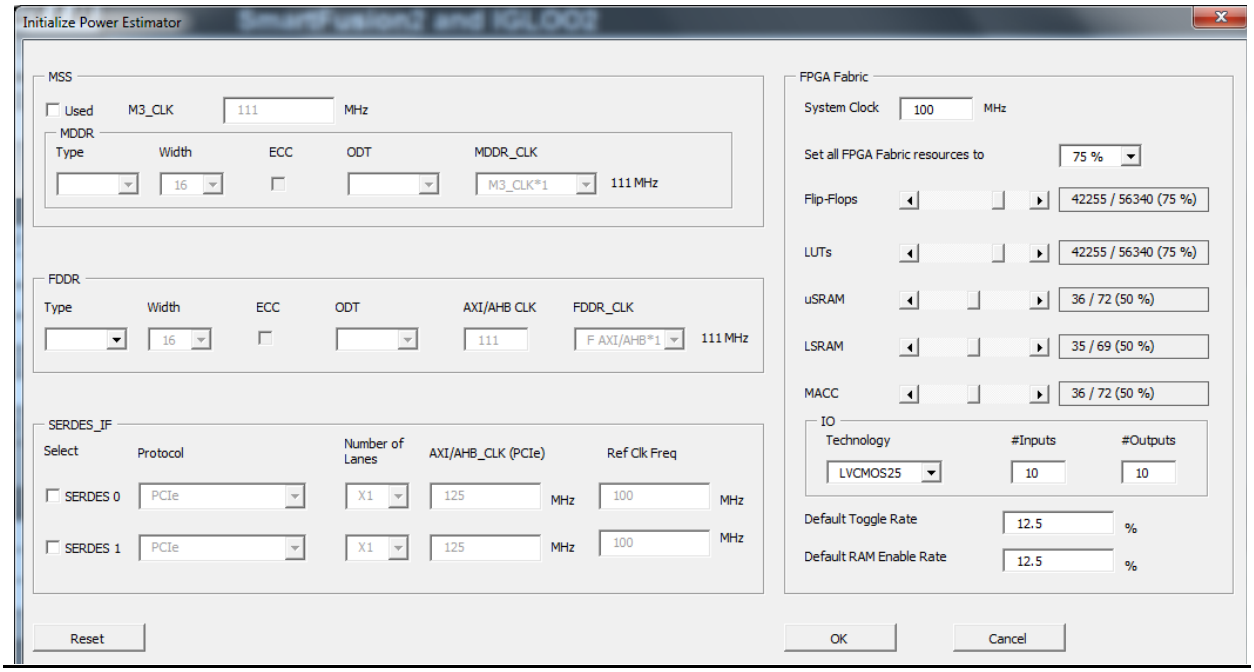

Figure 5 • **Power Estimator Wizard**

The **Power Estimator** wizard provides following fields depending on the product family selected:

- MSS/HPMS

  Select the check box to enable MSS/HPMS entries. The following options are available:

  – **M3_CLK/ HPMS_CLK**:

  Specify the Cortex-M3 processor/HPMS clock frequency. By default, it is set to 111 MHz, valid entries are between 0 and 167 MHz.

  – **MDDR/ HPMS_DDR**:

  Select the memory type, width, ECC, ODT and MDDR_CLK / HPMS_DDR_CLK. Maximum frequency of MDDR_CLK / HPMS_DDR_CLK is 333 MHz.

- **FDDR**

  Select the memory type, width, ECC, ODT and FDDR_CLK. Maximum frequency of FDDR_CLK is 333 MHz.

- **SERDES_IF**

  Select SERDES, Protocol, Number of Lanes and AXI/AHB_CLK (PCIe) clock.

- **FPGA Fabric**

  – **System Clock**

  Specify the Fabric clock frequency. By default, it is set to 100 MHz. Valid entries are between 0 and 400 MHz.

  – **Design Utilization**

Use the drop down menu against **Set all FPGA Fabric Resources to** set a percentage value for all the resources at one go. Percentage value for each resource to be utilized can be set using the slide bar against the resources. Following are the available resources:

* Flip-Flops

* LUTs

* uSRAM

* LSRAM

* MACC

– **I/O**

Select the I/O technology and enter the number of inputs and outputs.

– **Default Toggle Rate**

Enter a toggle rate in percentage. This toggle rate applies to all logic module and I/Os.

– **Default RAM Enable Rate**

Enter an enable rate in percentage. This enable rate applies to uSRAM and LSRAM.

Note: When the slider thumb moves between the end points of the slider track, the value is updated in the corresponding text field.

To populate the power calculator spreadsheet with the entered values, click **OK**.

FPGA Fabric Components

This section describes the design specific information for FPGA Fabric components that are used to calculate dynamic power. The SmartFusion2and IGLOO2 Power Estimator workbook provides separate worksheets for each FPGA Fabric component. These worksheets are described in the following subsections:

- "Clock" on page 17
- "Logic" on page 18
- "LSRAM" on page 19
- "uSRAM" on page 20
- "Math Block" on page 21
- "FAB_CCC and Oscillators" on page 22

Clock

SmartFusion2 SoC FPGA and IGLOO2 FPGA support only global clock networks. Each row in the clock worksheet represents a separate clock domain. Enter the following parameters for each clock domain.

- Name
- Clock Frequency (MHz)
- Fanout
- Global Enable Rate

Figure 6 shows the *Clock* worksheet in the *Power Estimator* workbook.

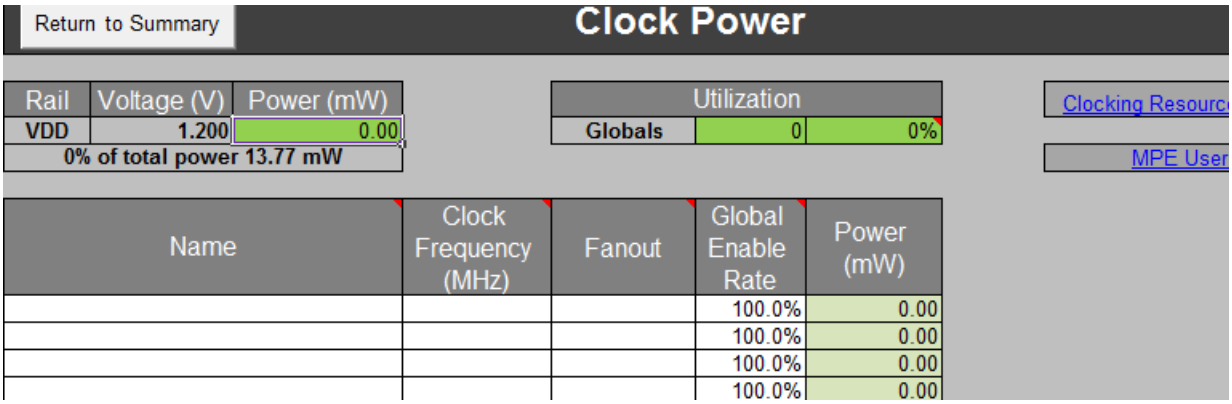

Figure 6 • **Clock Worksheet**

Table 6 shows the parameters to be entered in the *Clock* worksheet.

Table 6 • **Clock Worksheet Parameters**

Parameters	Description
Name	Enter a name for each clock domain (optional)
Clock Frequency (MHz)	Enter the clock frequency of the domain. The maximum frequency of the FPGA fabric is 400 MHz.
Fanout	Enter the number of registers and other synchronous elements (LSRAM, uSRAM, Math Block and I/O) clocked.
Global Enable Rate	Enter the average percentage of time that clock enable is high for each clock domain.

For more information about the clock networks of the supported device families, refer to the respective device clocking resources user guides.

Logic

Each row in the *Logic* worksheet represents a separate clock domain. Enter the following parameters for each clock domain.

- Name
- Clock Frequency (MHz)
- Number of Registers
- Number of LUTs
- Fanout
- Toggle Rate

Figure 7 shows the *Logic* worksheet.

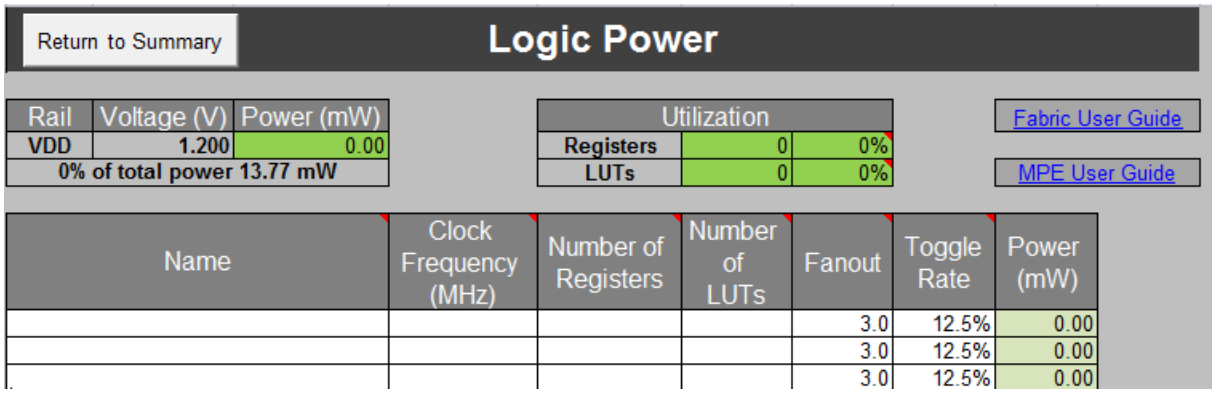

Figure 7 • **Logic Worksheet**

Table 7 shows the parameters to be entered in the *Logic* worksheet.

Table 7 • **Logic Worksheet Parameters**

Parameters	Description
Name	Enter a name for each clock domain (optional)
Clock Frequency (MHz)	Enter the clock frequency of the domain. The maximum frequency of the FPGA fabric is 400 MHz.
Number of Registers	Enter the number of registers for each clock domain.
Number of LUTs	Enter the number of regular LUT (combinatorial) modules.
Average Fanout	Enter the average fanout of the nets driven by the registers and LUTs.
Toggle Rate	Enter the toggle rate of register and LUTs outputs.

For more information about the Logic Element of the supported device families, refer to the respective device fabric architecture user guides.

LSRAM

Each row in the LSRAM worksheet represents a separate clock domain. Enter the following parameters for each clock domain.

- Name
- Number of LSRAM blocks
- Port A - Clock Frequency (MHz)
- Port A - Write Rate
- Port A - Enable Rate
- Port B - Clock Frequency (MHz)
- Port B - Write Rate
- Port B - Enable Rate

Figure 8 shows the *LSRAM* worksheet.

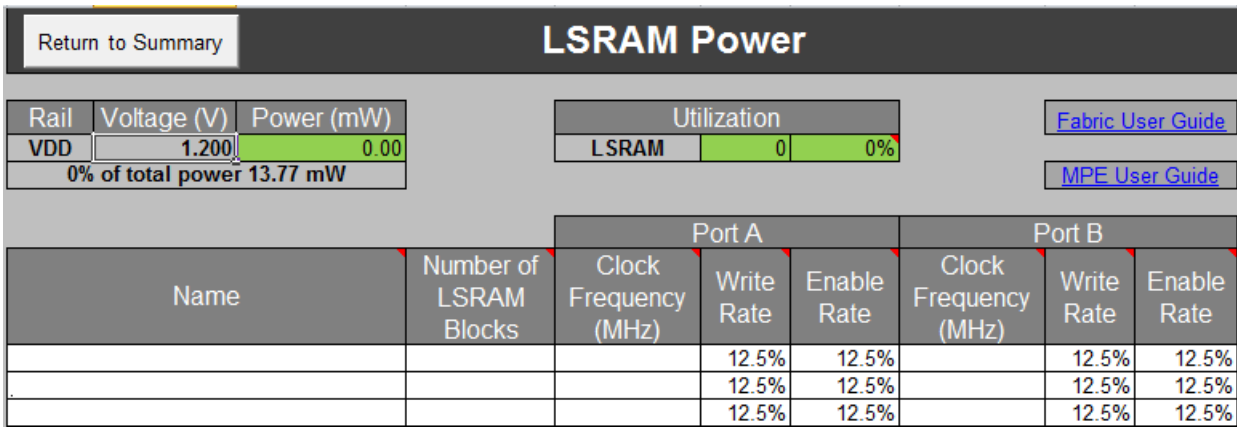

Figure 8 • **LSRAM Worksheet**

Table 8 shows the parameters to be entered in the *LSRAM* worksheet.

Table 8 • **LSRAM Worksheet Parameters**

Parameters	Description
Name	Enter the name of the module or clock domain containing the LSRAM.
Number of LSRAM blocks	Enter the number of LSRAM blocks.
Port A - Clock Frequency (MHz)	Enter the clock frequency for Port A of the LSRAM blocks. It supports a maximum frequency of up to 400 MHz.
Port A - Write Rate	Enter the percentage of time that Port A is used for write operations. The remaining time is used for read operations.
Port A - Enable Rate	Enter the percentage of time that Port A is enabled.
Port B - Clock Frequency (MHz)	Enter the clock frequency for Port B of the LSRAM blocks. It supports a maximum frequency of up to 400 MHz.
Port B - Write Rate	Enter the percentage of time that Port B is used for write operations. The remaining time is used for read operations.
Port B - Enable Rate	Enter the percentage of time that Port B is enabled.

For more information about the LSRAM of the supported device families, refer to the respective device fabric architecture user guides.

uSRAM

Each row in the uSRAM worksheet represents a separate clock domain. Enter the following parameters for each clock domain.

- Name
- Number of uSRAM blocks
- Port A - Read Clock Frequency (MHz)
- Port A - Enable Rate
- Port B - Read Clock Frequency (MHz)
- Port B - Enable Rate
- Port C - Write Clock Frequency (MHz)
- Port C - Enable Rate

Figure 9 shows the *uSRAM* worksheet.

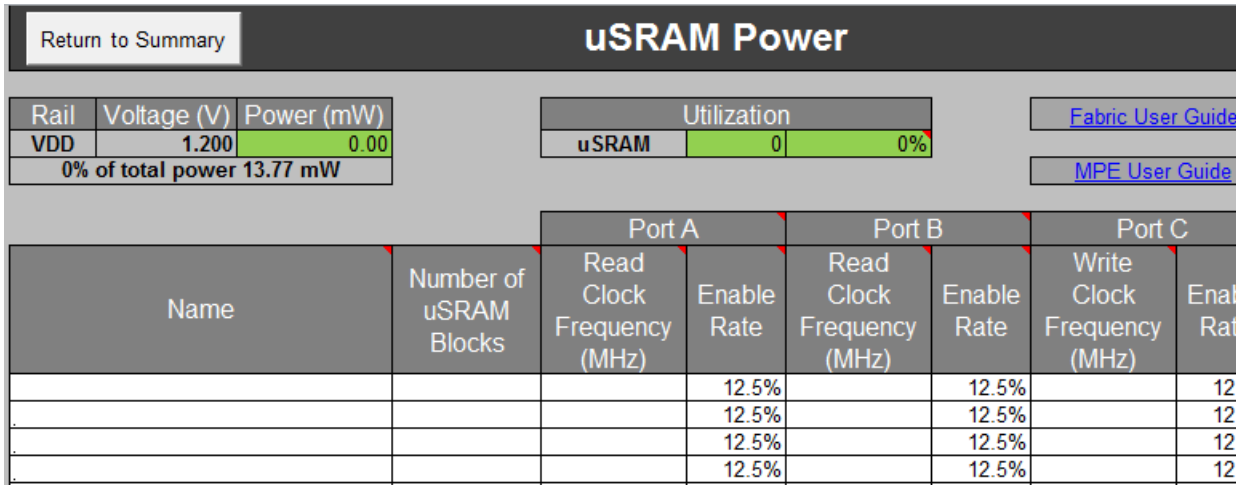

Figure 9 • **uSRAM Worksheet**

Table 9 shows the parameters to be entered in the uSRAM worksheet.

Table 9 • **uSRAM Worksheet Parameters**

Parameters	Description
Name	Enter the name of the module or clock domain containing the uSRAM.
Number of uSRAM blocks	Enter the number of uSRAM blocks.
Port A - Read Clock Frequency (MHz)	Enter the read clock frequency for Port A of the uSRAM blocks. It supports a maximum frequency of up to 400 MHz.
Port A - Enable Rate	Enter the percentage of time that Port A is enabled.
Port B - Read Clock Frequency (MHz)	Enter the read clock frequency for Port B of the uSRAM blocks. It supports a maximum frequency of up to 400 MHz.
Port B - Enable Rate	Enter the percentage of time Port B is enabled.
Port C - Write Clock Frequency (MHz)	Enter the write clock frequency for Port C of the uSRAM blocks. It supports a maximum frequency of up to 400 MHz.
Port C - Enable Rate	Enter the percentage of time that Port C is enabled.

For more information about the uSRAM of the supported device families, refer to the respective device fabric architecture user guides.

Math Block

Each row in the Math Block worksheet represents a separate clock domain. Enter the following parameters for each clock domain.

- Name
- Clock Frequency (MHz)
- Number of Math Blocks
- Data Toggle Rate

Figure 10 shows the Math Block worksheet.

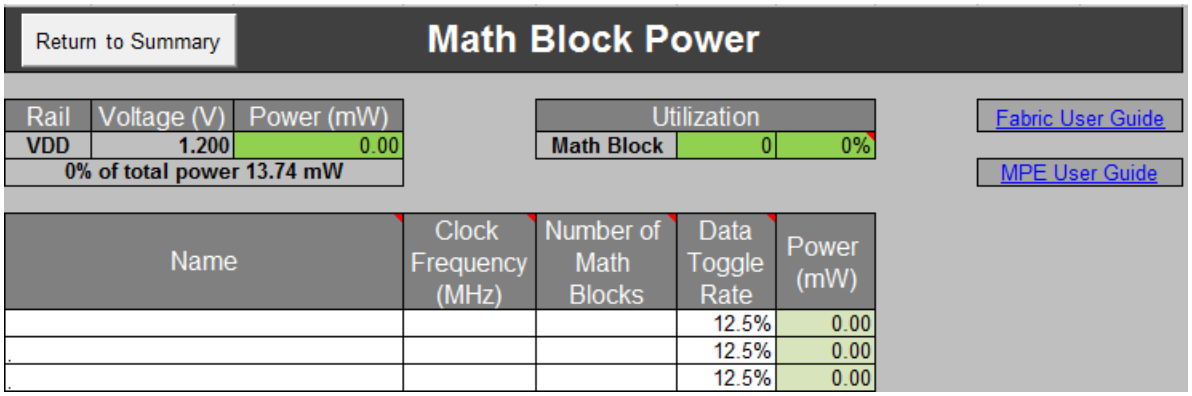

Figure 10 • **Math Block Worksheet**

Table 10 lists the parameters to be entered in the Math block worksheet.

Table 10 • **Math Block Worksheet Parameters**

Parameters	Description
Name	Enter the name of the module or clock domain containing Math Block.
Clock Frequency (MHz)	Enter the clock frequency of the domain. The maximum frequency of the Math Block is 400 MHz.
Number of Math Blocks	Enter the number of math blocks for each clock domain.
Data Toggle Rate	Enter the average data bus toggle rate.

For more information about the Math Block of the supported device families, refer to the respective device fabric architecture user guides.

FAB_CCC and Oscillators

SmartFusion2 devices have an external main crystal oscillator and an auxiliary crystal oscillator that is dedicated to the MSS RTC clocking as an alternative clock source. IGLOO2 devices have only an external main crystal oscillator. If either of the oscillators is used, select **Yes** from the corresponding drop-down list under the **Used** column of the **Oscillator Power** table. Input frequencies for the oscillators must be entered.

Figure 11 shows the Oscillator Power section of the CCC & Oscillator worksheet.

Return to Summary

FAB_CCC and Oscillator Power

Rail	Voltage (V)	Power (mW)
VDD	1.200	0.00
PLL_VDDA	2.500	0.00
Total Power		0.00
0% of total power 6.44 mW		

Resource	Power (mW)
CCC	0.00
Oscillator	0.00

Uti
CCC

Clocking Resource

MPE User

Oscillator Power

Oscillator	Used	Frequency (MHz)	VDD Power (mW)
Ext. Main Crystal	No		0.00
RTC Ext. Crystal	No		0.00

Figure 11 • **Oscillator Power Section**

For more information about the On-Chip Oscillators of the supported device families, refer to the respective device Clocking Resources User Guides.

SmartFusion2/IGLOO2 devices have two, six, or eight fabric CCCs. Each fabric CCC enables flexible clocking schemes for the logic implemented in the FPGA fabric and can provide the base clock for on-chip hard IP blocks such as MSS/HPMS, FDDR, and SERDESIF. Enter the following parameters for each fabric CCC:

- Name
- Reference Clock Frequency (MHz)
- PLL Output Frequency (MHz)
- Output1 Frequency (MHz)
- Output2 Frequency (MHz)
- Output3 Frequency (MHz)
- Output4 Frequency (MHz)

Figure 12 shows the FAB_CCC Power section in the CCC & Oscillators worksheet.

FAB_CCC Power

Name	Reference Clock Frequency (MHz)	PLL Output Clock Frequency (MHz)	Output1 Frequency (MHz)	Output2 Frequency (MHz)	Output3 Frequency (MHz)	Output4 Frequency (MHz)	VDD Power (mW)	PLL_VDDA Power (mW)
							0.00	0.00
							0.00	0.00
							0.00	0.00
							0.00	0.00
							0.00	0.00
							0.00	0.00
							0.00	0.00
							0.00	0.00

Figure 12 • **FAB_CCC Power Section**

Table 11 shows the parameters to be entered in the FAB_CCC Power section of the CCC & Oscillator worksheet.

***Table 11* • FAB_CCC Section Parameters**

Parameters	Description
Name	Enter the name of the CCC module.
Reference Clock Frequency (MHz)	Enter the reference clock frequency.
PLL Output Frequency (MHz)	Enter the PLL output frequency.
Output1 Frequency (MHz)	Enter the output1 (GL0/Y0) frequency.
Output2 Frequency (MHz)	Enter the output2 (GL1/Y1) frequency.
Output3 Frequency (MHz)	Enter the output3 (GL2/Y2) frequency.
Output4 Frequency (MHz)	Enter the output4 (GL3/Y3) frequency.

For more information about the FAB_CCC of the supported device families, refer to the respective device Clocking Resources User Guides.

I/Os

Design specific information are entered in the *IO* worksheet for the I/Os used to calculate dynamic power. Each row represents a clock frequency and an I/O domain. Enter the following parameters for each row:

- Name
- Bank Type
- I/O standard
- I/P Pins
- O/P Pins
- Bidir Pins
- ODT
- Output Drive (mA)
- Output Load (pF)
- Clock (MHz)
- Data Rate
- Toggle Rate
- Output Enable
- ODT Enable

Figure 13 shows the I/O Power worksheet.

Return to Summary

I/O Power

Rail	Voltage (V)	Current (mA)	Power (mW)
VDD	1.200	0.00	0.00
VDDI 1.2	1.200	0.00	0.00
VDDI 1.5	1.500	0.00	0.00
VDDI 1.8	1.800	0.00	0.00
VDDI 2.5	2.500	0.00	0.00
VDDI 3.3	3.300	0.00	0.00
Total Power			0.00
0% of total power 7.89 mW			

MPE User Guide

Fabric User Guide

Utilization		
Inputs	0	0%
Outputs	0	0%
Bidirectional	0	0%
MSIO	0	0%
MSIOD	0	0%
DDRIO	0	0%
I/O Count	0	0%

☐ Show Advanced I/O Settings

I/O Bank Settings

	I/O Settings								I/O Activity					Power (mW)		
Name	Bank Type	I/O Standard	I/P Pins	O/P Pins	Bidir Pins	ODT	Output Drive (mA)	Output Load (pF)	Clock (MHz)	Data Rate	Toggle Rate	Output Enable	ODT Enable	VDD	VDDI	Total
	MSIO	LVCMOS25				NO_ODT	2	5		data	12.5%	50.0%		0.00	0.00	0.00
	MSIO	LVCMOS25				NO_ODT	2	5		data	12.5%	50.0%		0.00	0.00	0.00
	MSIO	LVCMOS25				NO_ODT	2	5		data	12.5%	50.0%		0.00	0.00	0.00
	MSIO	LVCMOS25				NO_ODT	2	5		data	12.5%	50.0%		0.00	0.00	0.00
	MSIO	LVCMOS25				NO_ODT	2	5		data	12.5%	50.0%		0.00	0.00	0.00

Figure 13 • **I/O Power Worksheet**

Table 12 shows the parameters to be entered in the IO Power worksheet. The advanced I/O settings, Schmitt trigger, Pre-emphasis, and Slew are not visible by default. Check the **Show Advanced I/O Settings** check box to unhide these columns.

***Table 12* • I/O Power Worksheet Parameters**

Parameters		Description
Name		Enter a name for each I/O, bus or module.
I/O Settings	Bank Type	Select the bank type. Supports the followings types of banks: • MSIO • MSIOD • DDRIO
	I/O standard	Select the appropriate I/O standard.
	I/P Pins	Enter the number of input pins or differential pair used for each I/O, bus or module. The differential pair should be considered as a single pin.
	O/P Pins	Enter the number of output pins or differential pair used for each I/O, bus or module. The differential pair should be considered as a single pin.
	Bidir Pins	Enter the number of bidirectional pins or differential pair used for each I/O, bus or module. The differential pair should be considered as single pin.
	ODT	Select the Input On-die termination impedance.
	Output Drive (mA)	Select the output drive current.
	Output Load (pF)	Enter the board and other external capacitance.
	Schmitt Trigger	Configure (Yes/No) Schmitt trigger.
	Pre-emphasis	The choices for Pre Emphasis depends on the I/O type (MSIO/MSIOD/DDRIO) and I/O standard. Configure (No/Low/Medium/High) Pre-emphasis.
	Slew	Configure (Slow/Medium/Medium_Fast/Fast) Slew. The choices for Slew depends on the I/O type (MSIO/MSIOD/DDRIO) and the I/O standard.
I/O Activity	Clock (MHz)	Enter the clock frequency of the domain. It supports a maximum frequency of up to 400 MHz.
	Data Rate	For I/Os used as clocks, select **clock** as Data Rate. For others, select **data**.
	Toggle Rate	Enter the average percentage of input, output, and bidirectional pins toggling.
	Output Enable	Enter the percentage of time output pins are enabled. For bidirectional I/Os the input pins are active when the output pins are disabled.
	ODT Enable	ODT Enable is applicable only: • For DDRIO Inputs and Bidirectional pins (if they are connected for FDDR or MDDR) • For the standards: LPDDR, SSTL18 and SSTL15 • If ODT is enabled

For more information about the I/Os of the supported device families, refer to the respective device FPGA Fabric Architecture User Guides.

I/O Bank Settings Wizard

The I/O worksheet has an integrated **I/O Bank Settings** wizard. Click the **I/O Bank Settings** button to invoke the **I/O Bank Settings** wizard. This wizard enables you to select the I/O bank voltage for each I/O Bank. Upon running the wizard, it populates the Bank static power in the **Active Mode: Type Breakdown** table in the Power Summary section of the *Summary* worksheet, as shown in Figure 20 on page 33. By default, voltages of all banks are set to 1.2 V and bank static power is populated accordingly.

Figure 14 shows the I/O Bank Settings wizard.

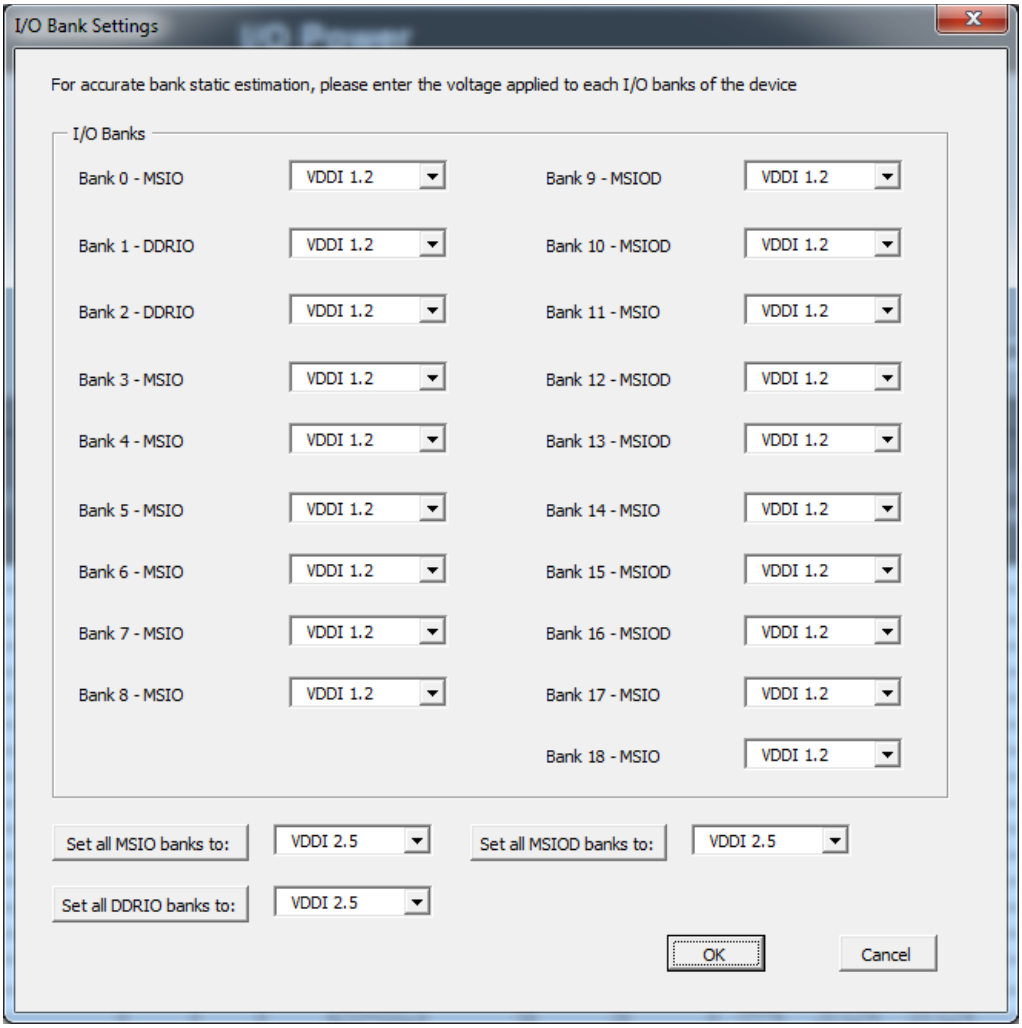

Figure 14 • **I/O Bank Settings Wizard**

Built-in Blocks

Design specific information for built-in blocks (MSS/HPMS, SERDES, and FDDR) are entered to calculate the dynamic power. This section contains the following subsections:

- "SERDES" on page 28
- "MSS/HPMS and FDDR" on page 29

SERDES

SERDES worksheet is visible only for T and TS devices. SmartFusion2/IGLOO2 devices have up to 4 hard high-speed serial interface blocks and it depends on the device selected. Each row in the SERDES worksheet represents a single (X1) or multiple (X2/X4) SERDES lane. Enter the following parameters for each SERDES block.

- Name
- Location
- Protocol
- Number of Lanes
- Speed (Gbps)
- PCI F AXI/AHB (MHz)
- Data Rate (Mbps)

Figure 15 shows the *SERDES* worksheet.

Name	Location	Protocol	Number of Lanes	Speed (Gbps)	Reference Clock Frequency (MHz)	Hard Block	PCIe F AXI/AHB (MHz)	Data Rate (Mbps)	VCO Rate (MHz)	FPGA Interface Frequency (MHz)	VDD Power (mW)	VDDAIO Power (mW)	VDDAPLL Power (mW)	PLL_VDDA Power (mW)
	Unused	PCIe	X1	2.5 (GEN1)	100	PCIe		N/A	N/A	N/A	0.00	0.00	0.00	0.00
	Unused	PCIe	X1	2.5 (GEN1)	100	PCIe		N/A	N/A	N/A	0.00	0.00	0.00	0.00
	Unused	PCIe	X1	2.5 (GEN1)	100	PCIe		N/A	N/A	N/A	0.00	0.00	0.00	0.00
	Unused	PCIe	X1	2.5 (GEN1)	100	PCIe		N/A	N/A	N/A	0.00	0.00	0.00	0.00
	Unused	PCIe	X1	2.5 (GEN1)	100	PCIe		N/A	N/A	N/A	0.00	0.00	0.00	0.00
	Unused	PCIe	X1	2.5 (GEN1)	100	PCIe		N/A	N/A	N/A	0.00	0.00	0.00	0.00
	Unused	PCIe	X1	2.5 (GEN1)	100	PCIe		N/A	N/A	N/A	0.00	0.00	0.00	0.00
	Unused	PCIe	X1	2.5 (GEN1)	100	PCIe		N/A	N/A	N/A	0.00	0.00	0.00	0.00
	Unused	PCIe	X1	2.5 (GEN1)	100	PCIe		N/A	N/A	N/A	0.00	0.00	0.00	0.00
	Unused	PCIe	X1	2.5 (GEN1)	100	PCIe		N/A	N/A	N/A	0.00	0.00	0.00	0.00
	Unused	PCIe	X1	2.5 (GEN1)	100	PCIe		N/A	N/A	N/A	0.00	0.00	0.00	0.00
	Unused	PCIe	X1	2.5 (GEN1)	100	PCIe		N/A	N/A	N/A	0.00	0.00	0.00	0.00
	Unused	PCIe	X1	2.5 (GEN1)	100	PCIe		N/A	N/A	N/A	0.00	0.00	0.00	0.00
	Unused	PCIe	X1	2.5 (GEN1)	100	PCIe		N/A	N/A	N/A	0.00	0.00	0.00	0.00
	Unused	PCIe	X1	2.5 (GEN1)	100	PCIe		N/A	N/A	N/A	0.00	0.00	0.00	0.00

Figure 15 • **SERDES Power Worksheet**

Table 13 shows the parameters to be entered in the SERDES worksheet.

***Table 13* • SERDES worksheet parameters**

Parameters	Description
Name	Enter a name for each SERDES block. Name is optional. Each SERDES block can be configured as X1, X2, or X4 lanes. Configurations can be: Four X1s or two X2s or a single X4. Depending on the configuration of lanes in SERDES block, the number of rows varies.
Location	Select the SERDES location. Each SERDES can use up to 4 lanes and it depends on the device selected.
Protocol	Select the protocol. It supports PCIe, XAUI and EPCS protocols. When EPCS protocol is chosen, the supported speeds are listed. Refer to Figure 16. Custom speed and data width can be selected from the **Data Rate (Mbps)** drop-down list. VCO Rate and FPGA Interface Frequencies are populated based on the data rate selected.
Number of Lanes	Select the number of lanes. It supports X1, X2, and X4.
Speed (Gbps)	Select the data rate for the selected protocol.
PCIe F AXI/AHB (MHz)	Enter the clock frequency of the AXI/AHB interface. It supports a maximum frequency of up to 200 MHz.
Data Rate (Mbps)	Select the custom speed and data width. This field is enabled only when EPCS protocol is selected.

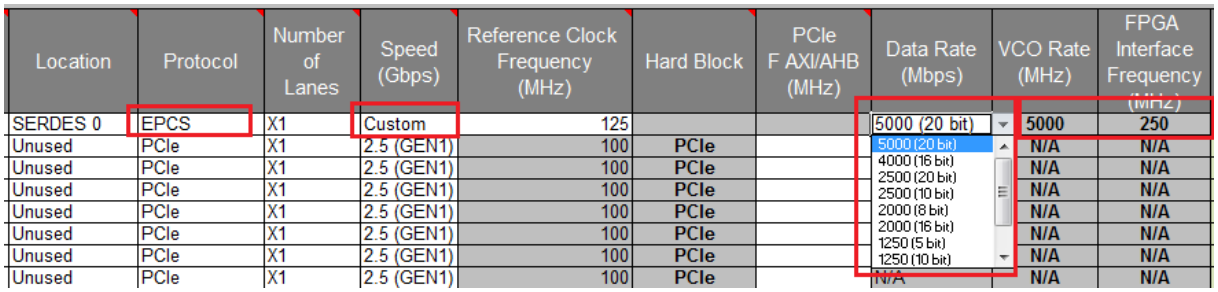

***Figure 16* • Custom EPCS Speed**

For more information about the SERDES of the supported device families, refer to the High Speed Serial Interfaces User Guide of the respective devices.

MSS/HPMS and FDDR

Based on the device selected, either *MSS & FDDR* or *HPMS & FDDR* worksheet is visible in the workbook. *MSS & FDDR* worksheet is visible when SmartFusion2 devices are selected and HPMS & FDDR worksheet is visible when IGLOO2 devices are selected. This section contains the following subsections:

- "FDDR" on page 30
- "MSS Power" on page 30
- "HPMS Power" on page 32

FDDR

Figure 17 shows the FDDR section in the MSS & FDDR/HPMS & FDDR worksheet. This section is same for both SmartFusion2 and IGLOO2 devices. Enter the following parameters for FDDR.

- Name
- F AXI/AHB (MHz)
- DDR Clock Multiplier

FDDR Power					
Name	F AXI/AHB (MHz)	DDR Clock Multiplier	DDR Clock Frequency (MHz)	VDD Power (mW)	PLL_VDDA Power (mW)
		F AXI/AHB*1	0.00	0.00	0.00

Figure 17 • FDDR Power Section

Table 14 shows the parameters to be entered in the FDDR section of the MSS/HPMS & FDDR worksheet.

***Table 14* • FDDR Power Section Parameters**

Parameters	Description
Name	Enter the name of the module containing FDDR.
F AXI/AHB (MHz)	Enter the clock frequency of AXI/AHB interface. It supports a maximum frequency of up to 167 MHz.
DDR Clock Multiplier	Select the frequency multiplication factor of DDR. DDR clock frequency (FDDR_CLK) must be less than 334 MHz (For example, if F AXI/AHB is 167 then DDR clock multiplier should not be more than F AXI/AHB*2).

For more information about FDDR of the supported device families, refer to the respective device FPGA High Speed DDR Interfaces User Guides.

MSS Power

MSS Power is available only when SmartFusion2 devices are selected. For IGLOO2 devices, *HPMS Power* replaces *MSS Power*. It contains the following sections:

- Cortex-M3, Switch Matrix and Memory
- MDDR
- APB Peripherals
- Switch Matrix Peripherals

Figure 18 shows the MSS Power section of the *MSS & FDDR* worksheet. Peripherals and their operating frequencies must be configured to get the estimation.

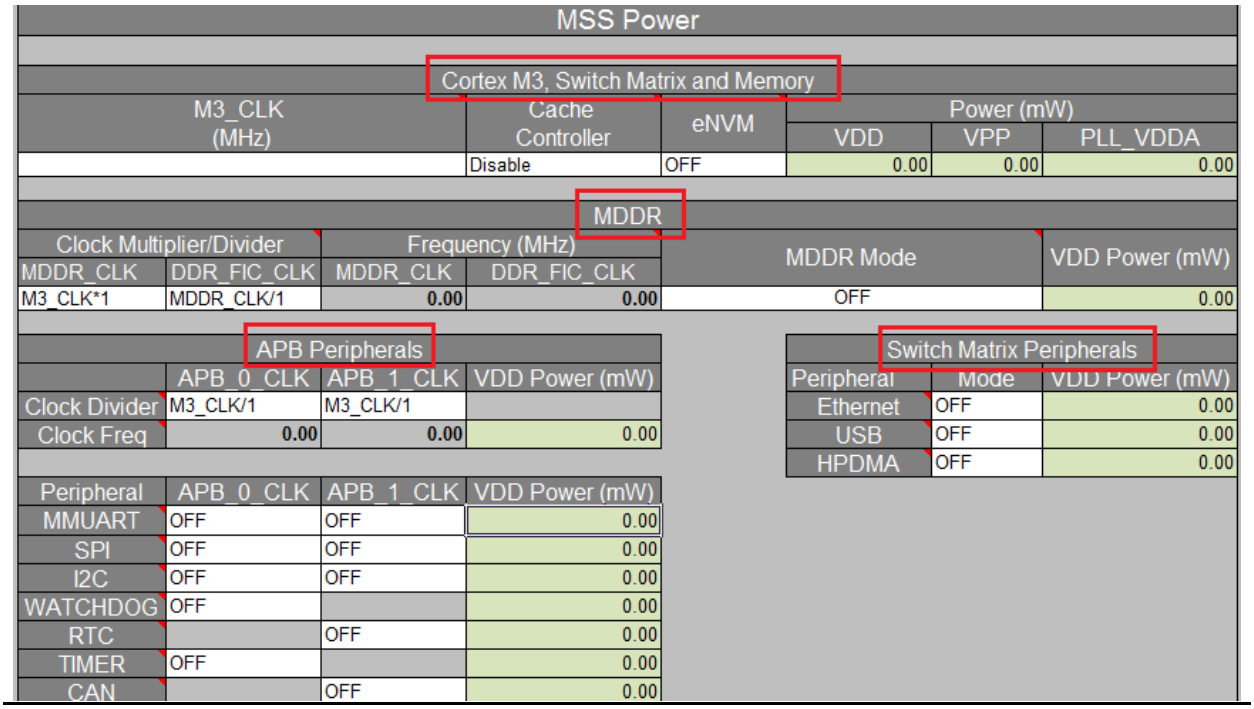

Figure 18 • MSS Power

Table 15 shows the parameters to be entered in the MSS power section of the MSS & FDDR worksheet.

Table 15 • **MSS Power Section Parameters**

Parameters	**Description**
Cortex-M3, Switch Matrix, and Memory	
M3_CLK (MHz)	M3_CLK is the main clock of the MSS that drives the Cortex-M3 processor. Other clock frequencies are derived based on the corresponding multiplier or divider. Enter the main clock frequency of the MSS (M3_CLK).
Cache Controller	Enable or disable the cache controller.
eNVM	Select ON or OFF to include or exclude eNVM.
MDDR	
MDDR_CLK	Select the clock multiplier
DDR_FIC_CLK	Select the clock divider
MDDR Mode	Disable the MDDR by selecting **OFF** or select the one of the following modes: • DDR mode - MSS bridge • DDR mode - DDR_FIC • DDR mode - MSS bridge and DDR_FIC • SMC_FIC mode
APB Peripherals	
Each column in this section represents a separate clock domain: APB_0_CLK and APB_1_CLK	
Clock Divider	Select the clock divider for APB_0_CLK and APB_1_CLK.

***Table 15* • MSS Power Section Parameters (continued)**

Parameters	Description
MMUART	Enable or disable MMUART
SPI	Enable or disable SPI
I2C	Enable or disable I2C
WATCHDOG	Enable or disable WATCHDOG
RTC	Enable or disable RTC
TIMER	Enable or disable TIMER
CAN	Enable or disable CAN
Switch Matrix Peripherals	
Ethernet	Disable Ethernet or select a PHY
USB	Disable USB or select a PHY
HPDMA	Enable or Disable HPDMA

Refer to the SmartFusion2 SoC FPGA Cortex-M3 User Guide for more information on the peripherals.

HPMS Power

HPMS Power is available only when IGLOO2 devices are selected. For SmartFusion2 devices, *MSS Power* replaces *HPMS Power.* It contains the following subsections:

- HPMS Switch Matrix Peripherals and Memory
- HPMS_DDR

Figure 19 shows the HPMS Power section in the HPMS & FDDR worksheet. Configuring the peripherals and their operating frequency has to be done.

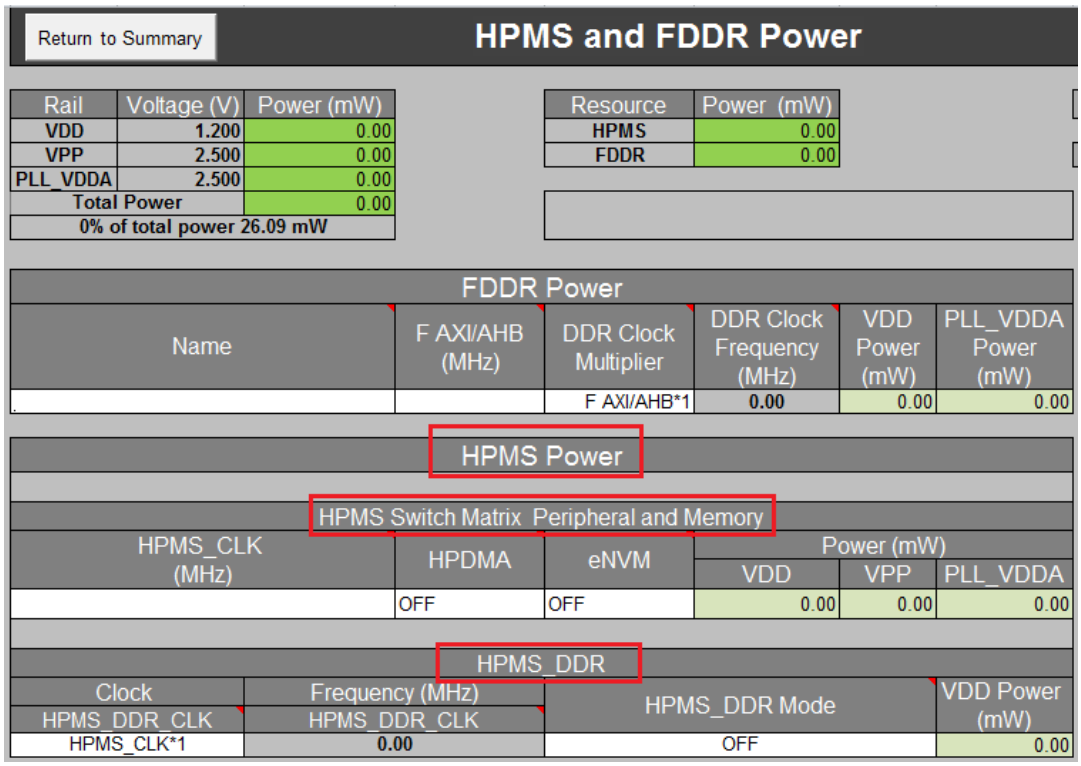

***Figure 19* •** HPMS Power

Table 16 shows the parameters to be entered in the **HPMS Power** section of the *HPMS & FDDR* worksheet.

***Table 16* • HPMS Power Section Parameters**

Parameters	Description
HPMS Switch Matrix Peripherals and Memory	
HPMS_CLK (MHz)	HPMS_CLK is the main clock of the HPMS system. Other clock frequencies are derived based on the corresponding multiplier. Enter the main clock frequency for HPMS.
HPDMA	Enable or disable HPDMA.
eNVM	Enable or disable the eNVM.
HPMS_DDR	
HPMS_DDR_CLK	Select the clock multiplier
HPMS DDR Mode	Enable or disable HPMS_DDR

Refer to the IGLOO2 High Performance Memory Subsystem user guide for more information on HPMS.

Step - 3: Scenarios

In this section, enter the device operational modes during its operational time, for instance, 50% of the time Active and 50% in Flash*Freeze. Enter the percentage of time the device is expected to be in Active, Static and Flash*Freeze modes. This section is available in the *Summary* worksheet and it is optional to provide these details.

Figure 20 shows the **Modes and Scenarios** section of the power estimator.

Modes and Scenarios

Low Power Mode Scenario			
Mode	% Time in Mode	Power in Mode (mW)	Power in scenario (mW)
Active	50.00%	8.25	4.13
Static	0.00%	8.25	0.00
Flash*Freeze	50.00%	2.95	1.48
		Scenario Power	5.60

Figure 20 • Modes and Scenarios Section

Step - 4: Power Estimation Summary

Figure 21 shows both the current summary and the power summary and also Modes and Scenarios of the *Summary* worksheet. The Power Summary section provides the total power and power breakdown based on the power sources and rails. It also provides thermal power summary.

Power Summary

Active Mode: Summary		
Total Power (mW)		6.44
Junction Temperature Tj (°C)		25.03
Effective Theta JA (°C/W)		5.01
Thermal Margin	Maximum Ta (°C)	84.97
	Maximum Power (mW)	11987.32

Active Mode: Type Breakdown		
Resource	%	Power (mW)
Core Static	100%	6.44
Bank Static	0%	0.00
Clock	0%	0.00
Logic	0%	0.00
RAMs	0%	0.00
Math Block	0%	0.00
CCC	0%	0.00
Oscillators	0%	0.00
IO	0%	0.00
MSS	0%	0.00
FDDR	0%	0.00
SERDES	0%	0.00

Modes and Scenarios

Low Power Mode Scenario			
Mode	% Time in Mode	Power in Mode (mW)	Power in scenario (mW)
Active	50.00%	6.44	3.22
Standby	0.00%	6.44	0.00
Flash*Freeze	50.00%	1.88	0.94
		Scenario Power	4.16

Current Summary

Rail Breakdown			
Rail Name	Current (mA)	Voltage (V)	Power (mW)
VDD	5.37	1.200	6.44
VDDI 1.2	0.00	1.200	0.00
VDDI 1.5	0.00	1.500	0.00
VDDI 1.8	0.00	1.800	0.00
VDDI 2.5	0.00	2.500	0.00
VDDI 3.3	0.00	3.300	0.00
SERDES_[01]_L[0123]_VDDAIO	0.00	1.200	0.00
SERDES_[01]_L[0123]_VDDAPLL	0.00	2.500	0.00
PLL_VDDA	0.00	2.500	0.00
VPP	0.00	2.500	0.00

Figure 21 • **Power Summary**

Device Utilization

Figure 22 shows the Device Utilization section displayed at the bottom of the summary worksheet.

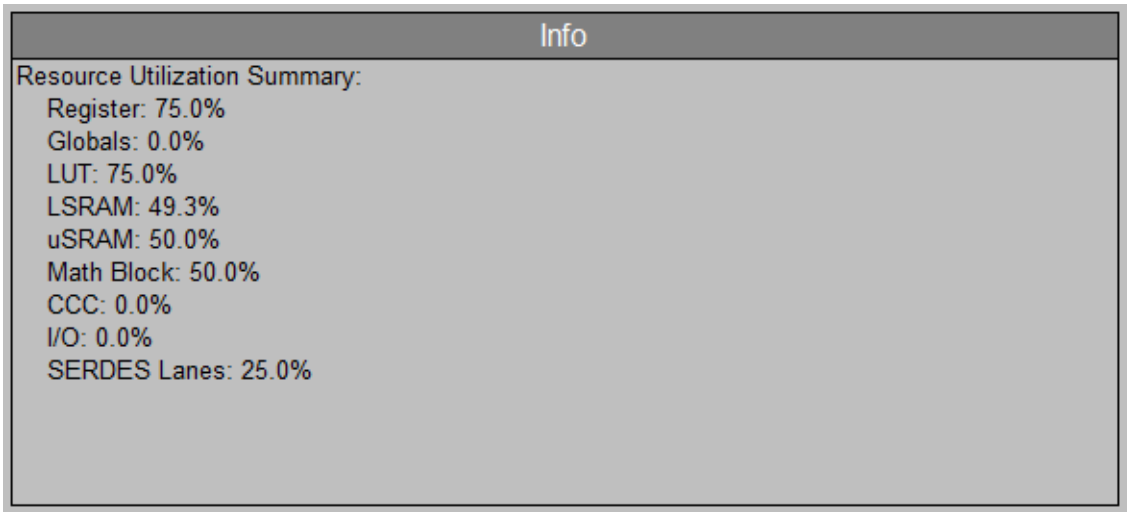

Figure 22 • **Device Utilization**

A – List of Changes

The following table lists critical changes that were made in each revision.

Date	Changes	Page
Revision 1 (August 2014)	Initial release.	NA

B – Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Customer Support website (www.microsemi.com/soc/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

Website

You can browse a variety of technical and non-technical information on the SoC home page, at www.microsemi.com/soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

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