AN3759

PCB Layout Guide for MEC172x

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INTRODUCTION

This application note provides information on design considerations for a printed circuit board (PCB) for the Microchip MEC1721/MEC1723 device.

The design of the PCB requires care to provide good supply and ground paths; in addition, other design issues are addressed in this document.

The functional blocks in the MEC1721/MEC1723 have different requirements for routing and external connections, which are also outlined in this application note.

Please see References for device-level information such as V_{CC1} power planes, and mechanical package information for the 176-Pin WFBGA.

This document includes the following topics:

Audience

This document is written for a reader that is familiar with hardware design. The goal of this application note is to provide information about sensitive areas of the MEC1721/MEC1723 PCB layout.

References

The following documents should be referenced when using this application note. Please contact your Microchip representative for availability.

- Microchip MEC1721/MEC1723 Data Sheet
- Microchip MEC1721/MEC1723 EVBs, ASSY. 6906A
- PCI Local Bus Specification (see www.pcisig.com)
- I^2C-bus specification and user manual, Rev. 6 - 4 April, 2014 or later (see www.nxp.com/documents/user_manual/UM10204.pdf)
- Intel, Enhanced Serial Peripheral Interface (eSPI) Specification (for Client Platform)
- Microchip “eSPI Controller” Specification

Package Information

The MEC1721/MEC1723 device is currently available in the following packages:

- MEC1721/MEC1723 for 176-pin, WFBGA/LJ
- MEC1721/MEC1723 for 144-pin, WFBGA/SZ

1.0 GENERAL LAYOUT CONSIDERATIONS

This section describes layout considerations for the MEC1721/MEC1723 device. This includes the following topics:

1.1 Decoupling Capacitors

This section includes the following topics:

Decoupling capacitors should be placed as close to the chip as possible to keep series inductance low. When the capacitors are mounted on the bottom side of the PCB, the capacitors are connected to the ground plane from the bottom layer directly using the shortest path to the device. Each VCC pin should have a 0.1 µF capacitor located as close to the pin as possible. Bypass capacitors should be placed close to the supply pins of the MEC1721/MEC1723 with short and wide traces.

The MEC1721/MEC1723 has an integrated voltage regulator to supply the core circuitry. Decoupling this regulator requires a critical capacitor of 1µF on the CAP pin. ESR of this 1µF capacitor, including the routing resistance, must be less than 100 mOhm.

Capacitors may carry large currents that generate magnetic fields, inducing noise on nearby traces. Sensitive traces such as the 32kHz crystal should be separated by at least five times the trace width from decoupling capacitors when possible.

Connecting decoupling caps to power and ground planes using two vias per pad will reduce series inductance.

- FIGURE 1-1: on page 3 shows decoupling for the MEC1721/MEC1723 176-pin WFBGA.

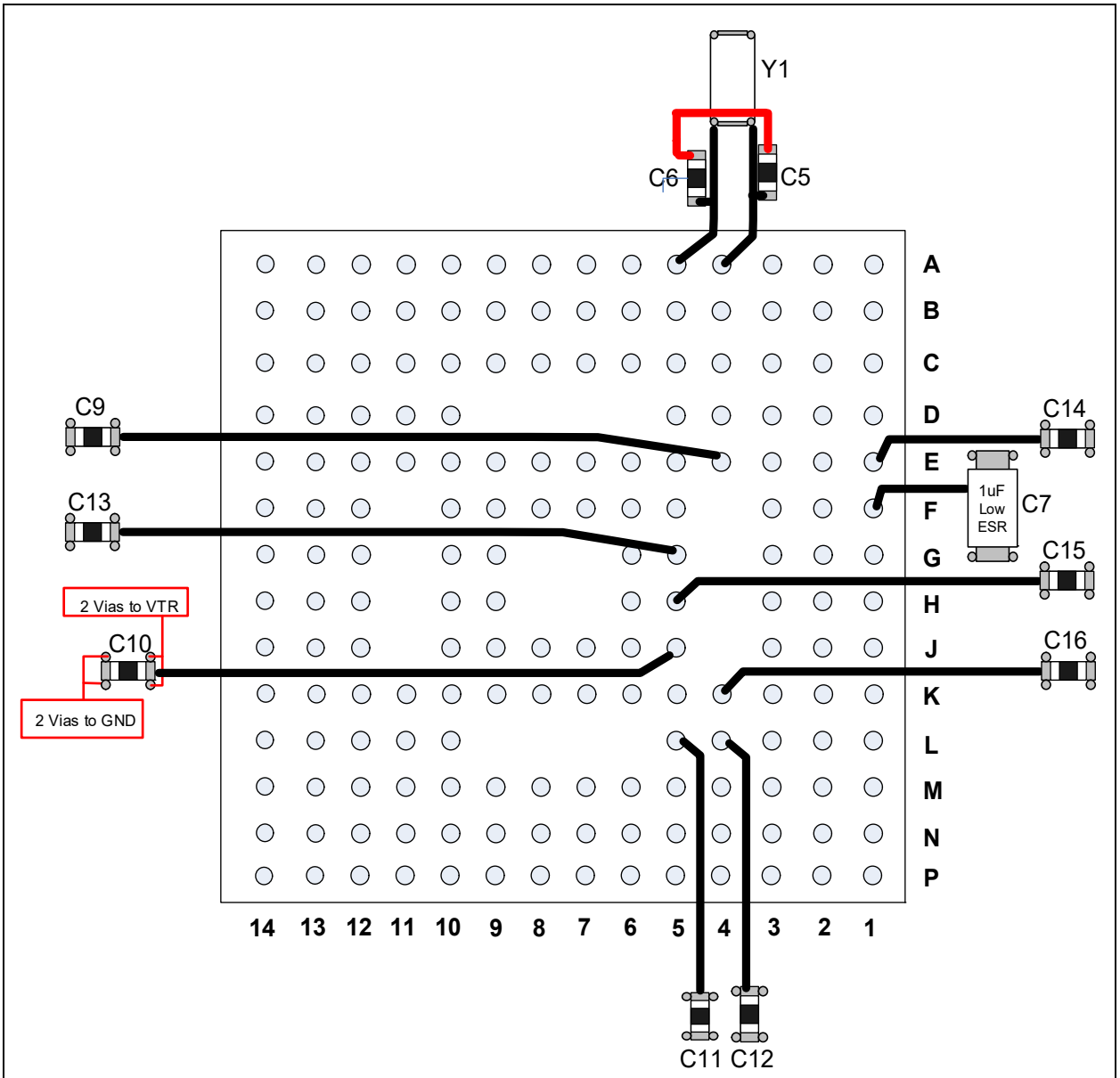
The VCC pin decoupling capacitors can use any typical 16V 10% Ceramic. See also the MEC1721/MEC1723 EVB Schematics and Bill of Materials.

1.1.1 MEC1721/MEC1723 WFBGA CAPACITORS

- Figure 1-1 shows decoupling for the MEC1721/MEC1723 176-pin WFBGA package.

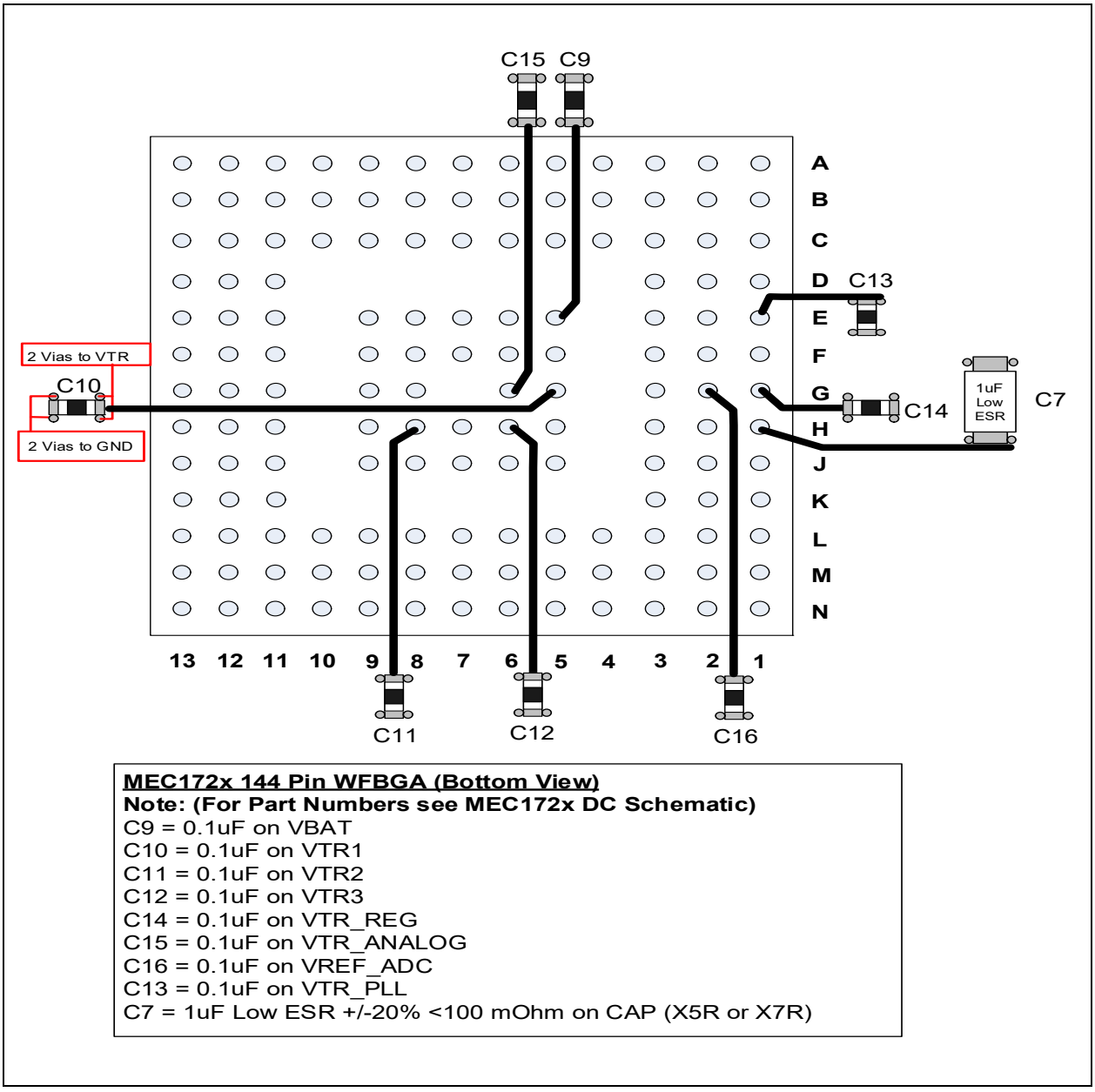
Note:	The capacitors can use any typical 16V 10% ceramic.

FIGURE 1-1: MEC1721/MEC1723 DECOUPLING IN 176-PIN WFBGA/LJ PACKAGE



MEC172x WFBGA (Bottom View)
Note: (For Part Numbers see ME172x DC Assy 6908 Schematic)
C9 = 0.1uF on VBAT
C10 = 0.1uF on VTR1
C11 = 0.1uF on VTR2
C12 = 0.1uF on VTR3
C14 = 0.1uF on VTR_REG
C15 = 0.1uF on VTR_ANALOG
C16 = 0.1uF on VREF_ADC
C13 = 0.1uF on VTR_PLL
C7 = 1uF Low ESR +/-20% <100 mOhm on CAP (X5R or X7R)
Y1 = 12.5pF load crystal, C5/C6 are 22pF XTAL1, XTAL2

FIGURE 1-2: MEC1721/MEC1723 DECOUPLING IN 144-PIN WFBGA/SZ PACKAGE



MEC172x 144 Pin WFBGA (Bottom View)
Note: (For Part Numbers see MEC172x DC Schematic)
C9 = 0.1uF on VBAT
C10 = 0.1uF on VTR1
C11 = 0.1uF on VTR2
C12 = 0.1uF on VTR3
C14 = 0.1uF on VTR_REG
C15 = 0.1uF on VTR_ANALOG
C16 = 0.1uF on VREF_ADC
C13 = 0.1uF on VTR_PLL
C7 = 1uF Low ESR +/-20% <100 mOhm on CAP (X5R or X7R)

1.2 32.768kHz Crystal Oscillator

The following formula may be used to calculate a parallel resonant crystal's external load capacitors:

CL = ((CX1 x CX2) / (CX1 + CX2)) + Cstray

where:

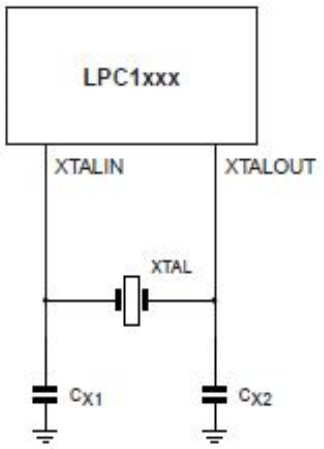
CL = the crystal load capacitance
Cstray = the stray capacitance in the oscillator circuit, which will normally be in the 2pF to 5pF range.

Assuming that CX1=CX2 then the equation becomes:

CL = ((CX1 x CX1) / (2 x CX1)) + Cstray
CL = (CX1 / 2) + Cstray

Rearranging the equation, we can find the external load capacitor value:

CX1 = 2(CL - Cstray)



The formula parameters:

CL is the cystals load cap, CX1 is equivalent to C12 and Cx2 is equivalent to C13 in our doc are the cap from pin to ground

The Cstray = trace Length cap (board layout) + pin cap (package) + pads parasitic cap (pad library)

1.2.1 SINGLE ENDED CLOCKING

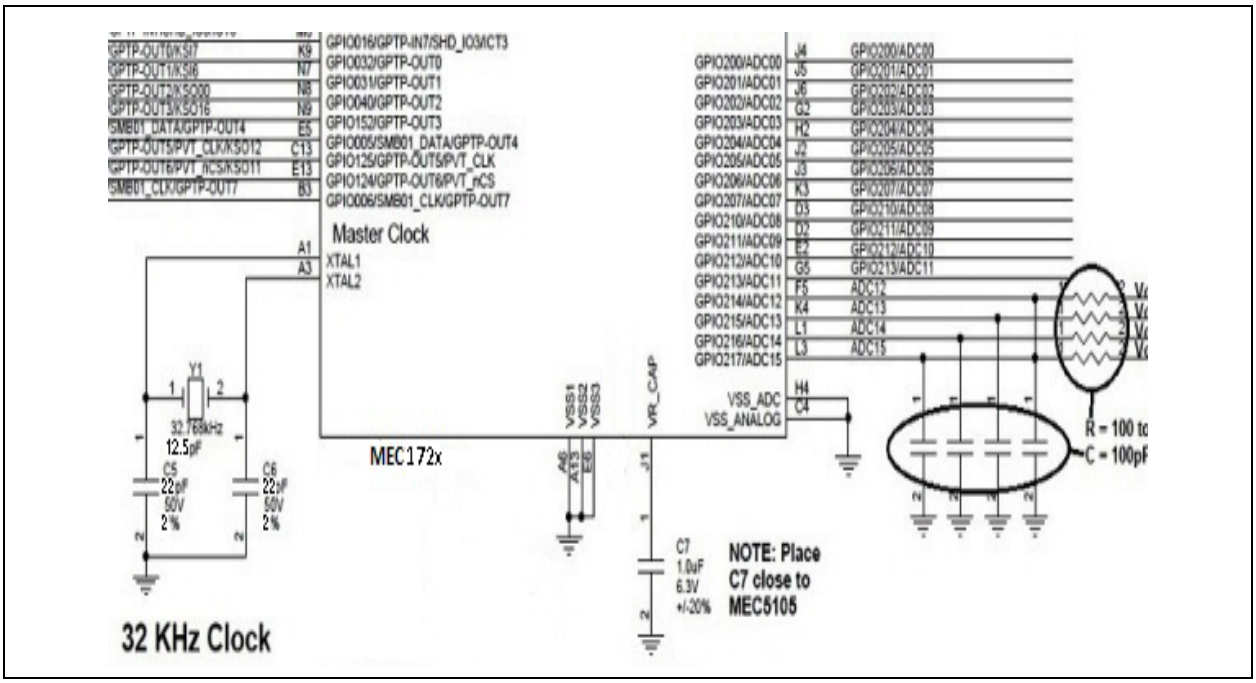
An External Crystal Oscillator can be used with MEC172x for sourcing the 32kHz clock domain. For dual ended configuration, XTAL is connected between XTAL1 and XTAL2.

For Single ended XTAL configuration, external clock should be connected to XTAL2 pin and XTAL1 pin should be grounded. If the 32KHz source will never be the crystal oscillator, then the XTAL1 and XTAL2 pins should be grounded.

1.3 CAP Pins, AVSS/GND Connection

The recommended filtering for the CAP pin on the MEC1721/MEC1723 is shown in Figure 1-3, for WFBGA connections. The filtering components shown should be placed close to the device and away from noise sources.

FIGURE 1-3: WFBGA CAP PIN REFERENCE AND AVSS DIRECTLY CONNECTED TO GND



1.4 BGA Package PCB Layout Considerations

The MEC1721/MEC1723 devices have BGA RoHS-Compliant package as follows:

- 176-pin WFBGA/LJ: 11mm x 11mm, 0.8mm ball pitch (see Figure 1-4)
- 144-pin WFBGA/SZ (see Figure)

Note:	Please refer to the latest data sheet for most up-to-date PCB LAND pattern information.

The following list summarizes BGA routing guidelines, but it is understood that final layout is process- dependent and your design should reflect your needs:

- Through-hole vias technology is not recommended for pitches less than 0.8mm (unless the ball matrix is depopulated in the center)
- NSMD ball pads for pitches 0.8mm – 0.4mm
- Solder Mask to be 1:1 scale of the land size, when routing 0.5mm pitch ball pads
- µVias – next generation PCB technology for tighter pitches
- Eliminate through-hole vias
- Increase routing density & enhance electrical performance
- Decrease routing layers
- Provide fan-out solutions for multiple layers (stacked Vias)

FIGURE 1-4: LAND PATTERN DIMENSIONS, 176-WFBGA/LJ, 0.65MM BALL PITCH

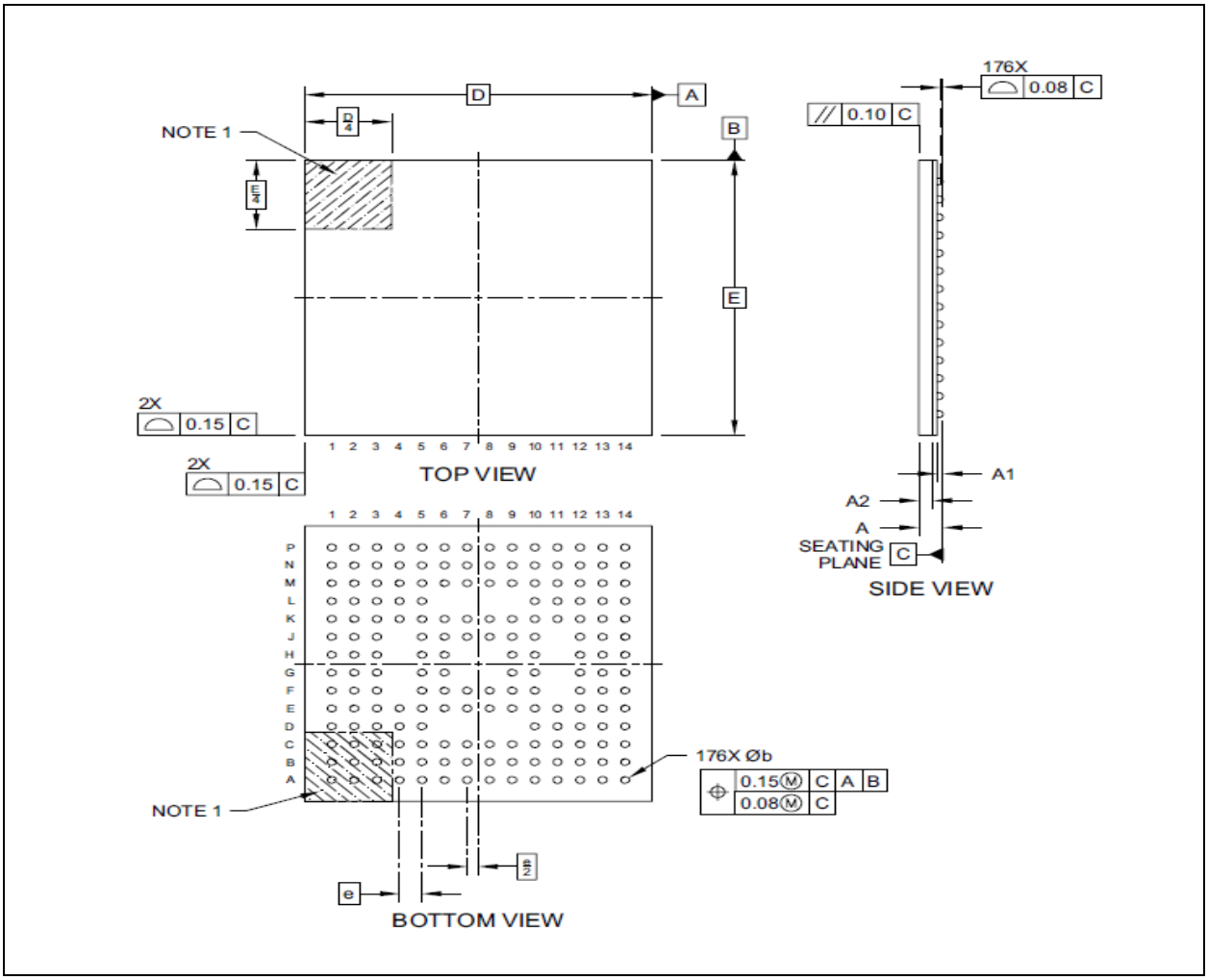
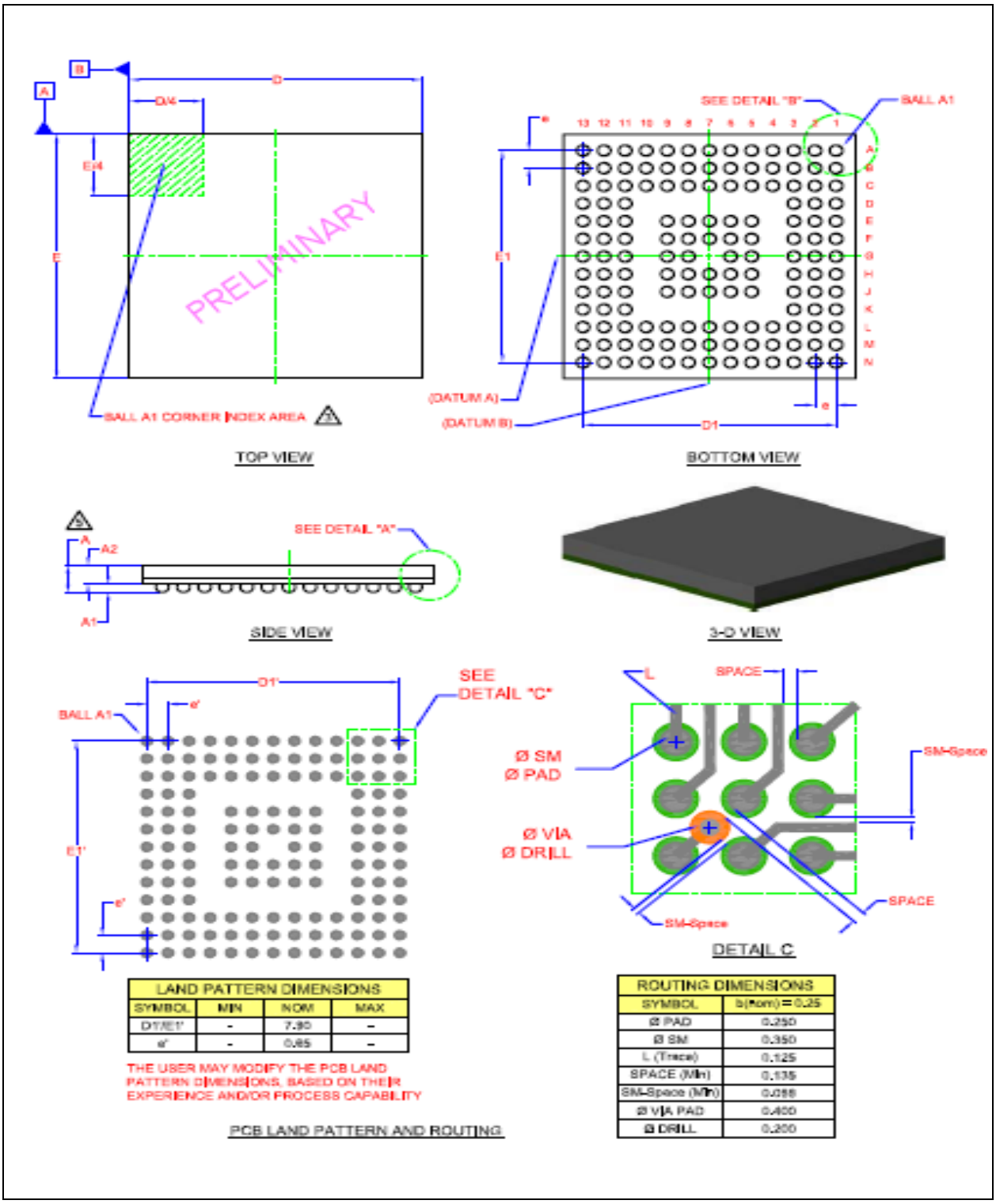


FIGURE 1-5: LAND PATTERN DIMENSIONS, 144-WFBGA/SZ



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
D1/E1'	-	7.90	-
e'	-	0.65	-

ROUTING DIMENSIONS	
SYMBOL	b(Nom) = 0.25
Ø PAD	0.250
Ø SM	0.350
L (Trace)	0.125
SPACE (Min)	0.135
SM-Space (Min)	0.055
Ø VIA PAD	0.400
Ø DRILL	0.200

2.0 MISCELLANEOUS CONSIDERATIONS

This section covers a variety of layout topics:

2.1 Strapping Options

Table 2-1 describes the MEC1721/MEC1723 strap option pins.

TABLE 2-1: MEC1721/MEC1723 STRAP OPTIONS

Pin Name	Strap Name	Strap Define and Value	I/O Power Rail
GPIO170	JTAG_STRAP	1=Use the JAG TAP Controller for Boundary Scan 0=The JTAG TAP Controller is used for debug (normal operation)	VTR1
GPIO045	GPIO045	Crisis Recovery Strap 1=Normal Boot Source 0=Use the Private SPI pins to boot from Crisis Recovery flash over Key scan connector Note: This pin requires an external pull-up for normal operation.	VTR1
GPIO207	CMP_STRAP	CMP_STRAP is the Comparator 0 Strap pin. This strap must be enabled in OTP. Note 3 1=Comparator 0 Enabled Note 4 0=Hardware Default (GPIO input)	VTR1
GPIO055/ SHD_CS 0#	BSS_STRAP	Boot Source Select Strap 1=Use the Shared SPI pins for Boot Note 2 0=Use the eSPI Flash Channel for Boot Note 1	VTR2
GPIO126	UART_BSTRAP	Crisis Recovery over UART 1=Normal Operation 0=Use UART interface for Crisis recovery Note 5	VTR1
GPIO227	PWRGD_STRAP	Power Good	VTR1

Note 1: If the eSPI Flash Channel is used for booting, i.e., eSPI Master Attached Flash Sharing (MAFS), the GPIO055/PWM2/SHD_CS0# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. In addition, the GPIO016/GPTP_IN1/SHD_IO3/ICT3 pin must be used as DSW_PWROK.This pin will also be driven high by the boot ROM code to support Deep Sleep Well timing requirements.

2: If the Shared SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

3: The comparator strap option is an optional feature that may be enabled in OTP to enable the Boot ROM to configure and lock the Comparator 0 pins. If the feature is enabled in OTP, and external pull-up/pull-down is required to determine the default comparator behavior. If the strap option is not enabled in OTP, the CMP_STRAP is not supported and no external pull-up or pull-down required. Application firmware may enable the comparator if supported by the specific package.

4: CMP_STRAP option is available only in the 144 pin package.

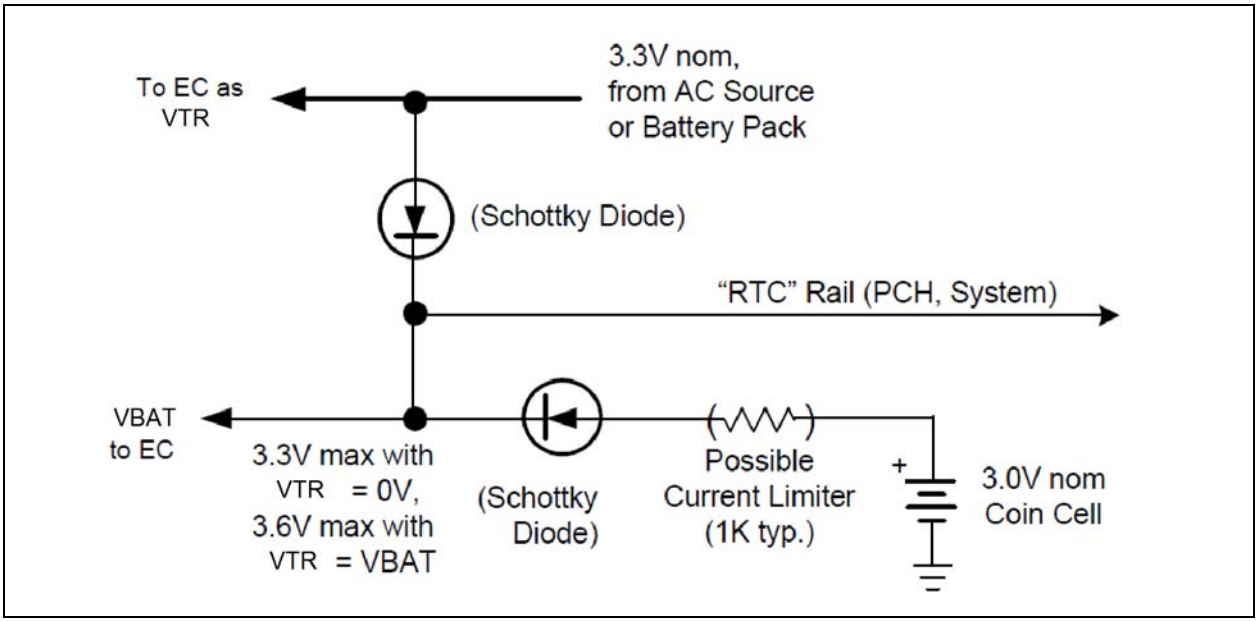
5: OTP byte 115 bit [3] allows selection of UART0/UART1 for Crisis Recovery, if UART_BSTRAP is enabled and sampled as 0x0.

2.2 Battery Circuit

Please see the Power Sources section of the MEC1721/MEC1723 Data Sheet.

For the battery circuity requirement, VBAT must always be present if VTR is present. The following circuit is recommended to fulfill this requirement.

FIGURE 2-1: RECOMMENDED BATTERY CIRCUIT



2.3 eSPI Interface

The firmware must configure the GPIO Pin Control Registers for the eSPI alternate function, configure the eSPI I/O Component Base Address Register, and activate the eSPI block.

2.3.1 VTRX POWER PIN

The eSPI Interface signals require the VTR3 power pin to be connected to the 1.8V rail.

2.3.2 HOST RESET SELECT

The platform reset signal that will be used to assert nSIO_RSET is determined by the POWER RESET CONTROL Register (40080114h) Bit 8 = 0 - eSPI_PLTRST# pin.

2.3.3 OTHER SIGNALS

All the eSPI I/F signals are connected to other eSPI signals that are already present in the system. The MEC1721/MEC1723 use 1.8V signaling for all eSPI signals. Please refer to the Intel Skylake Ultrabook Platform U-Series RVP Customer Reference Board Schematic, Microchip MEC1721/MEC1723 Evaluation Board Schematic, and reworks instruction for detailed information.

Note a few design notes below:

- LPC_AD0_ESPI_IO0, LPC_AD1_ESPI_IO1, LPC_AD2_ESPI_IO2, LPC_AD3_ESPI_IO3, LPC_-FRAME_ESPI_CS#, and LPC_CLK_0_ESPI_CLK signals have 15 ohm series resistor close to each chipset pin and another 15 ohm series resistor close to the MEC1721/MEC1723 for eSPI mode.
- GPP_C5/SML0ALERT# (Intel Skylake chipset pin W1) is used as strapping pin to determine either LPC mode (Low) or eSPI mode (High).

2.4 PS/2 Interface

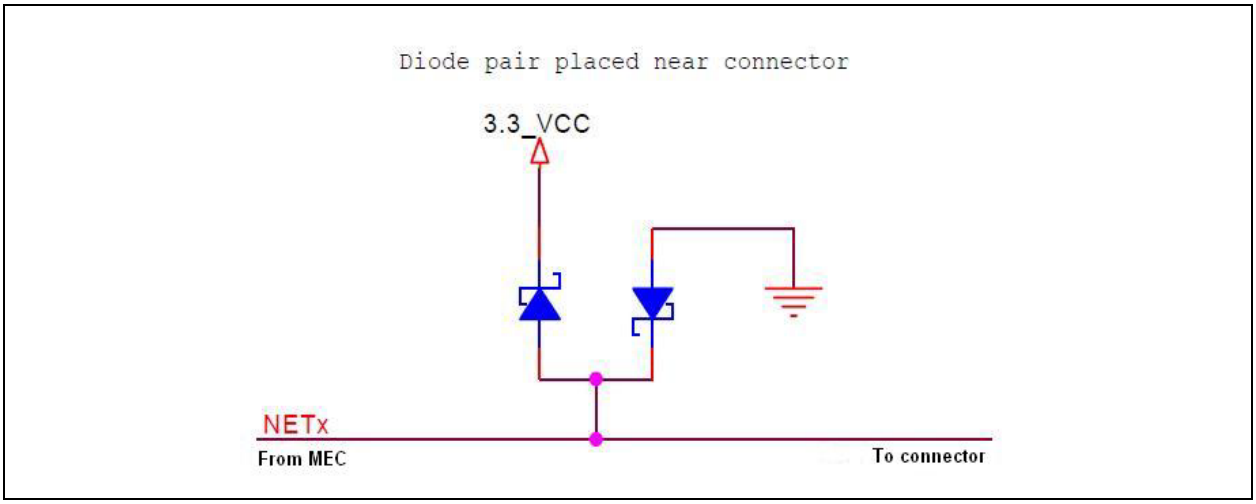
The routing of the PS/2 interface is also not critical, except that it should not be routed next to rapidly switching signals. The Clock and Data pins are Open Drain and require pullup resistors. A small 10 - 100pF (typ) capacitor to ground and 4.7kΩ (typ) pullups are recommended. The power pin of the PS/2 pin should be decoupled with a capacitor that is large enough to adequately filter the supply to PS/2 devices. Unused PS/2 clock and data pins should be pulled up to VCC with a 10kΩ (typ) resistor.

Note:	Two PS/2 ports are 5V tolerant when in 3.3V mode. The other three PS/2 ports are not.

2.5 EOS Considerations

For SMBus signals that terminate external to the main system board (for example, Smart Battery) the designer should take care in protecting these signals from EOS (Note 2-1) and ESD (Note 2-2). Please refer to the SMBus 2.0 specification, section 3.1.2.2 for appropriate guidelines. The specification recommends a series protection resistor and an optional ESD transorb on these nets. In addition to the SMBus specification recommendation, past experience shows that using 2 high speed diodes on each SMBus trace (instead of the transorb in the SMBus spec) is an effective way to improve immunity to EOS and ESD events. A Schottky diode pair is a good example. Figure 2-2 shows the suggested circuit implementation for each net that goes to a connector.

FIGURE 2-2: SCHOTTKY DIODE PAIR EXAMPLE



It should also be noted that any other signal that goes to an external connector should also be considered for EOS/ESD susceptibility. For instance, an ID pin (tied to a GPIO) that might seem benign, but is routed near high voltage sources could suffer transient EOS events. A similar protection scheme should be considered for these nets.

Note 2-1 EOS is defined as damage to the part caused by the application of voltages (to any pin) beyond the power supply rails, usually forward biasing internal protection diodes and resulting in high levels of

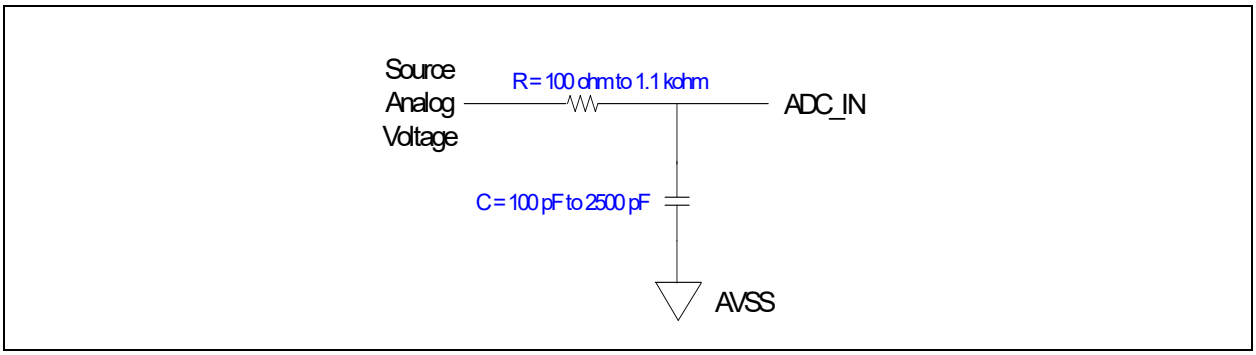
current flow. This typically induces open failures by damaging the metal inside the part. EOS is typically a low voltage, high current situation.

Note 2-2 ESD is the applied reverse bias to the PN junction -- heat due to power dissipation melts the silicon in the part. ESD is typically a high transient voltage spike with low current situation.

2.6 ADC Input Layout Requirements

- It is suggested that the Analog-Digital Converter (ADC) Source AVSS reference connects to the MEC1721/MEC1723 AVSS via a low noise AVSS island, which is shown in Figure 1-3.
- It is suggested that a low pass filter, see Figure 2-3, be used on each ADC input of MEC1721/MEC1723. Filter components below are a good starting point, the R should has value between 100 ohm to 1.1 kohm and the C should has value between 100pF to 2500pF. The RC values are based on high frequency cut off desired for the application, F = 1 / (2π * RC).

FIGURE 2-3: ADC INPUT LOW PASS FILTER



- It is recommended that the ADC nets are spaced at least 20 mils from any high speed switching signals to prevent cross talk that could add noise.

2.7 SPI Flash Implementation

The MEC1721/MEC1723 SPI flash interface enables the host and embedded controller (EC) access to an external SPI flash device. The MEC1721/MEC1723 Data Sheet and Boot ROM Application Note have more details on detail information (see References on page 1). This section describes specific PCB layout design considerations to setup this feature.

Note: The SPI Flash Interface of MEC1721/MEC1723 can be selected either 3.3V or 1.8V. The SHD SPI interface is on VTR2 power rail, and PVT SPI interface is on VTR1 power rail.

The standard set of SPI flash signals are designated with “SHD_” for shared connections, for example, SHD_CLK; for details, see Section 2.7.3, "Shared SPI Flash Interface". MEC1721/MEC1723 has an added set of signals for connection to another SPI flash device as private, protected data; these signals are designated with “PVT_,” for example, PVT_CLK; for details, see Section 2.7.4, "Non-shared SPI Flash Interface". The MEC1721/MEC1723 has a third SPI interface as a general SPI interface labeled as “SPI_,” for example, SPI_CLK.

TABLE 2-2: SPI INTERFACE SIGNALS

Generic Pin Signal Name	Pin Signal Function Name	MEC1721/MEC1723 Pin Number	Pin Function Signal Description
SPICLK	SHD_CLK	N7	Shared SPI Clock
	PVT_CLK	E12	Private SPI Clock
SPI_CS#	SHD_CS0#	P5/P8	Shared SPI Chip Selects
	PVT_CS#	G12	Private SPI Chip Selects

TABLE 2-2: SPI INTERFACE SIGNALS (CONTINUED)

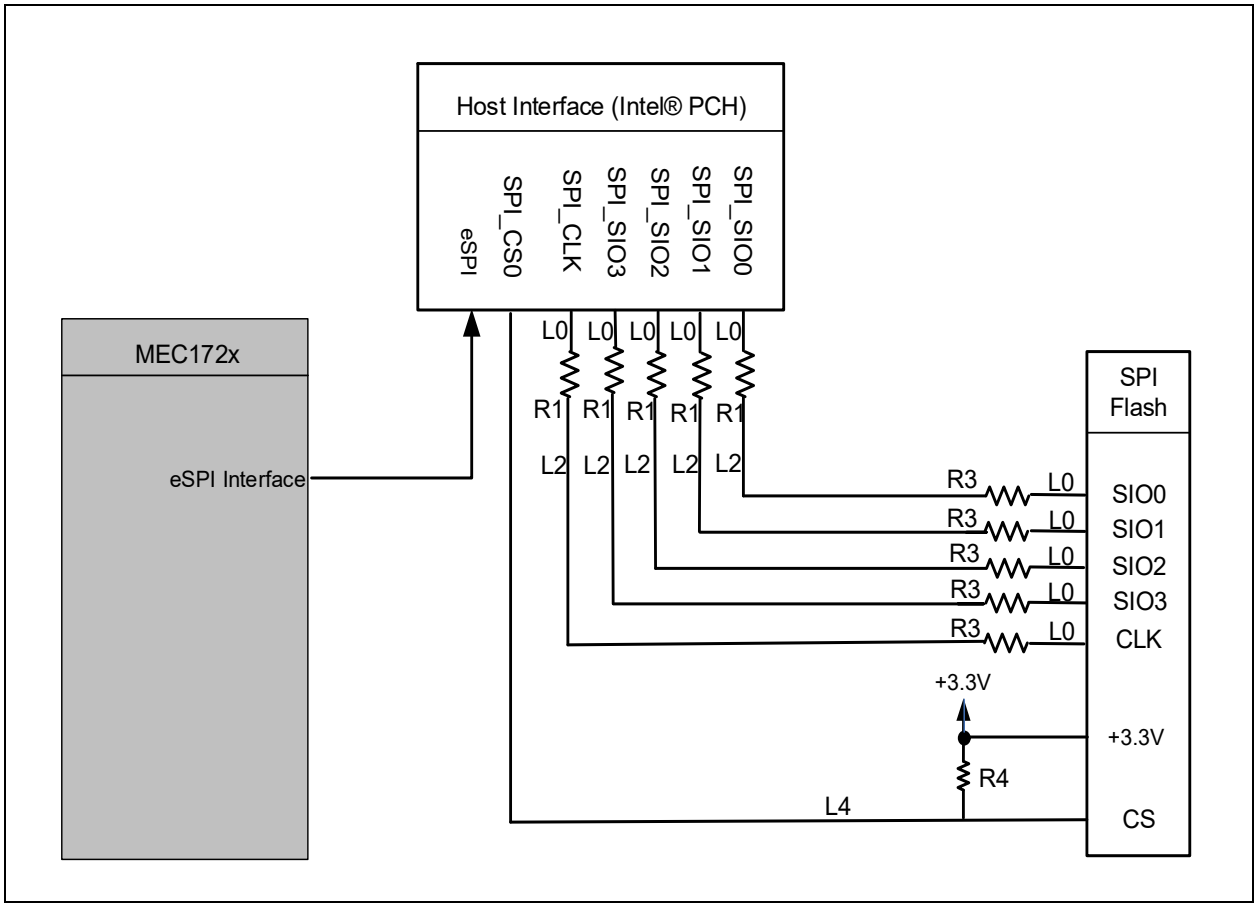
Generic Pin Signal Name	Pin Signal Function Name	MEC1721/MEC1723 Pin Number	Pin Function Signal Description
IO0 / MOSI	SHD_IO0 / SHD_MOSI	P6	Shared SPI Data I/O 0.
	PVT_IO0 / PVT_MOSI	H12	Private SPI Data I/O 0.
	Note: Also used as SPI_MOSI when the interface is used in single wire mode.		
IO1 / MISO	SHD_IO1 / SHD_MISO	M7	Shared SPI Data I/O 1.
	PVT_IO1 / PVT_MISO	F12	Private SPI Data I/O 1.
	Note: Also used as SPI_MISO when the interface is used in single wire mode.		
IO2	SHD_IO2	N6	Shared SPI Data I/O 2
	PVT_IO2	G13	Private SPI Data I/O 2
	Note: Only used in Quad Mode. Also can be used by firmware as WP.		
IO3	SHD_IO3	N5	Shared SPI Data I/O 3
	PVT_IO3	E13	Private SPI Data I/O 3
	Note: Only used in Quad Mode. Also can be used by firmware as HOLD.		

2.7.1 SELECTION OF SPI PORT & RSMRST#

The MEC1721/MEC1723 Boot ROM firmware selects two potential sources, the Shared SPI port or the eSPI Flash Channel, from which to load the application firmware. The selection is done by sampling the BSS_STRAP pin.

When used with a PC-based core logic, the EC must supply the RSMRST# signal to the core. If the eSPI Flash Channel is used as the source for EC firmware, the **BSS_STRAP pin MUST be used as the RSMRST# signal**. A weak-pulldown resistor to ground must be connected to the pin as shown in Figure 2-4. The pull-down both holds RSMRST# low glitch-free during the power-on sequence, as required by the core logic, and informs the Boot ROM in the MEC1721/MEC1723 to use the eSPI Flash Channel.

FIGURE 2-4: MEC1721/MEC1723 SHARED SPI FLASH DEVICE THRU ESPI FLASH CHANNEL



Note: For the required components and values that need to be used to connect between the Core Logic & external SPI flash, please refer to the corresponding core logic design guidelines and documentation for reference. The Figure 2-4 is used for illustration purpose only.

If the EC firmware is sourced from an external SPI Flash device directly to the Shared SPI Flash interface, **the BSS_STRAP pin MUST NOT be used as the RSMRST# signal**. Any other GPIO can serve as RSMRST#, if connected to ground with a weak pull-down resistor as shown in Figure 2-5. Once firmware is loaded and executed, it can release RSMRST# by setting the selected GPIO high.

2.7.2 SHARED VS. NON-SHARED SPI IMPLEMENTATION

Section 2.7.3, "Shared SPI Flash Interface" describes implementing the SPI Flash Interface using the shared signals (for example, SHD_CLK); Section 2.7.4, "Non-shared SPI Flash Interface" describes implementing the SPI Flash Interface using private signals (for example, PVT_CLK).

See Section 2.7.4, "Non-shared SPI Flash Interface," on page 16 for further details of this setup.

2.7.3 SHARED SPI FLASH INTERFACE

2.7.3.1 Shared SPI Flash Implementation

Figure 2-5 is a topology for implementing a single MEC1721/MEC1723 SPI flash for shared SPI flash devices. See Table 2-3 for specifications on PCB trace recommendations represented by “L1,” “L2,” and so forth.

FIGURE 2-5: MEC1721/MEC1723 SHARED SPI FLASH DEVICE THRU SHD SPI INTERFACE

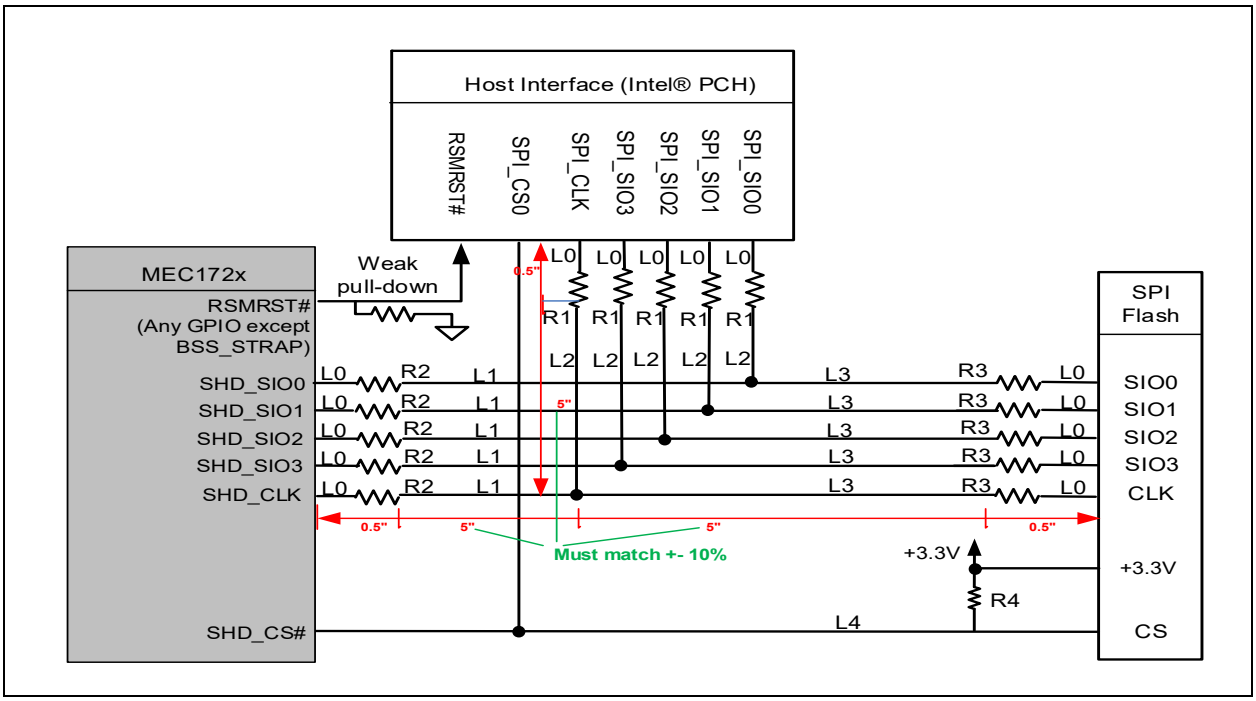


TABLE 2-3: MEC1721/MEC1723 SHARED SPI FLASH DEVICE SPECIFICATIONS (3.3V OR 1.8V, 24MA DRIVERS AT 48MHZ)

	Description	Spec
L0	Connection between MEC1721/MEC1723, Host/PCH, or SPI flash device and termination resistors.	0.1-inch to 0.5-inch
L1	PCB trace from the MEC1721/MEC1723 termination resistor to the PCB trace connection from the SPI flash and Host/PCH.	L1 = L2 = L3 within +/- 10% These trace connections can equal 1-inch up to 5-inches. See Note 2-5.
L2	PCB trace from the Host/PCH termination resistor to the PCB trace connection from the SPI flash and MEC1721/MEC1723.	
L3	PCB trace from the SPI flash termination resistor to the PCB trace connection from the MEC1721/MEC1723 or Host/PCH.	
L4	PCB trace from Host/PCH or MEC1721/MEC1723 to SPI flash for chip select.	L4 = L1 + L3 + (2 x L0) or L4 = L2 + L3 + (2 x L0) +/- 0.100 inches.
R1	These resistors are between the PCB trace and the Host/PCH.	3.3V - 35 ohm 1.8V - 20 ohm See Note 2-3, Note 2-4.
R2	These resistors are between the PCB trace and the MEC1721/ MEC1723.	3.3V - 10 ohm; 1.8V - 2.5 ohm See Note 2-3, Note 2-4.
R3	These resistors are between the PCB trace and the SPI flash.	3.3V - 2.5 ohm; 1.8V - 0 ohm See Note 2-3, Note 2-4.
R4	Pull-high resistor to +3.3V for SPI CS connections; between the MEC1721/MEC1723 or Host/PCH and the SPI flash device. This pull-high must connect to the same power rail of the SPI flash.	4.7K ohm

Note 2-3 The final value of the series resistors should be chosen based on performing electrical analysis to ensure the electrical timings and min/max voltage specifications are met for each device (SPI, EC, PCH or other Host SPI controller) including the undershoot/ overshoot specifications for the MEC1721/MEC1723 (-0.3V min. to V_{CC1}+0.3V max).

Note 2-4 Resistor recommendations are based on testing with Cannon Lake Server PCH IBIS model and Winbond SPI flash IBIS model w/ proper drivers in the system design.

Note 2-5 L1, L2, L3 must be equal to each other. For example, if L1 = 2-inches, then L3 must be 2-inches.

2.7.4 NON-SHARED SPI FLASH INTERFACE

Note:	Either Shared SPI or SAFS (Slave Attached Flash Sharing) interface can support a dedicated SPI chip.

2.7.4.1 Non-Shared Single SPI Flash Implementation (3.3V @ 16mA or 1.8V @ 24mA at 96MHz)

Figure 2-6 is a topology for implementing the MEC1721/MEC1723 SPI flash for a single non-shared SPI flash device. See Table 2-4 for specifications on PCB trace recommendations represented by “L1,” “L2,” and so forth.

FIGURE 2-6: MEC1721/MEC1723 TOPOLOGY FOR NON-SHARED SPI FLASH DEVICE

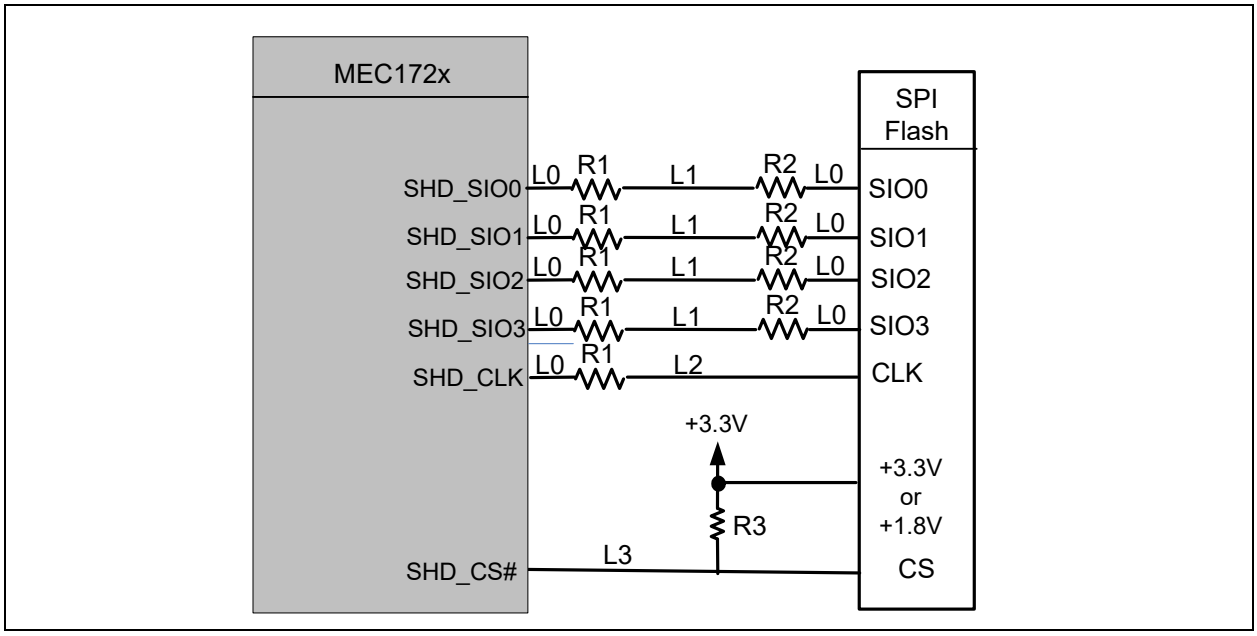


TABLE 2-4: MEC1721/MEC1723 NON-SHARED SPI FLASH DEVICE SPECIFICATIONS

	Description	Spec
L0	Connection between MEC1721/MEC1723 or SPI flash device and termination resistors.	0.1-inch to 0.5-inch
L1	The PCB trace between terminating resistors on the IO lines.	1-inch to 10-inch
L2	The PCB trace from MEC1721/MEC1723 or R1 resistor to SPI flash.	1-inch to 10-inch
L3	PCB trace from MEC1721/MEC1723 to SPI flash for chip select.	L3 = L0 + L1
R1	These resistors are between the trace and the MEC1721/MEC1723.	3.3V - 45 ohm; 1.8V - 40 ohm, see also Note 2-6
R2	This resistor is on the IO lines between the SPI flash and trace.	3.3V - 2.5 ohm; 1.8V - 7.5 ohm, see Note 2-6.
R3	This is a Pull-High resistor (to +3.3V) for SPI CS connections. This pull-high must connect to the same power rail of the SPI flash.	4.7K ohm

Note 2-6 The final value of the series resistors should be chosen based on performing electrical analysis to ensure the electrical timings and min/max voltage specifications are met for each device (SPI, EC, PCH or other Host SPI controller) including the undershoot/ overshoot specifications for the MEC1721/MEC1723 (-0.3V min. to V_{CC1} +0.3V max).

2.7.4.2 Non-Shared Dual SPI Flashes Implementation (3.3V @ 16mA or 1.8V @ 24mA at 48MHz)

Figure 2-6 is a topology for implementing the MEC1721/MEC1723 SPI flash for a single non-shared SPI flash device. See Table 2-4 for specifications on PCB trace recommendations represented by “L1,” “L2,” and so forth.

FIGURE 2-7: MEC1721/MEC1723 TOPOLOGY FOR NON-SHARED DUA: SPI FLASH DEVICE

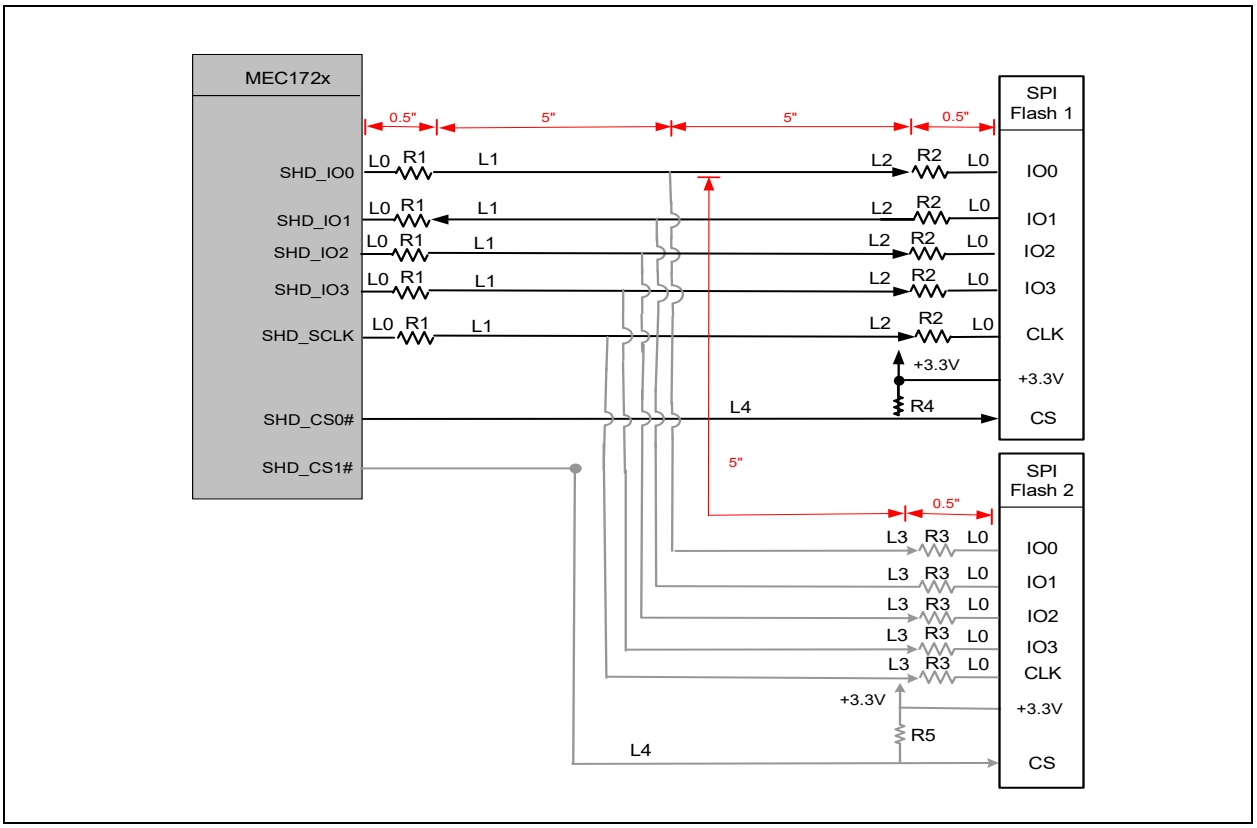


TABLE 2-5: MEC1721/MEC1723 NON-SHARED DUAL SPI FLASH DEVICE SPECIFICATIONS

	Description	Spec
L0	Connection between MEC1721/MEC1723, 2 SPI flash devices and termination resistors.	0.1-inch to 0.5-inch
L1	PCB trace from the MEC1721/MEC1723 termination resistor to the PCB trace connection from 2 SPI flash devices.	L1 = L2 = L3 within +/- 10% These trace connections can equal 1-inch up to 5-inches. See Note 2-5.
L2	PCB trace from the first SPI Flash termination resistor to the PCB trace connection from the second SPI flash and MEC1721/MEC1723.	
L3	PCB trace from the second SPI flash termination resistor to the PCB trace connection from the MEC1721/MEC1723 and the first SPI flash.	
L4	PCB trace from MEC1721/MEC1723 to the dual SPI flash for chip select.	L4 = L1 + L3 + (2 x L0) or L4 = L2 + L3 + (2 x L0) +/- 0.100 inches.
R1	These resistors are between the PCB trace and the MEC1721/MEC1723.	3.3V - 35 ohm 1.8V - 20 ohm See Note 2-7.

TABLE 2-5: MEC1721/MEC1723 NON-SHARED DUAL SPI FLASH DEVICE SPECIFICATIONS

	Description	Spec
R2	These resistors are between the PCB trace and the first SPI flash.	3.3V - 10 ohm; 1.8V - 2.5 ohm See Note 2-7.
R3	These resistors are between the PCB trace and the second SPI flash.	3.3V - 2.5 ohm; 1.8V - 0 ohm See Note 2-7
R4/R5	This is a Pull-High resistor (to +3.3V) for SPI CS connections. This pull-high must connect to the same power rail of the SPI flash.	4.7K ohm

Note 2-7 The final value of the series resistors should be chosen based on performing electrical analysis to ensure the electrical timings and min/max voltage specifications are met for each device (SPI, EC, PCH or other Host SPI controller) including the undershoot/ overshoot specifications for the MEC1721/MEC1723 (-0.3V min. to V_{CC1} +0.3V max).

2.7.5 SPI FLASH IMPLEMENTATION RECOMMENDATIONS

The following recommendations are for both Shared and Non-Shared SPI Flash Implementations.

- The MEC1721/MEC1723 SPI memory interface has serial flash device compatibility requirements that are defined in the MEC1721/MEC1723 Data Sheet. Please make sure the selected SPI flash meets these requirements.
- SPI_CLK must be 20mils spacing from any other high frequency (>1GHz) signal.
- The SPI flash parts should support operating at 12MHz for the ROM code loader, and up to 48MHz clock speed in RAM code loading.
- The designer should follow the SPI interface host design guidelines.
- IBIS models are available to aid in simulating the SPI system topology.
- The chip select CS# signals should have weak pullup resistors to the same power rail as the SPI flash. The pullup resistor value should meet the rise time requirements of the SPI flash.
- EC firmware must configure the MEC1721/MEC1723 SPI memory interface to disable mode, which will tri-state the SPI memory interface from MEC1721/MEC1723 to the SPI flash, before releasing the RSMRST# signal.
- This configuration requires that the PCH tri-state its SPI flash pins when RSMRST# is asserted.
- The characteristic impedance of the PCB trace should be 50 ohms +/-15% at 50MHz operating frequency.
- Within the SPI flash device, Schmitt trigger inputs are assumed on both the clock line and IO data lines.
- Within the Intel PCH, a Schmitt trigger input is assumed on the IO data lines.
- The output drivers for the SPI flash chip select pins should be programmed as open-drain using the GPIO Pin Control registers.
- The SPI Data IO traces should be length-matched to the CLK lines within 0.100-inch.
- Signal Integrity should be checked for each SPI part on your BOM.

2.7.6 SPI FLASH EXTERNAL PROGRAMMER

The SPI Flash on either Shared or Non-Shared SPI Flash interface must be programmed externally using a suitable programmer, such as Dediprog's SF100 (http://www.dediprog.com/pd/spi-flash-solution/sf100).

Provisions for a programming header on each SPI flash are recommended if the SPI is not socketed.

2.8 1MHz Pullup Resistor Requirement

Please refer to the I^2C-bus specification and user manual as indicated in the section References on page 1 for more information.

2.9 5V Tolerant Pins

There are fourteen 3.3V/5V tolerant pins on the MEC1721/MEC1723. Please see the MEC1721/MEC1723 Data Sheet section 2.5.7 for more information.

2.10 1.8V Capability

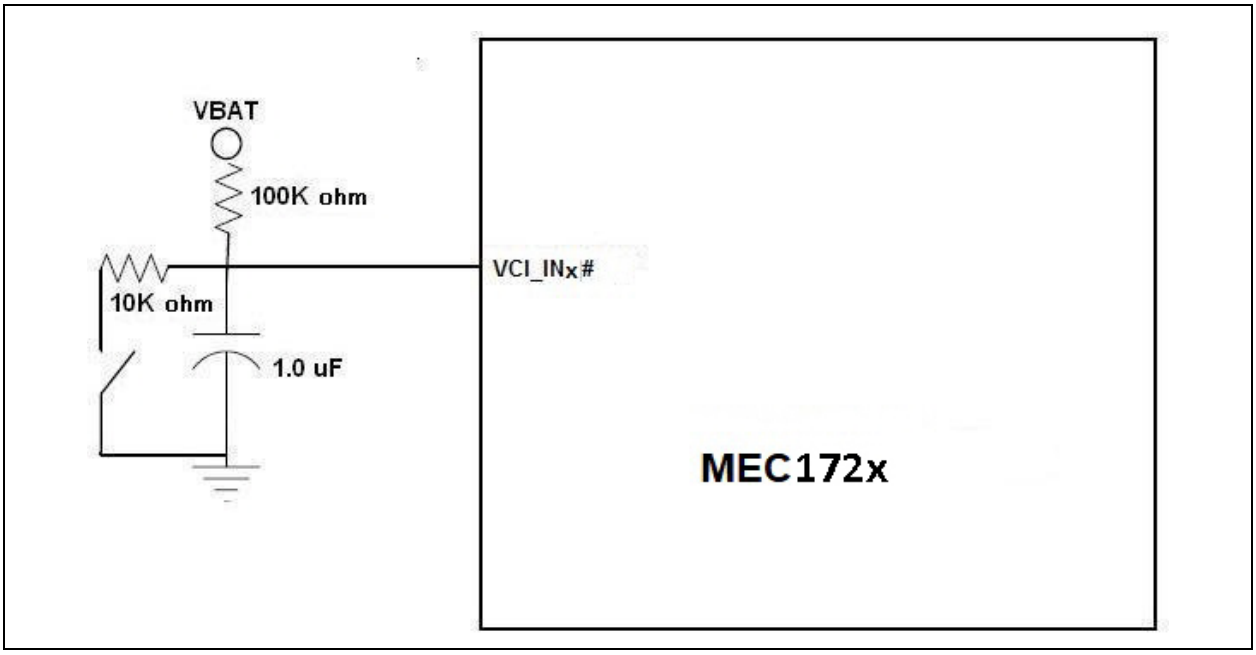
There are three voltage supply regions for all GPIO pins powered by VTR1, VTR2, and VTR3. Each region may be either 3.3V or 1.8V. Please refer to the MEC1721/MEC1723 Data Sheet section 2 for more information.

Note:	The LPC Interface Signals require the VTR3 power pin to be connected to the 3.3V or 1.8V VTR rail. The eSPI Interface signals require the VTR3 power pin to be connected to the 1.8V rail.

2.11 Power Switch Input

For the VBAT-powered power switch inputs (VCI_INx#) there is a specific requirement for the input circuit as illustrated in Figure 2-8. The resistors can use any typical 1/10W, +/- 1% carbon, thick, metal, or thin film. The capacitors can use any typical 16V 10% ceramic. Unused VCI pins should be pulled up to VBAT via a 100K resistor. Please refer to the MEC1721/MEC1723 EVB Schematics and Bill of Materials.

FIGURE 2-8: VBAT-POWERED CONTROL INPUT CIRCUIT



2.12 VCI_IN Pins When Used as GPIO

All the VCI_IN pins can be used as GPIOs. The firmware must program the VCI_BUFFER_EN bit[6:0] at VCI Buffer Enable Register to disable power up functionality on these VCI pins if these are used as GPIOs.

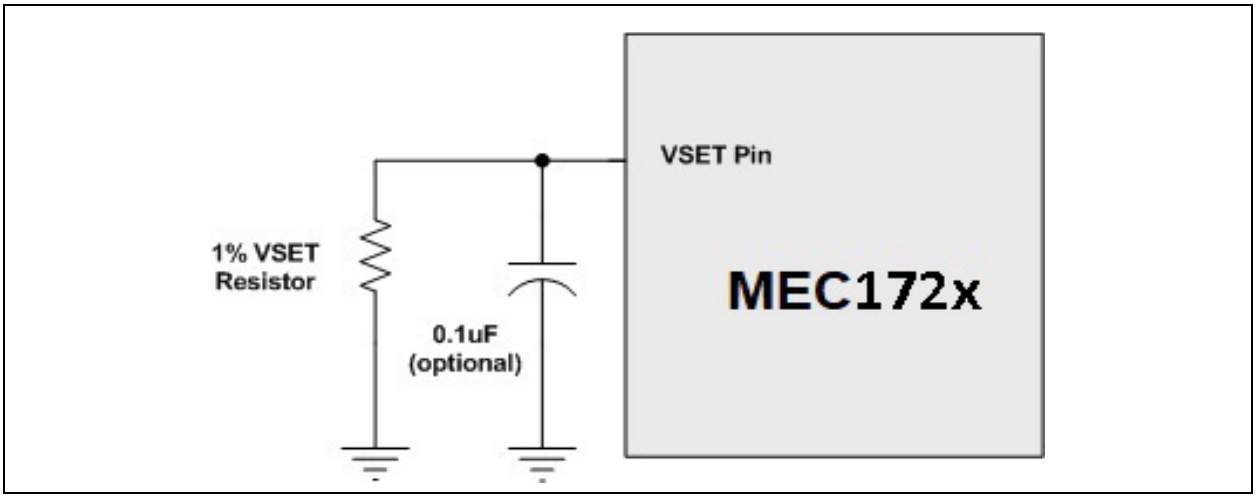
2.13 VSET Pin (MEC1725 Only)

The MEC1721/MEC1723 VSET pin is an input to the ThermTrip block which sets the ThermTrip shutdown temperature. The system designer creates a voltage level at these input through a resistor connected to GND as shown in Figure 2-9. The value of this resistor is used to create an input voltage on the TRIP_SET pin that is translated into a temperature ranging from 60°C to 123°C; see the VSET Resistor Settings table in the MEC1721/MEC1723 PCS for these values (see your Microchip representative for availability).

Note 1: VSET is designed to operate using a 1% resistor. If a 5% resistor is used, the decoded temperature may have an error more than 1°C.

2: An open condition on the VSET pin is decoded as a minimum temperature threshold level.

FIGURE 2-9: VSET CIRCUIT



2.14 Guardian Connections (MEC1725 Only)

The Guardian block is a combination temperature sensor, voltage monitor, hardware set thermal monitor, and fan controller. It monitors one internal diode and four external diodes. Details for this block are included in the MEC1721/MEC1723 Data Sheet (or PCS). This section includes describes layout considerations for this feature.

2.14.1 THERMAL DIODE LAYOUT CONSIDERATIONS

2.14.1.1 Remote Diode Hardware Considerations

- The remote diode positive (+) and negative (-) tracks should be kept close together (a 10 mil track minimum width and spacing is recommended), in addition a separation of the diode traces from any other trace by at least a 20 mil spacing is recommended.
- Place a capacitor between the two leads, as close as possible to the MEC1721/MEC1723 chip. 470pF (beta enabled) is used for the processor diode and 2200pF (beta disabled) is used for the 3904 diode.
- Both remote temperature sensor channel inputs should be terminated with a thermal diode, a transistor or resistor, even if they are not used in the design. Transistors that are suitable for use are MMBT3904 or an equivalent. Termination resistor values for use can be from 510 ohm to 1K ohm, see Figure • and Table 2-6 for generated temperature values for selected resistors.

FIGURE 2-10: UNUSED DIODE PIN CONNECTION

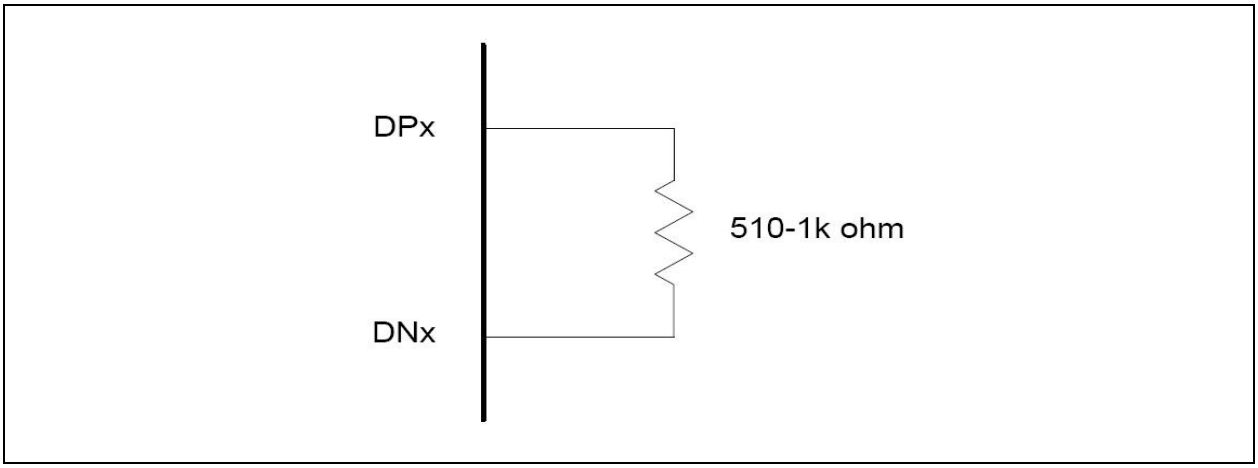


TABLE 2-6: TERMINATION RESISTOR VALUES FOR USE WITH THERMAL DIODE INPUTS

Value of Resistor between DPx and DNx	Nominal Temperature Value Generated
510 Ω	-121°C
680 Ω	-69°C
820 Ω	+33°C
1K Ω	+83°C

2.14.1.2 Thermal Diode Configuration

This section provides information on the recommended values for the filter capacitor placed across the thermal diode lines in order to use MEC1721/MEC1723 with various thermal diodes including CPU diodes, GPU diodes, and diode-connected devices such as a discrete 2N3904 device.

TABLE 2-7: TEMPERATURE SENSOR CONFIGURATION (CONTINUED)

Thermal Diode	MAX. Filter Capacitor	Recommended Filter Capacitor
Intel Processor Diode	up to 2200pF +/- 20%	470pF +/- 20%
AMD Processor Diode	up to 2200pF +/- 20%	470pF +/- 20%
nVIDIA GPU Diode	up to 2200pF +/- 20%	470pF +/- 20%
2N3904	up to 2200pF +/- 20%	2200pF +/- 20%

2.14.1.3 Noise Filter Capacitor Recommendation

Microchip recommends adding an optional footprint for a 100pF filter capacitor directly across the diode, which would only be populated if noise on each diode channel needs to be reduced.

2.14.2 ADC/THERMISTOR SUPPORT ON EXTERNAL DIODE LINES

To allow a longer trace run to the CPU well, the Guardian can also use a thermistor as a critical shutdown thermal sensor. The resistor/thermistor divider voltage is driven out on selected DP/DN channels when a measurement is made, and the voltage measurement is made on DN channel. This reading can be capacitively filtered with a 0.1µF capacitor; the results are very immune to noise.

Note: When configured to measure a thermistor on the External Diode channel, it is your responsibility to set the VSET voltage (see Section 2.12, "VCI_IN Pins When Used as GPIO," on page 19) to an appropriate level to emulate the desired threshold temperature. The Guardian will perform no calculations to translate the VSET voltage to an equivalent thermistor voltage. In addition, high and low limit comparisons are not changed so you should set these limits to the appropriate values.

2.15 PECI

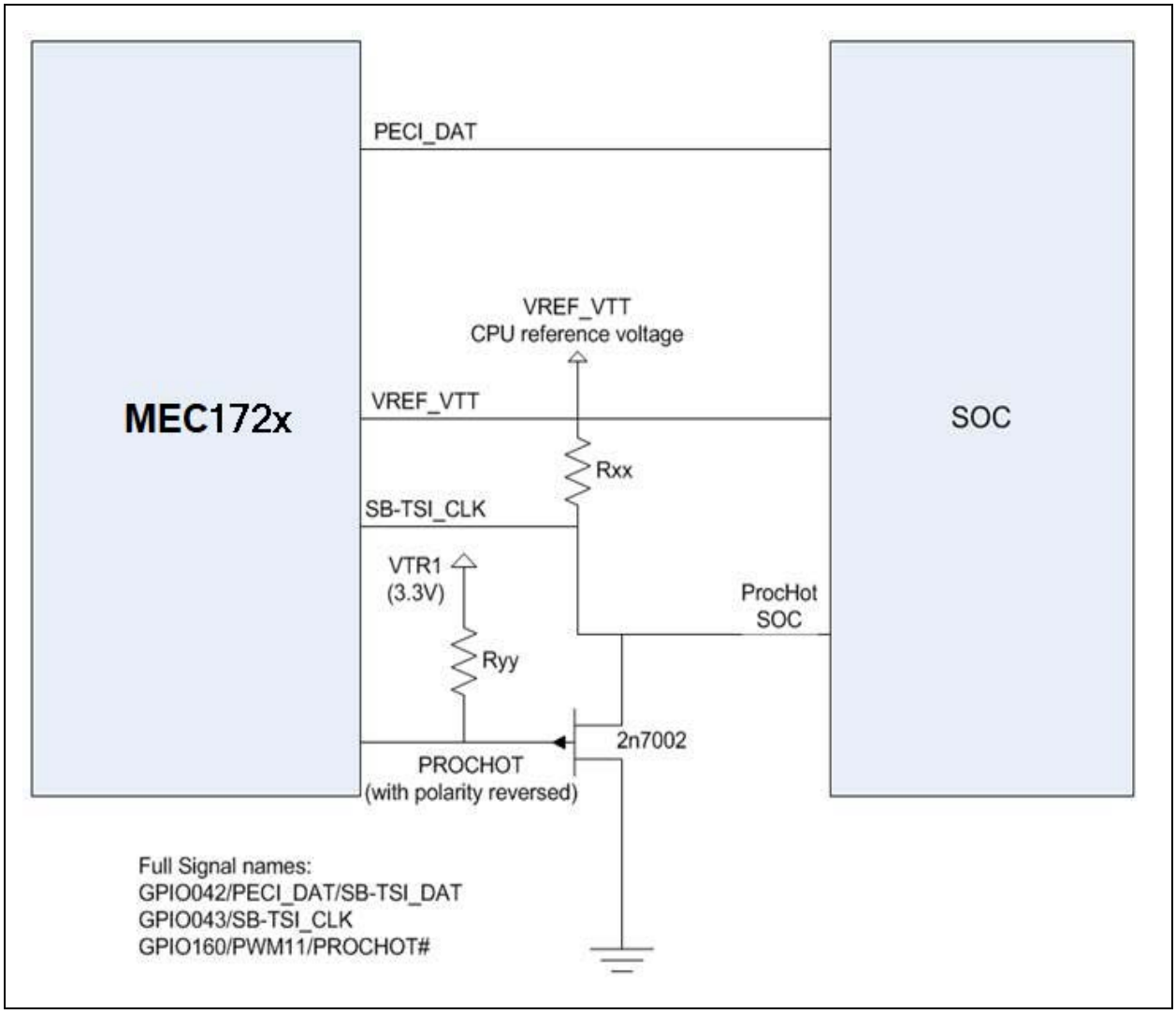
The PECI Interface core logic is powered by VTR1; the physical interface power domain is VREF_VTT. If PECI is not used, the corresponding MUX_CONTROL field for GPIO044 should be set to GPIO in order to minimize leakage current when VREF_VTT is not required.

2.16 Prochot Implementation

For the MEC1721/MEC1723, the Prochot signal is a VTR1 bidirectional signal, which VTR1 can be either 1.8V or 3.3V. This will require an external voltage translator circuit. This issue has no impact on the functionality of PECI.

The recommended implementation shown here is a circuit that uses an inexpensive 2n7002 FET. It drives GPIO160/PWM11/PROCHOT has an output only, but with polarity inversed to use a 2n7002 FET. It optionally accepts a PROCHOT input on the SB-TSI_CLK pin if an input is needed.

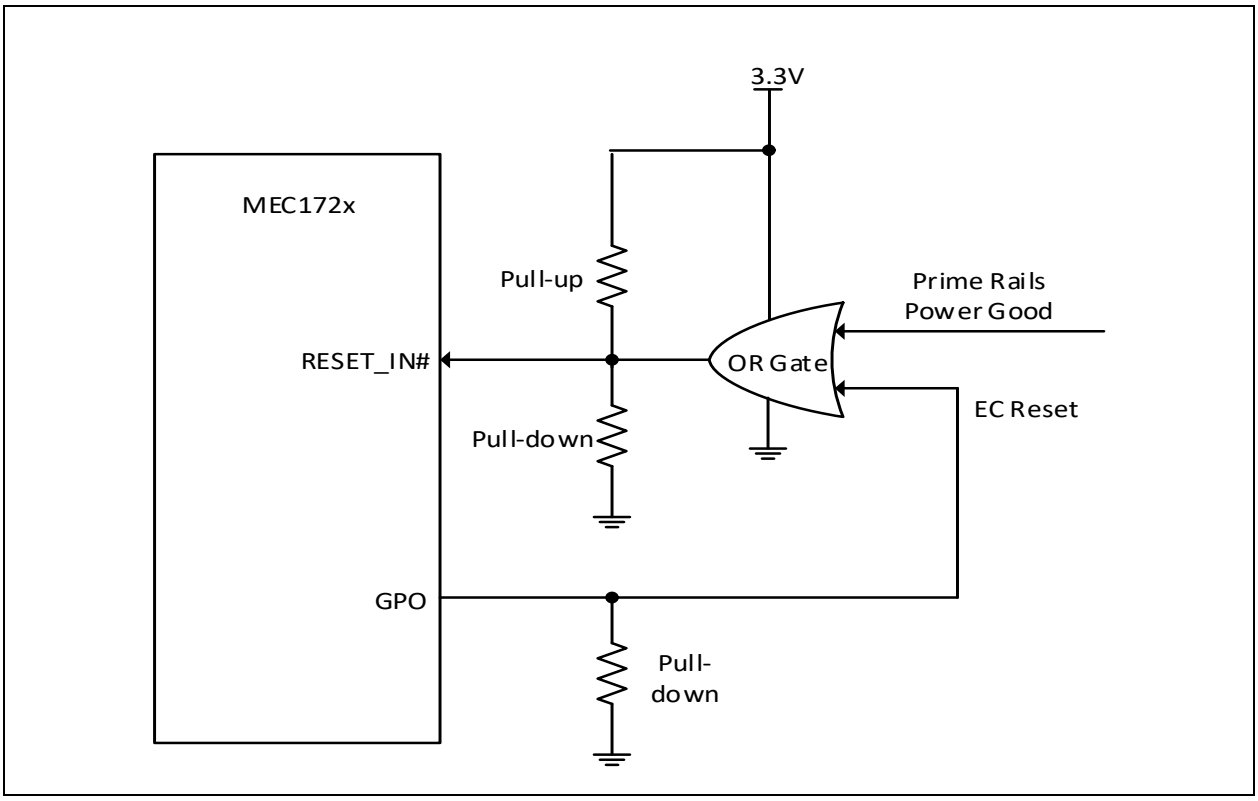
FIGURE 2-11: PROCHOT IMPLEMENTATION



2.17 MEC1721/MEC1723 Shared SPI Flash Isolation Requirement

Per latest Intel PCH design, all the SPI lines to the PCH are tied to GND until the prime rails come up. In this case, designer has to implement one of the below:

- Isolation on all Shared SPI pins or
- Keep th PCH powered all the time or
- Wait for the Prime Rails to come up by holding the EC in reset by the RESET_IN# pin. The example circuitry is shown in the figure below.


3.3V
MEC172x
Pull-up
Prime Rails
Power Good
RESET_IN#
OR Gate
EC Reset
Pull-down
GPO
Pull-
down

3.0 JTAG DESIGN AND LAYOUT GUIDE

This section provides general hardware information for using the MEC1721/MEC1723 JTAG interface and working with JTAG master and slaves.

This document includes the following topics:

3.1 MEC1721/MEC1723 JTAG Capabilities

MEC1721/MEC1723 devices have the following debug capabilities:

- JTAG-Based DAP Port, Comprised of SWJ-DP and AHB-AP Debugger Access Functions
- Full DWT Hardware Functionality: 4 Data Watchpoints and Execution Monitoring
- Full FPB Hardware Breakpoint Functionality: 6 Execution Breakpoints and 2 Literal (Data) Breakpoints
- Accessed via 4-wire JTAG or 2-wire ARM SWD
- Comprehensive ARM-Standard Trace Support: Full DWT, ITM, ETM, TPIU functionalities

3.2 General PCB Layout Considerations for JTAG

Please follow the PCI Specification's Routing and Layout Guidelines for the JTAG interface signals to support the JTAG interface speed up to 33MHz.

- In order to improve the clock transmission line's signal integrity, the following is recommended:
  - Keep the clock traces as straight as possible.
  - Use arc-shaped traces instead of right-angle bends.
  - Do not use multiple signal layers.
  - Do not use vias to reduce impedance change and reflection.
  - Place a ground plane next to the outer layer to minimize noise effect.
  - Terminate clock signals to minimize reflection.
- The JTAG cable that attaches to the MEC1721/MEC1723 motherboard has a standard 20-pin .1" spacing female connector on it. Normally, the MEC1721/MEC1723 motherboard just has a 20-pin 0.1" spacing pin strip on the board to mate with it.
- If the MEC1721/MEC1723 motherboard design does not have the space for a 20-pin male pin strip, then the board designer can place a 6 pin header on the motherboard and build a 6-pin to 20-pin adapter cable to attach to the 20-pin female connector on the JTAG cable. This is shown in Figure 3-1, "6-Pin to 20-Pin Adapter Board (w/ BOM)".

3.3 Pin Connections

3.3.1 4-WIRE JTAG CONNECTION

Six signals are the minimum number required on the motherboard side; these are described in Table 3-1 and illustrated in FIGURE 3-1: 6-Pin to 20-Pin Adapter Board (w/ BOM) on page 25.

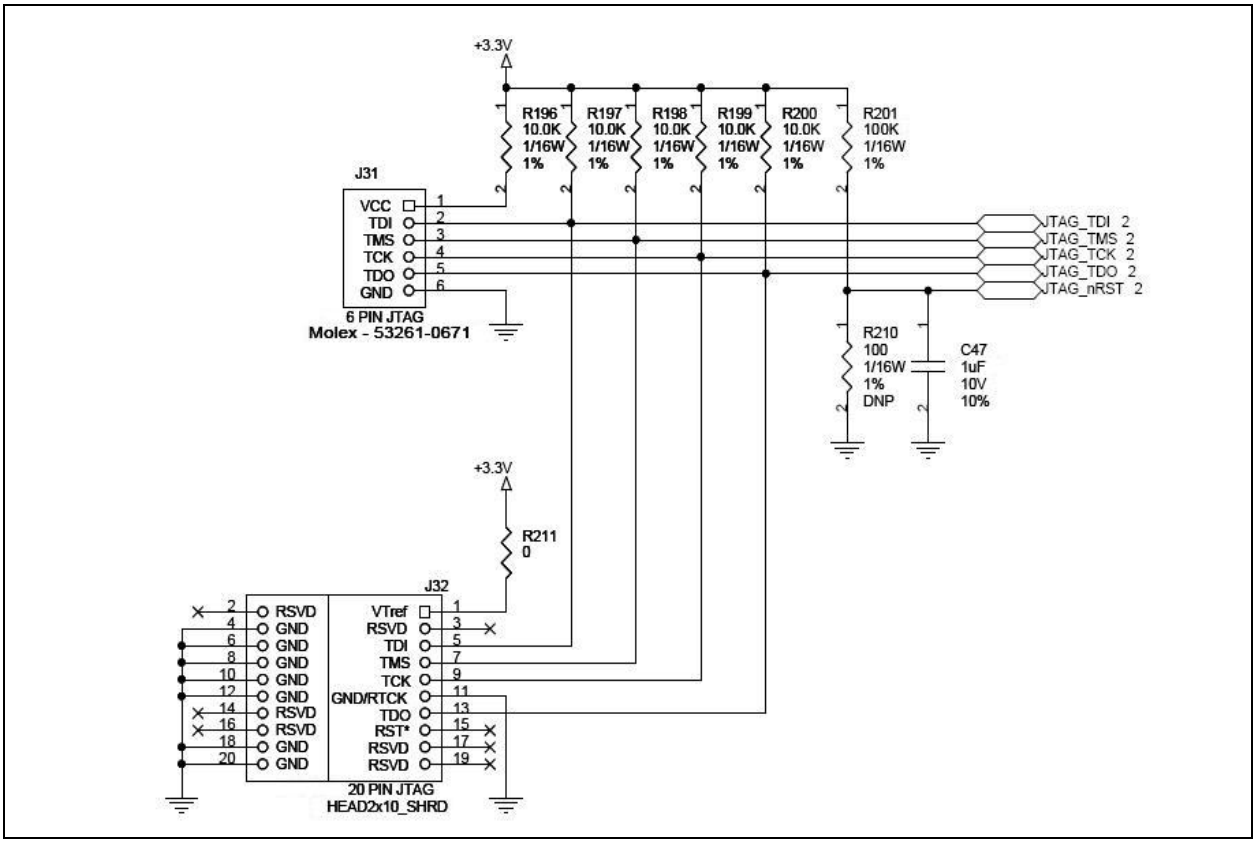
TABLE 3-1: MEC1721/MEC1723 4-WIRE JTAG PINS

Name	JTAG Cable Connection
VTR	The motherboard VTR is always 3.3V. It is recommended to add a 49-ohm series resistor for motherboard protection. The JTAG cable senses the voltage level on this line and drives the JTAG logic levels to the same voltage level from the target system.
TDI	Test Data In
TMS	Test Mode Select
CLK	Test Clock

TABLE 3-1: MEC1721/MEC1723 4-WIRE JTAG PINS (CONTINUED)

Name	JTAG Cable Connection
TDO	Test Data Out
GND	Motherboard ground connect

FIGURE 3-1: 6-PIN TO 20-PIN ADAPTER BOARD (W/ BOM)



Note 1: The 10K pullups that are shown in Figure 3-1 are used on MEC1721/MEC1723 JTAG inputs to prevent them from floating when the JTAG cable is not attached.

2: The MEC1721/MEC1723 JTAG RST# pin connects to a 100K pullup to always enable the JTAG interface. Board design can provide pads for a pullup and pulldown for this pin in motherboard layout.

3: In order to prevent potential damage, use a keyed connector to avoid plugging the cable in backward which would result in a short between VTR and ground.

4: Add zero-ohm resistors to the JTAG link if there is a JTAG chain is used.

3.3.2 2-WIRE JTAG CONNECTION

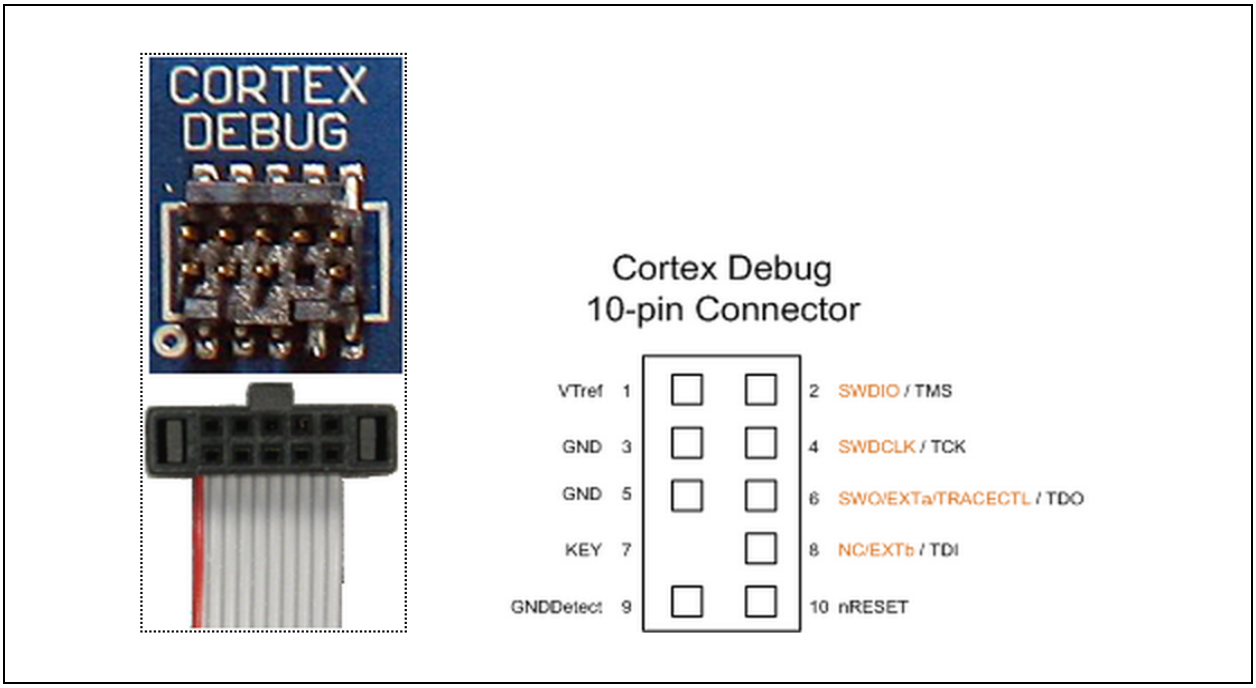
Five signals are the minimum number required on the motherboard side; these are described in Table 3-2.

TABLE 3-2: MEC1721/MEC1723 2-WIRE JTAG PINS

Name	JTAG Cable Connection
VTR	The motherboard VTR is always 3.3V.
SWDCLK	Use on JTAG_CLK pin if selected.
SWO	Use on JTAG_TDO pin if selected.
SWDIO	Use on JTAG_TMS pin if selected.
GND	Motherboard ground connect

Figure 3-2 shows the standard ARM Cortex 10 pins connector (a Samtec FTSH-105-01 w/ pin 7 removed).

FIGURE 3-2: 10-PIN CORTEX DEBUG (0.05”) CONNECTOR



3.3.3 TRACE FUNCTIONS CONNECTION

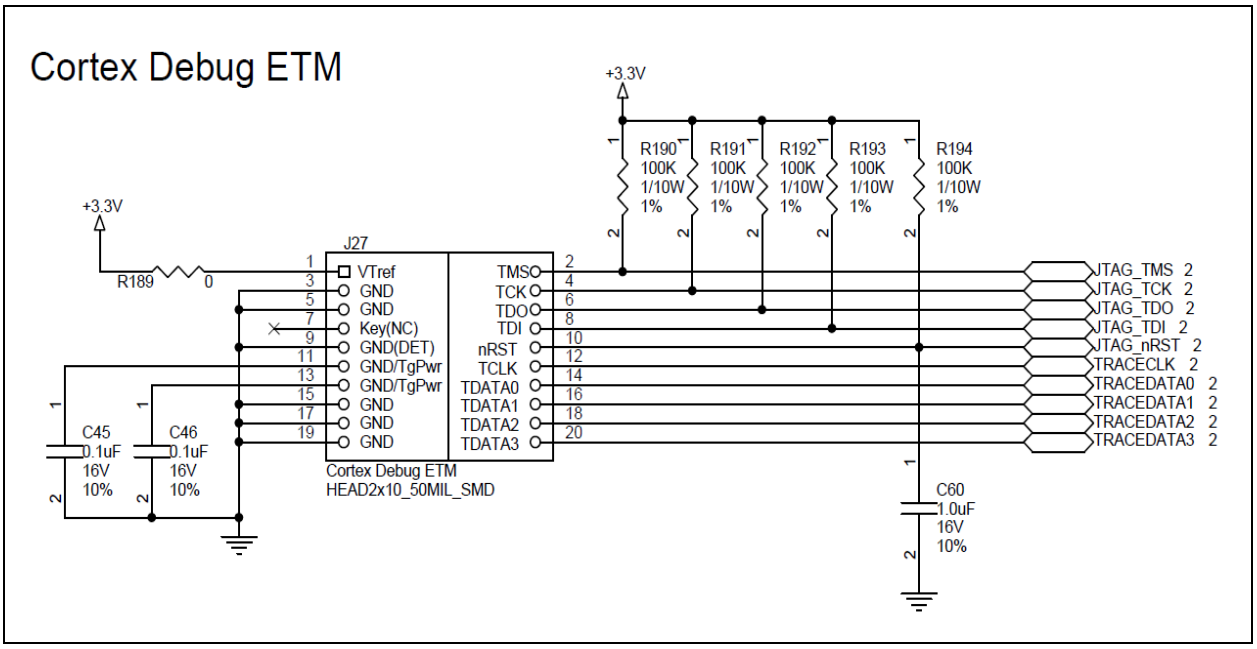
To use the trace support functionalities, the additional signals are required on the motherboard side; these are described in Table 3-3 and illustrated in FIGURE 3-3: 20-Pin cortex debug with trace support (0.05”) Connector on page 27.

TABLE 3-3: MEC1721/MEC1723 JTAG PINS TO SUPPORT TRACE FUNCTIONS

Name	JTAG Cable Connection
TRACEDAT0	ARM Embedded Trace Macro Data 0
TRACEDAT1	ARM Embedded Trace Macro Data 1
TRACEDAT2	ARM Embedded Trace Macro Data 2
TRACEDAT3	ARM Embedded Trace Macro Data 3
TRACECLK	ARM Embedded Trace Macro Data Clock

The 20 pin connector is a Samtec FTSH-110-01 with pin 7 removed.

FIGURE 3-3: 20-PIN CORTEX DEBUG WITH TRACE SUPPORT (0.05”) CONNECTOR



3.4 JTAG Internal Pull-Up

The firmware can select which debug pins to enable the internal pull-high. Default is disabled. Please see the MEC1721/MEC1723 Data Sheet DEBUG ENABLE REGISTER (4000_FC20h) at section 47.8.5 for more information.

3.5 JTAG Reset

When the JTAG_RST# pin is not asserted (logic'1'), the JTAG_TDI, JTAG_TDO, JTAG_TCK, JTAG_TMS signal functions in the JTAG interface are unconditionally routed to the JTAG interface; the Pin Control register for these pins has no effect. When the JTAG_RST# pin is asserted (logic'0'), the JTAG_TDI, JTAG_TDO, JTAG_TCK, JTAG_TMS signal functions in the JTAG interface are not routed to the interface and the Pin Control Register for these pins controls the muxing. The pin control registers cannot route the JTAG interface to the pins. The system board designer should terminate this pin in all functional states using jumpers, pullup or pulldown resistors, and so forth.

JTAG registers are set to their initial values by the assertion of the JTAG_RST# pin. The JTAG_RST# pin must be held low while the MEC1721/MEC1723 devices are powering up so the registers can be set to their proper default values. If JTAG_RST# is high during power up, the JTAG registers may be set to unpredictable values. This can trigger unwanted test modes and the system may not run correctly. As a result, the JTAG_RST# pin must be held low for at least 5.00 msec when applying VTR power.

Note:	For more details on the JTAG_RST# pin, in particular JTAG_RST# functionality with respect to VTR power up events, as well as RESETI# reset input pin transitions, see the JTAG section in the MEC1721/MEC1723 Data Sheet.

The minimum required JTAG signals as shown in Table 3-1 does not include the JTAG_RST# signal. There are several options to handle the absence of this pin as followed:

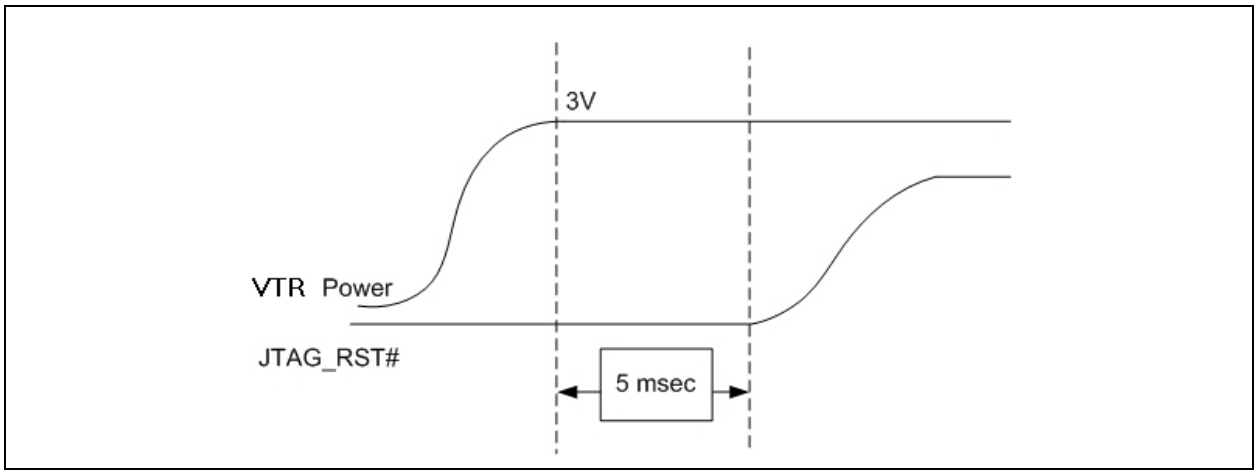
- Production Mode with JTAG Port Disable:
  - Hold the JTAG_RST# pin low with pulldown resistor to disable the JTAG port. Add a pullup resistor option (do not populate) for potential failure analysis to allow use of the JTAG interface. In this case, the JTAG_RST# pin must be manually held low at least 5.00 msec on power up.
- Production Mode with JTAG Port Enable:
  - Add a jumper to hold the JTAG_RST# line low during power up, then remove the jumper in order to ensure that it meets the 5.00 msec timing requirement.

Optionally, put in hardware Resistor-Capacitor (RC) circuitry to force the JTAG_RST# signal low for at least 5.00 msec. For example:

1. Use a MEC1721/MEC1723 EVB with external power supply which shows the rise time less than 100µs.
2. RC = 100K ohms resistor pullup to VTR and 1µF capacitor.
3. The rising timing of VTR related to the JTAG_RST# signal is shown in Figure 3-4; the falling time should be a reverse of the rising time.

Note:	The RC values need to be changed in order to compensate for the power supply time to ensure a 5.00 msec reset pulse, measured from VTR = 3.3V to JTAG_RST# = 0.8V.

FIGURE 3-4: VTR VS. JTAG RISING TIME



APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00003759A (12-01-20)	Document Release	

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