



Galvanically Isolated Gate Driver Design with SG1524

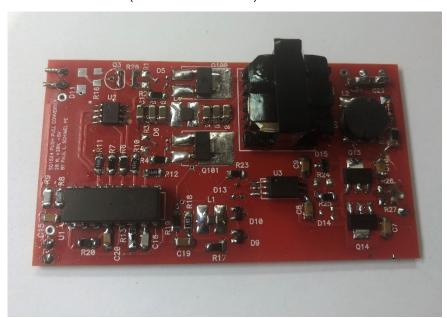
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1. Galvanically Isolated Gate Driver Design with SG1524

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10W Galvanically Isolated Gate Drive Supply for Space Applications based on Microchip SG1524 PWM Controller and MRH10N22U3SR (JANSR2N7587U3/746) Rad-Hard MOSFETs



2. Introduction

The SG1524 Pulse Width Modulation (PWM) controller has been around for a long time. It has been used, modified, and repurposed in applications that include motor controls, hot-swap circuitry, electronic fuse/circuit breaker, multiphase converters, DC to DC converters, and class D audio amplifiers in markets spanning industrial, consumer, automotive, and aerospace, defense and space. This well copied, well exploited PWM controller IC is one of the foundational building blocks of power electronics.

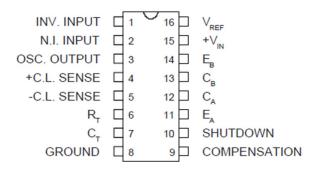
This design will showcase the Microchip SG1524 PWM controller IC and Microchip Radiation Hardened MOSFETs in a 10W push pull converter designed to run a galvanically isolated gate driver channel. The push pull is the simplest topology that drives both positive and negative flux excursions in the transformer at this power level. This has the added advantage of operating both primary switches with respect to ground.

The output stage will use diodes and not synchronous rectification. Recall, this is a small converter, running a driver that switches large MOSFETs in a large motor drive. Synchronous rectification MOSFETs require added expense, added complexity and often come with noise immunity and current sinking concerns. Simple diodes do not have these problems. If we are driving a high-side switch that commutates from 1000V down to 0V quickly, a simpler output rectification stage is better.



SG1524 Features

- 8V to 40V operation
- 5V reference
- · Reference line and load regulation of 0.4%
- 100 Hz to 300 kHz oscillator range
- · Excellent external sync capability
- Dual 50 mA output transistors
- Current limit circuitry
- · Complete PWM power control circuitry
- · Single-ended or push-pull outputs
- · Total supply current less than 10 mA



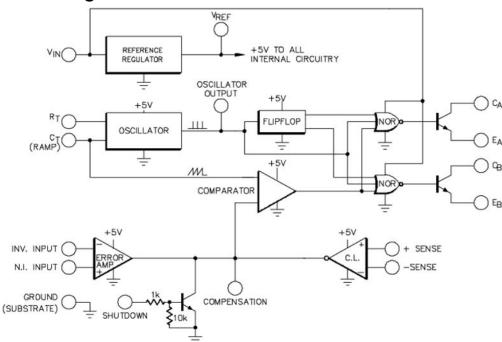
SG1524 High Reliability Features

- Available to MIL-STD-883, ¶ 1.2.1
- MIL-M38510/12601BEA SG1524J-JAN

Introduction

- MSC-AMS Level "S" processing available
- Available to DSCC-standard microcircuit drawing (SMD)

3. Block Diagram



4. Basic Power Discussion

Whether a pump jack in an oil field or a processor core in a satellite, the load requires both current and voltage to do any work in an electrical domain. Most would consider this as "stating the obvious", but there have been many cases where this wasn't considered and proved catastrophic, usually right after a decree to the effect of "it works great in simulation, thereby it works great and we are done."

How much power should the isolated DC-to-DC converter then deliver to the driver channel? To answer this question, we need to understand the power switches being driven. The days of driving buried Base Emitter (BE) junctions in large Darlington power switches and then attempting to sweep out the carriers to speed-up recombination time are over, thankfully.

Most all modern power switches for fast switching applications are MOS devices. An Insulated Gate Bipolar Transistor (IGBT) is a combination of a high voltage (HV) intrinsic PNP transistor and an N channel MOSFET. The stand-alone MOSFET whether in silicon (Si), silicon carbide (SiC), gallium nitride (GaN), or perhaps even futuristic graphene, has a gate capacitance. No DC current to the gate. If we look at a large, modern SiC MOSFET module, the MSCSM120AM02CT6LIAG for example, we see a total gate charge of 2.8 μ C. By comparison, an equivalent Si IGBT module of similar ampacity and voltage would have a total gate charge on the order of 12 μ C to 15 μ C for a Field Stop Trench technology. Older IGBT technologies could reach twice this number. In light of this, it's easy to see why SiC is attractive. It's capable of switching much faster.

If modelled as strictly an input capacitance (Ciss) interaction, total gate charge is ALWAYS greater than Ciss*V. This is because there are different MOSFET capacitances interacting. If we consider a MOSFET gate drive waveform, the first region is purely driving Ciss, the input capacitance. Once the channel accumulates enough charge, the drain starts to swing, this typically happens at the onset of the Miller plateau. At this point Crss and Coss are being discharged. These interactions contribute to the total gate charge due to the capacitances forming a voltage divider.

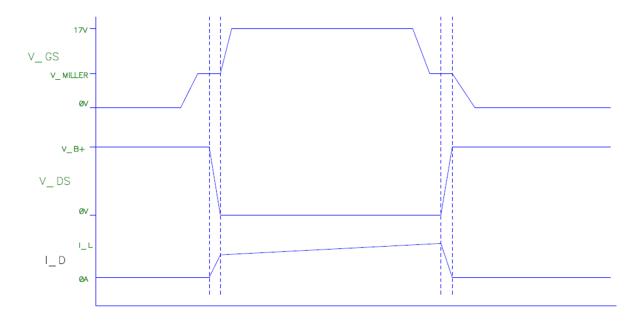
Total gate charge offers a convenient means of looking at peak current and timing. Remember:

$$Q = CV = \int A^*dt$$

If, for example, we were pursuing the fastest switching frequencies, we may choose to have a rise and fall time of 200 ns. If the total gate charge is 2.784 μ C, the driver will have to deliver a peak current of about 14A. This is not a task for a small, fashionable driver IC. The totem pole output impedance required to deliver 14A peak to the gate/source terminals of the module is less than 1 Ω . A driver IC with a totem pole output of 10 Ω is a non-starter in this application.

Clearly the isolated DC-to-DC converter has to do work to run this driver, but how much work does it have to do? If we traversed 0V to 17V in 200 ns using 14A of current, each and every turn-on cycle draws a 14 µJ impulse of energy. If we operate the power switch at a carrier frequency of 30 kHz, we would then need approximately 1/2W of power delivered to the driver channel to deliver this energy at the given rate.

Figure 4-1. VGS Waveform



To compare this estimate to a simple CV2/2 calculation, Ciss is given as 36.2~nF for the MSCSM120AM02CT6LIAG module. We then know that the on-state voltage is 17V. The energy that is then delivered to Ciss is then $5.23~\mu J$. To deliver this energy at a rate of 30 kHz, we would need 0.16W. This is strictly using Ciss when we know there is more interaction.

A classic faux pas in gate driver design is the bypassing capacitance on the rail of the isolated DC-to-DC converter. If the gate source charge (Cgs) of the MOSFET being driven were 36 nF as depicted as above, and the bypassing capacitance on the isolated DC-to-DC converter output were perhaps 10 nF, each gate-drive event would pull the rail down to a very low voltage. Remember, the feedback network in the isolated DC-to-DC converter has a dominant pole somewhere near the natural resonant frequency of the output LC circuit. This is usually in the range of a few kHz.

A discussion of these topics can be found in the "Back to Basics: Understanding Switching Power Supplies" design articles (See reference 3). This is surely much slower than the rise time of the MOSFET being driven. The converter will then droop momentarily, likely pushing the driver into undervoltage lockout then overshoot a bit when it comes back up. This is not a good design practice. In most instances it's catastrophic. The solution is simple: keep the bypassing capacitance of the output of the isolated DC-to-DC converter much larger than the capacitance being driven, keep the ESR low enough to source the current.

From this brief discussion, we can determine the isolated converter output and power specifications. We know we need about 1/2W of power. The isolated DC-to-DC converter should then be designed to deliver at least 5W continuous. The good news is that 5W isn't a lot of power. The insulation system in the transformer will take up more space in the build than the wire.

For this application, we are designing a more universal driver that may be used in much larger IGBT drive applications. This design will deliver a 10W isolated DC-to-DC supply. The MOSFET driver should be able to produce a 20A peak with very low collector to emitter saturation voltage (Vce,sat) or totem pole output impedance (for BJT and MOSFET structure respectively).

Converter specifications

- P_{out} = 10W
- V_{IN} = 8V to 16V DC, 12V nominal
- V_{OUT} = -5V, 0 (return), +17V
- Fsw = 300 kHz
- Isolation: 3500V rms for 60 seconds
- · Capacitance from primary to secondary: 30 pF or less

- -55°C to +120°C ambient
- Minimal airflow (vacuum; space)

5. Transformer Design

The transformer starting point is a bit unconventional. We know that this converter will drive high-side MOSFETs on a DC bus up to perhaps 1kV. The insulation system that isolates the primary and secondary should be substantive. The insulation system will take up more space than the windings. We can't really look at a minimal core set to start this design.

We know the output voltages to be –5V and +17V. Due to pin and build constraints, the output will use a 5V Zener to stabilize the negative rail. There aren't enough pins to have two secondary windings. As for feedback, where most converters would rely on an opto-isolator and secondary shunt reference (perhaps a PC817 and a TL431), this design will use a primary side sense winding. This was done to allow for future applications in Low Earth orbit or higher space orbits where opto-isolators degrade severely over both single event effects and Total lonizing Dose radiation. The primary sense winding is not susceptible to these things at all, although it will not be as precise as direct secondary side control due to non-ideal flux coupling between the primary sense winding and the secondaries.

The best starting point for the transformer design is to go back to Abraham Pressman's core selection formula in Chapter 7. (see references, 1). This formula looks at the available winding window area, core cross section, desired maximum flux swing and switching frequency.

WaAc = Pout*Dcma / Kt*Bmax*fsw

Where:

Wa = Window area in core*core cross section (cm^4)

Po = Output power (Watts)

Dcma = Current Density (circular mils/ampere)

Bmax = maximum flux density (Gauss)

Fsw = switching frequency (Hz)

Kt = topology constant (0.001 for push pull converter, 0.0003 for flyback)

If we use the converter specifications and a reasonable current density of 350CM/A (circular mils per ampere), a Bmax of 1000Gauss (good conservative starting point), Kt of 0.001 and Fsw of 300 kHz, we calculate WaAc of 0.023cm4.

If we apply this to the selection tables from the core manufacturer (Mag Inc. used in this case, EE type core set), we see that the 41707 pattern core set will work in the design. This core set has a beam width of 16.8 mm, a beam length of 7.11 mm, an Ae of 0.126 cm², a window area of 0.24 cm² and WaAc of 0.031 cm⁴. The next larger core size is the 41808. This has a beam width of 19.3 mm, a beam length of 8.1 mm, an Ae of 0.228 cm², a window area of 0.333cm2 and WaAc of 0.076cm4.

For this design, the 41808 is a better deal. Al value is higher, which means we get more magnetizing inductance per turn, Ae is larger so we get lower deltaB for a given number of turns, and the winding window is larger which should allow for the augmented insulation system. This is traded for a little extra space claim on the PCB.

With this, we have selected a reasonable core set based on known good engineering principles. But what to do with it? I once heard an "expert" describe a transformer as "arbitrary iron and copper." Said expert never designed a transformer that worked, so there is likely a little more to it than "iron and copper."

The core material still hasn't been selected. Remember this is a power transformer in a push-pull converter. There is an output inductor after the rectifiers. The transformer is to transfer power from primary to secondary. For this, we don't want a low permeability material. Powdered iron would be silly in this case. We aren't trying to store energy in a distributed air-gap in the core, we are trying to transfer power and store minimal energy in the core. For this, we need high permeability and low loss at the switching frequency.

Powdered iron, even at its highest concentrations has relatively low permeability, perhaps $\mu r = 250*\mu 0$ maximum. We can dismiss that material for this design. If we tried something silly like 29Ga grain oriented M6 silicon steel laminations in this design, we'd discover that the permeability is great, probably on the order of 15,000* μ 0 but the eddy current losses in the steel from high frequency switching are astronomical. Another asymptotic non-starter. With these boundaries, we drill into soft ferrites in the core selection process.

NiZn ferrites are expensive and have lower permeability. Ni is good for lower losses at higher RF frequencies. At 300 kHz, it's not worth the added expense. MnZn ferrite materials work well in the 50 kHz to 500 kHz range. This is our best starting point for this design.

But which material should we use? There are two top contenders in the Mag Inc. line. These are known as P and R material. They both have good permeability and good losses. P material tends to be more common, R material is used for higher ambient temperature designs. Let's go with P material, knowing that the allocation monster has arrived and most anything that deviates from a standard product is hard to find.

The core set we are looking at from Mag Inc. is then part number 0P41808. Let's size the windings and build it up.

It seems sensible to start the design looking at the output section first. At lower voltage, duty cycle goes up in a closed loop design. The output inductor will have to maintain continuous conduction mode at some point.

Before we can calculate the output inductor value, we need to calculate the turns ratio. At 8V input (minimum specification), the duty cycle of the SG1524 controller will be at its maximum. Often safe to assume this as 45%. At a switching frequency of 300 kHz, each push pull primary switch will be on for 1.5 µs of the 3.33 µs total cycle.

The secondary side will rectify this waveform into the output inductor and deliver the output. The secondary side then looks like a buck derived circuit, with an on time of 1.5 µs for both the positive and negative leg of the converter. The duty cycle effectively doubles to 90% as does the switching frequency The inductor will see a pulsed voltage source of (Vsecondary -1Vf) feeding the inductor.

If we set the volt-time product of the driven side of the inductor and the freewheel current path equal, we get: $((Vsec-1Vf)-Vout)*1.5 \mu s = (Vout-1vF)*0.166 \mu s$.

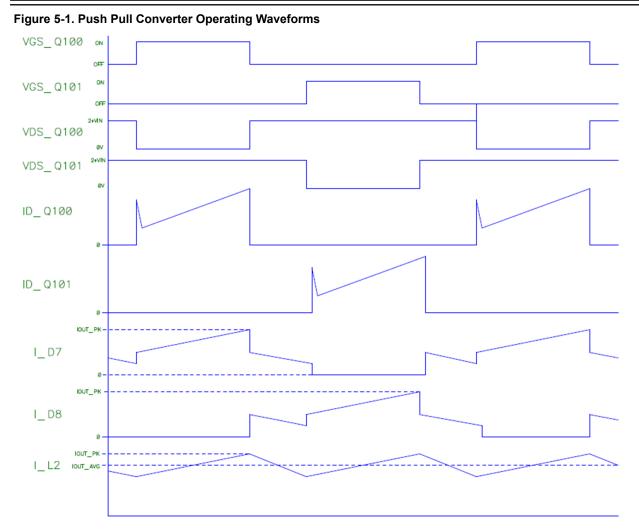
If we assume Vf to be about 1V for the PN output diodes, and Vout = (17 + 5V) or 22V. The secondary voltage must be (22V + 1Vf)/0.90% duty cycle or about 25.5V. This determines our turns ratio.

With this as a guide, let's see what the primary turns should be. We know we don't want a higher flux density. We are trying to run this converter with fairly low temp rise in the transformer core and windings. It operates in an environment with no airflow (space, i.e., a vacuum).

For flux density we use the classic volt-time method: deltaB = (Vpeak*t-on*108)/(2*N*Ae). If we set deltaB at 1000 Gauss, we get N = (8V*1.5us*108)/(1000G*2*0.228cm2) or N=2.63 turns. It's hard to wind that and it comes with sensitivity problems and low flux coupling.

Let's change this a bit and take the primary to 7 turns. This will leave us with a wonderfully low flux density of deltaB = 376 Gauss and a build that really didn't change from 3 turns. If each half of the primary is 7 turns, the secondary then rounds up to 23 turns.

At minimum line (input) voltage, each half of the center tapped primary is driven at 8V, each half of the secondary must deliver at least 25.5V at the maximum duty cycle of the converter.



The framework is in place to easily calculate the output inductor value. If the output is 17V+5V or 22V in total, the maximum average output current is then 10W/22V or 0.46A. If we put the continuous conduction mode (CCM) boundary at 150 mA average, di/dt is then 300 mA peak to peak. The maximum driven on time is 1.5 μ s. As per V = -Ldi/dt, we get L=((26V-23V)*1.5 μ s)/0.3A or L = 15 μ H. The saturation current of the structure should be above 0.5A, let's specify 1.5A. The maximum volt*time product the structure will see will be 3V*1.5 μ s or 4.5V* μ s.

Output inductor specification (with added headroom): 15 µH, Isat = 1.5A, max V*t of 12V* µs.

At this point, let's walk through the output stage one more time with the proper turns and output inductor. If the primary has 7 turns, the secondaries have 23 turns. The output inductor is 15uH. If the output is 22V + 1Vf or 23V, the duty cycle the PWM must provide is 23/26 or roughly. The on time of each secondary pulse is then 1.5 μ s on a 1.66 μ s total cycle. The inductor current is then 0.46A average with a peak of (0.45+(0.300/2)) or 600 mA and a minimum of 300 mA and a duty cycle of 90%.

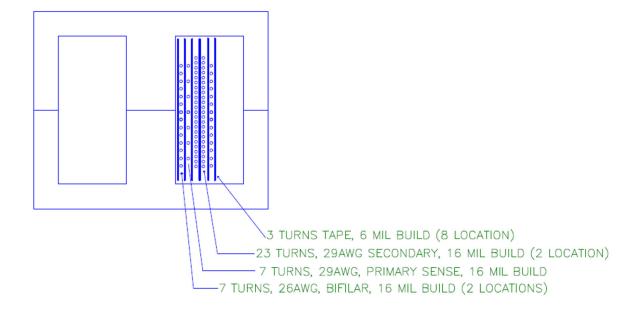
The next logical thing to do is to size the wire for the transformer and start building the windings. At maximum output, we know that the secondary current delivers an average of 0.45A to the load. We also know that di/dt into the inductor is 0.3A or so. The peak secondary current is then 600 mA. The peak primary current reflects this across the turns ratio to get a peak of 23T/7T*600 mA or 2A. And this is where most make a mistake. The driven inductor current isn't the only thing the secondary winding is conducting. We have to recall the circuit operation. The output inductor freewheels through both halves of the primary winding during the freewheel cycle. This freewheel current adds to the secondary current. The freewheel event largely cancels out in that both secondary windings are conducting during a freewheel event. Freewheel current does not reflect to the primary. See waveforms in Figure 1 above.

To improve flux coupling, the windings should be interleaved to the extent that the build will allow. In this case, we know we have a substantive insulation system between primary and secondary. Too many layers of this is too much build. Let's start with a simple "Primary, Secondary, Primary" interleaving array with both primaries ran in parallel. The downside of interleaving is that the secondary will have a capacitance to the primary on both the inside and outside surface of the winding. Increased flux coupling delivers more primary to secondary capacitance.

Each primary then has to carry about half of the total primary current. But it's not exactly half due to the proximity effect the the Dowell curves.(see References 2.) The inside primary will carry more current than the outside primary when they are operated in parallel. Most old salt transformer designers will usually speak of the inner most winding being the hottest. This is why. Each primary is seeing an average current of about 1A peak *0.45% Duty cycle or 450 mA. To size the primary conductor, if we use 500CM/A we are looking for a wire with a cross section of 225CM. Looking at the wire table, we see that 26AWG wire has a cross section of 254CM and a diameter of 16 mils. The depth of penetration in copper is defined by Dpen = 7.6/sqrt(f) where the result is in cm. At 300KHz this is 0.014cm or 5.5mil. (mil = 0.001"). The solid wire is a little thicker than Dpen, but in this case it should suffice. Each primary winding can then be wound with 26AWG wire, two primary windings will be used in parallel.

For the secondary wire selection, the average current in each half of the winding is around 0.45*600 mA or 270 mA. There will be only one secondary winding per half, no interleaving. For a 500CM/A current density we then need about 135CM of cross section. Looking at the wire table 29AWG wire will accommodate this nicely with a diameter of roughly 11.3 mils.

Figure 5-2. Transformer build. The total build is 128 mil. Should fit the window!.



6. Core Loss

Looking at core loss, we have a deltaB of about 376 Gauss in Magnetics Inc. P material ferrite at 300 kHz. Looking at the loss curves we see a normalized loss of 70 mW/cm³. For this core set, we will then see about 0.13W for the core pair.

7. Copper Loss

Looking at Rac/Rdc losses, we have to go to the Dowell curves, we have worst case layer thickness/dpen = 16mil wire OD/5.5mil Dpen or about 2.9. The total number of layers in the design is five; however, the magnetomotive force (MMF) is stacked up such that only two adjacent layers conduct at the same time. Worst case Rac/Rdc is then about 7.0.

But what is Rdc? In the primary, Rdc is the resistance of the total length of the conductor. The mean length turn for this structure can be approximated as 0.800 inches. Eight turns is then roughly 6.4 inches, where this will have a resistance of about 0.0543 Ω / foot at 105 °C. Rdc is then 30 m Ω . Rac is then roughly 210 m Ω . At a 450 mA primary current, the total copper losses should be around 50 mW per primary. With two primary windings, we then have 100 mW. Assuming the secondary losses are similar to the primary, we have a total of 200 mW in copper loss.

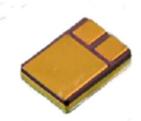
To predict temperature rise, we would need to know the airflow, and maximum ambient temperature, the specific heat of the materials and the orientations and thermally model the structure. For this approximation, those tools are not forthcoming. From experience we would not expect much more than 15 °C rise at the hotspot in the transformer for 200 mW copper loss and 130 mW core loss.

With the iron and copper wrapped up, we can finish up the converter design task.

8. MOSFET and Diode Selection

Based on the waveforms, we have to choose applicable primary MOSFETs and secondary rectifier diodes. The primary has to block twice the maximum voltage when the power switch is in the off condition. For an 16V maximum input, this means the primary switch has to block 32V.

For reasonably low losses, Rdson should be around 50 m Ω . We are then looking for a standard threshold, Vds > 60V, Rdson < 50 m Ω , N-channel MOSFET. We then use our own portfolio and the MRH10N22U3SR in SMD 0.5 package, which is the smallest R6 Microchip die. This MOSFET is radiation hardened by design (See JANSR2N7587U3/746 slash sheet) and furnished in the SMD 0.5 package. The devices have been developed for total ionizing dose (TID) and single-event environments (SEE). I2MOS tm will perform in extreme-environment applications and will remain within specifications in radiation environments up to 300 krad TID.



SMD 0.5

R6 Rad Hard MOSFET Features

- Low Rdson
- · Fast switching
- · Single-event hardness
- · Low gate charge
- · Simple drive
- Ease of paralleling
- · Hermetically sealed
- Surface mount ceramic package, roughly 0.4" × 0.3" × 0.125"
- –55 °C to +175 °C operating temperature range

R6 Rad Hard MOSFET Applications

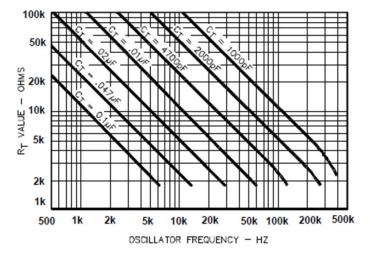
- DC-to-DC converters
- Motor control
- · Switch mode power supplies
- · HVAC linear applications

For the rectifier diodes, a 1A diode will suffice. The diode has to block a maximum of about 52V. A voltage rating of 100V then makes sense for suitable design margin. Microchip UES1002 looks like a good candidate.

SG1524 Setup

Setting up the SG1524 controller is fairly straightforward. CT and RT are chosen in accordance with the datasheet to provide a 300 kHz switching frequency.

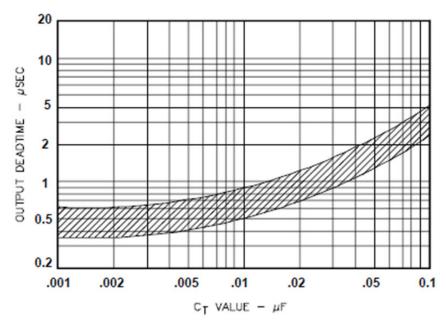
Figure 8-1. Oscillator frequency setup graph



Ct = 1000 pF and Rt = 3300Ω respectively. Both Ct and Rt must be placed as close the IC pins as possible in layout (pins 7 and 6 respectively). Use an NPO or COG dielectric for the ceramic timing capacitor to maintain stable switching frequency over temperature.

It is also noteworthy to mention the sink current in the timing circuit comprised of the SG1524 IC and its respective Rt and Ct values. Ct charges via Rt, forming the ramp used in the PWM comparator, however it discharges through an internal current sink. This is a nuance that is often overlooked, but if the design needs to have a large maximum duty cycle, then it is better to go with a smaller Ct and a larger Rt. This allows the falling edge of the ramp to be as fast as possible. Minimal deadtime, maximal duty cycle. For most designs, this is not problematic, but it is good to know.

Figure 8-2. Note increasing deadtime with increasing Ct.



Vref and Vin both require good bypassing, placed as close to their respective pin as possible. Use an MLCC, X7R dielectric capacitor in the 0.1 µF to 0.47 µF range.

The current sense and error amplifier circuitry should be located as far from the noisy switching circuitry as possible. It is best to use a ground plane, tied directly to the ground pin of the IC. Keep the signal side ground currents on the signal side, keep the power side ground currents on the power side.

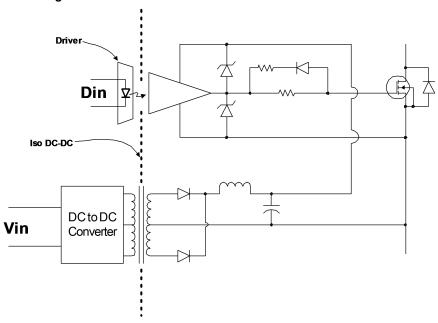
The internal output transistors in the SG1524 are single ended. It is not recommended to use them for driving MOSFETs directly. The added external driver will deliver large peak currents to the driven MOSFETs. This driver requires its own bypassing. Something in the 0.47 μ F to 1 μ F range in X7R MLCC will suffice.

Further, the outputs of the SG1524 can be combined in other applications requiring perhaps a single ended duty cycle of up to Dmax (where it is in the 50% range in this circuit). The emitters should not be tied together directly as the off-state device will sink current from the on-state device and likely be damaged. Rather than directly connecting the emitters, use a diode OR circuit like a pair of 1N4148s to combine the two outputs. Note the maximum duty cycle is in the > 90% range and the relative output frequency doubles as a result of this combination.

9. Driver Design

This is a driver that is applicable to prime movers in the tens of kW to MW power range. In this particular design, there were no advanced features required. Desaturation sensing across the power switch, auxiliary Miller clamps, or voltage and current monitoring were not required. This driver is a galvanically isolated buffer, pure and simple. The power supply design above delivers the energy to the isolated driver across the isolation boundary.

Figure 9-1. Driver block diagram



Note: The opto had to be used for the driver stage due to parts shortages. SOI solution, preferably magnetic is required for this application.

The schematic of the finished driver is as simple as the discussion, however it is worth mentioning that the emitter follower BJTs are the low Vcesat, low BE storage time, high Ft type devices specifically designed for gate driver buffers.

Figure 9-2. Power Supply Schematic

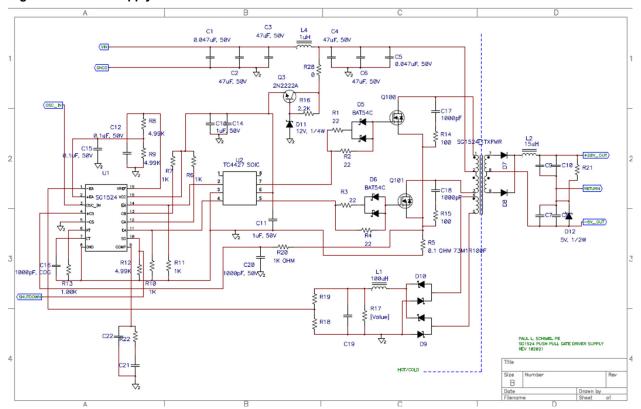
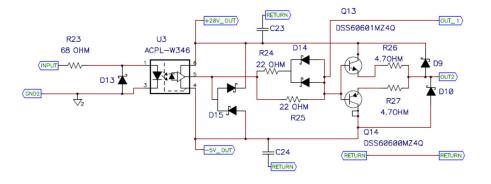


Figure 9-3. Driver Schematic



The following table lists the BOM for the SG1524 device.

Table 9-1. SG1524 BOM

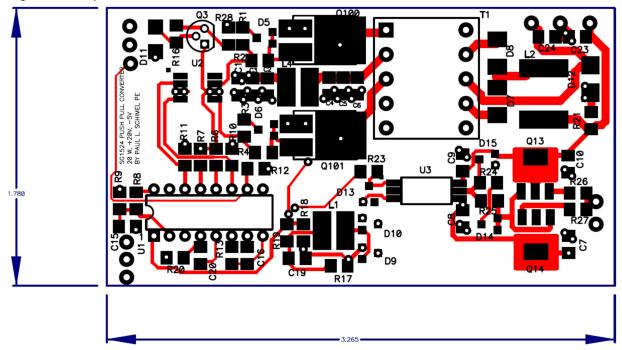
Line Number	Ref. Des.	Value	Description
1	C1, C5, C7, C8, C9, C10	0.047 μF	50V, MLCC, X7R
2	C2, C3, C4, C6	22 µF	50V, MLCC, X7R
3	C11, C13, C14, C23, C24	1.0 µF	50V, MLCC, X7R
4	C12, C15	0.1 μF	50V, MLCC, X7R
5	C16	1000 pF	50V, MLCC, COG

6	C17, C18, C20	1000 pF	50V, MLCC, X7R
7	C21	4.7 nF, 1206	50V, MLCC, X7R
8	C22	470 pF, 1206	50V, MLCC, X7R
9	D5, D6, D13, D14	BAT54C	
10	D7, D8	UES1002SM-1	MICROCHIP
11	D9, D10, D15	BAT54S	
12	D11	DO NOT POPULATE	
13	D12	1N5231BUR1	MICROCHIP
14	L1	100 μH, 1/4A	
15	L2	47 μH, 2A	MSS1048-473ML
16	L4	1 μH, 3A	
17	Q3	NPN, 50V, 800 mA	2N2222A
18	Q13	NPN BJT	DSS60601MZ4Q
19	Q14	PNP BJT	DSS60600MZ4Q
20	Q100, Q101	Nch MOSFET 100V, 0.042 Ω	2N7587U3
21	R1, R2, R3, R4	22Ω, 1206	
22	R5	0.1Ω	73M1R100F
23	R6, R7, R10, R11, R19, R20	1.00K, 1206	
24	R8, R9, R12, R13	4.99K, 1206	
25	R14, R15	100Ω, 1206	
26	R16, R28	DO NOT POPULATE	
27	R17, R21	2.00K, 1206	
28	R18	680Ω, 1206	
29	R22	10.0K, 1206	
30	R23	330Ω, 1206	
31	R24	NO POPULATE	
32	R25	49.9Ω, 1206	
33	R26, R27	4.7Ω, 1206	
34	T1	Transformer	Cramer CSM 19VT-058
35	U1	SG1524	Microchip ST1524
36	U2	TC4427	Microchip TC4427
37	U3	ACPL-W346	

10. PCB Layout

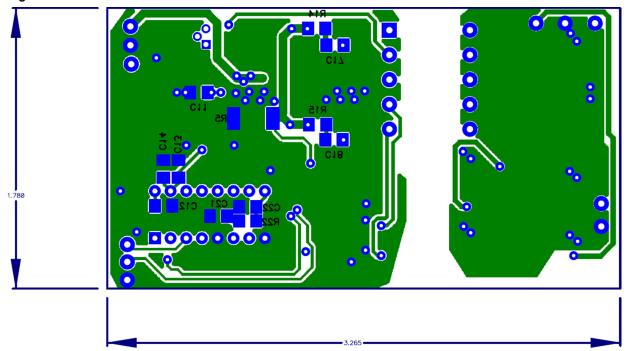
The PCB design task was fairly straightforward. It was desired to keep the solution small and yet serviceable, such that the series gate resistors in the output could be easily replaced and or adjusted. The layout priority went to the push pull MOSFETs, transformer, output and rectifiers. The driver layout priority was simply the buffer. These traces were wide, paths short, ground planes use as much as possible. The setup component around the controller were kept as close as possible. Minimal loop areas on the current and voltage sense connections, best possible bypassing.

Figure 10-1. Top of PCB



Note: Short power paths, controller as far away from stray transformer flux and fast dv/dt as possible.

Figure 10-2. Bottom of PCB

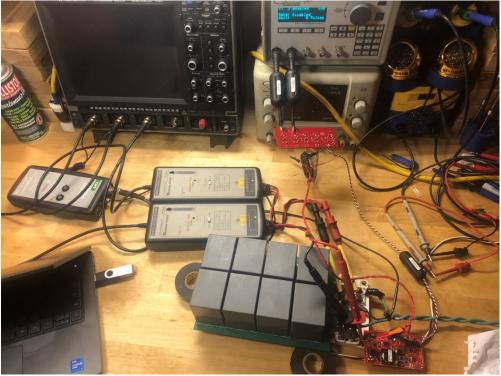


Note: Ground plane layers on both the hot and cold side. Isolation line extends through transformer and opto driver IC.

11. Waveforms

The DC-to-DC converter was validated. A step load showed a well damped response with no ringing. Due to time constraints, gain and phase were not measured, but they are believed to be very stable. The driver output is show below driving the Microchip MSCSM120AM02CT6LIAG SP6LI module in a double pulse tester. Note that this driver is turning on a 1200V, 800A power switch with Cgs of 36 nF in less than 50 ns without showing any gate oscillations or detrimental operation.

Figure 11-1. Double Pulse Test Setup



In the double pulse test setup, the module is mounted directly to cap board with multilayer interleaved PCB and MLCCs as close to terminations as possible. The driver is mounted as close to module as possible.

Figure 11-2. Closeup of Driver in situ

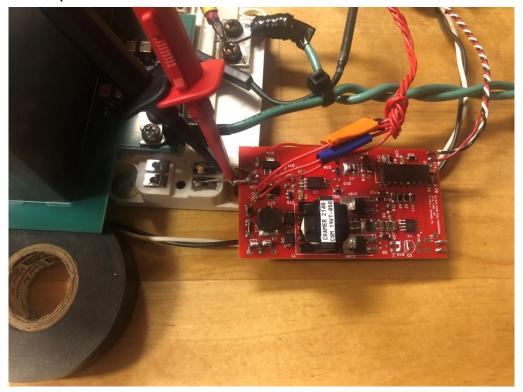


Figure 11-3. Double Pulse Waveform

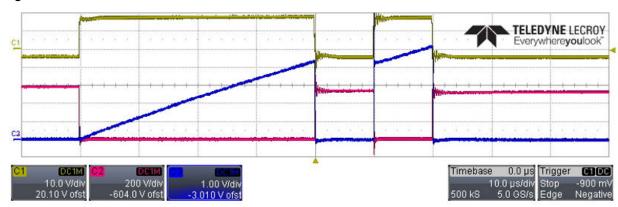


Figure 11-4. Closeup of turn off waveform. No oscillations, No C*dv/dt turn on

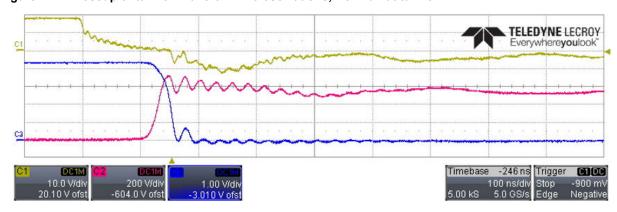
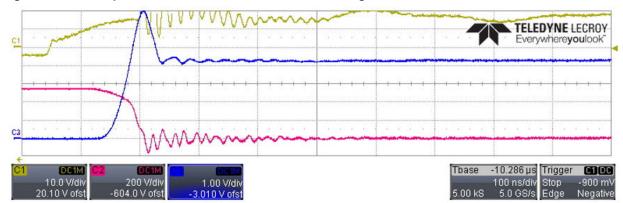


Figure 11-5. Closeup of turn on waveform. No oscillation through Miller Plateau



12. **Conclusions**

This brief design note should offer a reasonable base line for designing a galvanically isolated, radiation hardened DC-to-DC converter. Further the driver efforts can provide a gate drive solution for large state of the art power transistors on HV DC mains in space missions. This product is not a PRF38534 class F or L nonhermetic hybrid module. There is no WCA available. This was designed to showcase Microchip rad hard devices, best circuit design practices and offer guidance for driving HV MOSFETs in space missions. The MOSFETs, controller, and discretes can all be obtained in Rad Hard.

May your electrons continue to flow as you intended!

13. References

- 1. "Switching Power Supply Design"; Abraham Pressman; Second Edition, McGraw Hill; ISBN 0-07-052236-7.
- 2. "Unitrode MAG100"; Lloyd Dixon; TI SLUP132; www.ti.com/seclit/ml/slup132/slup132.pdf.
- 3. Aerospace and Defense Newsletter Edition 7-11: "Back to Basics, Understanding the Switching Power Converter (part 1-5)", Paul L. Schimel PE.
- 4. Wire Table.

14. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 14-1. Revision History

Revision	Date	Description
A	12/2022	Document created.

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