SmartFusion®2 M2S050 (T, TS) Errata

Introduction

This errata sheet contains the device-specific errata and the affected SmartFusion® 2 M2S050 (T, TS) revisions for all the temperature grade devices (commercial/industrial/military).

Revisions Released per Device

The following table lists the revisions released per device and the device status.

Table 1. Revisions Released per Device

Silicon Devices	Revisions	Device Status
M2S050 (T, TS)	Commercial/Industrial/Military	Production

Table of Contents

1. Errata for SmartFusion2 M2S050 (T, TS) SoC FPGA Devices

1.1 Summary of SmartFusion2 M2S050 (T, TS) Device Errata

The following table gives the summary of SmartFusion2 M2S050 (T, TS) Device errata items:

Table 1-2. Summary of SmartFusion2 M2S050 (T, TS) Device Errata

S.No.	Errata	Silicon Revisions		Software Errata
		M2S050 (T, TS)		
		0, 1	2	
1.	The MDDR and FDDR AXI Interface does not Support Exclusive Access	X	X	—
2.	Apply DEVRST_N after ISP Programming	X	—	—
3.	AXI Wrap Transfers with more than 32 bytes in Burst Mode are not Supported for MDDR and FDDR	X	X	—
4.	The MDDR and FDDR Controller must be Used with the Sequential Burst Mode with BL = 8 and PHY = 32, or PHY = 16	X	X	—
5.	Use USBD I/O Group for USB-ULPI Mode in the M2S050-FG896 Devices	X	X	—
6.	Set VPP to 2.5V while Programming/Writing the eNVM at an Industrial Temperature Range	X	—	—
7.	Over-Voltage Support on MSIOs during Flash*Freeze Mode	X	—	—
8.	Verification of the FPGA Fabric at Junction Temperatures Higher than 50 °C Erroneously Indicates a Failure	X	—	—
9.	DDR_OUT and I/O-Reg Functional Errata due to a Software Bug	—	—	X
10.	Dedicated Differential I/O Driving the Reference Clock of the CCC may Cause a Functional Failure due to a Software Bug	—	—	X
11.	NVM Ready bit in eNVM Status Register can Generate a False READY Signal	X	—	—
12.	Power-up Digest is Not Supported	X	—	—
13.	NVM Programming Must only Occur as Part of a Bitstream that Contains the FPGA Fabric	—	—	X
14.	Updating eNVM from the MSS or the FPGA Fabric Requires Changes in NV_FREQRNG Register	X	X	—
15.	SYSCTRL_RESET_STATUS Macro is not Supported	X	X	—
16.	Zeroization is Not Supported	X	X	—
17.	Arm® Cortex®-M3 Register Corruption Under Very Specific Literal Loads from eNVM and Cache Miss/Hit Sequences	X	X	—
18.	PCIe Hot Reset Support Requires a Soft Reset Solution	X	X	—
19.	After Successful Completion of CM3 ISP (without a SYSRESET), LSRAM Read and Write Access Fails From the Fabric Path	X	X	—
20.	Disable Cortex-M3 While Programming eNVM only	X	X	—
21.	The DDR I/Os in M2S050 (T, TS)-FG896 are Non-compliant with the DDR3 Standard	X	X	—

.....continued

S.No.	Errata	Silicon Revisions		Software Errata
		M2S050 (T, TS)		
		0, 1	2	
22.	For S (security) Grade Devices, User Must not Enable Write Protection for Protected 4K Regions	X	X	—
23.	User eNVM Write is Incorrectly Allowed for the Protected 4K Regions	X	—	—
24.	Avoid eNVM Page Lock and Unlock if Code is being Executed from eNVM both in Release and Debug Mode	X	X	—
25.	PCIe hard IP core receive FIFO may reach the full condition resulting in incorrect data passed to PCIe subsystem and cause the PCIe core to ignore subsequent PCIe traffic	X	X	—

Notes:

- "X" indicates that the errata is available for that device and revision number.
- "—" indicates that the errata is not available or the feature does not exist for that device and revision number.

Software errata can be avoided by using the Libero® SoC v11.4 SP1 or later versions.

Contact Microchip Global support for any additional questions. To order a specific die, contact your local Microchip sales office.

2. Errata Descriptions and Solutions

This section lists the device-specific erratas and their workarounds.

2.1 The MDDR and FDDR AXI Interface does not Support Exclusive Access

The MDDR and FDDR Advanced Extensible Interface (AXI) in the M2S050 device is compliant with Advanced Microcontroller Bus Architecture (AMBA) AXI Protocol Specification v1.0, except for the exclusive access functionality. The future version of the errata will have updated information about the exclusive access functionality for the AXI interface in the M2S050 device.

2.2 Apply DEVRST_N after ISP Programming

The M2S050 devices support device programming in JTAG, slave SPI, and ISP programming modes. However, after ISP programming, DEVRST_N needs to be asserted to reset the device or power-cycle the device to run the new design.

2.3 AXI Wrap Transfers with more than 32 bytes in Burst Mode are not Supported for MDDR and FDDR

Do not use wrap transfers with more than 32 bytes.

2.4 The MDDR and FDDR Controller must be Used with the Sequential Burst Mode with BL = 8 and PHY = 32, or PHY = 16

Although the MDDR and FDDR controllers in the M2S050 devices support various burst modes/ lengths and PHY settings (as specified in the UG0446: SmartFusion2 and IGLOO2 FPGA High Speed DDR Interfaces User Guide), only a subset of these settings are supported.

Workaround

Use only sequential burst mode with BL = 8 for PHY16, or PHY32 modes for the MDDR or FDDR.

2.5 Use USBD I/O Group for USB-ULPI Mode in the M2S050-FG896 Devices

For interfacing the USB OTG controller with ULPI PHY, the USB MSIO signals are connected to four separate mutually exclusive I/O groups: USBA, USBB, USBC, and USBD I/O. In the M2S050-F896 devices, only the USBD I/O group must be used.

Excluding the M2S050-FG896, other SmartFusion2 devices' availability of the USB ULPI I/O group are package specific and some of the packages do not have any USB ULPI I/O group.
For more information, see the DS0115: SmartFusion2 Pin Descriptions Datasheet. In addition, USB is not supported in the VF400, FG484, and FCS325 packages for the M2S050 device.

Workaround

Use channel D for USB I/Os with the M2S050-FG896 devices. For example, The USB_ DATA6 can be connected to the I/O through USB_DATA6_A, USB_DATA6_B, and USB_DATA6_C. Use only USB_DATA6_D in the M2S050-FG896 COM/IND/MIL device.

2.6 Set VPP to 2.5V while Programming/Writing the eNVM at an Industrial Temperature Range

VPP can be set to 2.5V or 3.3V. However, while writing or programming the eNVM of the M2S050 devices below 0 °C, VPP must be set to 2.5V. For VPP minimum and maximum settings, see the DS0128: IGLOO2 FPGA and SmartFusion2 SoC FPGA Datasheet.

Note: The eNVM reading with VPP set to 3.3V or 2.5V operates as intended.

2.7 Over-Voltage Support on MSIOs during Flash*Freeze Mode

When the input voltage is driven above the reference voltage for that bank, additional current can be consumed in the Flash*Freeze mode.

2.8 Verification of the FPGA Fabric at Junction Temperatures Higher than 50 °C Erroneously Indicates a Failure

Run the standalone verification (STAPL VERIFY action) at temperatures lower than 50°C. If a VERIFY action is run at temperatures higher than 50°C, a false verify failure may be reported.
Note: The Check Digest system services can be used to confirm design integrity at temperatures within the recommended operation conditions.

2.9 DDR_OUT and I/O-Reg Functional Errata due to a Software Bug

This errata is only applicable if you create or update your design using Libero SoC v11.1 SP1 or v11.1 SP2. The corresponding I/O will not function properly in the silicon device due to the wrong software implementation of the I/O macro, if there is one of the following conditions in your design.

- Using DDR_OUT macro in your design.
- Combining an output or output enable register with an I/O using the PDC command `set_io <portName> -register yes`.

Workaround

Both the erratas are fixed in Libero SoC v11.1 SP3. Migrate your design to Libero SoC v11.1 SP3 or a newer version, and re-run compile and layout.

2.10 Dedicated Differential I/O Driving the Reference Clock of the CCC may Cause a Functional Failure due to a Software Bug

If your design has the dedicated differential I/O pair driving the reference clock of the CCC, the input clock may not propagate to CCC due to a software bug and the device will fail during silicon testing. There are several options to drive the ref clock of the CCC. One of the options is to drive from “Dedicated Input PAD x” (x = 0 to 3); this uses hardwired routing. In this option, choose single-ended I/O or differential I/O as the reference clock. This errata exists when you choose the differential I/O option, meaning the dedicated differential I/O is used as CCC reference clock input.

This errata cannot be detected in any functional simulation, and can only be detected in silicon testing.

Workaround

The errata is fixed in the Libero SoC v11.1 SP3. Migrate your design to the Libero SoC v11.1 SP3 or newer version, and re-run compile and layout.

2.11 NVM Ready bit in eNVM Status Register can Generate a False READY Signal

If you send an instruction to the eNVM controller and then start polling the READY signal (bit0 of the eNVM Status register) to check when the eNVM controller is ready for the next function, the first assertion of the READY signal occurs when the eNVM controller is not yet ready, resulting in the generation of a false READY signal. However, the immediate next assertion of the READY signal will correctly indicate that the eNVM controller is ready.

The errata is fixed in the Libero SoC v11.1 SP3. Migrate your design to the Libero SoC v11.1 SP3 or newer version, and re-run compile and layout.

Workaround

Add an extra eNVM Status bit read that will poll/read the eNVM Status bit twice as READY.

2.12 Power-up Digest is Not Supported

Workaround:

Use NVM Data Integrity Check System service after the device is ON and check the data integrity.

2.13 NVM Programming Must only Occur as Part of a Bitstream that Contains the FPGA Fabric

The Bitstream Configuration dialog box in the Libero SoC allows the user to program eNVM and the FPGA fabric, separately. However, for the current production of SmartFusion2 SoC FPGAs, the user needs to program the eNVM along with the FPGA fabric. The fabric can be programmed separately, if needed.

Workaround:

The errata is fixed in the Libero SoC v11.1 SP3. Migrate your design to the Libero SoC v11.1 SP3 or newer version, and re-run compile and layout.

2.14 Updating eNVM from the MSS or the FPGA Fabric Requires Changes in NV_FREQRNG Register

While updating the eNVM from the MSS or FPGA fabric, NV_FREQRNG register must be changed from the default value 0x07 to 0x0F, eNVM reads are not affected.

For more details, see "Appendix 2: eNVM and eSRAM Write/Read" of *AC429 SmartFusion2 and IGLOO2 - Accessing eNVM and eSRAM from FPGA Fabric Operations* Application Note.

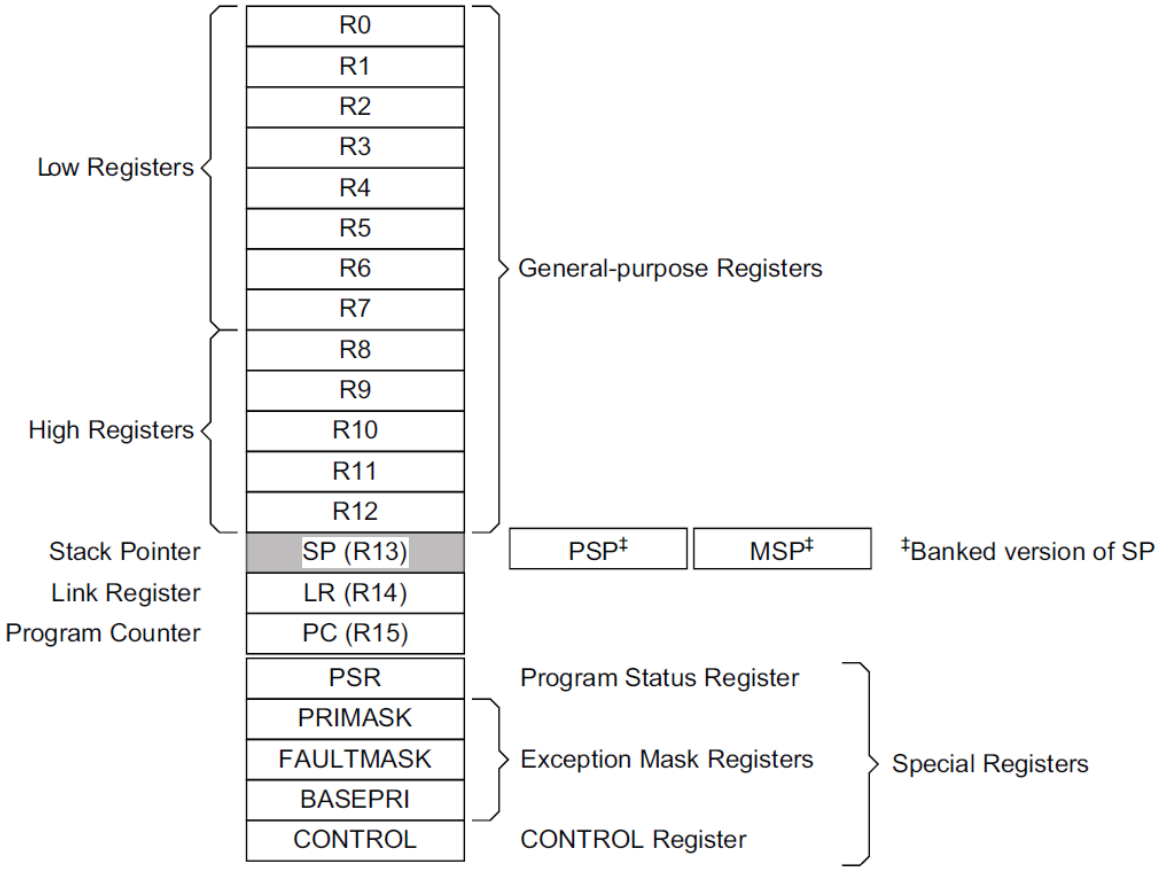
2.15 SYSCTRL_RESET_STATUS Macro is not Supported

2.16 Zeroization is Not Supported

2.17 Arm® Cortex®-M3 Register Corruption Under Very Specific Literal Loads from eNVM and Cache Miss/Hit Sequences

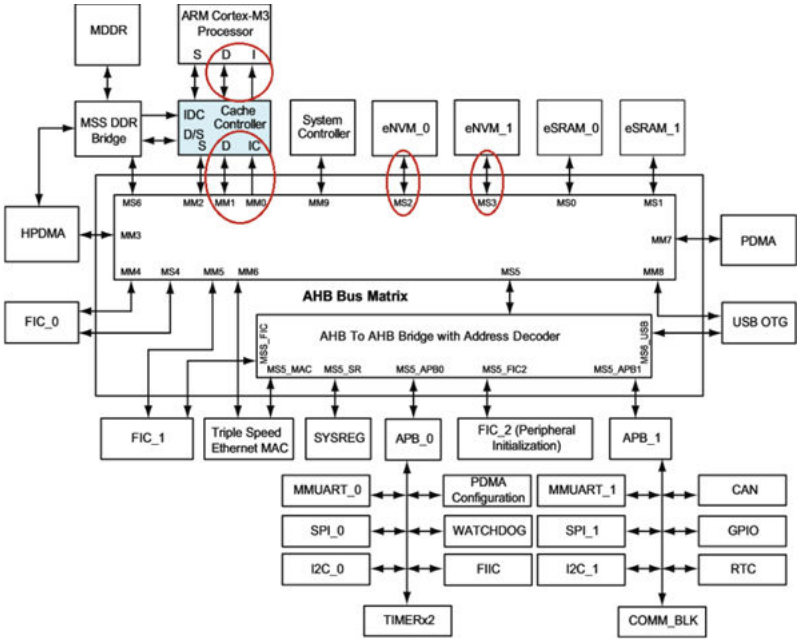
Cortext-M3 internal general-purpose registers (for example R6) gets corrupted when two nested D-Bus (must be a non-64-bit-aligned access) and I-Bus cache miss cycles occur in cache controller fetching from eNVM followed immediately by a D-Bus read without cache miss.

Figure 2-1. Cortex-M3 Core Register Set



SmartFusion2 system implements a cache controller in between Cortex-M3 and the memory subsystems (eNVM, eSRAM, Fabric sRAM, and DDR). An AHB matrix is used to arbitrate between eNVM, eSRAM, and Fabric sRAM access while a separate dedicated bus interfaces with DDR.

Figure 2-2. Cache Controller Interfaces and Paths Affected by CN (Red Circles)



SmartFusion2 Cache Controller allows mapping these memories, that is eNVM, on cacheable code regions. All M2S devices, apart from M2S050 (see Microchip SmartFusion2 Microcontroller Subsystem User Guide (UG0331)), come with a Cortex-M3 configuration that explicitly avoids simultaneous I-Bus and D-Bus address phases to ease arbitration of cache resource.

When the cache controller is enabled and mapped to eNVM, the following sequence of operations causes I-Bus and D-Bus accesses to be queued internally, leading to a state analogous to an I-Bus and D-Bus concurrent access.

1. A D-Bus miss has occurred to a non-aligned 64-bit address causing the cache controller to fetch the data from eNVM. This misaligned transaction extends the memory bus cycle.
2. While the cache logic is completing the cache fill operation after fetching from eNVM, an I-Bus miss occurs. The I-Bus operation is put on hold while waiting for cache filling operation to complete.
3. While I-Bus operation is in a wait state, a D-Bus read without a cache miss occurs. For this event to occur the D-Bus read must be within three cycles (the number of Cortex-M3 pipeline stages) to the I-Bus read/miss, a situation that mimics a simultaneous I-Bus and D-Bus read access.

A D-Bus read takes the precedence over an I-Bus but the data loaded into the Cortex-M3 internal register (for example, R6) is erroneously the I-Bus data which causes the corruption and consequently the application fails in an unpredictable manner.

Impact

The occurrence of this scenario described is rare. Moreover, the applications that meet any one of the four conditions listed are **not** impacted:

- The application executable has been 100% functionally tested across all supported operating conditions on every production unit and no such failures are observed.
- The cache controller is disabled in the design MSS configuration.
- The application is executed in any memory space other than eNVM.
- D-Bus literal loads are disabled during the compile of the code.

However, the corruption happens every time the specific cache miss/hit sequence occur regardless of the operating conditions or clock frequency.

Workaround

1. Add one the following compiling options depending on the toolchain used. This option prevents a D-Bus read to happen after I-Bus read. The following is a list of most common compilers used.
   - Keil, `--no_integer_literal_pools` or similar options
   - IAR, `--no_literal_pool`
   - GCC-ARM, `-mpure-code`
2. Recompile the code and update the executable code on the boot medium.

If using SoftConsole, you might need to update the project to the v5.1 or newer version, since the `-mpure-code` option is available only in recent gcc-arm toolchains.

2.18 PCIe Hot Reset Support Requires a Soft Reset Solution

On SmartFusion2 devices, a PCI Express hot reset requires a soft FPGA logic reset scheme, which clears the sticky bits of the PCI configuration space.

Workaround

The AC437: Implementing PCIe Reset Sequence in SmartFusion2 and IGLOO2 Devices application note describes the PCIe hot reset scheme. However, this reset scheme causes PCIe violations in some cases.

- For devices at Gen1 rates, there are no violations.
- For devices at Gen2 rates, there are two PCIe CV violations.
  - Test case 1: TD_1_7 (Advanced Error Reporting Capability)
  - Test case 2: TD_1_41 (LinkCap2Control2Status2 Reg)

2.19 After Successful Completion of CM3 ISP (without a SYSRESET), LSRAM Read and Write Access Fails From the Fabric Path

If LSRAM Read and Write access fails from the fabric path after performing CM3 ISP, perform a system reset or Flash*Freeze Entry/Exit.

Workaround

The user application must execute system reset as soon as the system service is completed. Otherwise, user write and read accesses to LSRAM/µRAM will not be possible. The system reset can be generated with the use of the tamper macro (availably in the Libero SoC Catalog). Immediately after the ISP service, the user logic checks the LSRAM/µRAM access. If access is denied, the user logic sends the reset request/interrupt to the system controller through the tamper macro (by enabling the RESET function in the tamper macro configuration window), and then the system controller executes the system-level reset.

For more information, see the UG0451: IGLOO2 and SmartFusion2 Programming User Guide.

The following application notes have more information and design examples on how to implement the workaround:

- DG0471: SmartFusion2 SoC FPGA - In-System Programming Using USB OTG Controller Interface - Libero SoC Demo Guide
- DG0454: SmartFusion2 SoC FPGA - In-System Programming Using UART Interface Demo - Libero SoC Demo Guide

2.20 Disable Cortex-M3 While Programming eNVM only

The user uses the Bitstream Configuration dialog box in the Libero SoC tool and generates an eNVM only stapl file. During programming, the system controller takes control of the eNVM. If the user

design has application code running from the eNVM, Cortex-M3 is halted because it cannot access eNVM. When the eNVM programming completes, the system controller releases eNVM. Cortex-M3 continues running from the same address it halted at, unless the device is restarted. If the device is not restarted, the Cortex-M3 behavior will be unpredictable as eNVM has the updated code.

Workaround

- Use the M3_Reset_N signal to hold Cortex-M3 in reset before programming eNVM
- Force a device restart
- Program eNVM and fabric

Libero v11.7 will fix the unpredictable behavior issue by forcing a restart of the device while programming eNVM only.

2.21 The DDR I/Os in M2S050 (T, TS)-FG896 are Non-compliant with the DDR3 Standard

The DDR I/Os in the M2S050-FG896 device are non-compliant with the DDR3 standard. Contact Microchip Global support for additional information.

2.22 For S (security) Grade Devices, User Must not Enable Write Protection for Protected 4K Regions

For S (security) devices, there are two or four 4 KB regions per eNVM array that can be protected for read and write. These regions are known as protected 4K regions or Special Sectors. If write protection is enabled for any of these regions, none of the locked pages inside the same eNVM block can be unlocked.

2.23 User eNVM Write is Incorrectly Allowed for the Protected 4K Regions

The eNVM protected 4K regions (0x6003FC80-0x6003FFFF) are reserved for use by the system controller to store information like the device certificate and digest information.

M2S050 Revision 0 and Revision 1 devices incorrectly allowed this eNVM area to be written. This was subsequently fixed in later versions of silicon devices to return an NVM_PAGE_LOCK_ERROR error on attempts to write this eNVM address range.

2.24 Avoid eNVM Page Lock and Unlock if Code is being Executed from eNVM both in Release and Debug Mode

Updating eNVM protected sectors requires a preliminary unlocking of the eNVM. In the time between unlocking and re-locking, no reads from eNVM are allowed.

Workaround

If the linker script places M3 code into eNVM, where it will execute-in-place, then the user should avoid eNVM page lock and unlock API's in both release mode and debug mode.

2.25 PCIe Hard IP Core Receive FIFO may Reach the Full Condition Resulting in Incorrect Data Passed to PCIe Subsystem and Cause the PCIe Core to Ignore the Subsequent PCIe Traffic

A condition has been identified with the SmartFusion 2 PCIe interface where the receive FIFO of the PCIe hard IP blocks may reach the full condition. This results in incorrect data passed to PCIe subsystem and cause the PCIe core to ignore the subsequent PCIe traffic. This only occurs under very specific conditions as outlined in the associated PCN SYST-18UJME493.

Workaround

This failure mechanism is isolated to the PCIe hard IP core within the FPGA device where it cannot be corrected. To avoid the issue, the posted receive buffer must not become full. This can be accomplished using one of the options in PCN SYST-18UJME493. For details, see

the following PCN attachment: https://ww1.microchip.com/downloads/aemDocuments/documents/FPGA/can/SF2_IGL2_RTG4_PCIe_Receive_FIFO_Full_CN.pdf

3. Usage Guidelines for SmartFusion2 Devices

Microchip recommends the following conditions for the SmartFusion2 device usage.

3.1 Programming Support

The following table lists the programming support details for the respective revisions of the devices.

Note: There may be package dependencies that may not expose certain programming interfaces. For more information on device/package specific features, see the DS0115: SmartFusion2 Pin Descriptions Datasheet.

Table 3-1. Revision 0 and Revision 1 Devices

Programming Mode	JTAG	SPI Slave	Auto Programming	Auto Update	2 Step IAP	Programming Recovery	M3 ISP
Programming Interface	JTAG	SC_SPI	SC_SPI	SPI_0	SC_SPI	SPI_0	N/A
M2S050 (T, TS)	Yes	Yes	No	No	No	No	Yes

Table 3-2. Revision 2 Device

Programming Mode	JTAG	SPI Slave	Auto Programming	Auto Update	2 Step IAP	Programming Recovery	M3 ISP
Programming Interface	JTAG	SC_SPI	SC_SPI	SPI_0	SC_SPI	SPI_0	N/A
M2S050 (T, TS)	Yes	Yes	Yes	No	Yes	No	Yes

3.2 SHA-256 System Service

Microchip recommends the message required to be on byte boundary when using SHA-256 System Service for the SmartFusion2 devices.

3.3 MSS Reset Mode

To keep the MSS in reset during normal operation, it is necessary to wait for the device to power-up, and then apply the reset. The US_POR_B signal from the MSS (the power-on-reset for the FPGA fabric) can be used to check the device's powered up state.

3.4 Accessing the PCIe Bridge Register in the High-Speed Serial Interface

The PCIe Bridge registers must not be accessed before the PHY is ready. Wait for the PHY_READY signal (which indicates when PHY is ready) to be asserted before updating the PCIe Bridge registers. The PHY_READY signal is normally asserted within 200 µs after the device is powered-up, so wait for 200 µs before accessing the PCIe Bridge registers.

4. Revision History

Revision	Date	Description
D	09/2024	The document was updated with the following change: • Added PCIe Hard IP Core Receive FIFO may Reach the Full Condition Resulting in Incorrect Data Passed to PCIe Subsystem and Cause the PCIe Core to Ignore the Subsequent PCIe Traffic
C	05/2024	The document was updated with the following change: • Updated the document to clarify that the document supports commercial/industrial/military temperature grade devices. Previously, the support was for the commercial and industrial grade devices.
B	04/2023	The document was updated with the following changes: • Added Avoid eNVM Page Lock and Unlock if Code is being Executed from eNVM both in Release and Debug Mode
A	10/2021	The document was updated with the following changes • Converted the document to Microchip standards • Added Arm® Cortex®-M3 Register Corruption Under Very Specific Literal Loads from eNVM and Cache Miss/Hit Sequences
1.6	—	Updated Errata "Concurrent Access of Arm® Cortex®-M3 I- and D-Bus is Not Allowed"
1.5	09/2016	Added Errata 23, User eNVM Write is Incorrectly Allowed for the Protected 4K Regions
1.4	04/2016	Added Errata 22, For S (security) Grade Devices, User Must not Enable Write Protection for Protected 4K Regions
1.3	01/2016	Table 3-1 and Table 3-2: Auto Programming and 2 Step IAP use SC_SPI programming interface are updated in revision 1.3 of this document.
1.2	01/2016	The following items were added: • Information about Revision 2 of the M2S050 device • Errata item 20, Disable Cortex-M3 While Programming eNVM only and errata item 21, The DDR I/Os in M2S050 (T, TS)-FG896 are Non-compliant with the DDR3 Standard are added • Table 3-2
1.1	05/2015	Updated to remove IAP from item 19, After Successful Completion of CM3 ISP (without a SYSRESET), LSRAM Read and Write Access Fails From the Fabric Path
1.0	05/2015	Revision 1.0 was the first publication of this document. All M2S050 (T, TS) device errata are combined in this revision.

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