MICROCHIP

AN3410

Design for PD System Surge Immunity PD701xx/PD702xx

Introduction

This document provides detailed design guidelines to sustaining high voltage or current surges per typical immunity requirements in PoE PD systems using Microchip controllers PD701xx and PD702xx, as well as active diode bridge PD70224.

The following table lists the Microchip PD interface family of devices.

Table 1. Microchip PD System Devices

Device Type	Power Capability	Integrates PWM
PD70100	IEEE 802.3at Type 1 (IEEE 802.3af)	No
PD70101	IEEE 802.3at Type 1 (IEEE 802.3af)	Yes
PD70200	IEEE 802.3at Type 2	No
PD70201	IEEE 802.3at Type 2	Yes
PD70210/A	IEEE 802.3at Type 2 (2/4 pair) HDBaseT (95 W)	No
PD70211	IEEE 802.3at Type 2 (2/4 pair) HDBaseT (95 W)	Yes
PD70224	IEEE802.3bt Type 4 (2/4 pair) HDBaseT (95 W)	N/A

Surge immunity is a basic feature required in telecommunication systems to increase system reliability when exposed to a surge event.

Surge protection is usually divided into the follwing two protection stages:

- Primary protection deals with high energy surges and is usually located between Equipment Under Test (EUT) and an external cable, subjected to the surge event. However, it can also be implemented at the EUT front end. It is used primarily for outdoor cable installations.
- Secondary protection deals with lower surge energies and is usually located within the EUT front end. It is used mainly for indoor cable installations.

The protection stages do not protect from direct lightning strike events. They protect from common surge events occurring near the telecommunication line. This application note enables the designer to implement a primary protection mechanism for protection from indoor or outdoor surge events.

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1. Immunity Requirements

Various agencies around the world define different surge voltage levels, source impedance, and maximum surge current. This application note provides information on IEC/EN 61000-4-5 (2014 Ed.3), ITU-T K21 (2019 Ed.), and GR-1089, which are the most common surge immunity standards in PoE PD systems.

The IEC 61000-4-5 (Par. 6.3.3.3) states that due to the nature of unshielded wiring, coupling to symmetrical interconnection lines (twisted pairs) is always in common mode, that is, between all lines to ground. However, ITU-T K.21 and GR-1089 specify for unshielded PoE lines a differential mode surge as well. Currently, IEEE 802.3 does not define the PoE surge requirements, so it is up to you to choose the standard that is the best fit for your application.

For indoor applications, IEC 61000 4-5 specifies 1.2/50 µs–8/20 µs common mode surge waveform with voltage level 0.5 kV to 2.0 kV, depending on installation class. However, few may choose meeting higher levels of protection, such as 4 kV, which are suitable for outdoors.

Common mode surge protection requires voltage limiting components that bridge the insulation between PoE domain and earth ground. The IEC/UL 60950-1 (Par.5.2.2) states that these limiters should be disconnected for insulation testing. Apart from this clause, subclause 6.1.2.1 of these standards specifies minimum rated operated voltage of these limiters as a function of AC mains supply in the area where the equipment is installed, unless the equipment qualifies for 6.1.2.2 exclusions. For a worldwide application, this requires minimum operation voltage of the surge protectors over their expected life to be at least 360 V. Similarly, ITU-T now requires 500 V_{DC} insulation test without removing any voltage limiters to verify the insulation is still good after the surge tests. For these reasons, voltage limiting devices rated 500 V_{DC} or above are used in our common mode surge tests. A 100 m CAT5 cable is used as a decoupling network.

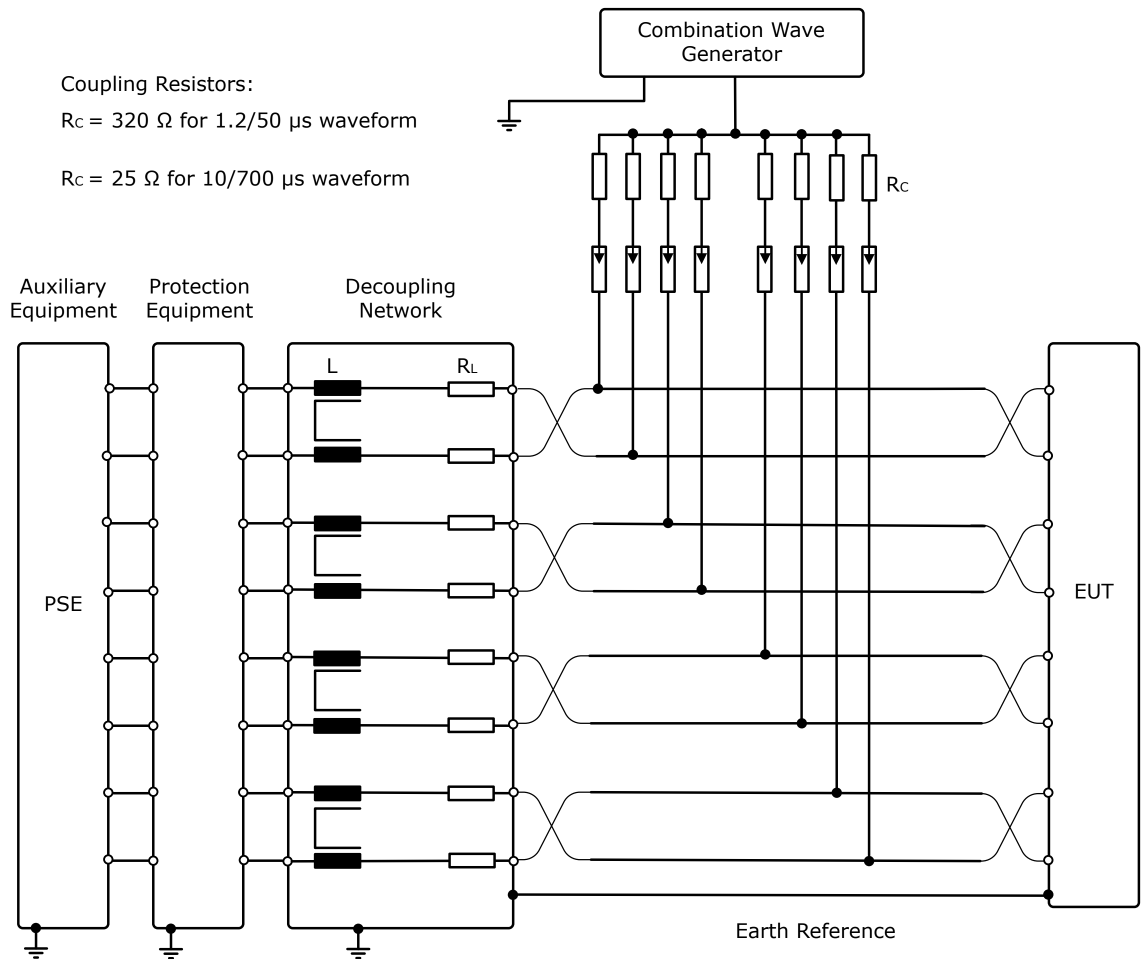
The following table provides a summary of the analyzed test requirements, which are typical for indoor and outdoor applications.

Table 1-1. Typical Surge Requirements for PoE

Number	Standard and Application	Wave Shape	Level	Criteria	Type	Setup
1	EN 61000 4-5 (indoors)	1.2/50 µs– 8/20 µs	±4 kV	A	All lines to earth	2 Ω internal plus 320 Ω + 90 V gas arrestor per line, port On and port Off. For more information, see Figure 1-1.
2	EN 61000 4-5 (indoors > 300 m)	10/700 µs	±4 kV	A	All lines to earth	15 Ω internal plus 25 Ω + 90 V gas arrestor per line, port On and port Off. For more information, see Figure 1-1.
3	ITU-T K21	1.2/50 µs–8/20 µs	±2.5 kV (basic test) ±4 kV (intermediate) ±6 kV (enhanced)	A	Line to line	2 Ω internal plus 10 Ω, port On and port Off. For more information, see Figure 1-2.
4	EN 61000 4-5 (shielded cable)	1.2/50 µs–8/20 µs	±4 kV	A	Chassis to earth	2 Ω internal plus 18 µF, port On and port Off. For more information, see Figure 1-3.
5	GR-1089	1.2/50 µs–8/20 µs	±800 V	A	Line to line	2 Ω internal plus 6 Ω, port On and port Off. For more information, see Figure 1-2.

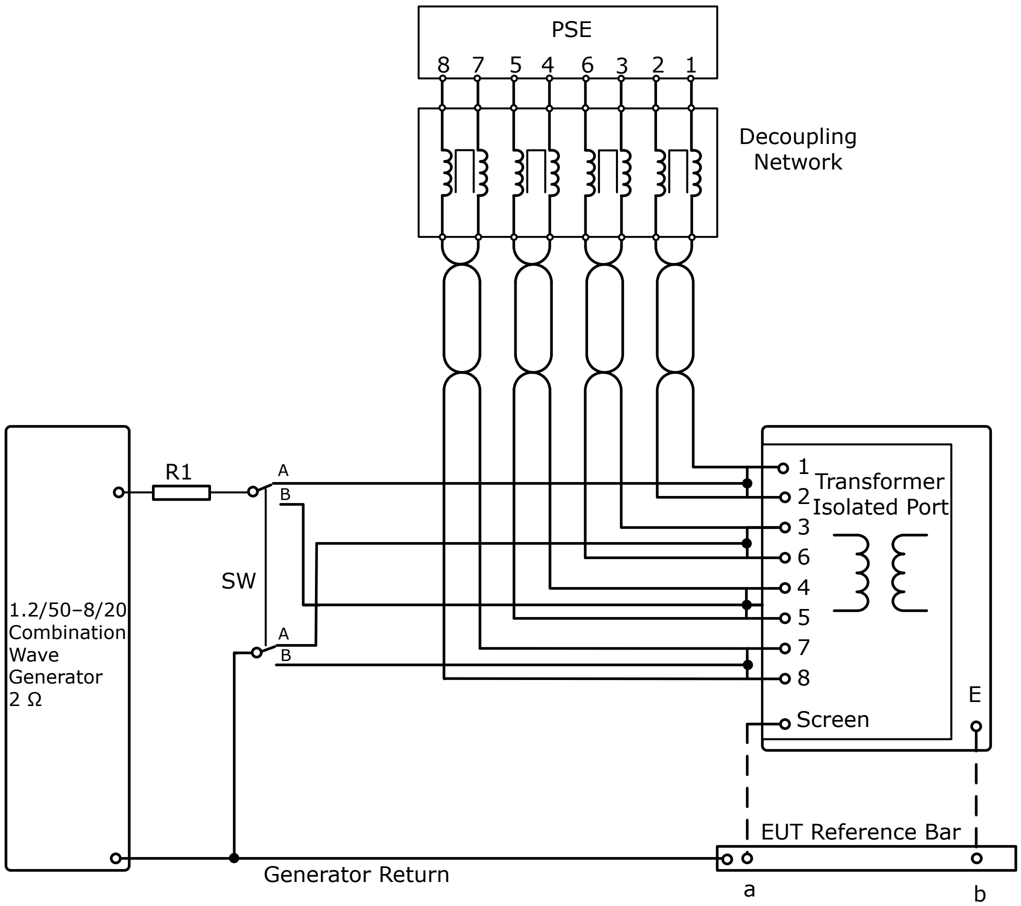
The following figures show the test setups for common mode and differential mode surges on PoE lines.

Figure 1-1. Example of Test Setup for Common Mode Surge in PoE PD Port



For 1.2/50 µs test, the effective internal impedance of the combination generator in the following figure is 2 Ω plus external resistors Rc = 40 Ω × n per line, where n = number of lines. For 4-pair cable, (n = 8) Rc = 320 Ω. For 10/700 µs tests, Rc = 25 Ω. Coupling resistors are connected in series with 90 V gas tube discharges Bourns p/n: 2027-09-BLF to allow PoE operation with connected generator.

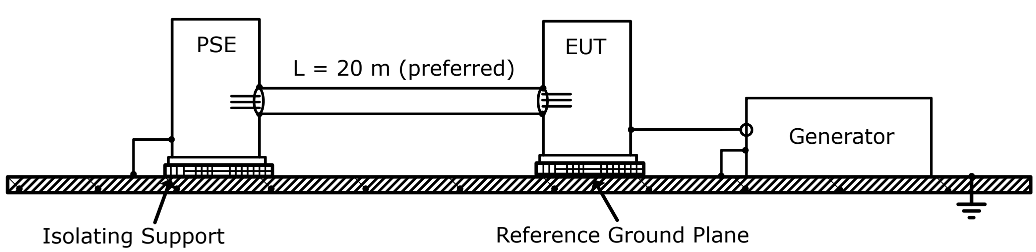
Figure 1-2. Example of Test Setup for Transverse/Differential Mode Surge on PoE PD Port



Here, R1 =10 Ω for ITU K21, R1 = 6 Ω for GR-1089.

The following figure shows an example of test setup for surges applied to shielded lines.

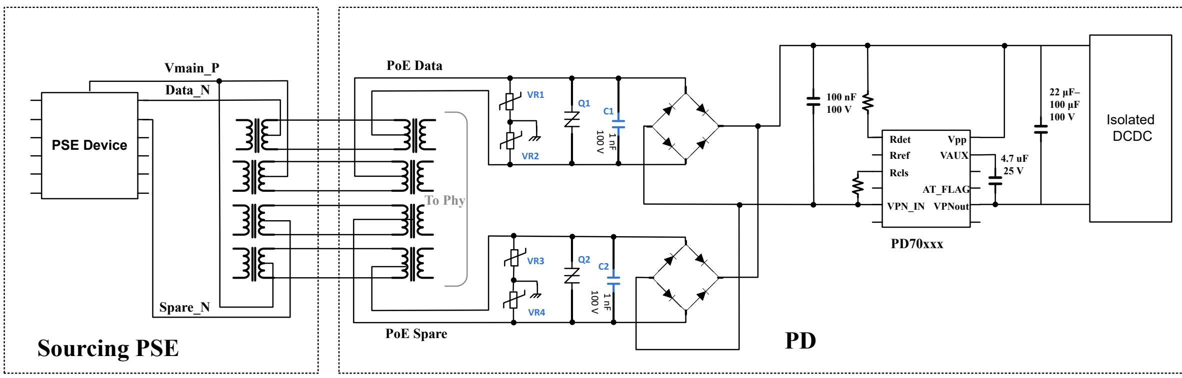
Figure 1-3. Example of Test Setup for Surges Applied to Shielded Lines



2. Surge Protection Circuit Design

The following figure shows the circuit that allows immunity for the test levels, as listed in the Microchip PD System Devices table (up to 4 kV common mode and up to 6 kV differential mode surges), tested with net amount of common mode capacitors up to 10 nF.

Figure 2-1. Surge Protection Circuit



The following table lists the parts that can be replaced by equivalent.

Table 2-1. Surge Protection Components per Port

Quality	Reference	Description	Size	Manufacturer	Part Number
4	VR1-VR4	Varistor 385 V_{AC}/505 V_{DC}, 27J 1200 A peak pulse current	11.4 mm × 8.3 mm x 6 mm (2-SMD)	Littelfuse	V385SM7
2	Q1, Q2	SIDACtor thyristor 800 A 8/20 µs (bi-directional)	DO-214	Littelfuse	P0640SDLRP
2	C1, C2	1 nF 100 V X7R	0603	Samsung	CL10B102KC8NNC

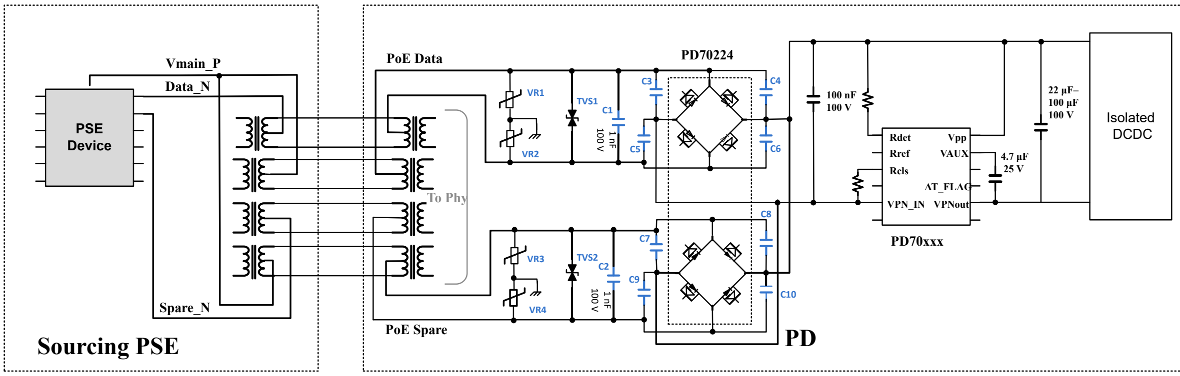
Note:

1. Transient voltage suppressors (TVS) p/n 8.0SMDJ58CA made by Littelfuse can be used instead of SIDACtors for Q1 and Q2 in the preceeding figure.
2. Surges can cause voltage transients in the DC-DC converter output. For sensitive circuits, additional TVS may need to be installed across the output bus.

2.1 Surge Protection Circuit for Use with PD70224 Ideal Bridge

The following figure shows the circuit that allows immunity for up to 4 kV 1.2/50 µs–8/20 µs common mode surge per IEC 61000 4-5, tested with the net amount of common mode capacitors up to 10 nF.

Figure 2-2. Surge Protection Circuit for PD70224



The following table lists the surge protection components and their description for PD70224 per port.

Table 2-2. Surge Protection Components for PD70224 per Port

Quantity	Reference	Description	Size	Manufacturer	Part Number
4	VR1-VR4	Varistor 385 V_{AC}/505 V_{DC}, 27 J 1200 A peak pulse current	144 mm disc	Epcos	B72214S2421K101
2	TVS1-TVS2	TVS Diode 58 VWM 5000 W (bi-directional)	SMD	Littelfuse	5.0SMDJ58CA
2	C1, C2	1 nF 100 V X7R	0603	Samsung	CL10B102KC8NNNC
8	C3-C10	10 nF 100 V X7R	0603	TDK	C1608X7R2A103K080AA

2.2 Avoid Additional Earth Ground Return Passes for Surge Current

Common mode TVS's divert surge currents to the earth ground and prevents them from flowing through the PD circuit. It is important to minimize additional low-impedance passes for the surge current downstream the rectifier bridge. Such additional pass can be created by common mode capacitors in EMI filter or by a wall adapter, with an internal output common mode capacitor or surge suppressor. When such adapter is connected after PD chip, a part of surge current flows to the adapter output through the PD chip's internal FET and can cause its damage.

Another example of unwanted additional ground return pass is a non-isolated PD-PSE system, in which PD front-end feeds PSE through a boost converter. In such a system, when a surge voltage is injected on either the PD or PSE connector, a portion of the surge current flows through common analog return of PD and PSE, and may damage the circuit. If PD system is intended to power a PSE, there should be an isolation between the two. Such isolation is provided by using an isolated flyback converter instead of boost. The compliance of the protection circuits in the Surge Protection Circuit figure and the Surge Protection Circuit for PD70224 figure was tested with net amount of all common mode capacitors up to 10 nF, and without auxiliary power sources.

2.3 Layout Considerations

Care should be taken on PCB layout with respect to surge immunity.

- Keep chassis traces close to RJ45 or ground screws (if any), and do not penetrate the PoE environment.
- Keep minimum of 80 mil creepage between chassis and PoE circuitry.
- Keep surge protection components as close as possible to RJ45 or chassis connection to minimize the high current loops.
- Make connections of surge protectors by short heavy traces capable of withstanding surge currents.
- Do not use these traces for connecting other components.

3. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
B	03/2020	Confidential footer added.
A	02/2020	• Updated the application note as per Microchip standards. • Updated the Microchip PD System Devices table in Introduction section. • Edited the Avoid Additional Earth Ground Return Passes for Surge Current section. • Updated the Surge Protection Circuit and the Surge Protection Circuit for PD70224 figures. • Changed AN223 to AN3410.
3.0	01/2020	• Updated the Typical Surge Requirements for PoE table in the Immunity Requirements section. • Updated the Surge Protection Circuit figure in the Surge Protection Circuit Design section. • Updated the Surge Protection Components per Port table in the Surge Protection Circuit Design section.
2.0	06/2018	• The format of this document was updated to the latest template. • Updated the Immunity Requirements and the Surge Protection Circuit Design sections in this publication.
1.21	07/2017	• Fixed typo in TVS p/n in the Surge Protection Components per Port table in the Surge Protection Circuit Design section.
1.2	07/2017	• Protection circuit for PD70224 and components list were added. • Updated the Surge Protection Components per Port table table and the Example of Test Setup for Common Mode Surge in PoE PD Port figure in the Immunity Requirements section, with note per IEC/EN 61000-4-5 Ed.3.
1.1	02/2017	Clarified test conditions and added test setup for shielded cables.
1.0	09/2016	This is the initial released version of this application note.

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