KSZ989x/KSZ956x/KSZ9477

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the KSZ 6 and 7 Port Gigabit Ethernet family switches, including the KSZ9896, KSZ9897R, KSZ9897S, KSZ9567R, KSZ9567S, and KSZ9477. In this hardware design checklist, KSZ989x/KSZ956x/KSZ9477 represents a whole family of switches. These checklist items should be followed when utilizing the KSZ989x/KSZ956x/KSZ9477 switch family in a new board design.

A summary of the hardware design checklist items is provided in Section 15.0, "Hardware Checklist Summary," on page 31. Detailed information for each checklist item can be found in the following sections:

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The KSZ989x/KSZ956x/KSZ9477 implementor should have the following documents on hand:

- *KSZ9897R, KSZ9897S, KSZ9567R, KSZ9567S, KSZ9477,* and *KSZ9896 Data Sheets*
- *KSZ9897R, KSZ9897S, KSZ9567R, KSZ9567S, KSZ9477,* and *KSZ9896 Silicon Errata and Data Sheet Clarification*
- *KSZ9897R, KSZ9897S, KSZ9567R, KSZ9567S, KSZ9477,* and *KSZ9896* IBIS Model
- EVB-KSZ9897 Board Schematic and PCB Layout
- EVB-KSZ9477 Board Schematic and PCB Layout
- *EVB-KSZ9897 Evaluation Board User's Guide*
- *EVB-KSZ9477 Evaluation Board User's Guide*
- *AN2647 Interfacing the SGMII Port on KSZ9xx7S and KSZ8567S Switches Application Note*

2.2 Pin Check

- Check to ensure that the package orientation and pin numbering with respect to the top view of the package are in the counterclockwise direction. Refer to the KSZ989x/KSZ956x/KSZ9477 family switch data sheets for additional information.
- Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking. It is important to always check the pin types in the data sheet of the connecting pins between two devices to ensure that the connected pins are not both inputs and not both outputs. Do not rely on just the pin name of the bus interface between two connecting devices. The same pin name may be defined as an input or an output, depending on the interface perspective. This is especially true for the **RGMII**, **RMII**, and **MII** pins, whose names may be counter intuitive.

- The KSZ989x/KSZ956x/KSZ9477 family of switches utilize configuration strap pins to configure the device for different modes. These strap pins are configured by using internal and external pull-up/pull-down resistors to create a high or low state on the pins that are sampled at the end of a device power-up or software Reset cycle. They are also latched when powering up from a hardware or software power-down or hardware Reset state (rising edge of **RESET_N**).
- Remember that the internal pull-up/pull-down resistor may not be sufficient to set the desired logic level during Reset. For example, the device connected to the RGMII/RMII/MII interface may also have internal pull-up or pull-down resistors on its inputs, and they may overpower the relatively weak internal resistors of the KSZ989x/KSZ956x/KSZ9477 and consequently cause the multiplexed strap-in pins on the RGMII/RMII/MII signals to be latched at the wrong level. When in doubt, use external resistors to establish the desired logic levels.
- When strapping an **LED** pin low, the effect of the **LED** must be considered. See Section 10.0, "LED Indicator Pins". The configuration strap pins and their associated functions are detailed in Table 2-1.

TABLE 2-1: CONFIGURATION STRAP DESCRIPTIONS

Configuration Strap Pin	Description
LED1_1	**Flow Control (All Ports)** 0 = Flow control disabled 1 = Flow control enabled (Default)
LED2_1	**Link-up Mode (All PHYs)** 0 = Fast Link-up: Auto-negotiation and auto MDI/MDI-X are disabled. 1 = Normal Link-up: Auto-negotiation and auto MDI/MDI-X are enabled (Default). See **Note 1**.
LED4_0, LED2_0	**When LED2_1 = 1 at strap-in (Normal Link-up):** **[LED4_0, LED2_0]: Auto-Negotiation Enable (All PHYs)/NAND Tree Test Mode** 00 = Reserved 01 = Auto-negotiation disabled, forced as 100 Mbps and half duplex. Auto-MDI-X is on. 10 = NAND Tree Test mode 11 = Auto-negotiation enabled (Default) **When LED2_1 = 0 at strap-in (Fast Link-up; All PHYs Full-Duplex; Auto-negotiation and Auto-MDI-X are off):** **LED2_0: 1000BASE-T Host/Client mode, 10/100BASE-T MDI/MDI-X mode (All PHYs)** 0 = 1000BASE-T: Client mode 10/100BASE-T: MDI-X 1 = 1000BASE-T: Host mode (Default) 10/100BASE-T: MDI (Default) **LED4_0: PHY Speed Select (All PHYs)** 0 = 1000BASE-T 1 = 100BASE-TX (Default)
LED4_1, LED3_1	**[LED4_1, LED3_1]: Management Interface Mode** 00 = MIIM (MDIO) 01 = I^2C 1x = SPI (Default)

Note 1: Since Fast Link-up disables auto-negotiation and auto-crossover, it is suitable only for specialized applications.

2: If Port 6 is configured for MII or RMII, set the speed to 100 Mbps.

3: If Port 7 is configured for MII or RMII, set the speed to 100 Mbps.

TABLE 2-1: CONFIGURATION STRAP DESCRIPTIONS

Configuration Strap Pin	Description
LED5_1	**Switch Enable at Startup** 0 = Start Switch is disabled. The switch will not forward packets until the Start Switch bit is set in the Switch Operation Register. 1 = Start Switch is enabled. The switch will forward packets immediately after Reset. (Default)
RXD6_3, RXD6_2	**[RXD6_3, RXD6_2]: Port 6 Mode** 00 = RGMII (Default) 01 = RMII 10 = GMII/MII (for KSZ9896 only) 11 = MII
RXD6_1	**Port 6 MII/RMII Mode** 0 = MII: PHY mode (Default) RMII: Clock mode. RMII 50MHz reference clock is output on **REFCLKO6**. (Default) GMII: PHY mode (for KSZ9896 only) RGMII: No effect 1 = MII: MAC mode RMII: Normal mode. RMII 50MHz reference clock is input on **REFCLKI6**. GMII: MAC mode (for KSZ9896 only) RGMII: No effect
RXD6_0	**Port 6 Speed Select** 0 = 1000 Mbps mode (Default) 1 = 100 Mbps mode See **Note 2**.
RXD7_3, RXD7_2 (not applicable to KSZ9567S, KSZ9477, KSZ9896, and KSZ9897S)	**[RXD7_3, RXD7_2]: Port 7 Mode** 00 = RGMII (Default) 01 = RMII 10 = Reserved 11 = MII
RXD7_1 (not applicable to KSZ9567S, KSZ9477, KSZ9896, and KSZ9897S)	**Port 7 MII/RMII Mode** 0 = MII: PHY mode (Default) RMII: Clock mode. RMII 50 MHz reference clock is output on **REFCLKO7**. (Default) RGMII: No effect 1 = MII: MAC mode RMII: Normal mode. RMII 50 MHz reference clock is input on **REFCLKI7**. RGMII: No effect
RXD7_0 (not applicable to KSZ9567S, KSZ9477, KSZ9896, and KSZ9897S)	**Port 7 Speed Select** 0 = 1000 Mbps mode (Default) 1 = 100 Mbps mode See **Note 3**.

Note 1: Since Fast Link-up disables auto-negotiation and auto-crossover, it is suitable only for specialized applications.

2: If Port 6 is configured for MII or RMII, set the speed to 100 Mbps.

3: If Port 7 is configured for MII or RMII, set the speed to 100 Mbps.

TABLE 2-1: CONFIGURATION STRAP DESCRIPTIONS

Configuration Strap Pin	Description
RX_DV7/CRS_DV7/ RX_CTL7 for KSZ9897R and KSZ9567R or IBA for KSZ9567S, KSZ9477, and KSZ9897S or RX_DV6/CRS_DV6/ RX_CTL6 for KSZ9896 only	**In-Band Management** 0 = Disable In-Band Management (Default) 1 = Enable In-Band Management
RX_ER6/RX_CLK6 for KSZ9896 only	**GMII/MII Clock Mode** 0 = 2-Wire Clock mode (Default) 1 = 3-Wire Clock mode These modes affect the GMII and MII clocks for outgoing data on the Port 6 RX signals. The strapped value is readable on bit 0 of the Port 6 XMII Port Control 0 Register and may be overwritten. In 2-Wire mode, pin 72 (RX_CLK6/REFCLKO6) is used for either the GMII output clock or the MII clock. In 3-Wire mode, pin 72 (RX_CLK6/REFCLKO6) is used for the GMII output clock, and pin 75 (RX_ER6/RX_CLK6) is used for the MII input clock when in MAC mode. The 3-Wire mode is intended as an option, when in MAC mode, for connection to a 1000/100/10 Mbps PHY which has separate pins for the GMII (1000 Mbps) GTX_CLK clock and the MII (100/10 Mbps) TX_-CLK clock. When the MAC interface does not need to be switchable between GMII and MII, or when in PHY mode, do not select the 3-Wire mode.

Note 1: Since Fast Link-up disables auto-negotiation and auto-crossover, it is suitable only for specialized applications.

2: If Port 6 is configured for MII or RMII, set the speed to 100 Mbps.

3: If Port 7 is configured for MII or RMII, set the speed to 100 Mbps.

Note: Traditionally, the SPI communication protocol uses the terminologies, “master” and “slave.” The equivalent Microchip terminologies used in this document are “host” and “client.”

3.0 POWER/GROUND CONNECTIONS

3.1 Power and Ground Block Diagram

The power and ground connections for KSZ9897R, KSZ9567R, and KSZ9896 are shown in Figure 3-1. KSZ9567S, KSZ9477, and KSZ9897S have a SGMII/SERDES interface and it requires 2.5V (**VDDHS**) and 1.2V (**VDDLS**). The power and ground connections for those switches are shown in Figure 3-2.

FIGURE 3-1: POWER AND GROUND CONNECTIONS FOR KSZ9897R, KSZ9896, AND KSZ9567R

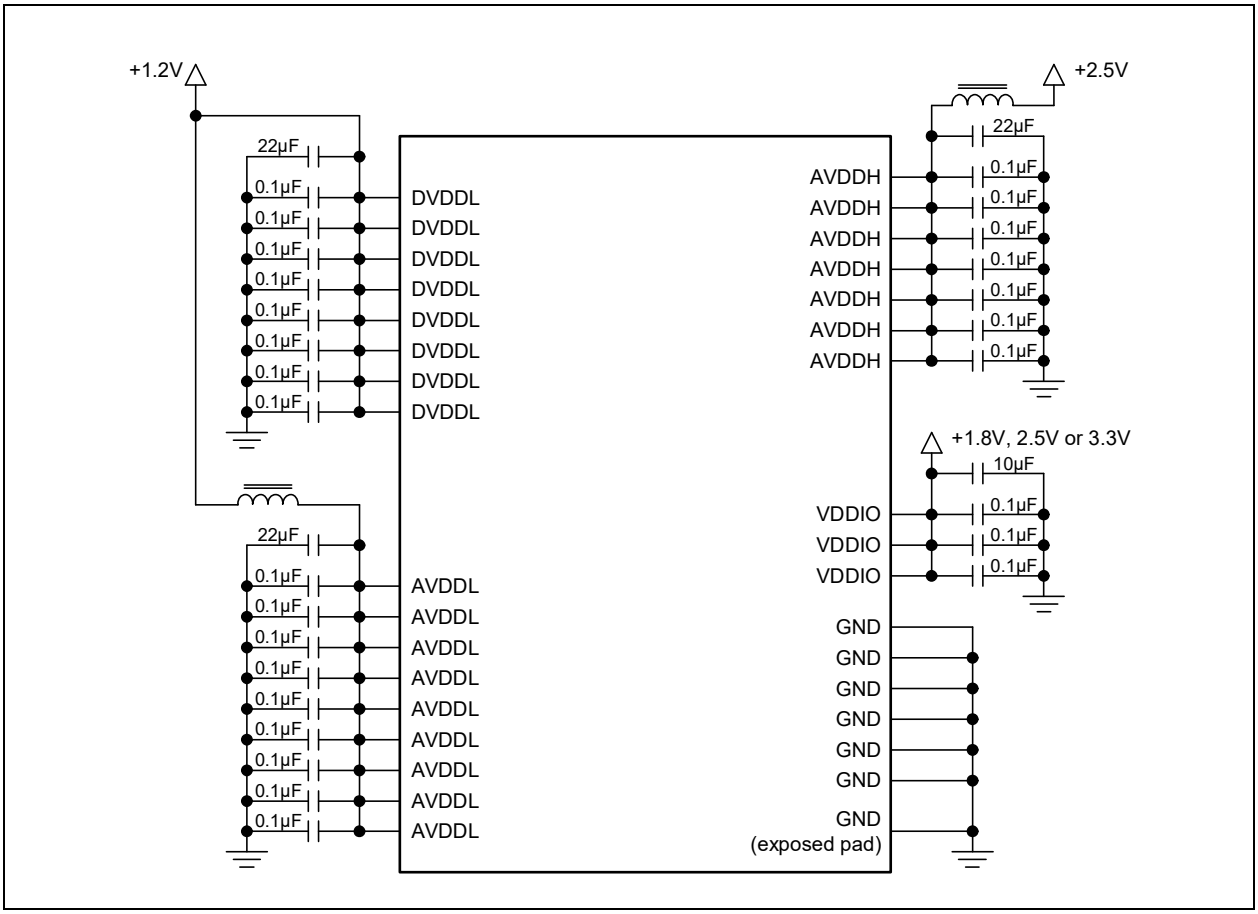
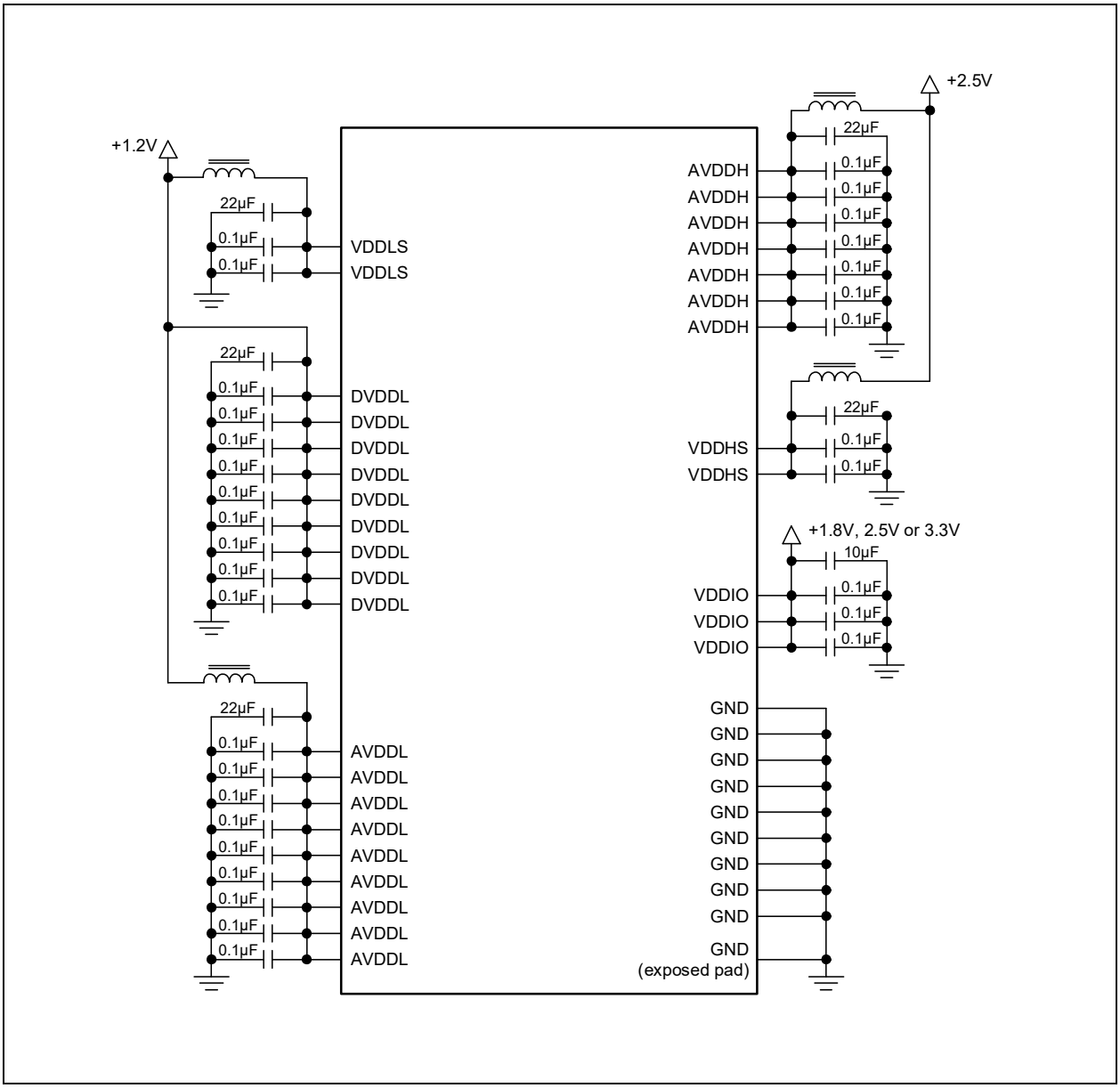


FIGURE 3-2: POWER AND GROUND CONNECTIONS FOR KSZ9567S, KSZ9477, AND KSZ9897S



3.2 Power Pins

The following notes for the power pins and their connections refer to Figure 3-1 and Figure 3-2.

- **VDDIO** powers the digital **I/O** pins and can operate at either +3.3V, +2.5V, or +1.8V.
- **AVDDH** powers the analog transceiver, can operate at +2.5V, and should have a series ferrite bead placed between board power supplies to provide further filtering.
- **DVDDL** powers the digital core and operates at +1.2V.
- **AVDDL** powers the analog core and operates at +1.2V. If a single 1.2V board supply is used, a series ferrite bead should be placed between the **AVDDL** power and the +1.2V supply to provide further filtering.
- **VDDLS** powers the SGMII/SERDES block (KSZ9567S, KSZ9477, and KSZ9897S) and operates at +1.2V. If a single 1.2V board supply is used, a series ferrite bead should be placed between **VDDLS** power and the +1.2V supply to provide further filtering.

- **VDDHS** powers the SGMII/SERDES block (KSZ9567S, KSZ9477, and KSZ9897S) and operates at +2.5V. If a single 2.5V board supply is used, a series ferrite bead should be placed between **VDDHS** power and the +2.5V supply to provide further filtering.
- Each power pin requires a 0.1 µF decoupling capacitor. These capacitors should be placed as close as possible to the power pins without using vias.
- The ferrite beads should have the following specifications: impedance 80Ω to 220Ω (at 100 MHz), R_{DC} ≤ 0.05Ω for 1.2V supply, and ≤ 0.1Ω for 3.3V supply.
  - 900 mA for **DVDDL** (if a ferrite bead is used for **DVDDL**)
  - 500 mA for **AVDDL**
  - 400 mA for **AVDDH**
- A bulk capacitor should be placed on each power rail near the device. These capacitors should have a typical capacitance value of 22 µF and an Equivalent Series Resistance (ESR) of no more than 1Ω. Microchip recommends a very low ESR ceramic capacitor for design stability.
- All four power rails (**VDDIO**, **AVDDH**, **DVDDL**, **AVDDL**, **VDDLS**, and **VDDHS**) should each have less than 50 mVp-p ripple.

3.3 Ground Pin and Exposed Pad

The following notes for the ground pin, the exposed pad ground, and their connections refer to Figure 3-1 or Figure 3-2.

- Exposed pad (E-pad) ground on the bottom side of the chip should connect directly to the solid ground plane on the board. See the device data sheet for the E-pad dimensions, recommended land pattern, and thermal via size and number requirements.
- All **GND** pins and the E-pad should tie directly together to the same common-ground plane.

3.3.1 POWER ON/OFF SEQUENCING

- It is recommended to bring up all voltages at the same time. If that cannot be attained, power up the transceiver (AVDDH) and digital I/Os (VDDIO) voltages before the low-voltage core (AVDDL and DVDDL). There is no power sequence requirement between transceiver (**AVDDH**) and digital I/Os (**VDDIO**) power rails. The power-up waveforms should be monotonic for all supply voltages. The preferred sequence for the SGMII/SERDES power is VDDLS before VDDHS.
- The recommended power-down sequence is to power down the low-voltage core before powering down the transceiver and digital I/O voltages or to have all supplies power down in unison.
- Before the next power-up cycle, all supply voltages to the device should reach less than 0.4V and there should be a minimum wait time of 150 ms from power-off to power-on.

4.0 REFERENCE CLOCK CIRCUITS AND CONNECTIONS

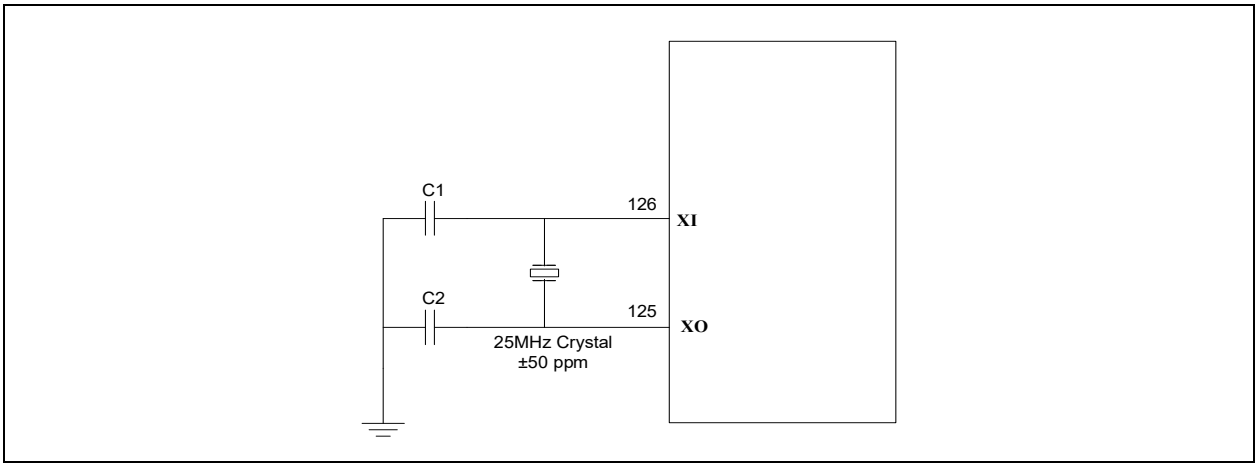
A 25 MHz reference clock is required for the device. Either a crystal or external clock source can be used to provide the clock.

4.1 Crystal Circuit

The following notes for the crystal circuit refer to Figure 4-1.

- Connect a 25 MHz (+/–50 ppm) crystal between **XI** (pin 126) and **XO** (pin 125). See the *KSZ989x/KSZ956x/KSZ9477 Family Switch Data Sheet* for crystal requirements.
- The crystal capacitor (C1 and C2) value should be calculated based on the C_L specification of the selected crystal and the stray capacitance of the PCB traces and **XI** and **XO** pins. Note that C1 and C2 ≠ C_L.
- The selected crystal and PCB design and layout contribute to the performance of the crystal circuit. Once the board is brought up and is operational, a check for frequency accuracy across the system operating conditions is recommended. Measure it on a clock output pin, not by probing **XI** or **XO**.

FIGURE 4-1: CRYSTAL CIRCUIT

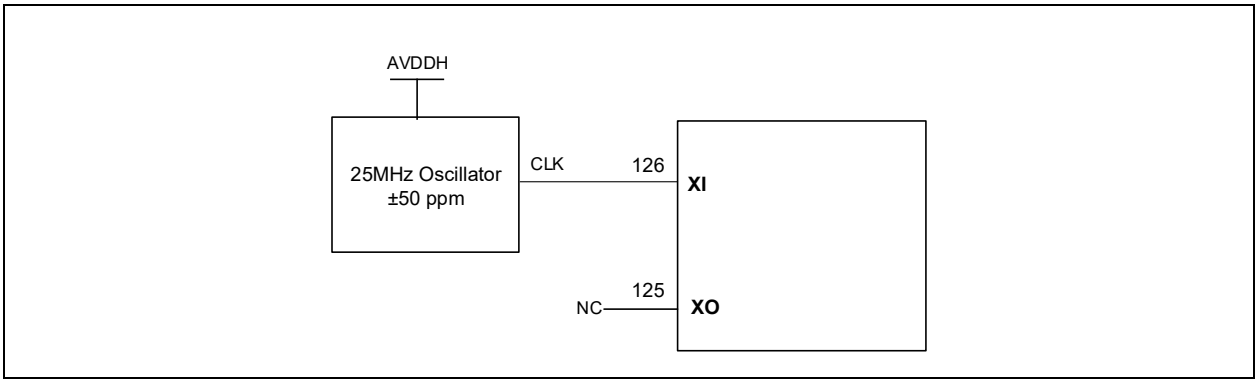


4.2 External Clock Source/Oscillator Circuit

The following notes for the external clock/oscillator circuit refer to Figure 4-2.

- **XI** (pin 126) is the input for the external clock source.
- **XO** (pin 125) is a no connect.
- Use a 25 MHz (±50 ppm) clock source, such as an oscillator, with a total period jitter (peak-to-peak) of less than 100 ps.
- A source series termination resistor is suggested at the clock output pin.
- The oscillator supply voltage should match the KSZ989x/KSZ956x/KSZ9477 AVDDH voltage. If it does not, then the clock should be AC coupled to the **XI** input by a 0.1 µF capacitor.

FIGURE 4-2: EXTERNAL CLOCK SOURCE/OSCILLATOR CIRCUIT



5.0 ISET RESISTOR

The **ISET** pin of the KSZ989x/KSZ956x/KSZ9477 should connect to signal ground through a single 6.04 kΩ 1% resistor.

- Place the resistor close to the **ISET** pin.
- Do not place any capacitor in parallel with the ISET resistor.
- Route all signals, especially clocks and high frequency signals, away from this pin to avoid coupling.
- Do not share the ISET resistor ground via with any other component's grounding via.

6.0 ETHERNET PHY PORTS

6.1 Unused PHY Ports

If a PHY port is unused, leave all eight pins unconnected.

6.2 Magnetics Selection

- 1:1 isolation transformers are required at the media interface. For designs exceeding FCC requirements, utilize one with integrated Common-mode chokes. An optional auto-transformer stage following the chokes provides additional Common-mode noise and signal attenuation.
- To support Auto MDI/MDI-X in designs with two-channel magnetics (supporting only 10/100 speeds), the two channels of the magnetics must be the same.

Table 6-1 provides a list of recommended magnetic characteristics.

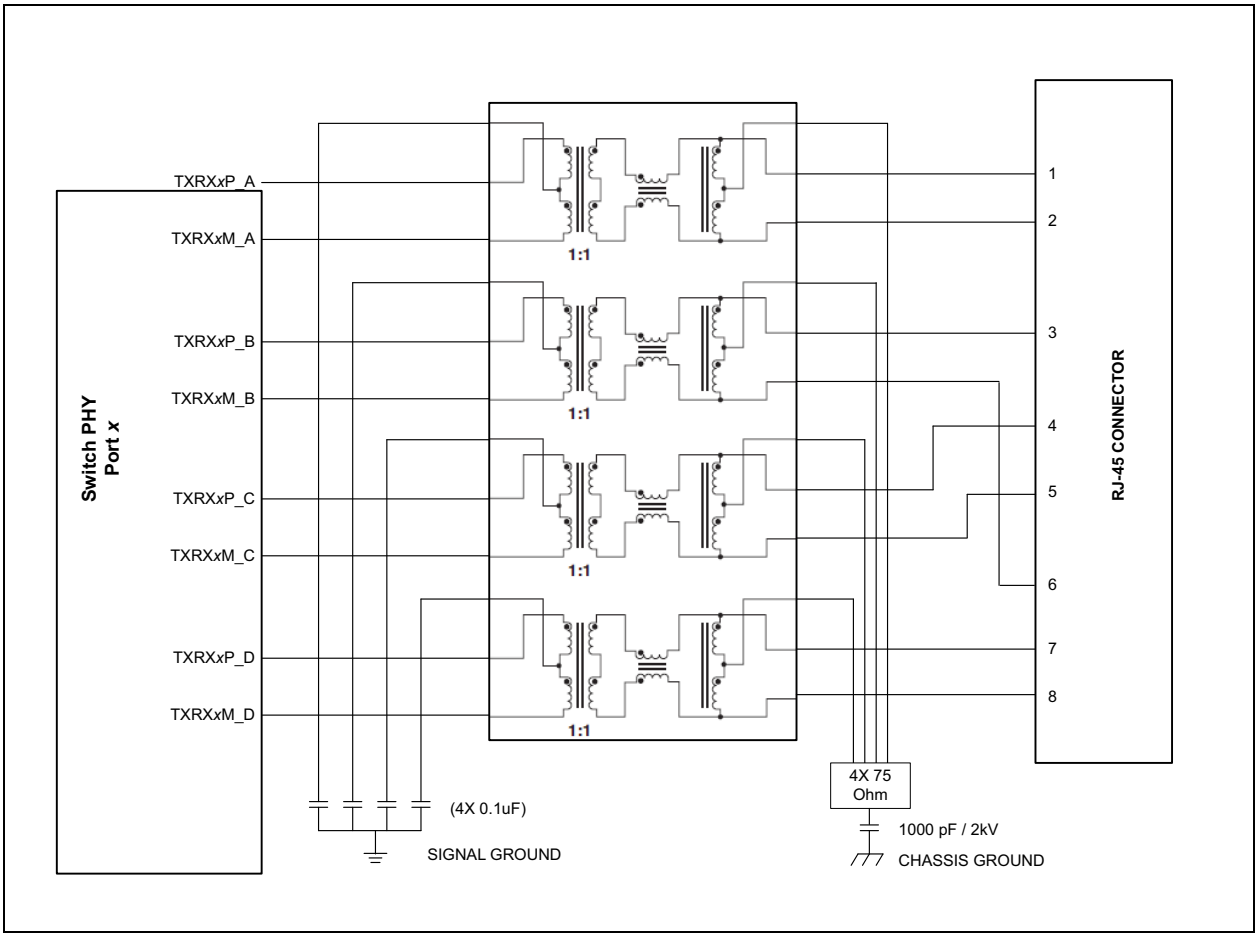
TABLE 6-1: MAGNETICS SELECTION CRITERIA

Parameter	Value	Test Condition
Turns ratio	1 CT:1 CT	—
Open-circuit inductance (minimum)	350 µH	100 mV, 100 kHz, 8 mA
Insertion loss (maximum)	1.0 dB	100 kHz to 100 MHz
HIPOT (minimum)	1500 Vrms	—

6.3 10/100/1000 Mbps (Gigabit) Ethernet Interface

The Ethernet signal connections between the KSZ989x/KSZ956x/KSZ9477 family switches, magnetics, and the RJ45 connector are shown in Figure 6-1 for Gigabit Ethernet support.

FIGURE 6-1: GIGABIT ETHERNET CONNECTIONS



This device has voltage mode drivers, which have different requirements from Current-mode drivers. Please adhere to the following points:

- All chip-side transformer center taps are independently connected to signal ground through 0.1 µF capacitors.
- Do not connect the center taps together. Many magnetics modules and integrated jacks tie the center taps together, so select the magnetics carefully. Performance may be degraded if they are tied together.
- Do not connect the center taps to a supply voltage.
- All line-side transformer center taps should be individually terminated to a common node through 75Ω resistors. The common node is then connected to chassis ground through a 1000 pF, 2 kV capacitor.
- The metal case shield of the RJ45 connector is also tied to chassis ground.

6.4 10/100 Mbps Ethernet Only

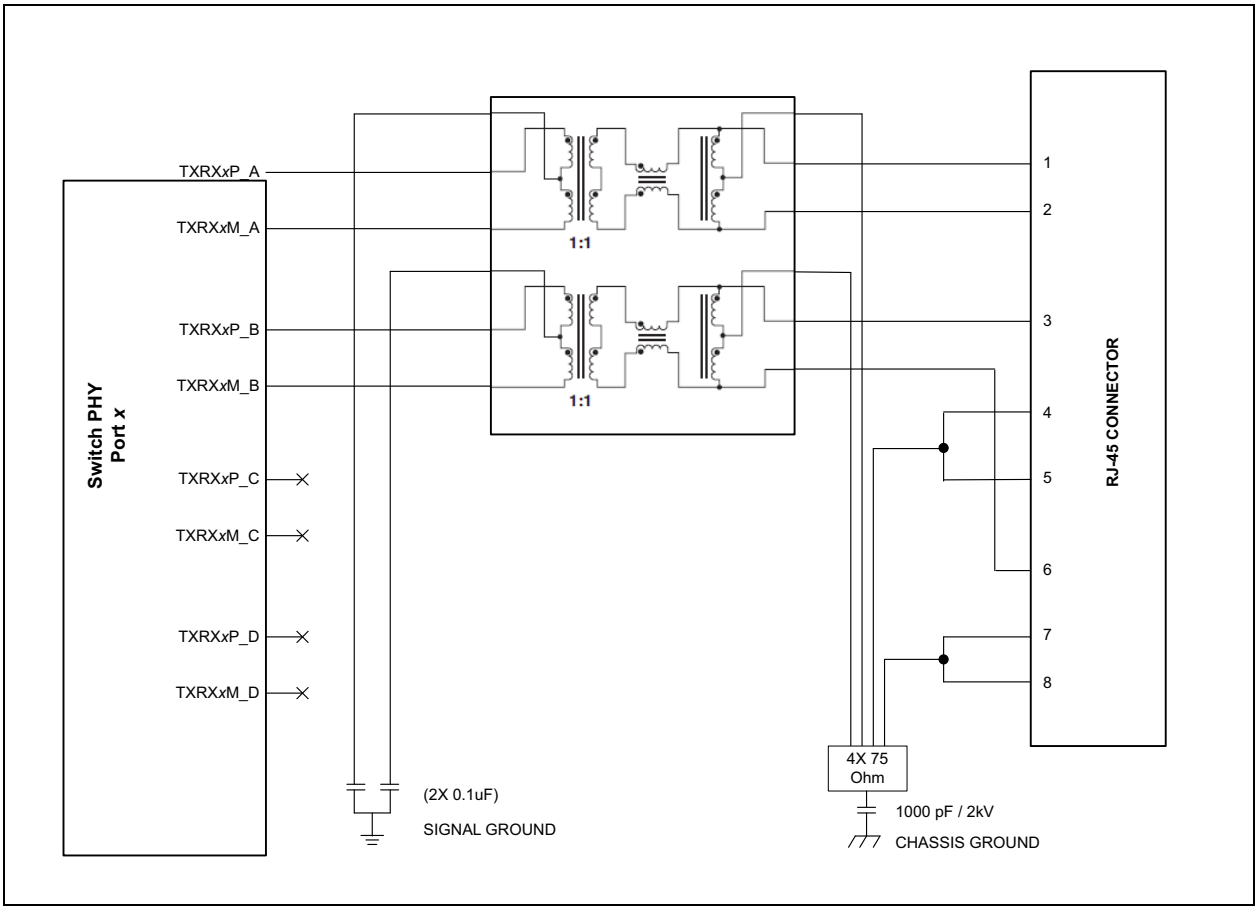
For applications that require a link-up limited to 10/100 Mbps speeds only, the auto-negotiation advertisement for 1000BASE-T capabilities should be disabled to avoid linkup failure when connecting to a link partner that is capable of 1000 Mbps. After power-up or Reset, program the following 16-bit Port N register bit settings, where N is 1 for Port 1, and 2 for Port 2, etc, with the following steps:

1. Set Port Register 0xN100, Bit [6] = '0' to remove 1000 Mbps speed.
2. Set Port Register 0xN112, Bits [9:8] = '00' to remove Auto-Negotiation advertisements for 1000 Mbps full-/half-duplex.
3. Write a '1' to Register 0xN100, Bit [9], a self-clearing bit, to force a restart of Auto-negotiation.

6.4.1 10/100 MBPS ETHERNET MAGNETICS AND CONNECTOR

The Ethernet signal connections between the KSZ989x/KSZ956x/KSZ9477, magnetics and RJ45 connector are shown in Figure 6-2 for a port supporting only 10 and 100 Mbps speeds.

FIGURE 6-2: FAST ETHERNET MAGNETIC CONNECTIONS (MDI MODE)



The magnetics configuration of a 10/100 Mbps port is similar to that of a gigabit Ethernet port.

- Differential pairs A and B are used, while pairs C and D are left unconnected.
- Both chip-side transformer center taps are independently connected to signal ground through 0.1 µF capacitors.
- Both line-side transformer center taps should be individually terminated to a common node through 75Ω resistors. The common node is then connected to chassis ground through a 1000 pF, 2 kV capacitor.
- The unused **RJ45** pins are shorted together as pin pairs (4, 5) and (7, 8) and terminated through separate 75Ω resistors to the same common node (in the previous bullet point).
- The metal case shield of the RJ45 connector is also tied directly to chassis ground.

The Ethernet signal mappings across the magnetics between the KSZ989x/KSZ956x/KSZ9477 device and the RJ45 connector are shown in Table 6-2. The first two columns are the same connections shown in Figure 6-2. The third column shows an alternate connector pin assignment.

TABLE 6-2: KSZ989x/KSZ956x/KSZ9477-to-RJ45 SIGNAL MAPPING – FAST ETHERNET

KSZ989x/KSZ956x/KSZ9477 Pinout	RJ45 Connector Pinout	RJ45 Connector – Option
TXRXxP_A	Pin 1	Pin 3
TXRXxM_A	Pin 2	Pin 6
TXRXxP_B	Pin 3	Pin 1
TXRXxM_B	Pin 6	Pin 2

6.5 Chassis Ground

- The signal ground should extend only to the edge of the magnetics, and there should be no signal ground under the magnetics, connector, and the area in between. If a true chassis ground is available, the connector shield and line-side termination should connect to it. If there is no true chassis ground, then route “chassis ground” with ample copper along the edge of the board to a place where it can be connected to the digital ground, preferably away from sensitive components and possibly near the board power connector.
- Incorporate a large SMD footprint (SMD_1210) to connect the chassis ground to the digital ground. This allows some flexibility at EMI testing for different grounding options. Leaving the footprint open will allow the two grounds to remain separate. Shorting them together with a zero ohm resistor will connect them. For best performance, short them together with a cap or a ferrite bead.

6.6 Capacitive Coupling Option

The KSZ989x/KSZ956x/KSZ9477 family switches may be used in transformer-less applications where the PHY-to-PHY connection is within one PCB or interconnected PCBs, and a cable is not needed.

- A single DC blocking 0.1 µF capacitor is placed in series on each of the eight signals.
- No additional components are needed between the KSZ989x/KSZ956x/KSZ9477 and the capacitor.
- The other device may require termination or other circuitry. Refer to Microchip documentation for that device.
- Another option is to achieve DC isolation using single magnetics, with or without Common-mode chokes. The orientation of the choke does not matter.
- Keep auto-negotiation enabled when 1000M speed is used. If connecting to another device at 100M or 10M speed, then it is suggested (but not required) to disable auto-negotiation for both devices.

7.0 MANAGEMENT BUS

- The management bus allows a management device to read and write the registers of the KSZ989x/KSZ956x/KSZ9477 family of switches. Management bus use is strongly recommended for all applications, even if only for working around device errata.
- Four pins provide a dedicated bus which is set to be either **SPI**, **I²C**, or **MIIM** (**MDIO**). Additionally, the In-Band Architecture (IBA) feature can be enabled to provide register access via special management packets through any of the device's PHY or MAC ports.
- **SPI**, **I²C**, and **IBA** are the preferred management options, with **SPI** having a speed advantage over **I²C**. All of these options provide access to all registers. **MIIM** is the least preferred option because it can access only the PHY registers, not the switch or xMII registers.
- The KSZ989x/KSZ956x/KSZ9477 switch and management device should have the same I/O voltage for the management bus. If not, voltage translators should be used.
- Refer to *AN2661 Getting Started with 3-Port Gigabit Ethernet Switch Configuration Options* application note for further details.

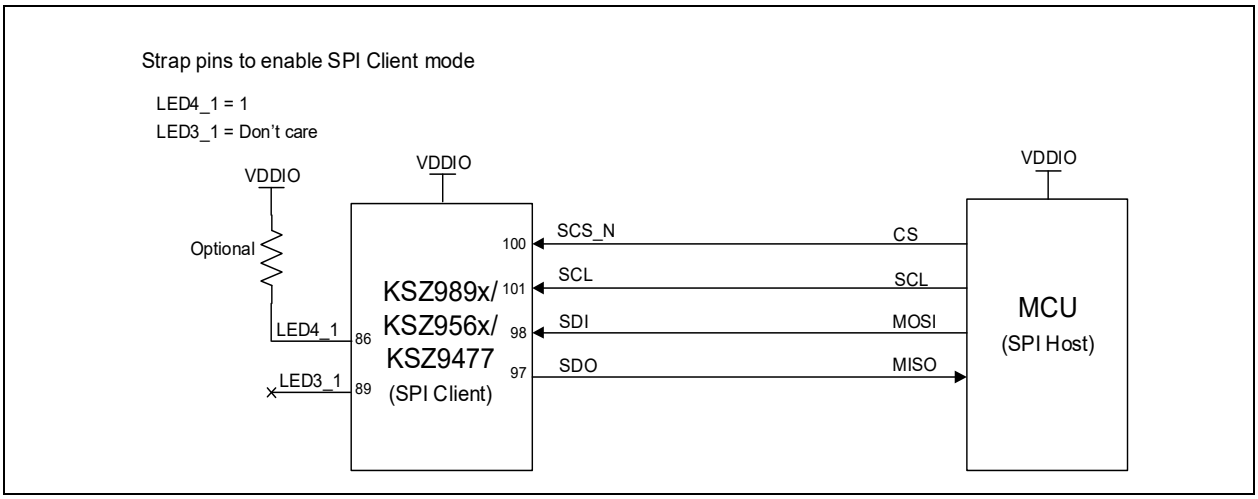
7.1 SPI Client Management

The SPI Client Management mode provides complete read and write access to all KSZ989x/KSZ956x/KSZ9477 device (PHY and switch) registers. The external SPI host device supplies the chip select (**SCS_N**), serial clock (**SCL**), and serial input data (**SDI**). Serial output data (**SDO**) is driven by the KSZ989x/KSZ956x/KSZ9477.

To select SPI Client mode, the **LED4_1** and **LED3_1** strap pins are set to 1 and x (either 1 or 0), respectively. Refer to Section 2.2, "Pin Check" for more details.

The SPI block diagram and pin connections between the KSZ989x/KSZ956x/KSZ9477 and management device are shown in Figure 7-1.

FIGURE 7-1: SPI BLOCK DIAGRAM



7.2 I²C Client Management

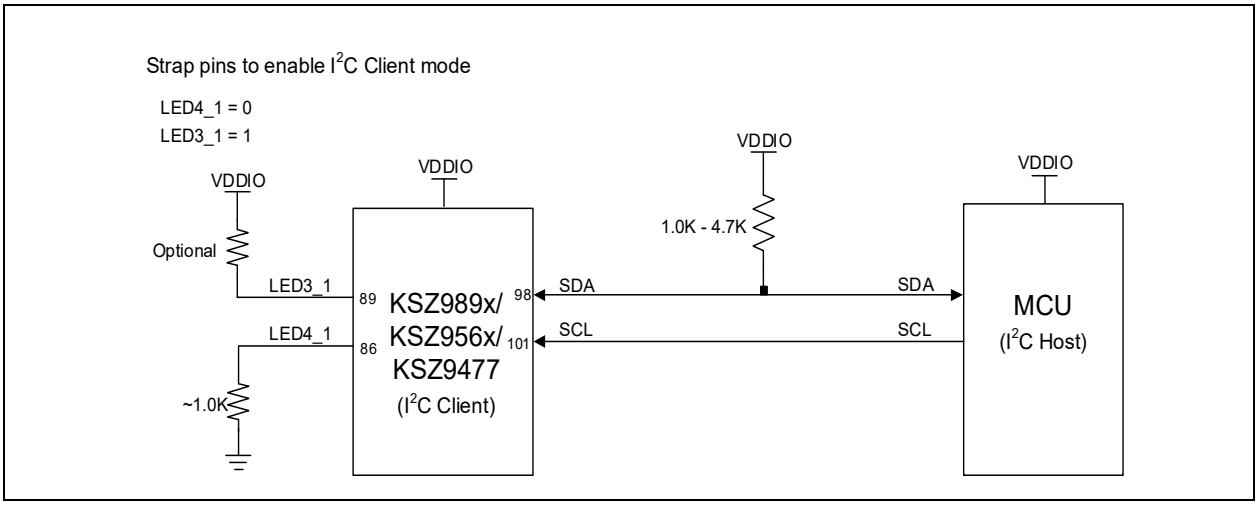
The I²C Client Management mode provides complete read and write access to all KSZ989x/KSZ956x/KSZ9477 (PHY and Switch) registers. The external I²C host device supplies the serial clock (SCL). The serial data (SDA) is a bidirectional open-drain that is driven by the I²C host for register read and write access and is driven by the KSZ989x/KSZ956x/KSZ9477 device to return the register read value.

To select and enable I²C Client mode, the **LED4_1** and **LED3_1** strap pins are set to 0 and 1, respectively. Refer to Section 2.2, "Pin Check" for more details.

An external 1.0 kΩ to 4.7 kΩ pull-up resistor is required on the SDA signal. The unused pins **SDO** and **SCS_N** are left unconnected.

The I²C block diagram and pin connections between the KSZ989x/KSZ956x/KSZ9477 device and the microcontroller (MCU) are shown in Figure 7-2.

FIGURE 7-2: I²C BLOCK DIAGRAM



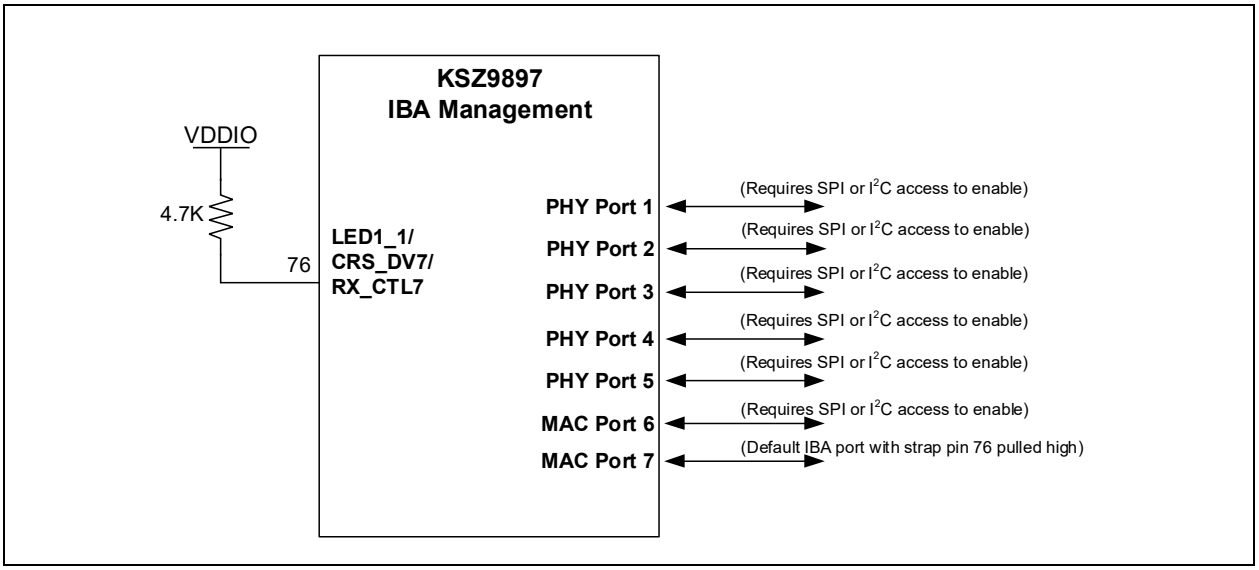
7.3 In-Band Access (IBA) Management

In-Band Access (IBA) Management is a proprietary feature that uses customized 64-byte Ethernet frames to provide complete read and write access to all KSZ989x/KSZ956x/KSZ9477 (PHY and Switch) registers. Any one of the seven data ports (PHY Ports 1 to 5 or MAC Ports 6 and 7) can be used for in-band register access.

To select and enable IBA Management mode, **RX_DV7/CRS_DV7/RX_CTL7** pin for KSZ9897R and KSZ9567R, **IBA** pin for KSZ9897S, KSZ9567S, and KSZ9477 or **RX_DV6/CRS_DV6/RX_CTL6** pin should be pulled high. Refer to Section 2.2, "Pin Check" for more details. With that pin strapping, PHY port 7 is assigned as the default IBA port for all switches except KSZ9896 which does not have the Port 7. The default IBA port is Port 6 for KSZ9896. SPI or I²C management is required to enable any other port as the IBA port. However, IBA is mutually exclusive with I²C and SPI. IBA is recommended to be disabled when the SPI or I²C is used to manage the switch.

Refer to the In-Band Management (IBA) Control Register at address locations 0x0104 – 0x0107 in the KSZ989x/KSZ956x/KSZ9477 family switch data sheets for the bit settings to select a particular port as the IBA port. Figure 7-3 shows the IBA block diagram.

FIGURE 7-3: IBA BLOCK DIAGRAM



7.4 MII Management (MIIM)

The MII Management mode provides access only to the KSZ989x/KSZ956x/KSZ9477 PHY registers. The external MDC/MDIO controller device supplies the serial clock (MDC). The serial data (MDIO) is a bidirectional open-drain that is driven by the controller for register read and write access, and is driven by the KSZ989x/KSZ956x/KSZ9477 device to return the register read value.

To select and enable MIIM mode, the **LED4_1** and **LED3_1** strap pins are both pulled low. Refer to Section 2.2, "Pin Check" for more details.

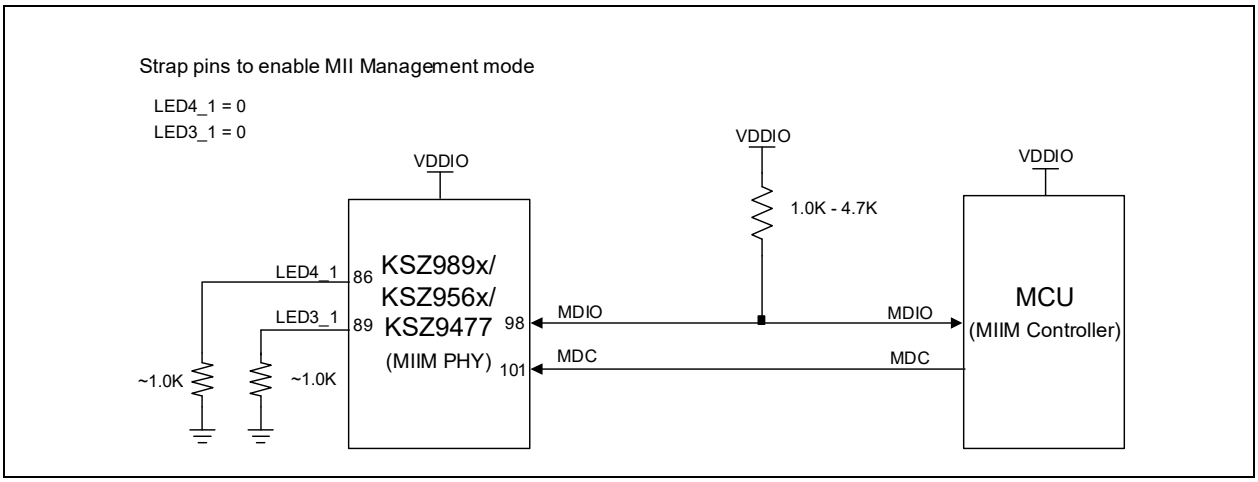
An external 1.0 kΩ to 4.7 kΩ pull-up resistor is required on the MDIO signal.

The unused pins **SDO** and **SCS_N** are left unconnected.

Note:	It is recommended to keep the pull-up resistor on the **MDIO** pin of the MCU even if this interface is not used.

The MII Management block diagram and pin connections between the KSZ989x/KSZ956x/KSZ9477 device and the microcontroller (MCU) are shown in Figure 7-4.

FIGURE 7-4: MII MANAGEMENT BLOCK DIAGRAM



8.0 PARALLEL MAC INTERFACES

MAC Port 6 of all KSZ989x/KSZ956x/KSZ9477 family switches and MAC Port 7 of KSZ9897R and KSZ9567R can be individually set to one of the following parallel MAC configurations:

- RGMII Interface: Supports 1000, 100, and 10 Mbps data rates
- RMII (Clock Mode) Interface: Supports 100 and 10 Mbps data rates, and outputs 50 MHz RMII REF_CLK
- RMII (Normal Mode) Interface: Supports 100 and 10 Mbps data rates, and inputs 50 MHz RMII REF_CLK
- MII (PHY Mode) Interface: Supports 100 and 10 Mbps data rates, and connects to external MII PHY
- MII (MAC Mode) Interface: Supports 100 and 10 Mbps data rates, and connects to external MII MAC

MAC Port 6 of KSZ9896 can also be set to work as GMII (MAC mode) interface or GMII (PHY mode) interface. For the selected data bus interface in the following subsections, check to ensure the listed design guidelines are followed.

8.1 Unused MAC Ports

If only one MAC port is needed, be aware of these differences between the two ports:

- Port 7 is the default port for In-Band Management.
- Port 6 has a timing errata for RGMII.

If one or both of Port 6 and Port 7 are unused, leave all pins of that interface unconnected. This will cause the port to be strapped to RGMII mode at 1000 Mbps. Note that a 125 MHz clock will be output on the **RX_CLK** pin.

If the **RX_CLK** output is undesirable for RF emission reasons, it can be disabled by doing the following:

1. Strap **LED5_1** low with a suitably small value resistor. This disables the switch at startup.
2. Strap **RXD_3**, **RXD_2**, and **RXD_1** (on the unused port only) high with 10 kΩ resistors. This configures the port for MII mode and MAC device mode. In MII (MAC) mode, there are no output clocks.
3. Block traffic to and from this port by clearing the Port Transmit and Port Receive Enable bits in the Port MSTP State Register (0xNB04). If MSTP will be used, repeat writing to register 0xNB04 for all eight possible values of MSTP Pointer in index register 0xNB01.
4. Enable the switch by setting the Start Switch bit in Switch Operation Register (0x0300).

Please be sure that Step 3 should not be skipped. Without that step, broadcast, multicast, and unknown unicast frames will all be forwarded to that port. Those frames are supposed to be sent out and removed from the internal frame buffer by the MAC on that port. However, since the MAC is configured in MAC mode, it requires external clock input to the **RX_CLK** pin to work. Without that clock, those frames will stay in the buffer permanently. When frames for that port cumulates, the whole switch will be congested and frame drop on all ports will happen eventually.

8.2 RGMII Interface

8.2.1 RGMII FUNCTIONAL CONFIGURATION

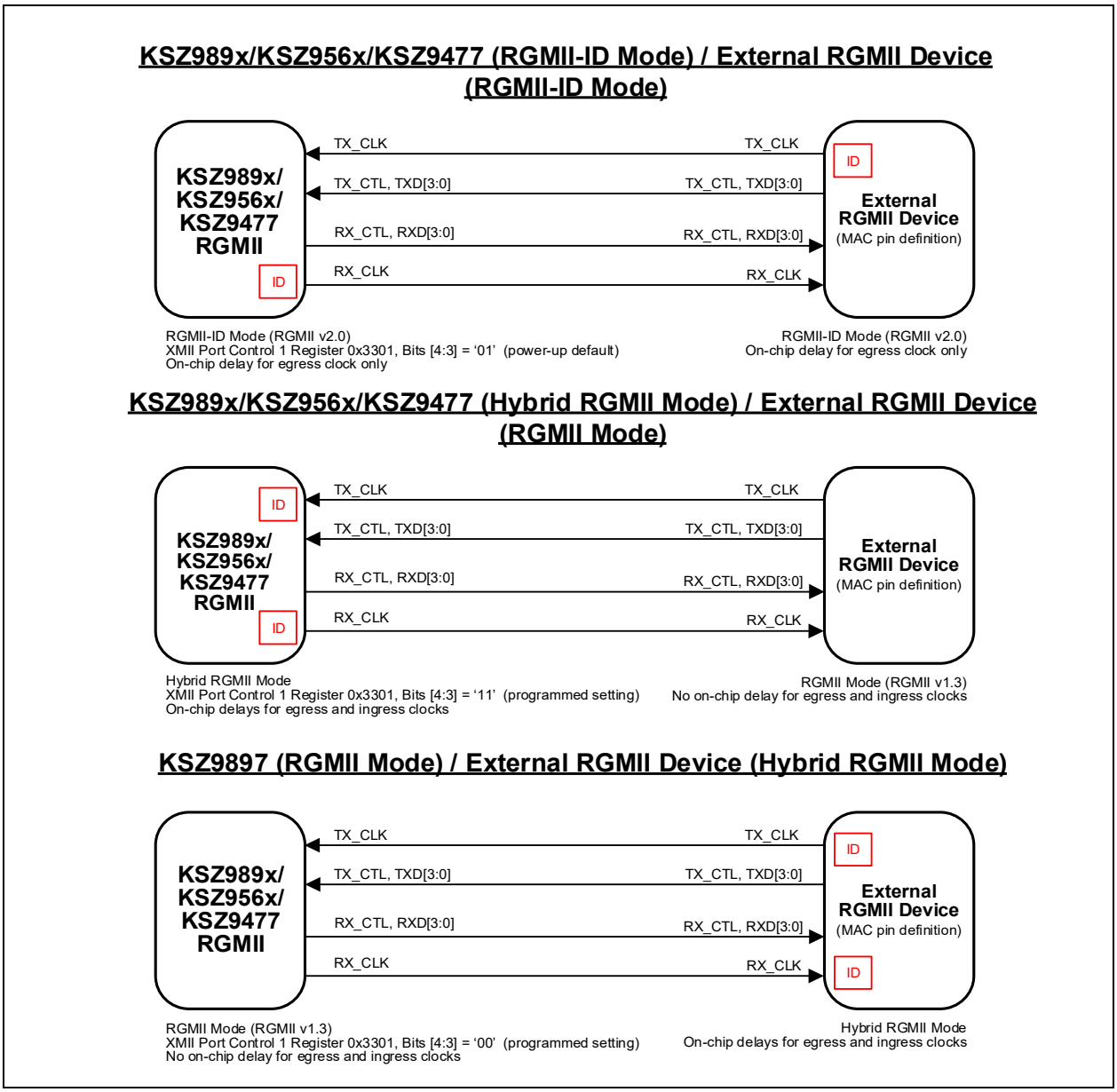
When Port 6 or Port 7 is set to RGMII mode, it is configured to support RGMII-ID mode (with internal delay for the egress output clock **RX_CLK**) as the power-up default setting. This supports RGMII v2.0, which calls for each device to delay its output clock relative to its output data and control.

Optionally, the KSZ989x/KSZ956x/KSZ9477 can be programmed after power-up to support either one of the following two modes:

- Hybrid RGMII mode (with internal delays for egress output clock **RX_CLK** and for ingress input clock **TX_CLK**) when interfacing with an RGMII device that is configured with no internal delay for egress output clock and ingress input clock.
- RGMII mode (without internal delay for egress output clock and ingress input clock) for interfacing with an RGMII device that is configured with internal delays for both egress output clock and ingress input clock. This configuration is uncommon.

Figure 8-1 shows the on-chip delays for the three aforementioned RGMII functional configurations. The on-chip clock delays (denoted by “ID”) are depicted in the figure with RGMII connections between KSZ989x/KSZ956x/KSZ9477 and an external RGMII device (MAC pin definition). KSZ989x/KSZ956x/KSZ9477 register bit settings to enable or disable the on-chip egress and ingress clock delays are provided in the figure.

FIGURE 8-1: KSZ989X/KSZ956X/KSZ9477 AND EXTERNAL RGMII DEVICE (MAC PIN DEFINITION) – RGMII FUNCTIONAL CONFIGURATION WITH ON-CHIP CLOCK DELAY OPTIONS



8.2.2 RGMII SKEW CALCULATION

RGMII is a source synchronous clock data bus. The clock is sourced from the device side that is sending out the 4-bit data and control signals. This allows for RGMII skew calculation and PCB trace length matching or delay (if applicable) to be applied separately for the RGMII transmit bus group (**TX_CLK**, **TX_CTL**, and **TXD[3:0]**) and RGMII receive bus group (**RX_CLK**, **RX_CTL**, and **RXD[3:0]**).

Internal delays are always preferred over PCB trace delay since signal integrity is a concern for RGMII.

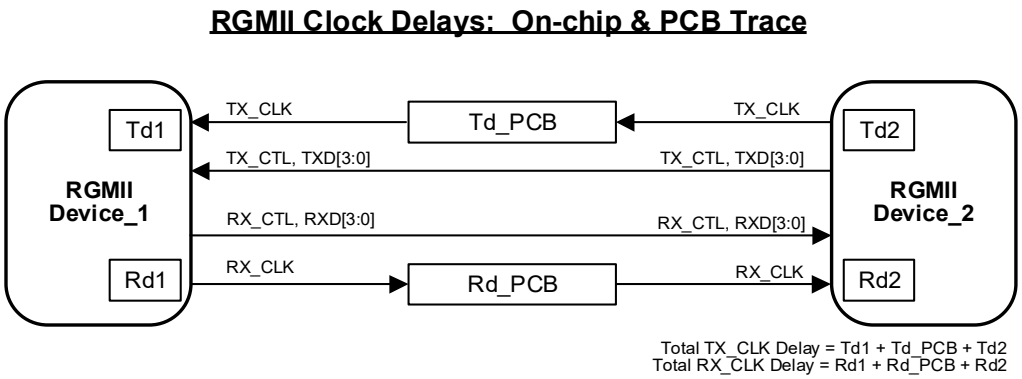
The RGMII clock skews are summarized in Figure 8-2 and are computed as follows:

- Total TX_CLK Delay = Td1 + Td_PCB + Td2
- Total RX_CLK Delay = Rd1 + Rd_PCB + Rd2

Separately, in each direction, the RGMII data/control signal to clock skew should be set between 1.2 ns (minimum) and 2.0 ns (maximum) if the receiving end adheres to the timing of the RGMII.

Note:	The KSZ989x/KSZ956x/KSZ9477 has a timing erratum for Port 6. It requires additional setup time for **TX_CTL** and **TXD[3:0]** relative to **TX_CLK**. The standard solution is to increase the delay on **TX_CLK** by enabling the ingress ID for Port 6 of the KSZ989x/KSZ956x/KSZ9477 in addition to the egress internal delay in the other RGMII device. If the other device does not have internal egress delay on **TX_CLK**, then it is necessary to add clock skew by increasing the length of the **TX_CLK** trace on the PCB relative to **TX_CTL** and **TXD[3:0]**.

FIGURE 8-2: RGMII CLOCK SKEW DIAGRAM



8.2.3 RGMII INTERFACE WITH EXTERNAL RGMII DEVICE

When Port 6 or Port 7 is used in RGMII mode, the key design guidelines to note are:

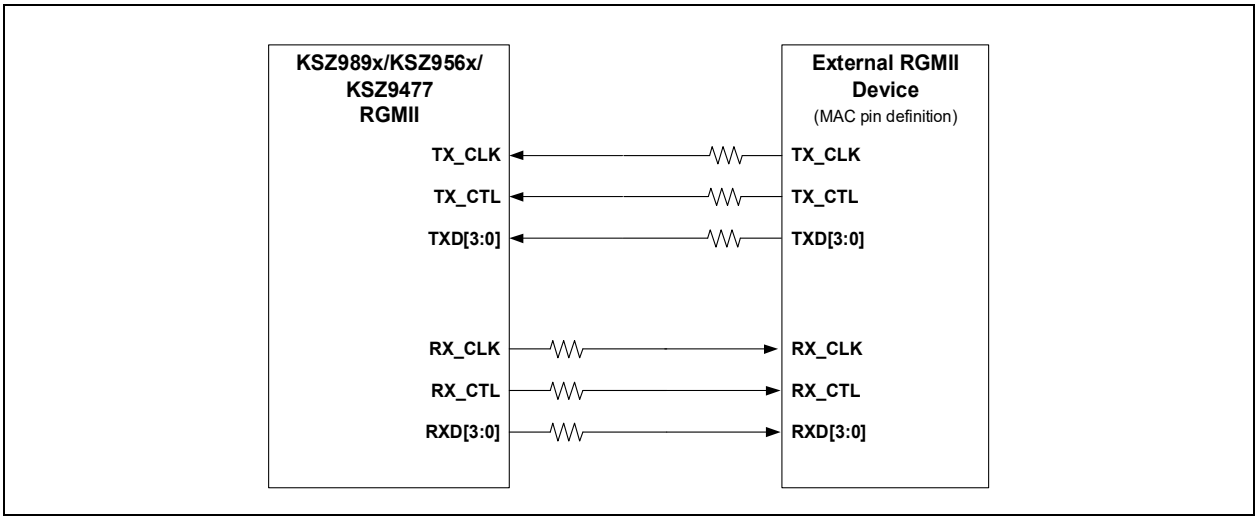
- To configure Port 6 or Port 7 to RGMII mode, strap **RXD_3** and **RXD_2** both low.
- Strap **RXD_0** low for 1000 Mpbs RGMII, or strap it high for 100 Mbps.
- Determine the RGMII functional mode (RGMII-ID, Hybrid, or RGMII) to use to connect with the external RGMII device as defined in Section 8.2.1, "RGMII Functional Configuration".
- For the selected RGMII functional mode, calculate the RGMII clock delay, and if needed, make additional skew adjustments to the RGMII clock, data, and/or control lines, as discussed in Section 8.2.2, "RGMII Skew Calculation". The additional skew adjustments can be achieved by inserting PCB trace length delays, and, if supported by the RGMII device, by programming RGMII pad skew step settings. (For example, Microchip KSZ9031RNX Gigabit Ethernet PHY has RGMII pad skew step registers.)
- Route RGMII signals over a continuous ground plane layer for 50Ω impedance control.
- Use connectors with caution. If the RGMII signals must go through a connector, use a high-speed connector, keep traces short, and ensure that signal integrity is not degraded.
- Match the signal traces within 7 mm (300 mils) for best performance. All transmit signals should be matched. All receive signals should also be matched. The transmit and receive signal groups do not need to be matched to each other.
- Place series termination resistors near all **RGMII** output pins. Refer to Figure 8-3 for output pin placement. The typical resistor value is 22Ω to 33Ω.
- Both devices should use the same I/O supply voltage.

8.2.3.1 KSZ989X/KSZ956X/KSZ9477 RGMII AND EXTERNAL RGMII DEVICE (MAC PIN DEFINITION)

The KSZ989x/KSZ956x/KSZ9477 RGMII signal connections with an external RGMII device (MAC pin definition), such as a MAC processor or the MAC port of a Gigabit Ethernet switch, are shown in Figure 8-3.

Note: Always check the data sheets for the connecting RGMII pins between two devices to ensure the connected pins are neither both inputs nor both outputs. Do not rely on just the pin name to determine if a pin is an input or an output.

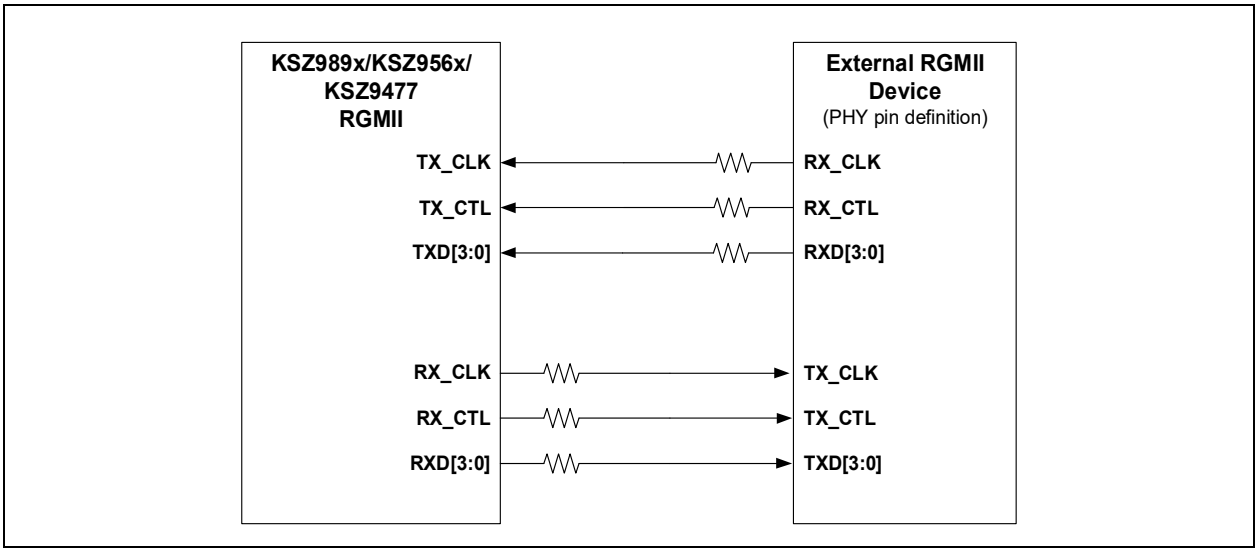
FIGURE 8-3: KSZ989X/KSZ956X/KSZ9477 RGMII AND EXTERNAL RGMII DEVICE (MAC PIN DEFINITION) – BLOCK DIAGRAM



8.2.3.2 KSZ989X/KSZ956X/KSZ9477 RGMII AND EXTERNAL RGMII DEVICE (PHY PIN DEFINITION)

The KSZ989x/KSZ956x/KSZ9477 RGMII signal connections with an external RGMII device (PHY pin definition), such as an Ethernet PHY or the MAC port of certain Ethernet switches, are shown in Figure 8-4.

FIGURE 8-4: KSZ989X/KSZ956X/KSZ9477 RGMII AND EXTERNAL RGMII DEVICE (PHY PIN DEFINITION) – BLOCK DIAGRAM



8.3 RMII (Clock Mode) Interface

When Port 6 or Port 7 is configured to RMII (Clock Mode), it will output the RMII Reference clock.

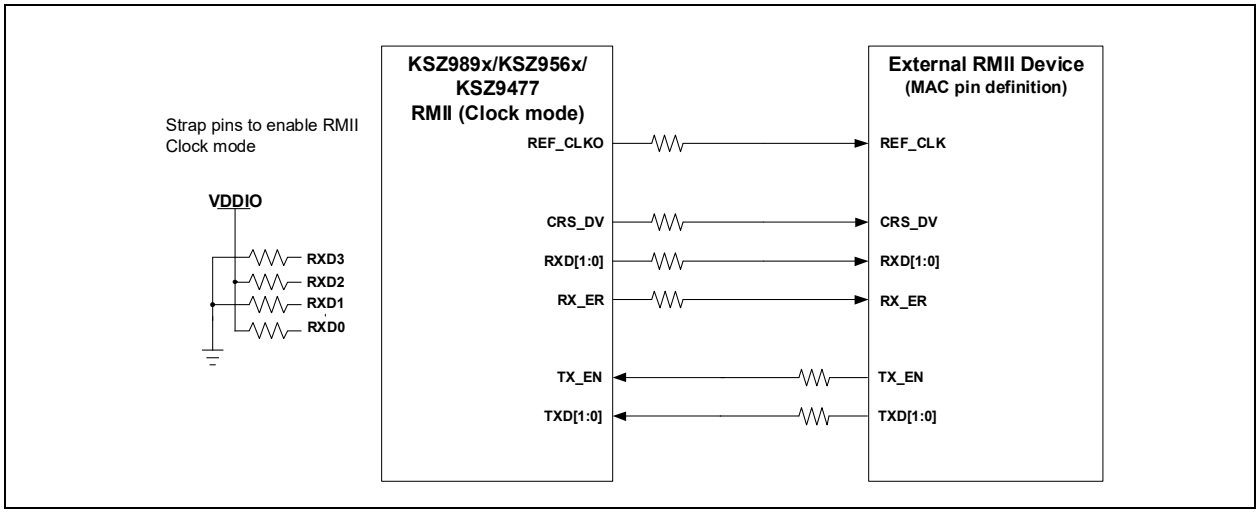
The key design guidelines to note are:

- To configure Port 6 or Port 7 to RMII Clock Mode, strap **RXD_3** low, **RXD_2** high, **RXD_1** low, and **RXD_0** high.
- To set the port speed to 10 Mbps instead of 100 Mbps, write to register 0xN300.
- The RMII 50 MHz reference clock (**REF_CLK**) is an output from the KSZ989x/KSZ956x/KSZ9477 and an input to the connecting RMII device.
- It is recommended to place series termination resistors at all **RMII** output pins for signal integrity and EMI purposes. The typical resistor value is 22Ω to 33Ω. Strapping resistors can be located on either side of the series resistors.
- Both devices should use the same I/O supply voltage.

The KSZ989x/KSZ956x/KSZ9477 RMII (Clock mode) signal connections with an external RMII device (MAC pin definition) are shown in Figure 8-5.

Note: Always check the data sheets for the connecting **RMII** pins between two devices to ensure the connected pins are neither both inputs nor both outputs. Do not rely on just the pin name to determine if a pin is an input or an output.

FIGURE 8-5: KSZ989x/KSZ956x/KSZ9477 RMII (CLOCK MODE) AND EXTERNAL RMII DEVICE (MAC PIN DEFINITION) – BLOCK DIAGRAM



8.4 RMII (Normal Mode) Interface

When Port 6 or Port 7 is configured to RMII (Normal Mode), it receives the RMII Reference clock as an input.

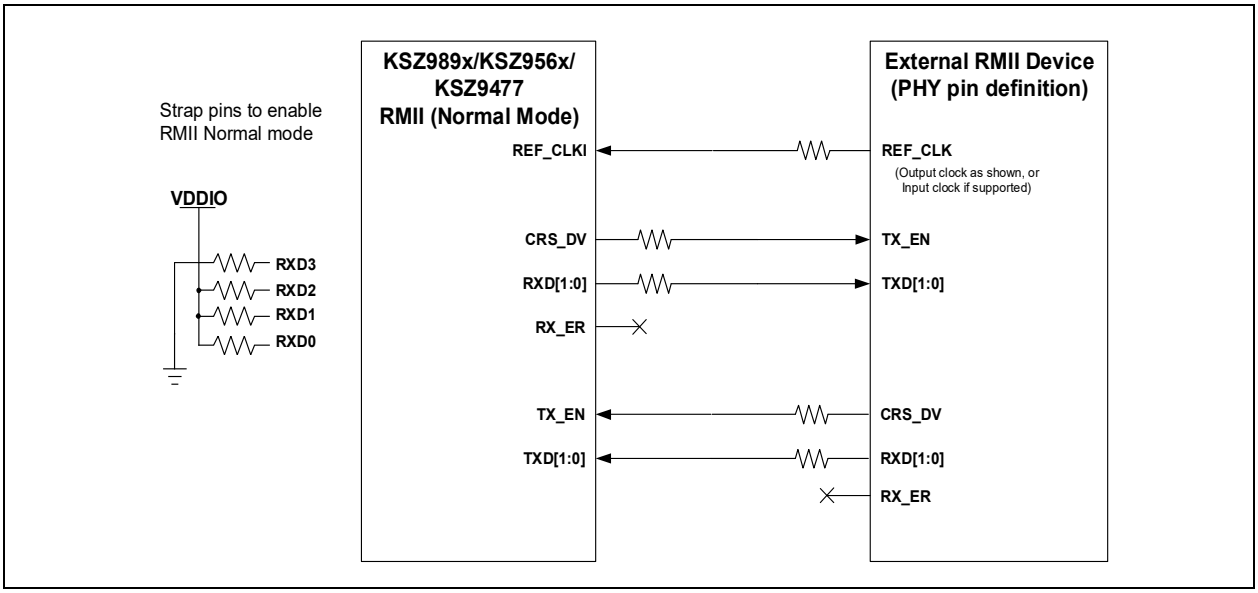
The key design guidelines to note are:

- To configure Port 6 or Port 7 to RMII Normal mode, strap **RXD_3** low, **RXD_2** high, **RXD_1** high and **RXD_0** high.
- To set the port speed to 10 Mbps instead of 100 Mbps, write to register 0xN300.
- The RMII 50 MHz reference clock (REF_CLK) is an input to the KSZ989x/KSZ956x/KSZ9477 and is sourced from either an external 50 MHz clock (for example, an oscillator) or the connecting RMII device. If sourced from the external clock, the **REF_CLK** is also an input to the connecting RMII device.
- It is recommended to place series termination resistors at all **RMII** output pins for signal integrity and EMI purposes. The typical resistor value is 22Ω to 33Ω. Strapping resistors can be located on either side of the series resistors.
- Both devices should use the same I/O supply voltage.

The KSZ989x/KSZ956x/KSZ9477 RMII (Normal mode) signal connections with an external RMII device (PHY pin definition) are shown in Figure 8-6.

Note: Always check the data sheets for the connecting RMII pins between two devices to ensure the connected pins are neither both inputs nor both outputs. Do not rely on just the pin name to determine if a pin is an input or an output.

FIGURE 8-6: KSZ989x/KSZ956x/KSZ9477 RMII (NORMAL MODE) AND EXTERNAL RMII DEVICE (PHY PIN DEFINITION) – BLOCK DIAGRAM



8.5 MII (PHY Mode) Interface

There are two MII modes of operation: PHY Mode and MAC Mode.

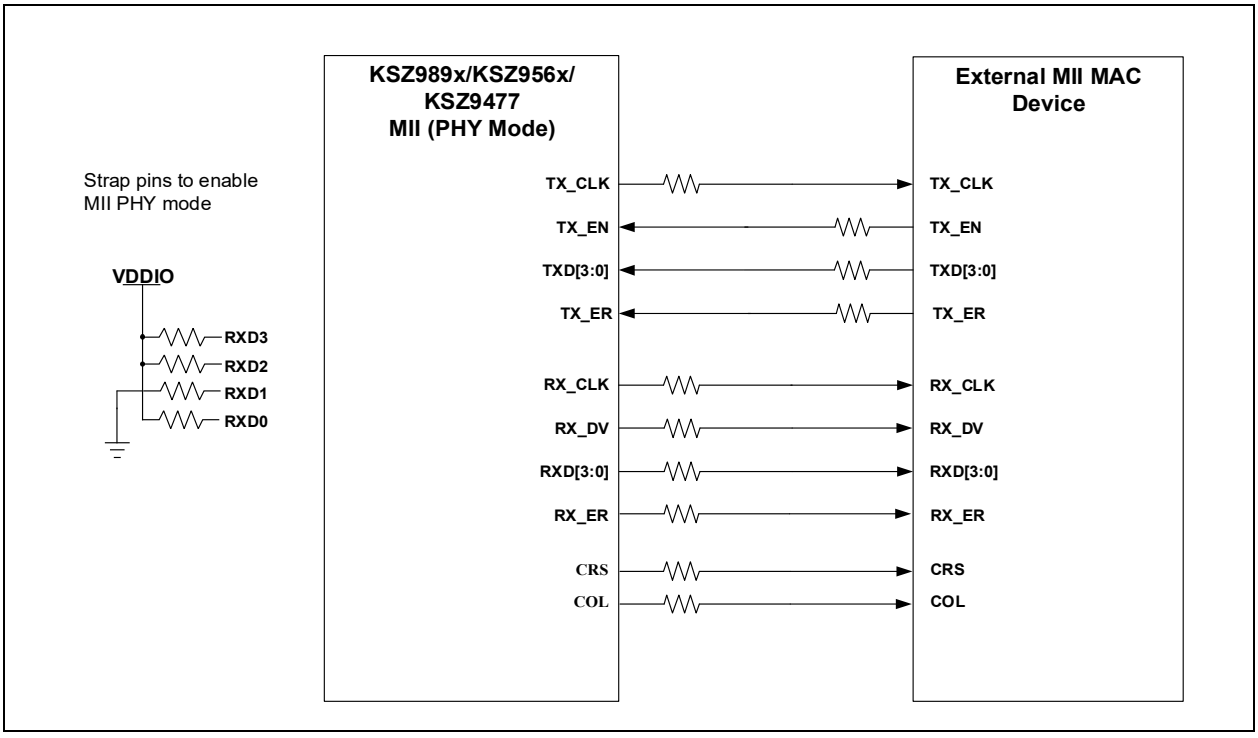
When Port 6 or Port 7 is configured to MII (PHY mode), its interface is like an MII PHY device, and it should connect to a device with an MII MAC interface such as an MCU. The key design guidelines to note are:

- To configure Port 6 or Port 7 to MII PHY Mode, strap **RXD_3** and **RXD_2** both high, **RXD_1** low, and **RXD_0** high.
- To set the port speed to 10 Mbps instead of 100 Mbps, write to register 0xN300.
- Transmit clock (**TX_CLK**) and receive clock (**RX_CLK**) are outputs from the KSZ989x/KSZ956x/KSZ9477 and inputs into the external MII MAC.
- Collision (COL) and carrier sense (CRS) outputs are also outputs from the KSZ989x/KSZ956x/KSZ9477 and inputs into the external MII MAC.
- It is recommended to place series termination resistors at all **MII** output pins for signal integrity and EMI purposes. The typical resistor value is 22Ω to 33Ω. Strapping resistors can be located on either side of the series resistors.

The KSZ989x/KSZ956x/KSZ9477 MII (PHY mode) signal connections with an external MII MAC are shown in Figure 8-7.

Note: Always check the data sheets for the connecting **MII** pins between two devices to ensure the connected pins are not both inputs and not both outputs. Do not rely on just the pin name to determine if a pin is an input or an output.

FIGURE 8-7: KSZ989x/KSZ956x/KSZ9477 MII (PHY MODE) AND EXTERNAL MII MAC – BLOCK DIAGRAM



8.6 MII (MAC Mode) Interface

When Port 6 or Port 7 is configured to MII (MAC mode), it should connect to an MII PHY or other device with an MII PHY interface. The key design guidelines to note are:

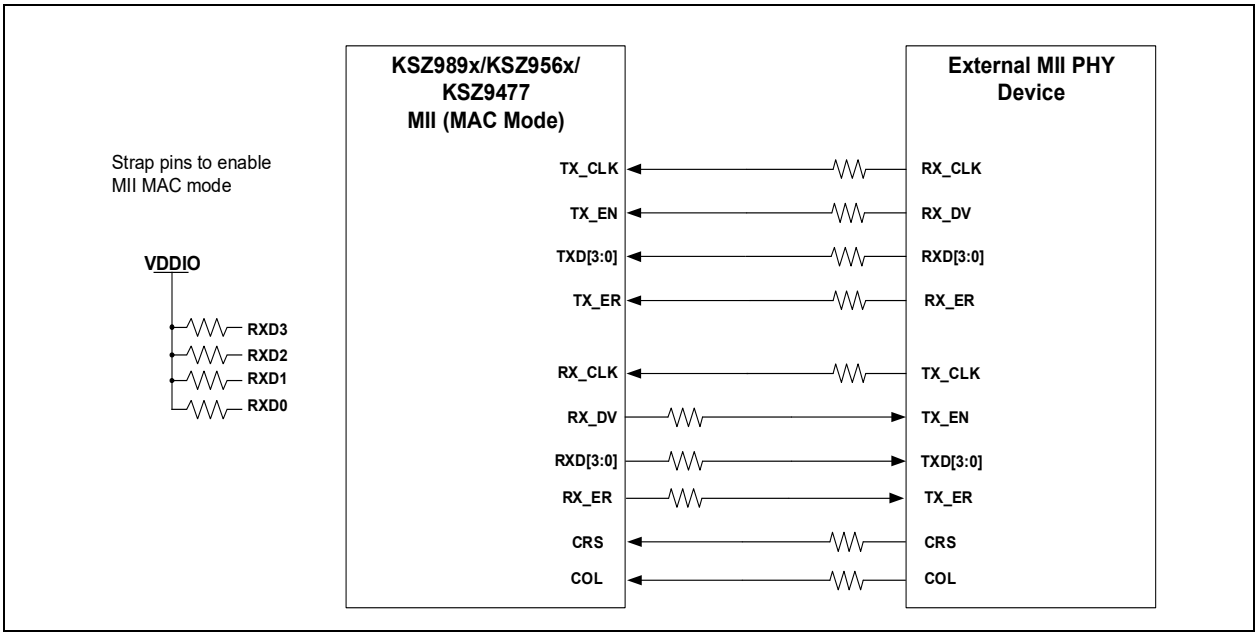
- To configure Port 6 or Port 7 to MII PHY Mode, strap **RXD_3** and **RXD_2** both high, **RXD_1** high, and **RXD_0** high.
- To set the port speed to 10 Mbps instead of 100 Mbps, write to register 0xN300.
- Transmit clock (**TX_CLK**) and receive clock (**RX_CLK**) are inputs to the KSZ989x/KSZ956x/KSZ9477 and outputs from the external MII PHY.

- Collision (**COL**) and carrier sense (**CRS**) inputs are also inputs to the KSZ989x/KSZ956x/KSZ9477 and outputs from the external MII PHY.
- It is recommended to place series termination resistors at all **MII** output pins for signal integrity and EMI purposes. The typical resistor value is 22Ω to 33Ω. Strapping resistors can be located on either side of the series resistors.

The KSZ989x/KSZ956x/KSZ9477 MII (MAC mode) signal connections with an external MII PHY are shown in Figure 8-8.

Note:	Always check the data sheets for the connecting **MII** pins between two devices to ensure the connected pins are not both inputs and not both outputs. Do not rely on just the pin name to determine if a pin is an input or an output.

FIGURE 8-8: KSZ989x/KSZ956x/KSZ9477 MII (MAC MODE) AND EXTERNAL MII PHY – BLOCK DIAGRAM



8.7 GMII (PHY Mode) Interface

GMII provides a common interface between GMII PHYs and MACs at 1000 Mbps. GMII is based heavily on the MII interface, with the key signal differences being the data bus width, clock rate, and direction of the transmit clock. Only KSZ9896 in the KSZ989x family supports GMII interface. Because the GMII interface has more number of signal pins than all the other MAC interfaces, the KSZ9896 is a six-port switch instead of seven-port as all the other variants in the family.

There are two GMII modes of operation: PHY mode and MAC mode.

When Port 6 of KSZ9896 is configured to GMII (PHY mode), its interface is like an GMII PHY device, and it should connect to a device with an GMII MAC interface, such as an MCU. The key design guidelines to note are:

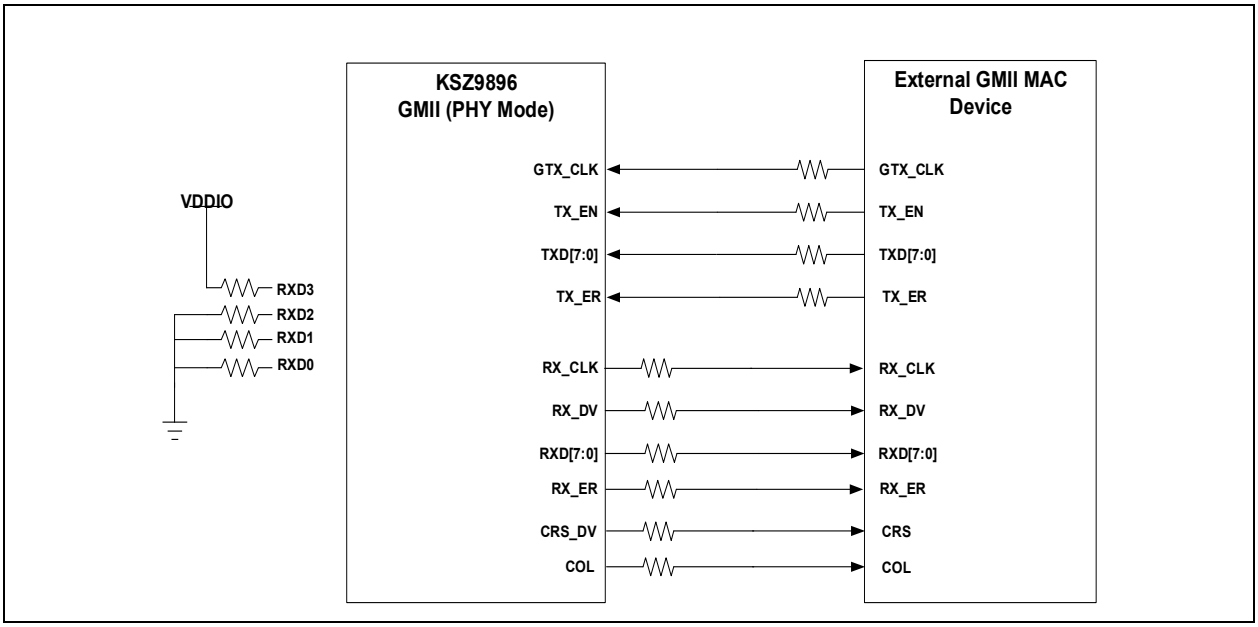
- To configure Port 6 of KSZ9896 to GMII PHY Mode, strap **RXD_3** high, **RXD_2** low, **RXD_1** low, and **RXD_0** low.
- Transmit clock (**GTX_CLK**) is input to KSZ9896 and receive clock (**RX_CLK**) is output from KSZ9896 and input into the external GMII MAC.
- Another configuration strap on the **RX_ER6/RX_CLK6** pin selects either 2-Wire mode or 3-Wire mode for the GMII/MII clocking. This option determines which pin is used for the KSZ9896's MII **RX_CLK**. The 3-Wire mode option is intended for use when connecting to a 1000/100/10 Mbps PHY, such as the Microchip KSZ9031MNX, which has separate pins for its **GTX_CLK** and **TX_CLK** signals. When 3-Wire mode is selected, the MII (MAC Mode) **RX_CLK6** input clock is on pin 75. When in 2-Wire mode, **RX_CLK6** is on pin 72. If GMII will not be used or when in PHY mode, the Clock mode should be 2-Wire.
- Collision (**COL**) and carrier sense (**CRS**) are outputs from the KSZ9896 and inputs into the external GMII MAC.

- It is recommended to place series termination resistors at all **GMII** output pins for signal integrity and EMI purposes. The typical resistor value is 22Ω to 33Ω. Strapping resistors can be located on either side of the series resistors.

The KSZ9896 GMII (PHY mode) signal connections with an external GMII MAC are shown in Figure 8-9.

Note:	Always check the data sheets for the connecting **GMII** pins between two devices to ensure the connected pins are not both inputs and not both outputs. Do not rely on just the pin name to determine if a pin is an input or an output.

FIGURE 8-9: KSZ9896 GMII (PHY MODE) AND EXTERNAL GMII MAC – BLOCK DIAGRAM



8.8 GMII (MAC Mode) Interface

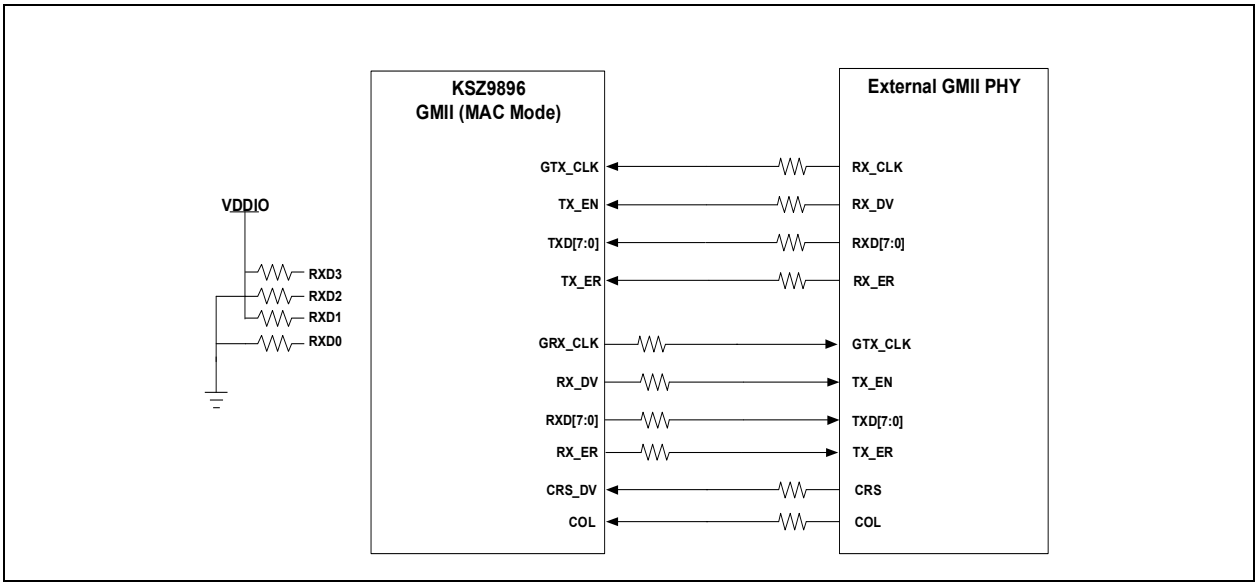
When Port 6 of KSZ9896 is configured to GMII (MAC mode), its interface is like a GMII MAC device, and it should connect to a device with an GMII PHY interface such as an 1000Base-T PHY. The key design guidelines to note are:

- To configure Port 6 of KSZ9896 to GMII MAC Mode, strap **RXD_3** high, **RXD_2** low, **RXD_1** high, and **RXD_0** low.
- Transmit clock (**GTX_CLK**) is input to KSZ9896 and receive clock (**RX_CLK**) is output from KSZ9896 and input into the external GMII MAC.
- Another configuration strap on the **RX_ER6/RX_CLK6** pin selects either 2-Wire mode or 3-Wire mode for the GMII/MII clocking. This option determines which pin is used for the KSZ9896's MII **RX_CLK**. The 3-Wire mode option is intended for use when connecting to a 1000/100/10 Mbps PHY such as the Microchip KSZ9031MNX, which has separate pins for its **GTX_CLK** and **TX_CLK** signals. When 3-Wire mode is selected, the MII (MAC Mode) **RX_CLK6** input clock is on pin 75. When in 2-Wire mode, **RX_CLK6** is on pin 72. If GMII will not be used, or when in PHY mode, the Clock mode should be 2-Wire.
- Collision (**COL**) and carrier sense (**CRS**) are inputs to KSZ9896 and outputs from the external GMII PHY.
- It is recommended to place series termination resistors at all **GMII** output pins for signal integrity and EMI purposes. The typical resistor value is 22Ω to 33Ω. Strapping resistors can be located on either side of the series resistors.

The KSZ9896 GMII (MAC mode) signal connections with an external GMII PHY are shown in Figure 8-10.

Note:	Always check the data sheets for the connecting **GMII** pins between two devices to ensure the connected pins are not both inputs and not both outputs. Do not rely on just the pin name to determine if a pin is an input or an output.

FIGURE 8-10: KSZ9896 GMII (MAC MODE) AND EXTERNAL GMII PHY – BLOCK DIAGRAM



9.0 SERIAL MAC INTERFACE

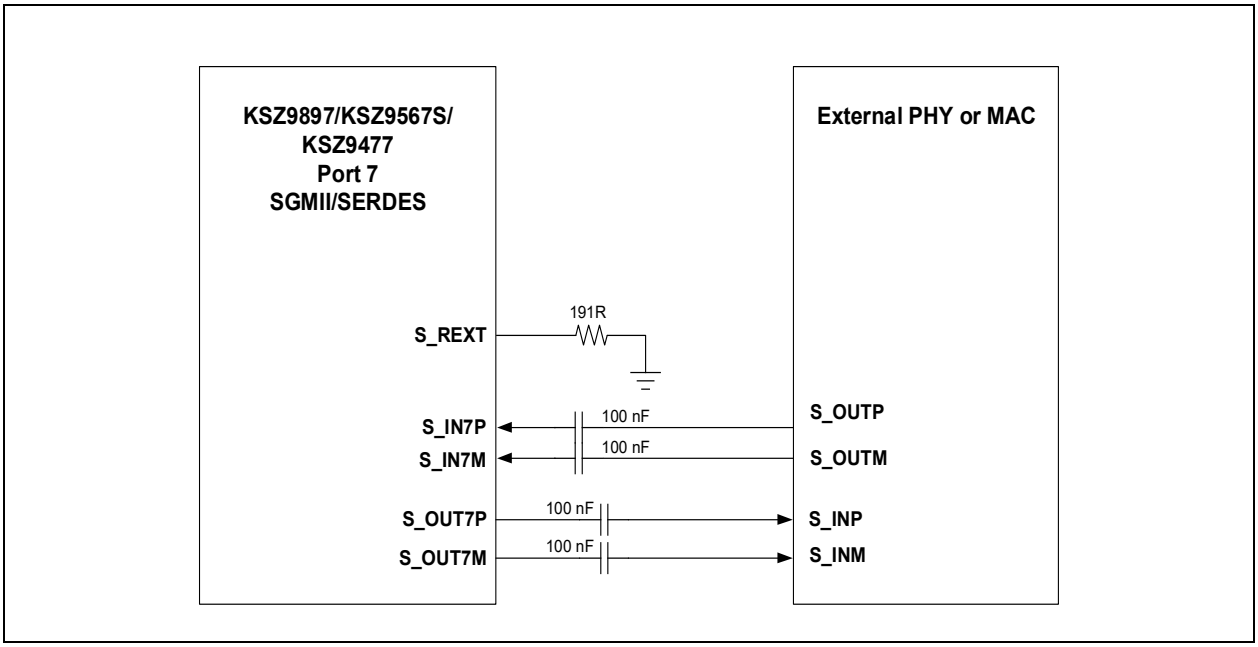
Port 7 of KSZ9567S, KSZ9477, and KSZ9897S will work as a serial MAC interface. By default, it works in Serial Gigabit Media Independent Interface (SGMII) mode for interfacing to an external 10/100/1000 BASE-T PHY that supports the SGMII interface or to another device with an SGMII interface. This interface also has a SerDes mode for interfacing to 1000BASE-X fiber optic modules or to other modules such as copper SFP modules which do not support SGMII.

The interface has one receive differential pair and one transmit differential pair for sending and receiving data and control at a serial bit rate of 1.25 Gbaud. The SGMII block recovers clock from the incoming data. Therefore, a separate input SGMII clock is not needed. Likewise, no output SGMII clock is provided, with the expectation that the connected device will also recover the clock from the receive data.

9.1 SGMII Connection to PHY or MAC Devices

AC coupling should be used on both of the SGMII differential pairs when it connects to a PHY or a MAC device. No external termination or biasing resisters are required at the KSZ switch side because there are internal termination and biasing circuits inside the KSZ989x/KSZ956x/KSZ9477 family switches. See Figure 9-1.

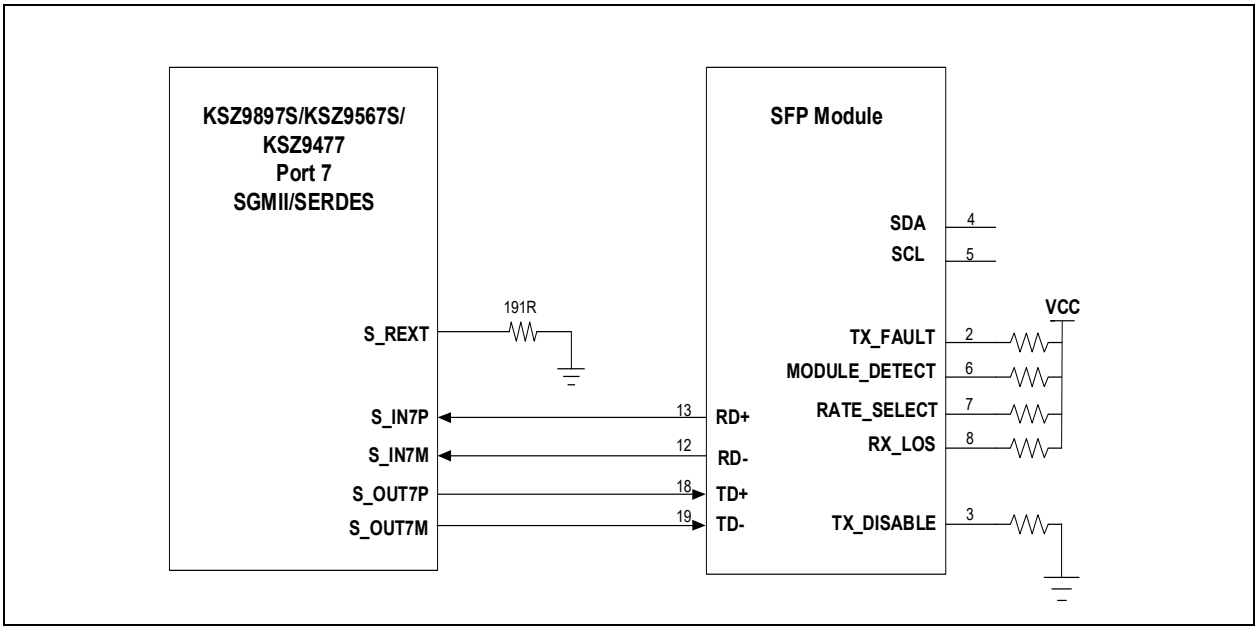
FIGURE 9-1: KSZ9567S, KSZ9477, AND KSZ9897S SGMII CONNECTIONS TO PHY OR MAC-BLOCK DIAGRAM



9.2 1000Base-X SerDes Connection to SFP Modules

The AC coupling capacitors are included in SFP modules so the SGMII/SerDes interface can be connected to an SFP module directly. Figure 9-2 shows an example of KSZ9567S, KSZ9477, or KSZ9897S connecting to an 1000Base-X SFP module. The I^2C interface and other SFP control signals can be connected to the MCU on the board, if that is possible, so that the software can have control on the SFP module. If that is not possible, then the **TX_Disable** pin from the SFP module should be pulled low to enable transmission from that SFP module.

FIGURE 9-2: KSZ9567S, KSZ9477, AND KSZ9897S SERDES CONNECTIONS TO SFP MODULE – BLOCK DIAGRAM



10.0 LED INDICATOR PINS

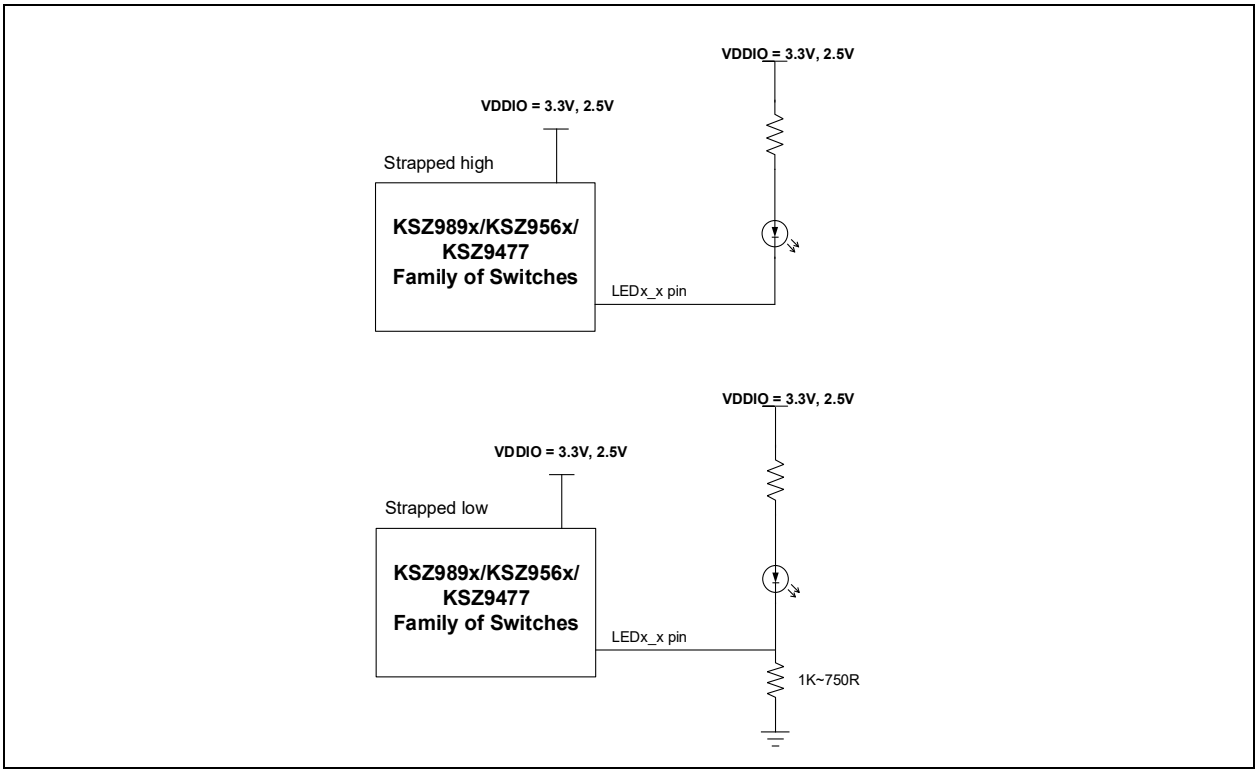
The **LEDx_x** pins are totem pole outputs to drive **LED** indicators to indicate the PHY ports' speed, link, and activity status. Many of them also function as configuration strapping inputs when the **RESET_N** input (pin 46) is asserted low. (See Section 2.2, "Pin Check".)

- **LED** pins are active low. They connect to the cathode side of the **LED**. The **LED** anode connects to 3.3V or 2.5V, and a current limiting resistor is also needed in series with the **LED**.
- If **VDDIO** is 1.8V for the KSZ989x/KSZ956x/KSZ9477 family switch, and 3.3V is used to power the **LED**, then the **LED** signals should be actively buffered.
- To strap an **LED** pin high, an external pull-up resistor is not needed since the **LED** has an internal pull-up.
- To strap an **LED** pin low, an appropriate value external pull-down resistor is required. Depending on the particular **LED** used, the **LED** supply voltage, the chip **VDDIO** voltage, and the current limiting resistor value, the pull-down resistor may need to be small in value. Usually it needs to be 1.0 kΩ to 750Ω. The smallest value is needed when **VDDIO** is less than the **LED** voltage source. Note that the pull-down resistor will cause the **LED** to partially turn on during Reset.
- The minimum **LED** supply voltage is 2.5V.
- The **LED** pins are a potential source of radiated and conducted emissions. If this is a concern, provide an option for a ferrite bead in series on each LED signal, positioned near the chip.

10.1 PHY Port LED Status and Pin Strapping – for VDDIO = 3.3V or 2.5V

Figure 10-1 shows the strap high and low reference circuits for the multiplexed PHY port LED status and pin strapping for 3.3V and 2.5V **VDDIO**.

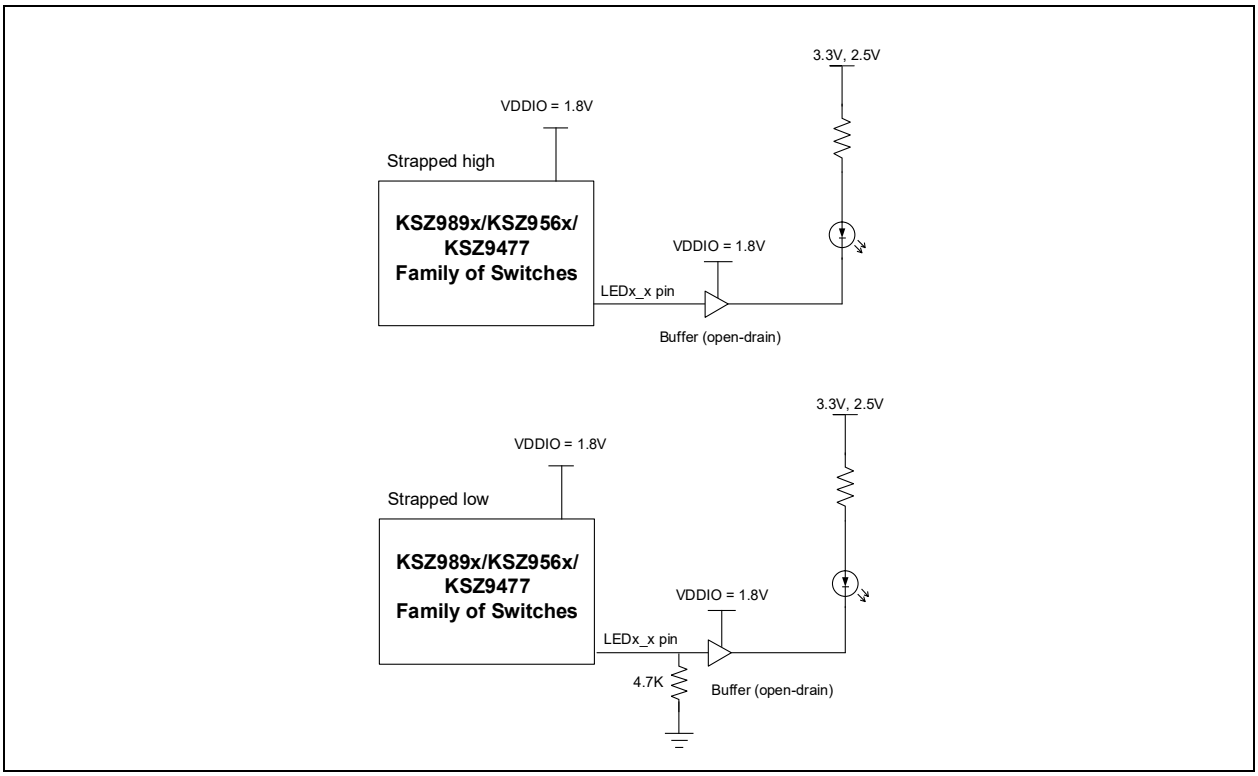
FIGURE 10-1: PHY Port LED Status and Pin Strapping – for VDDIO = 3.3V or 2.5V



10.2 PHY Port LED Status and Pin Strapping – for VDDIO = 1.8V

Figure 10-2 shows the strap high and low reference circuits for the multiplexed PHY port LED status and pin strapping for 1.8V **VDDIO**. The open-drain buffers serve as level shifters and are needed to turn on the LED indicators that require voltage drops of 1.6V to 2.2V, depending on the LED color.

FIGURE 10-2: PHY Port LED Status and Pin Strapping – for VDDIO = 1.8V



11.0 GPIO PIN (FOR KSZ9567R, KSZ9567S, AND 9477 THAT SUPPORT 1588)

- The **GPIO_1** pin is designed to support IEEE 1588 Precision Time Protocol (PTP) applications and is configurable to implement event trigger outputs and timestamp capture inputs to support real-time application requirements. **GPIO_1** has very limited general purpose input or output capabilities.

12.0 CLKO_25_125 PIN (FOR KSZ9897R, KSZ9897S, AND KSZ9896)

- The **CLK_25_125** provides a 25 MHz or 125 MHz output clock. It is derived from the main chip reference clock. Register control is used to configure or disable this output.

13.0 SYNCLKO (FOR KSZ9567R, KSZ9567S, AND KSZ9477 THAT SUPPORT SYNCE)

- The **SYNCLKO** provides a 25 MHz or 125 MHz output clock. At power-up, it is derived from the main chip reference clock. Optionally, it can be derived from a recovered PHY clock for use in synchronous Ethernet applications. Register control is used to configure or disable this output.

14.0 MISCELLANEOUS

14.1 INTRP_N Output

- The **INTRP_N** pin is the interrupt output. It is active-low and requires an external 1.0 kΩ to 4.7 kΩ pull-up resistor to the KSZ989x/KSZ956x/KSZ9477 **VDDIO** power rail. If it is not used, then the pull-up is not needed.

14.2 PME_N Output

- The **PME_N** pin output provides the Power Management Event (PME) interrupt output for the Wake-on-LAN (WoL) function. When the **PME_N** pin is asserted, it indicates that the KSZ989x/KSZ956x/KSZ9477 device has detected an energy event and is outputting the interrupt to wake up the system from a Low-power mode.
- The **PME_N** asserted polarity is programmable. (Default is active-low.) An external pull-up resistor is required for active-low operation. An external pull-down resistor is required for active-high operation. For both cases, the external resistor value is 1.0 kΩ to 4.7 kΩ. If it is not used, then the pull-up is not needed.

14.3 EMI Considerations

- Use chassis ground and incorporate a large SMD footprint (SMD_1210) to connect the chassis ground to the digital ground. This will allow some flexibility at EMI testing for different grounding options. Leaving the footprint open will allow the two grounds to remain separate. Shorting them together with a zero-ohm resistor will connect them. For best performance, short them together with a cap or a ferrite bead.

Note:	Ensure that the switching DC-DC converter is filtered and properly shielded as the DC-DC power converter can produce a great deal of EMI noise.

- When an MII, RMII, and RGMII ports are not used, they can be configured in MII PHY mode, RMII clock output mode, or RGMII mode, so the MAC TX block can work without an external clock input. This is fine because frames destined to those unused ports will not cumulate in the switch buffer. However, one disadvantage of this solution is the switch outputs a MII/RMII/RGMII clock which can be an additional source of emissions. To minimize emissions, do not connect a trace to the output clock pin(s). Another solution is to disable frame forwarding to the unused port through register settings which is mentioned in Section 8.1, "Unused MAC Ports".
- It is also recommended to place series termination resistors on all **MII/RMII/RGMII** output pins. Combined with the output pin impedance, these series resistors provide the means to tune and match the PCB trace impedance to minimize ringing, and thus improve signal integrity and reduce EMI. The typical resistor value ranges from 22Ω to 50Ω with the optimum value being dependent on the board layout. Disable output clock on **CLKO_25_125** or **SYNCLKO** pins through register settings if they are not needed.

15.0 HARDWARE CHECKLIST SUMMARY

TABLE 15-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet. Ensure that pin type is compatible with all pins between the KSZ989x/KSZ956x/KSZ9477 family devices and interfacing components. (For example, ensure that one chip is not connected to the input of another chip.)		
		Ensure that the intended pin strapping is selected. Add external pull-ups/pull-downs (as needed) to prevent connecting components from overriding the intended high/low value.		
Section 3.0, "Power/Ground Connections"	Section 3.1, "Power and Ground Block Diagram"	Check power/ground connections. Use Figure 3-1 for switches without SGMII and Figure 3-2 for switches with SGMII.		
	Section 3.2, "Power Pins"	Ensure that each power pin has a 0.1 µF decoupling capacitor and each power rail (**AVDDH**, **VDDIO**, **AVDDL**, **DVDDL**, **VDDLS**, and **VDDHS**) has sufficient bulk storage capacitance for less than 50 mVp-p ripple. Use ferrite beads to provide further filtering for analog power rails (**AVDDH** and **AVDDL**).		
	Section 3.3, "Ground Pin and Exposed Pad"	Ensure that the ground pins and exposed pad are tied directly to a common ground plane. Use the recommended land pattern and thermal vias for the exposed pad.		
Section 4.0, "Reference Clock Circuits and Connections"	Section 4.1, "Crystal Circuit"	If selected, follow the crystal circuit recommendation and crystal specifications (25 MHz, +/–50 ppm, less than 100 ps total period jitter peak-to-peak).		
	Section 4.2, "External Clock Source/ Oscillator Circuit"	If selected, follow the external clock/oscillator recommendation and clock specifications (25 MHz, +/–50 ppm, less than 100 ps total period jitter peak-to-peak).		
Section 5.0, "ISET Resistor"		Ensure that the resistor value is 6.04 kΩ, 1% and is placed close to the **ISET** pin.		

TABLE 15-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 6.0, "Ethernet PHY Ports"	Section 6.1, "Unused PHY Ports"	Ensure that all eight pins are unconnected if a PHY port is unused.		
	Section 6.2, "Magnetics Selection"	Ensure that the selected magnetic has separated center taps for the four differential pairs on the KSZ989x/KSZ956x/ KSZ9477 family device side.		
	Section 6.3, "10/100/1000 Mbps (Gigabit) Ethernet Interface"	If selected, ensure that the magnetic and RJ45 connections match Figure 6-1.		
		Ensure that no external termination is placed on the differential signals for the PHY ports and the magnetic center taps on the KSZ989x/KSZ956x/KSZ9477 family devices side are not shorted together and not connected to any external power rail.		
	Section 6.4, "10/100 Mbps Ethernet Only"	If selected, ensure that the magnetic and RJ45 connections match Figure 6-2.		
		Ensure that no external termination is placed on the differential signals for the PHY ports and the magnetic center taps on the KSZ989x/KSZ956x/KSZ9477 family devices side are not shorted together and not connected to any external power rail.		
	Section 6.5, "Chassis Ground"	Use chassis ground for the connector shield and line-side terminations. Incorporate a large SMD footprint to connect the chassis ground to the digital ground.		
	Section 6.6, "Capacitive Coupling Option"	Check if pull-ups are required by the link partner (needed for Current mode line driver).		
Section 7.0, "Management Bus"	Section 7.1, "SPI Client Management"	If selected, ensure that pin strapping and **SPI** pin connections match Figure 7-1.		
	Section 7.2, "I^2C Client Management"	If selected, ensure that pin strapping and **I^2C** pin connections match Figure 7-2.		
	Section 7.3, "In-Band Access (IBA) Management"	If selected, ensure that pin strapping and **IBA** pin connections match Figure 7-3. Disable IBA through pin strapping if it is not used.		
	Section 7.4, "MII Management (MIIM)"	If selected, ensure that pin strapping and **MIIM** pin connections match Figure 7-4. Note that MIIM is limited to PHY register access only.		

TABLE 15-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 8.0, "Parallel MAC Interfaces"	Section 8.1, "Unused MAC Ports"	Strap unused MAC ports to MII PHY mode, RMII clock output mode, or RGMII mode if RF emission is not a big concern. Strap unused MAC ports to MII MAC or RMII Clock Input mode with register settings to disable frame forwarding towards them.		
	Section 8.2, "RGMII Interface" and Section 8.2.1, "RGMII Functional Configuration"	If selected, determine the KSZ989x/KSZ956x/KSZ9477 RGMII functional configuration (RGMII-ID mode, Hybrid mode, or RGMII mode) to be used with the external RGMII device using Figure 8-1.		
	Section 8.2.2, "RGMII Skew Calculation"and Section 8.2.3, "RGMII Interface with External RGMII Device"	If selected, determine the RGMII skew using Figure 8-2. Ensure that RGMII connections match either Figure 8-3 or Figure 8-4.		
	Section 8.3, "RMII (Clock Mode) Interface"	If selected, ensure that RMII connections match Figure 8-5.		
	Section 8.4, "RMII (Normal Mode) Interface"	If selected, ensure that RMII connections match Figure 8-6.		
	Section 8.5, "MII (PHY Mode) Interface"	If selected, ensure that MII connections match Figure 8-7.		
	Section 8.6, "MII (MAC Mode) Interface"	If selected, ensure that MII connections match Figure 8-8.		
	Section 8.7, "GMII (PHY Mode) Interface"	If selected, ensure that GMII connections match Figure 8-9.		
	Section 8.8, "GMII (MAC Mode) Interface"	If selected, ensure that GMII connections match Figure 8-10.		
Section 9.0, "Serial MAC Interface"	Section 9.1, "SGMII Connection to PHY or MAC Devices"	If selected, ensure that SGMII/SerDes connections match Figure 9-1.		
	Section 9.2, "1000Base-X SerDes Connection to SFP Modules"	If selected, ensure that SGMII/SerDes connections match Figure 9-2.		
Section 10.0, "LED Indicator Pins"	Section 10.1, "PHY Port LED Status and Pin Strapping – for VDDIO = 3.3V or 2.5V"	If selected, ensure that LED connections match Figure 10-1.		
	Section 10.2, "PHY Port LED Status and Pin Strapping – for VDDIO = 1.8V"	If selected, ensure that LED connections match Figure 10-2.		
Section 11.0, "GPIO Pin (for KSZ9567R, KSZ9567S, and 9477 that support 1588)"		Ensure that **GPIO** pins are used only for PTP output event trigger or input timestamp capture. Remember that general purpose input/output usage is not supported.		
Section 12.0, "CLKO_25_125 Pin (for KSZ9897R, KSZ9897S, and KSZ9896)"		Check data sheet to enable or disable the **CLKO_25_125** pin through register settings.		
Section 13.0, "SYNCLKO (for KSZ9567R, KSZ9567S, and KSZ9477 that support SYNCE)"		Check data sheet to enable or disable SYNCLKO through register settings.		

TABLE 15-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 14.0, "Miscellaneous"	Section 14.1, "INTRP_N Output"	If used, ensure there is a 1.0 kΩ to 4.7 kΩ pull-up resistor to the **VDDIO** power rail.		
	Section 14.2, "PME_N Output"	If used, ensure that there is a 1.0 kΩ to 4.7 kΩ resistor pulled-up to the **VDDIO** power rail for active low or pulled-down to ground for active-high.		
	Section 14.3, "EMI Considerations"	Incorporate a large SMD footprint (SMD_1210) to connect the chassis ground to the digital ground and disable unwanted clock output through register settings.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004151A (08-20-21)	Initial release	

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