AN1565

Configuring and Using the WDT Module of MCP795WXX Real-Time Clock/Calendars

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INTRODUCTION

This application note is designed to take the design engineer through the steps needed to configure and setup the Watchdog Timer (WDT) module of Microchip SPI MCP795WXX Real-Time Clock/Calendar (RTCC) family. Topics covered include:

- Configuring the WDT module
- Using the WDT module
- Overview of the provided drivers/libraries

The information presented in this document is designed serve as an example of possible configurations. The code supplied can be modified to change the device functionality.

This application note should be read in conjunction with the application note AN1365 – *"Recommended Usage of Microchip Serial RTCC Devices"* (DS 00001365) and the device data sheet. The latest documentation can be found at this location on the Microchip website: http://www.microchip.com/rtcc.

WHAT IS THE WDT MODULE?

A WDT is an electronic module that performs a specific task (such as generating an interrupt) after a programmed period of time, if a critical event does not appear before the end of the delay period. WDTs are most commonly used to detect when the software enters an unintended operation and then helps it recover.

If the software cannot clear the WDT in time, it is usually because two parts or programs conflict, a process is stuck, or an important event did not occur in time.

A WDT has a digital counter that counts up to its programmed limit. If the software loop does not clear the WDT at regular intervals of time (shorter than the WDT period), the WDT will launch an interrupt, forcing/resetting the system to a known state.

The Watchdog Timer in the MCP795WXX is a free-running counter that operates from the crystal. This counter is independent of the time and date counters and can be used to generate an interrupt after a programmable period of time.

The counter can be reset at any time using either an SPI bus command or by toggling an external pin (EVHS), if configured. Note that using the EVHS pin in this manner prevents the use of the high-speed event detect feature.

SCHEMATIC DIAGRAM

The schematic illustrated in Figure 1 shows the minimum components required to operate the RTCC.

The schematic also shows the required components for battery backup operation using a lithium coin cell (for other options refer to AN1365). If the V_{BAT} input and battery backup feature are not required, this pin should be tied to V_{SS}.

The SPI RTCC is directly connected to the MSSP1 module of the PIC18 MCU. There is an additional connection between the $\overline{WDO}$ signal of the RTCC and the RB2/INT2 pin of the MCU. The RTCC is selected through the RC2 GPIO of the MCU.

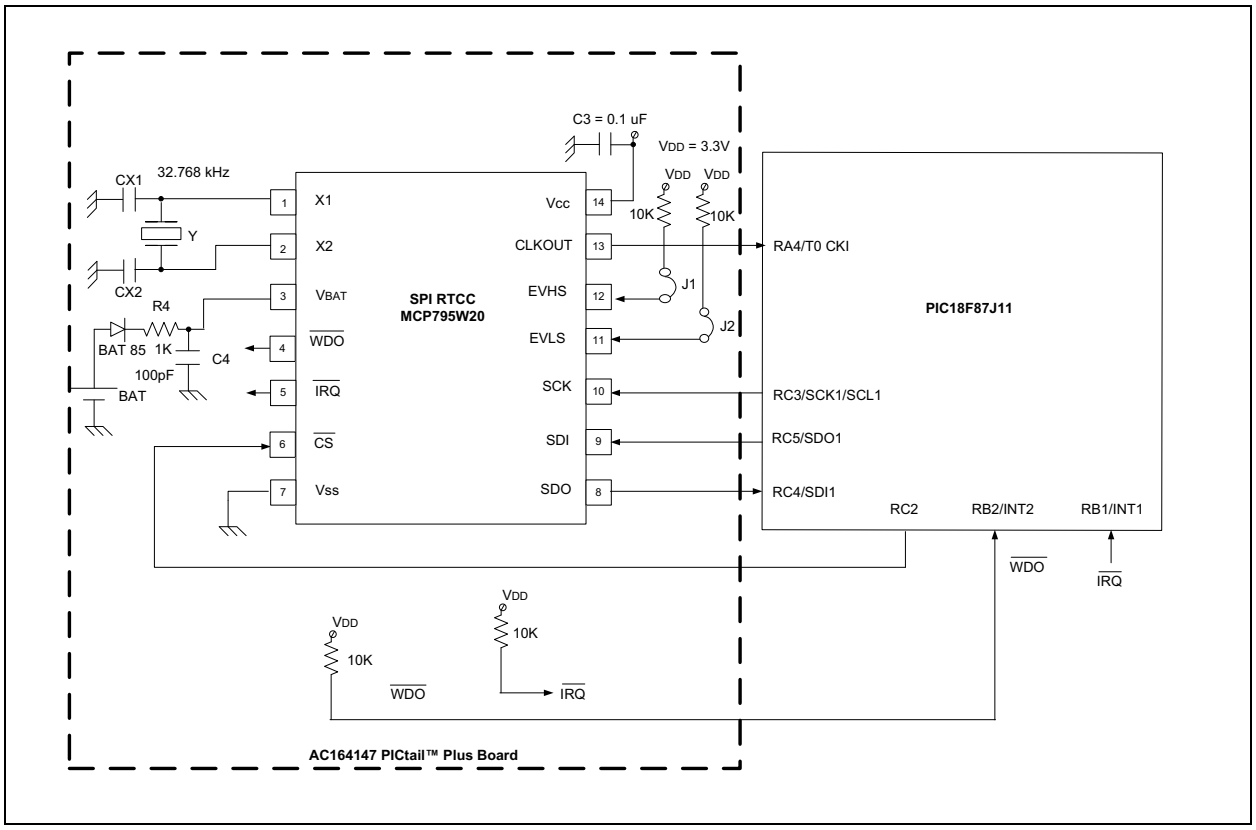
In the provided code, the following signal is defined:

```
#define NCS_SPI_RTCC PORTCbits.RC2
// CS for the SPI RTCC.
```

The RTCC offers interrupts at a programmed time interval on the $\overline{WDO}$ pin, connected to the INT2 pin (external hardware interrupt 2) of the MCU. The related interrupt functions are used and described in the main function.

The easiest way to start the project is by using the related SPI RTCC PICtail™ Plus Board (AC164147).

FIGURE 1: SCHEMATIC



FIRMWARE OVERVIEW

The host MCU will communicate with the RTCC using the SPI protocol, based on the MSSP1 serial module of the PIC18 MCU.

The code presented with this application note is designed to compile with the XC8 (V 1.34) compiler and MPLAB® X IDE (V3.55) for the following hardware:

- Explorer 18 Evaluation Board (DM183032)
- PIC18F87J11 PIM Module (MA180020)
- RTCC SPI PICtail Module (AC164147)

The code is presented in C and is portable with minimal effort to other PIC© MCU devices. This code is designed to be a starting point for application development and is based on the drivers/libraries presented in this text and the related code.

APPLICATION DESCRIPTION

The code presents the basics of the WDT's configuration and usage. After initializing the RTCC and the WDT, the code displays the value of the WDT register in binary on LEDs. The code then waits for the time-out period to expire, at which point all of the LEDs are turned on to indicate that the WDT has triggered.

CONFIGURATION OF THE WDT MODULE

TABLE 1: WATCHDOG REGISTER

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
WDTEN	WDTIF	WDTDLYEN	WDTPWS	WDTPS3	WDTPS2	WDTPS1	WDTPS0
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’

bit 7 **WDTEN:** Watchdog Timer Enable bit
This is a read/write bit that is set by the user and can be cleared by the user of the hardware. This bit is set to enable the WDT function and cleared to disable the function. This bit is cleared by the hardware when the VCC supply is not present, it is not set again when VCC is present.

bit 6 **WDTIF:** Watchdog Timer Interrupt Flag bit
This is a read/write bit that is set in hardware when the WDT times out and the WD pin is asserted. This bit must be cleared in software to restart the WDT.

bit 5 **WDTDLYEN:** Watchdog Timer Delay bit
This is a read/write bit and is set to enable a 64-second delay before the WDT starts to count. If this bit is set and the WDTIF bit is cleared then there will be a 64 second delay before the WDT starts to count. This bit should be set before the WDTEN bit is set.

bit 4 **WDTPWS:** Watchdog Timer Reset Pulse Width bit
This is a read/write bit that is used to select the pulse width on the WD pin when the WDT times out.
0 = 122 µs Pulse
1 = 125 ms Pulse

bit 3-0 **WDTPS<3:0>:** Watchdog Timer Configuration bits
These are read/write bits that are used to set the WDT time-out period as below (all times are based off the uncalibrated crystal reference). Bit 3 should be cleared and is reserved for future use:
000 = 977 µs
001 = 15.6 ms
010 = 62.5 ms
011 = 125 ms
100 = 1s
101 = 16s
110 = 32s
111 = 64s

To program the register, several masks were used, as shown in Example 1:

EXAMPLE 1:

```
#define WDTEN          0x80            // WDT enable bit
#define WDTDLYEN       0x20            // enable WDT delay
#define WDTIF          0x40            // WDT interrupt flag
#define WDTPWS         0x10            // WDT pulse-width: 125 ms
                                       // (0 value -> 122 µs)
                                       // WDT time-out periods
#define WDT_TOP_00     0x00            // 977 µs
#define WDT_TOP_01     0x01            // 15.625 ms
#define WDT_TOP_02     0x02            // 62.5 ms
#define WDT_TOP_03     0x03            // 125 ms
#define WDT_TOP_04     0x04            // 01 sec
#define WDT_TOP_05     0x05            // 16 sec
#define WDT_TOP_06     0x06            // 32 sec
#define WDT_TOP_07     0x07            // 64 sec
#define WDTCON         0x0a            // the address of the WDT register
```

A representation of how to initialize the WDT register is shown in Example 2:

EXAMPLE 2:

```
spi_rtcc_wr(WDTCON, WDTEN + WDTDLYEN + WDTPWS + WDT_TOP_00)
```

Table 2 presents all possible combinations of period and pulse width values, depending on the bits: WDTDLYEN, WDTPWS, WDTPS<3:0> bits, included in the Watchdog register.

TABLE 2:

WDTDLYEN	WDTPWS	WDTPS<3:0>	Total Period	Pulse Width
0	0	0-7	977 µsec, 15.625 msec, …….. , 64 sec	122 µsec
0	1	4-7(1)	1 sec, 16 sec, 32 sec, 64 sec	125 msec
1	0	0-7	64 sec + [977 µsec, 15.625 msec,.., 64 sec]	122 µsec
1	1	0-7	64 sec + [977 µsec, 15.625 msec,.., 64 sec]	125 msec

Note 1: The user must ensure that the WDT period is longer than the pulse width. For example, if the pulse width is 125 msec and the delay is '0', the WDT time-out period must be longer than one second.

RE-ENABLING THE WDT

To allow repetitive interrupts (coming from the WDT), the related WDT interrupt flag must be cleared after every action. Two methods could be used:

- Write the initial configuration value again
  `spi_rtcc_wr(WDTCON, wdt_mask);`

`// including WDTEN=1, WDTIF = 0;`

- Clear only the interrupt flag
  `rtcc_buff=spi_rtcc_rd(WDTCON);`

`spi_rtcc_wr(WDTCON,(rtcc_buf&~WDTIF));`

CLEARING THE WDT

When the state of the WDT counter is unknown, or whenever a WDT time out and subsequent interrupt are not desired, the WDT counter must be cleared. This is performed using the MCP795WXX's CLRWDT command. The related `#define directive` is shown in Example 3, while Example 4 shows the function in the provided code that executes the CLRWDT command.

EXAMPLE 3:

```
#define  SPI_RTCC_CLRWDT   0x44       // SPI CLEAR WDT  COMMAND
```

EXAMPLE 4:

```
void spi_rtcc_clw(void){              // clear WD timer/counter
spi_rtcc_start()               ;      // START SPI COMMUNICATION
spi_wrbyte(SPI_RTCC_CLRWDT)    ;      // launch the CLEAR WDT command
spi_rtcc_stop()                ;  }   // stop SPI COMMUNICATION
```

CONCLUSION

Following the steps in this application note, along with the included MPLAB X IDE project, will help setup the basic configuration and usage of the WDT module available on the Microchip MCP795WXX SPI RTCC. By using available off-the-shelf development tools, any hardware issues will be mitigated, allowing the engineer to concentrate on the firmware development.

The code is presented in C (XC8-V1.34 compiler on MPLAB X IDE-V3.55) and can easily be ported to other PIC device platforms.

APPENDIX A: MAIN FUNCTION OF THE WDT TEST/USAGE CODE

```
wdt_mask = WDTPWS+WDT_TOP_05       ; // mask to write in the WDT register
                                     // PLS = 125 msec ; period = 16 sec
                                    // you may write any other combination presented
                                     // in the text of the application note
wdt_mask |= WDTEN                  ; // enable the WDT
LATD = wdt_mask                    ; // display the control byte on LEDs
num_per = 0x00                     ; // init the counter of WDT periods
ini_spi_rtcc()                     ; // init the SPI RTCC
spi_rtcc_wr(WDTCON,wdt_mask)       ; // set the WDT register, enabling the module
ini_wdt_int2()                     ; // init   INTR2 on PIC18 (for the WDT)
start_wdt_int2()                   ; // enable INTR2 on PIC18 (for the WDT)
while(num_per==0) {;}                // waiting the first interrupt from WDT
stop_wdt_int2()                    ; // stop interrupts from WDT / RTCC
spi_rtcc_wr(WDTCON,0x00)           ; // clear WDT register, disable WDT.
LATD = 0xff                        ; // message for the end of the WDT period
while(1) { ; }                       // loop for ever
```

APPENDIX B: DRIVERS LIBRARY

Delay Drivers (`delay_drivers.h`)

Not accessed in the present project. Used by the LCD drivers or as general purpose timing functions.

Represent a good starting point for further development on PIC18-based projects, as they use the timers of the MCU (see AN1355, AN1364, AN1413 for the usage of these drivers).

LCD Drivers (`lcd_drivers.h`)

Not accessed in the present project. Represent a good starting point on Explorer18-based projects (see AN1355, AN1364, AN1413 for the usage of these drivers).

SPI Drivers (`spi_drivers.h`)

Represent the low-level communication between the MSSP1 module of the PIC18 and the SPI RTCC.

The related functions will be detailed in the next paragraph, as called functions.

SPI RTCC Drivers (`spi_rtcc_drivers.h`)

Represent the medium-level communication between the MSSP1 module of the PIC18 and the SPI RTCC.

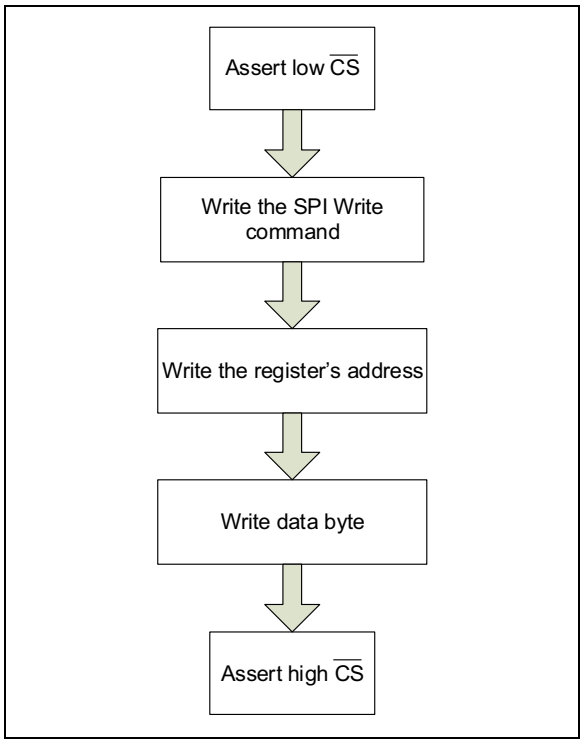
The related functions call the SPI drivers, as described below. Moreover, the library defines all necessary constants, as register addresses and masks.

EXAMPLE 5: WRITING A BYTE TO THE SPI RTCC

```
void spi_rtcc_wr (unsigned char rtcc_reg, unsigned char time_var){
                                          // SPI write to the SPI RTCC
spi_rtcc_start()                        ;   // start SPI comm with the SPI RTCC
spi_wrbyte(SPI_RTCC_WRITE)              ;   // send the SPI WRITE command
spi_wrbyte(rtcc_reg)                    ;   // send the register's address
spi_wrbyte(time_var)                    ;   // send the SPI data byte
spi_rtcc_stop()                         ; } // stop SPI comm
```

The firmware for writes to the RTCC follows in Example 6.

EXAMPLE 6:

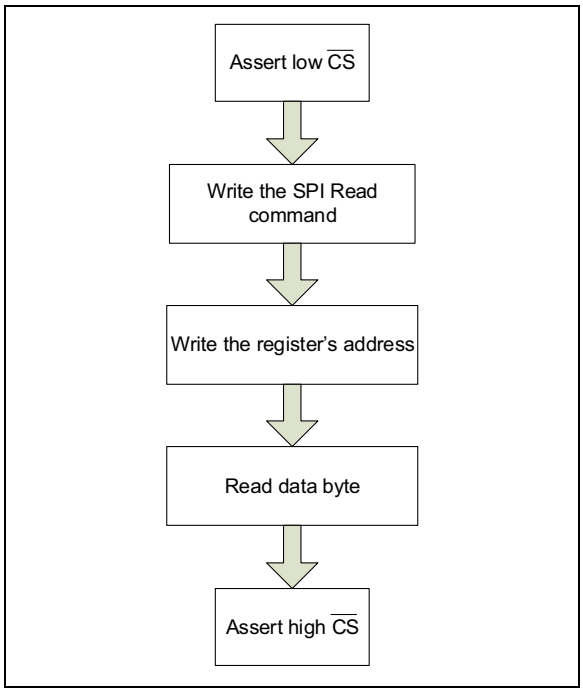


EXAMPLE 7: READING A BYTE FROM THE SPI RTCC

```
unsigned char spi_rtcc_rd(unsigned char rtcc_reg){
                                              // SPI read from the SPI RTCC
spi_rtcc_start()                            ;  // start the SPI comm with the SPI RTCC
spi_wrbyte(SPI_RTCC_READ)                   ;  // send the SPI READ command
spi_wrbyte(rtcc_reg)                        ;  // send the register's address
rtcc_buf = spi_rdbyte()                     ;  // read the result and store it
spi_rtcc_stop()                             ;  // stop the SPI comm with the SPI RTCC
return rtcc_buf                             ;} // return the read result
```

The firmware for reads from the RTCC is shown in Example 8.

EXAMPLE 8:



APPENDIX C: REVISION HISTORY

Revision A (09/2013)

Initial release of this document.

Revision B (10/2017)

Updated register and bit names.

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