Section 54. Comparator with Blanking

HIGHLIGHTS

This section of the manual contains the following major topics:

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Note:	This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33F/PIC24H devices. Please consult the note at the beginning of the **"Comparator"** chapter in the current device data sheet to check whether this document supports the device you are using. Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com

54.1 INTRODUCTION

The dsPIC33F/PIC24H Comparator with Blanking module provides multiple comparators that can be configured in different ways. The individual comparator options are specified by the Comparator with Blanking module's Special Function Register (SFR) control bits. The SFRs control bits associated with Comparator with Blanking module allow users to:

- Select the edge for trigger and interrupt generation
- Select low-power control
- Configure the comparator voltage reference and band gap
- Configure output blanking and masking

The comparator operating mode is determined by the input selections (that is, whether the input voltage is compared to a second input voltage, to an internal voltage band gap reference, or to an internal reference voltage). The internal reference voltage is generated by a resistor ladder network that is configured by the Comparator Voltage Reference Control register (CVRCON).

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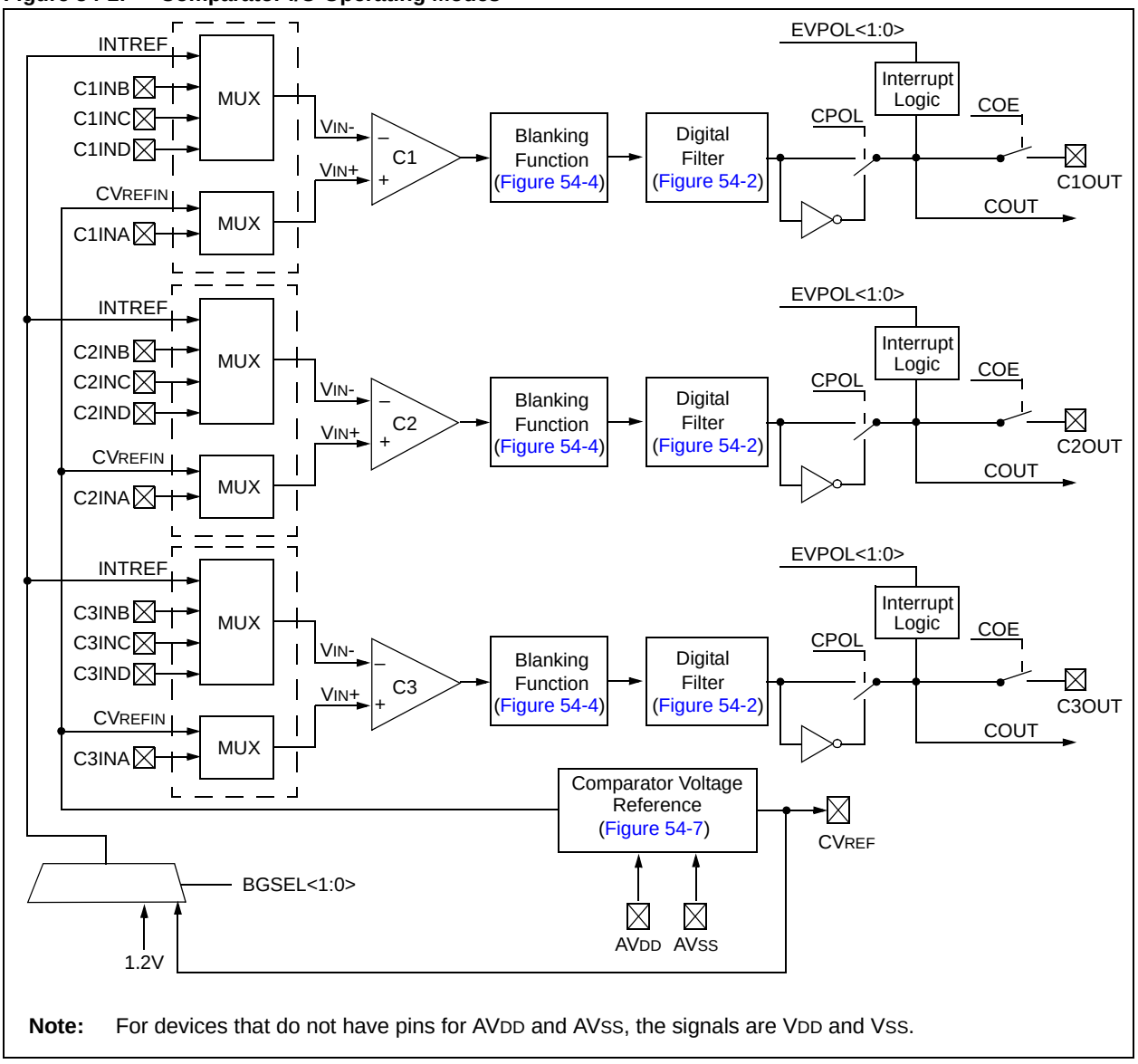
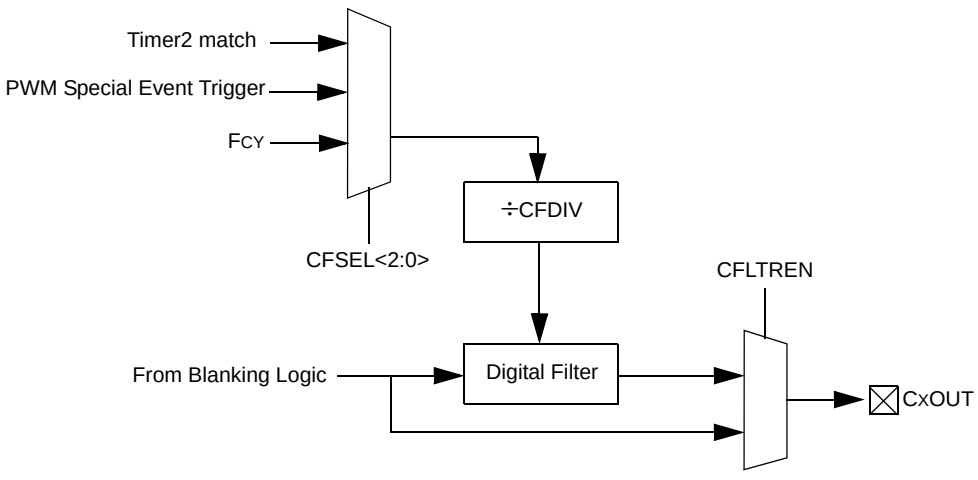
Figure 54-1: Comparator I/O Operating Modes



Note: For devices that do not have pins for AVDD and AVSS, the signals are VDD and VSS.

Figure 54-2: Digital Filter Interconnect Block Diagram



54.2 COMPARATOR REGISTERS

The Comparator with Blanking module uses the following registers:

- **CMSTAT: Comparator Status Register**

  This register enables control over the operation of all comparators when the device enters Idle mode. It also provides the status of all comparator results, as well as all of the comparator outputs and event bits, which are replicated as read-only bits.

- **CMxCON: Comparator Control Register (x = 1, 2 or 3)**

  This register allows the application program to enable, configure and interact with the individual comparators.

- **CMxMSKSRC: Comparator Mask Source Select Control Register**

  This register allows the application program to select sources for the inputs for the blanking function.

- **CMxMSKCON: Comparator Mask Gating Control Register**

  This register allows the application program to specify the blank function logic.

- **CMxFLTR: Comparator Filter Control Register**

  This register enables comparator filter configuration.

- **CVRCON: Comparator Voltage Reference Control Register**

  This register allows the application program to enable, configure and interact with the comparator internal voltage reference generator. For more information, see **54.6 “Comparator Voltage Reference Generator”**.

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Register 54-1: CMSTAT: Comparator Status Register

R/W-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
CMSIDL	—	—	—	—	C3EVT	C2EVT	C1EVT
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
—	—	—	—	—	C3OUT	C2OUT	C1OUT
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CMSIDL:** Stop in Idle Mode bit
1 = All comparators continue to operate but do not generate interrupts in Idle mode
0 = All comparators continue to operate and generate interrupts in Idle mode

bit 14-11 **Unimplemented:** Read as '0'

bit 10 **C3EVT:** Comparator 3 Event Status bit
1 = Comparator event occurred
0 = Comparator event did not occur

bit 9 **C2EVT:** Comparator 2 Event Status bit
1 = Comparator event occurred
0 = Comparator event did not occur

bit 8 **C1EVT:** Comparator 1 Event Status bit
1 = Comparator event occurred
0 = Comparator event did not occur

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **C3OUT:** Comparator 3 Output Status bit
When CPOL = 0:
1 = VIN+ > VIN-
0 = VIN+ < VIN-

When CPOL = 1:
1 = VIN+ < VIN-
0 = VIN+ > VIN-

bit 1 **C2OUT:** Comparator 2 Output Status bit
When CPOL = 0:
1 = VIN+ > VIN-
0 = VIN+ < VIN-

When CPOL = 1:
1 = VIN+ < VIN-
0 = VIN+ > VIN-

bit 0 **C1OUT:** Comparator 1 Output Status bit
When CPOL = 0:
1 = VIN+ > VIN-
0 = VIN+ < VIN-

When CPOL = 1:
1 = VIN+ < VIN-
0 = VIN+ > VIN-

Register 54-2: CMxCON: Comparator Control Register (x = 1, 2 or 3)

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R-0
CON	COE	CPOL	—	—	—	CEVT	COUT
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CON:** Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled

bit 14 **COE:** Comparator Output Enable bit
1 = Comparator output is present on the CxOUT pin
0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **CEVT:** Comparator Event bit
1 = Comparator event according to EVPOL<1:0> settings occurred; disables future triggers and interrupts until the bit is cleared
0 = Comparator event did not occur

bit 8 **COUT:** Comparator Output bit
When CPOL = 0 (non-inverted polarity):
1 = $V_{IN+} > V_{IN-}$
0 = $V_{IN+} < V_{IN-}$
When CPOL = 1 (inverted polarity):
1 = $V_{IN+} < V_{IN-}$
0 = $V_{IN+} > V_{IN-}$

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits
11 = Trigger/Event/Interrupt generated on any change of the comparator output (while CEVT = 0)
10 = Trigger/Event/Interrupt generated only on high to low transition of the polarity-selected comparator output (while CEVT = 0)
If CPOL = 1 (inverted polarity):
Low-to-high transition of the comparator output
If CPOL = 0 (non-inverted polarity):
High-to-low transition of the comparator output
01 = Trigger/Event/Interrupt generated only on low to high transition of the polarity-selected comparator output (while CEVT = 0)
If CPOL = 1 (inverted polarity):
High-to-low transition of the comparator output
If CPOL = 0 (non-inverted polarity):
Low-to-high transition of the comparator output
00 = Trigger/Event/Interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

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Register 54-2: CMxCON: Comparator Control Register (x = 1, 2 or 3) (Continued)

bit 4	**CREF:** Comparator Reference Select bit (V_{IN}+ input) 1 = V_{IN}+ input connects to internal CV_{REFIN} voltage 0 = V_{IN}+ input connects to CxINA pin
bit 3-2	**Unimplemented:** Read as '0'
bit 1-0	**CCH<1:0>:** Comparator Channel Select bits 11 = V_{IN}- input of comparator connects to INTREF 10 = V_{IN}- input of comparator connects to CxIND pin 01 = V_{IN}- input of comparator connects to CxINC pin 00 = V_{IN}- input of comparator connects to CxINB pin

Register 54-3: CMxMSKSRC: Comparator Mask Source Select Control Register

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	RW-0
—	—	—	—	SELSRCC<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SELSRCB<3:0>				SELSRCA<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as ‘0’

bit 11-8 **SELSRCC<3:0>:** Mask C Input Select bits

1111 = Reserved
1110 = Reserved
•
•
•
0111 = Reserved
0110 = Reserved
0101 = PWM1H3
0100 = PWM1L3
0011 = PWM1H2
0010 = PWM1L2
0001 = PWM1H1
0000 = PWM1L1

bit 7-4 **SELSRCB<3:0>:** Mask B Input Select bits

1111 = Reserved
1110 = Reserved
•
•
•
0111 = Reserved
0110 = Reserved
0101 = PWM1H3
0100 = PWM1L3
0011 = PWM1H2
0010 = PWM1L2
0001 = PWM1H1
0000 = PWM1L1

bit 3-0 **SELSRCA<3:0>:** Mask A Input Select bits

1111 = Reserved
1110 = Reserved
•
•
•
0111 = Reserved
0110 = Reserved
0101 = PWM1H3
0100 = PWM1L3
0011 = PWM1H2
0010 = PWM1L2
0001 = PWM1H1
0000 = PWM1L1

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Register 54-4: CMxMSKCON: Comparator Mask Gating Control Register

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **HLMS:** High or Low Level Masking Select bits
1 = The masking (blanking) function will prevent any asserted ('0') comparator signal from propagating
0 = The masking (blanking) function will prevent any asserted ('1') comparator signal from propagating

bit 14 **Unimplemented:** Read as '0'

bit 13 **OCEN:** OR Gate C Input Inverted Enable bit
1 = MCI is connected to OR gate
0 = MCI is not connected to OR gate

bit 12 **OCNEN:** OR Gate C Input Inverted Enable bit
1 = Inverted MCI is connected to OR gate
0 = Inverted MCI is not connected to OR gate

bit 11 **OBEN:** OR Gate B Input Inverted Enable bit
1 = MBI is connected to OR gate
0 = MBI is not connected to OR gate

bit 10 **OBNEN:** OR Gate B Input Inverted Enable bit
1 = Inverted MBI is connected to OR gate
0 = Inverted MBI is not connected to OR gate

bit 9 **OAEN:** OR Gate A Input Enable bit
1 = MAI is connected to OR gate
0 = MAI is not connected to OR gate

bit 8 **OANEN:** OR Gate A Input Inverted Enable bit
1 = Inverted MAI is connected to OR gate
0 = Inverted MAI is not connected to OR gate

bit 7 **NAGS:** Negative AND Gate Output Select
1 = Inverted ANDI is connected to OR gate
0 = Inverted ANDI is not connected to OR gate

bit 6 **PAGS:** Positive AND Gate Output Select
1 = ANDI is connected to OR gate
0 = ANDI is not connected to OR gate

bit 5 **ACEN:** AND Gate A1 C Input Inverted Enable bit
1 = MCI is connected to AND gate
0 = MCI is not connected to AND gate

bit 4 **ACNEN:** AND Gate A1 C Input Inverted Enable bit
1 = Inverted MCI is connected to AND gate
0 = Inverted MCI is not connected to AND gate

bit 3 **ABEN:** AND Gate A1 B Input Inverted Enable bit
1 = MBI is connected to AND gate
0 = MBI is not connected to AND gate

Register 54-4: CMxMSKCON: Comparator Mask Gating Control Register (Continued)

bit 2 **ABNEN:** AND Gate A1 B Input Inverted Enable bit
1 = Inverted MBI is connected to AND gate
0 = Inverted MBI is not connected to AND gate

bit 1 **AAEN:** AND Gate A1 A Input Enable bit
1 = MAI is connected to AND gate
0 = MAI is not connected to AND gate

bit 0 **AANEN:** AND Gate A1 A Input Inverted Enable bit
1 = Inverted MAI is connected to AND gate
0 = Inverted MAI is not connected to AND gate

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Register 54-5: CMxFLTR: Comparator Filter Control Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	I-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-4 **CFSEL<2:0>:** Comparator Filter Input Clock Select bits
111 = Reserved
110 = Reserved
101 = Reserved
100 = Reserved
011 = Reserved
010 = Timer2 Match(1)
001 = PWM Special Event Trigger(2)
000 = Instruction Clock (FCY)(3)

bit 3 **CFLTREN:** Comparator Output Digital Filter Enable bit
1 = Digital filter enabled
0 = Digital filter disabled

bit 2-0 **CFDIV<2:0>:** Comparator Output Filter Clock Divide Select bits
111 = Clock Divide 1:128
110 = Clock Divide 1:64
101 = Clock Divide 1:32
100 = Clock Divide 1:16
011 = Clock Divide 1:8
010 = Clock Divide 1:4
001 = Clock Divide 1:2
000 = Clock Divide 1:1

Note 1: For more information, refer to the **"Timers"** chapter in the specific device data sheet, or refer to **Section 11. "Timers"** (DS70205) in the *"dsPIC33F/PIC24H Family Reference Manual"*.

2: For more information, refer to the **"Motor Control PWM"** chapter in the specific device data sheet, or refer to **Section 14. "Motor Control PWM"** (DS70187) in the *"dsPIC33F/PIC24H Family Reference Manual"*.

3: For more information, refer to the **"Oscillator"** chapter in the specific device data sheet, or refer to **Section 7. "Oscillator"** (DS70186) in the *"dsPIC33F/PIC24H Family Reference Manual"*.

Register 54-6: CVRCON: Comparator Voltage Reference Control Register

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	VREFSEL	BGSEL<1:0>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVREN	CVROE(1)	CVRR	CVRSS	CVR<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **VREFSEL:** Voltage Reference Select bit
1 = CVREFIN = CVREF pin
0 = CVREFIN is generated by the resistor network

bit 9-8 **BGSEL<1:0>:** Band Gap Reference Source Select bits
11 = INTREF = CVREF pin
10 = INTREF = 1.2V (nominal)
01 = Reserved
00 = Reserved

bit 7 **CVREN:** Comparator Voltage Reference Enable bit
1 = Comparator voltage reference circuit powered on
0 = Comparator voltage reference circuit powered down

bit 6 **CVROE:** Comparator Voltage Reference Output Enable bit(1)
1 = Voltage level is output on CVREF pin
0 = Voltage level is disconnected from CVREF pin

bit 5 **CVRR:** Comparator Voltage Reference Range Selection bit
1 = CVRSRC/24 step size
0 = CVRSRC/32 step size

bit 4 **CVRSS:** Comparator Voltage Reference Source Selection bit
1 = Comparator voltage reference source, $CVRSRC = (VREF+) - (VREF-)$(2)
0 = Comparator voltage reference source, $CVRSRC = AVDD - AVSS$

bit 3-0 **CVR<3:0>** Comparator Voltage Reference Value Selection bits
When CVRR = 1:
$CVREFIN = (CVR<3:0>/24) * (CVRSRC)$
When CVRR = 0:
$CVREFIN = 1/4 \cdot (CVRSRC) + (CVR<3:0>/32) * (CVRSRC)$

Note 1: The CVROE bit overrides the TRIS bit setting.

2: Selecting BGSEL<1:0> = 11 and CVRSS = 1 is invalid and will produce unpredictable results.

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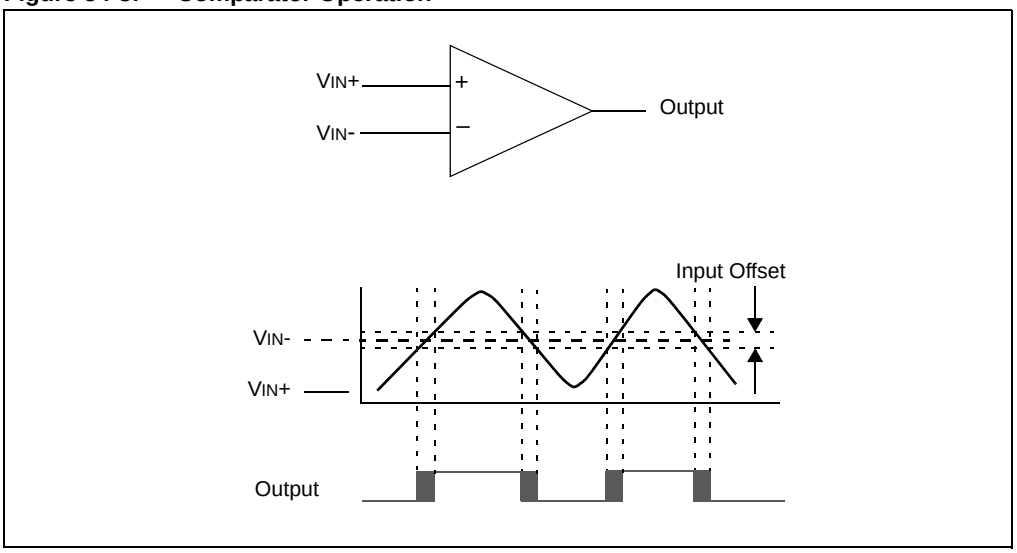
54.3 COMPARATOR OPERATION

The operation of a typical comparator, along with the relationship between the analog input levels and the digital output is illustrated in Figure 54-3. Depending on the comparator operating mode, the monitored analog signal is compared to either an external or internal voltage reference.

In Figure 54-3, the VIN- is a fixed voltage. The analog signal present at VIN+ is compared to the reference signal at VIN-, and the digital output of the comparator is created by the difference between the two signals. When VIN+ is lesser than VIN-, the output of the comparator is a digital low level. When VIN+ is greater than VIN-, the output of the comparator is a digital high level. The shaded areas of the output represent the area of uncertainty due to input offsets and response time. The polarity of the comparator output can be inverted, so that it is a digital low level when VIN+ is greater than VIN-.

Figure 54-3: Comparator Operation



Input offset represents the range of voltage levels within which the comparator trip point can occur. The output can switch at any point within this offset range. Response time is the minimum time required for the comparator to recognize a change in input levels.

Each of the comparators can be configured to use the same or different reference sources. For example, one comparator can use an external reference while the others use the internal reference. For more information on operation of comparator voltage references, see **54.6 "Comparator Voltage Reference Generator"**.

54.4 COMPARATOR CONFIGURATION

Each of the comparators in the Comparator with Blanking module is configured independently by various control bits in the following registers:

- Comparator Status register (CMSTAT) (see Register 54-1)
- Comparator Control register (CMxCON) (see Register 54-2)
- Comparator Mask Source Control register (CMxMSKSRC) (see Register 54-3)
- Comparator Mask Gating Control register (CMxMSKCON) (see Register 54-4)
- Comparator Filter Control register (CMxFLTR) (see Register 54-5)
- Comparator Voltage Reference Control register (CVRCON) (see Register 54-6)

54.4.1 Comparator Enable/Disable

The comparator under control may be enabled or disabled using the corresponding Comparator Enable bit, CON (CMxCON<15>). When the comparator is disabled (CON = 0), the corresponding trigger and interrupt generation is also disabled.

It is recommended to first configure the CMxCON register with all bits to the desired value, and then set the CON bit (CMxCON<15>).

54.4.2 Comparator Output Blanking Function

In many power control and motor control applications, there are periods of time in which the inputs to the analog comparator are known to be invalid. The blanking (masking) function enables the user to ignore the comparator output during predefined periods of time. In this document, the terms ‘masking’ and ‘blanking’ are used interchangeably.

Figure 54-4 illustrates a block diagram of the comparator blanking circuitry. A blanking circuit is associated with each analog comparator.

Each comparator’s blanking function has three user selectable inputs:

- MAI (Mask A Input)
- MBI (Mask B Input)
- MCI (Mask C Input)

The MAI, MBI and MCI signal sources are selected through the Mask A Input Select, SELSRCA<3:0> (CMxMSKSRC<3:0>), Mask B Input Select, SELSRCB<3:0> (CMxMSKSRC<7:4>), and the Mask C Input Select, SELSRCC<3:0> (CMxMSKSRC<11:8>), bit fields.

The MAI, MBI and the MCI signals are fed into an AND-OR function block, which enables the user to construct a blanking (masking) signal from these inputs.

The blanking (masking) function is disabled following a system Reset.

The High or Low Level Masking Select bit, HLMS (CMxMSKCON<15>), configures the masking logic to operate properly depending on the default (deasserted) state of the comparators.

If the comparator is configured for ‘positive logic’ so that a ‘0’ represents a deasserted state and the comparator output is a ‘1’ when it is asserted, the HLMS bit (CMxMSKCON<15>) should be set to ‘0’ so that the blanking function (assuming the blanking function is active) will prevent the ‘1’ signal of the comparator from propagating through the Comparator module.

If the comparator is configured for ‘negative logic’ so that a ‘1’ represents a deasserted state and the comparator output is a ‘0’ when it is asserted, the HLMS bit (CMxMSKCON<15>) should be set to a ‘1’ so that the blanking function (assuming blanking function is active) will prevent the ‘0’ signal of the comparator from propagating through the Comparator module.

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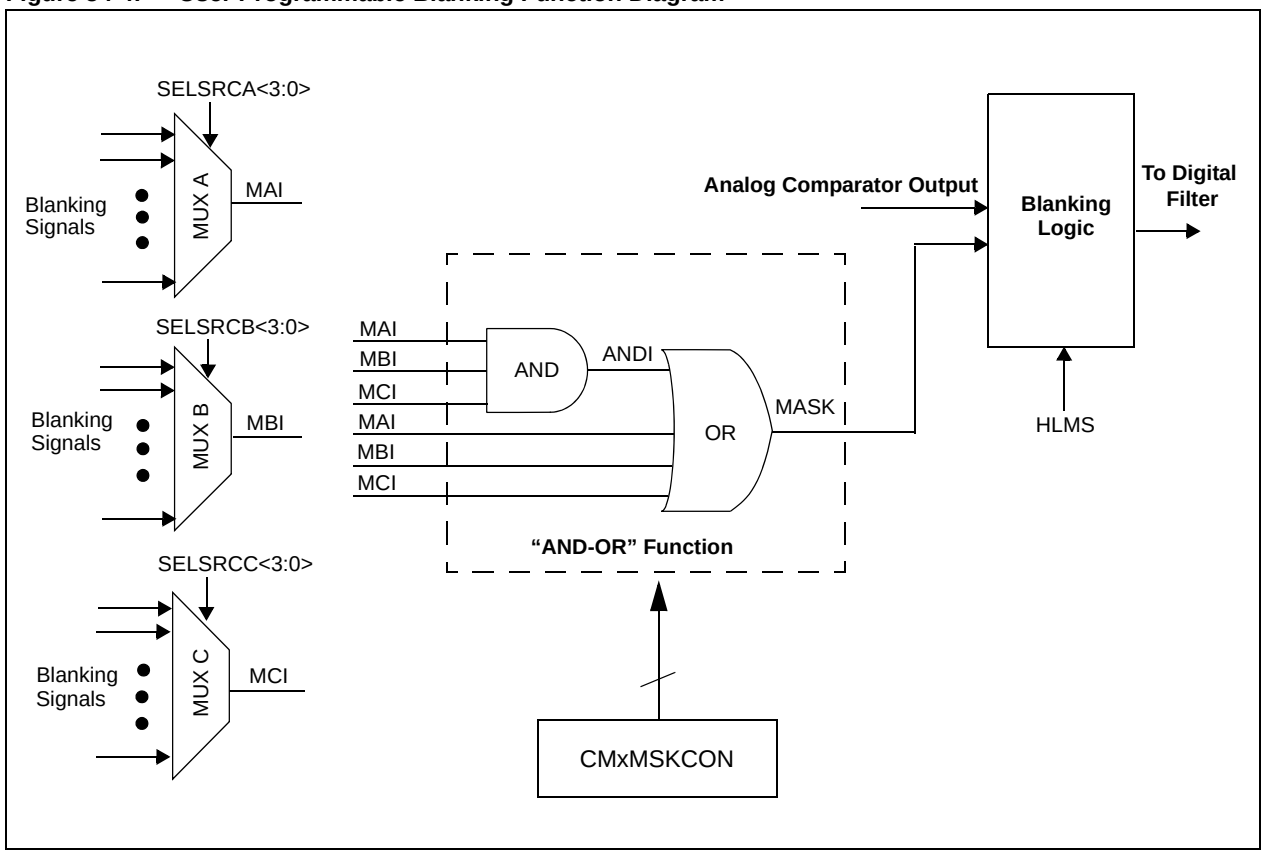
Figure 54-4: User Programmable Blanking Function Diagram



54.4.3 Digital Output Filter

In many motor and power control applications, the analog comparator input signals can be corrupted by the large electromagnetic fields generated by the associated external switching power transistors. Corruption of the analog input signals to the comparator can cause unwanted comparator output transitions. The programmable digital output filter can minimize the effects of input signal corruption.

The digital filter requires three consecutive input samples to be similar before the output of the filter can change state. Assuming the current state is '0', a string of inputs such as '001010110111', will only yield an output state of '1' at the end of the example sequence after the three consecutive '1's. Similarly, a sequence of three consecutive '0's are required before the output will change to a zero state.

Because of the requirement of three similar consecutive states for the filter, the chosen digital filter clock period must be one-third or less than the maximum desired comparator response time.

The digital filter is enabled by setting the Comparator Output Digital Filter Enable bit, CFLTREN (CMxFLTR<3>). The Comparator Output Filter Clock Divide Select bits, CFDIV<2:0> (CMxFLTR<2:0>), select the clock divider ratio for the clock signal input to the digital filter block. The Comparator Filter Input Clock Select bits, CFSEL<2:0> (CMxFLTR<6:4>), select the desired clock source for the digital filter. The digital filter is disabled (bypassed) following a system Reset.

54.4.4 Comparator Polarity Selection

To provide maximum flexibility, the output of the comparator may be inverted using the Comparator Output Polarity Select bit, CPOL (CMxCON<13>). This is functionally identical to reversing the inverting and non-inverting inputs of the comparator for a particular mode.

The CPOL bit (CMxCON<13>) should be changed only when the comparator is disabled (CON = 0). Internal logic will prevent the generation of any corresponding triggers or interrupts when CON = 0. The logic allows both the CON bit (CMxCON<15>) and the CPOL bit (CMxCON<13>) to be set with a single register write.

54.4.5 Event Polarity Selection

In addition to a programmable comparator output polarity, this module also allows software selection for trigger/interrupt edge polarity through the EVPOL<1:0> bits (CMxCON<7:6>). This feature allows independent control of the comparator output, as seen on any external pins, and the trigger/interrupt generation.

Note:	The corresponding comparator must be enabled (CON = 1) for the specific trigger/interrupt generation to be enabled.

54.4.6 Comparator Reference Input Selection

The input to the non-inverting input of the comparator, also known as the reference input, can be selected between the following settings:

- CxINA pin (CON = 1, CREF = 0)
- Internal CV_{REF} voltage (CON = 1, CREF = 1)

54.4.7 Comparator Channel Selection

The input to the inverting input of the comparator, also known as the channel input, can be selected between the following settings:

- CxINB pin (CON = 1, CCH<1:0> = 'b00)
- CxINC pin (CON = 1, CCH<1:0> = 'b01)
- CxIND pin (CON = 1, CCH<1:0> = 'b10)
- Band Gap Reference (CON = 1, CCH<1:0> = 'b11). The source of the band gap reference can be selected by the user-assigned application through the Band Gap Reference Source Select bits, BGSEL<1:0> (CVRCON<9:8>).

54.4.8 Low-Power Selection

Depending on the capabilities of the comparator modules, this interface provides a low-power mode selection bit, CLPWR (CMxCON<12>). Using this bit, a user can trade-off power consumption for the speed of the comparator.

When CLPWR = 0, Standard Power mode is active. When CLPWR = 1, the low-power setting of the corresponding comparator is enabled.

Note:	The comparator power setting should not be changed while CON = 1.

54.4.9 Comparator Event Status Bit

The Comparator Event Status bit, CEVT (CMxCON<9>), reflects whether or not the comparator has gone through the preconfigured event. After the CEVT bit (CMxCON<9>) is set, all future triggers and interrupts from the corresponding comparator will be blocked until the user-assigned application clears the CEVT bit (CMxCON<9>). Clearing the CEVT bit (CMxCON<9>) begins rearming the trigger. Once the CEVT bit (CMxCON<9>) is cleared, it takes an extra CPU cycle for the comparator triggers to be fully rearmed.

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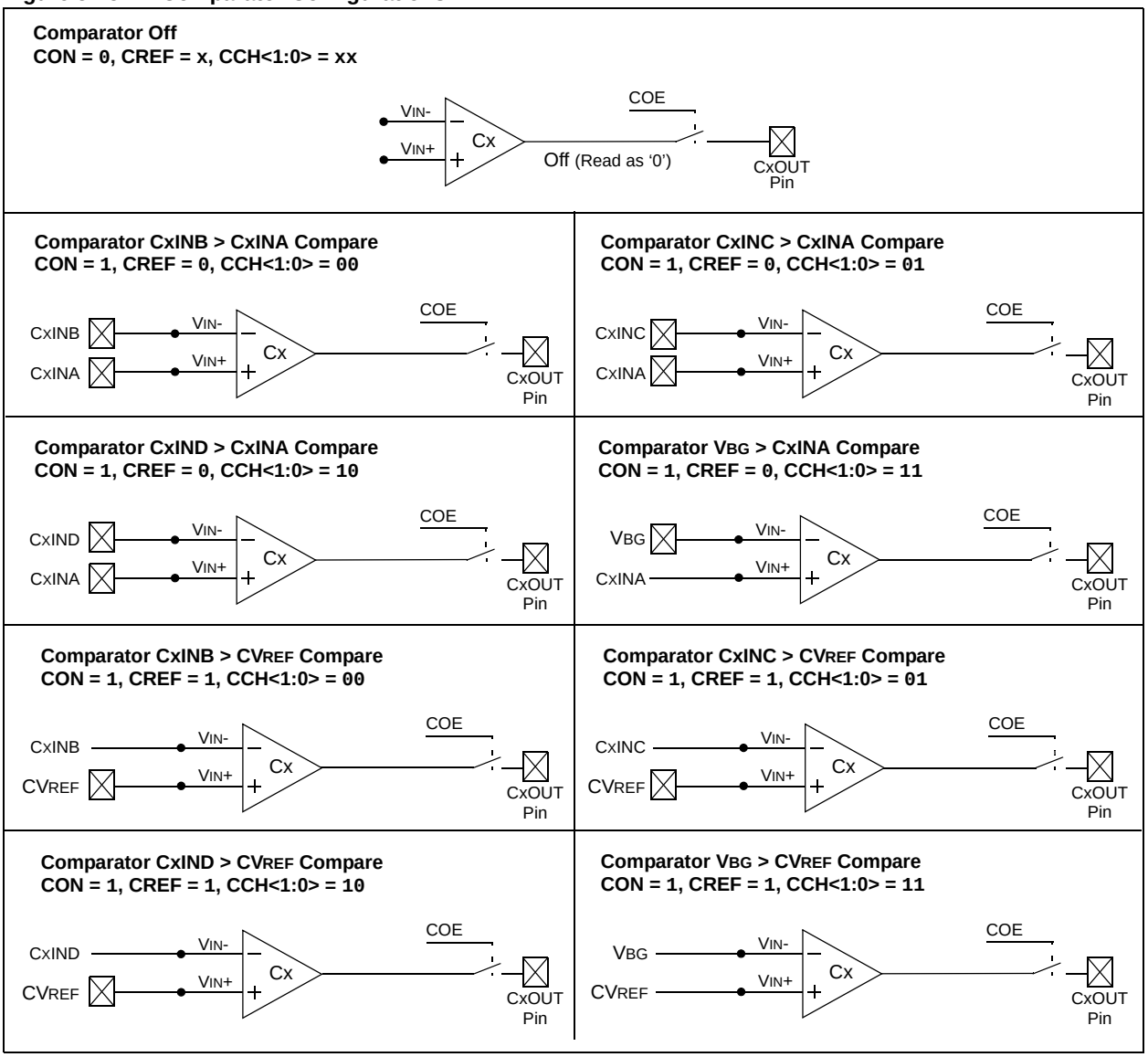
54.4.10 Status Register

To provide an overview of all comparator results, the Comparator Output bits, COUT (CMxCON<8>), and the Comparator Event bits, CEVT (CMxCON<9>), are replicated as status bits in the CMSTAT register.

These bits are read-only and can be altered only by manipulating the corresponding CMxCON register or the comparator input signals. Figure 54-5 illustrates the comparator configurations.

Figure 54-5: Comparator Configurations



54.5 COMPARATOR INTERRUPTS

The Comparator Interrupt Flag bit, CMIF (IFS1<2>), is set when the synchronized output value of any of the comparator changes with respect to the last read value. The following bits can be read by the user application to detect an event:

- Comparator 1 Event Status bit, C1EVT (CMSTAT<8>)
- Comparator 2 Event Status bit, C2EVT (CMSTAT<9>)
- Comparator 3 Event Status bit, C3EVT (CMSTAT<10>)

User-assigned software can read the CxEVT and CxOUT bits to determine the change that occurred. Because it is possible to write a '1' to this register, a simulated interrupt can be software initiated. Both the CMIF bit (IFS1<2>) and CxEVT bits must be reset by clearing them in software. These bits can be cleared in the Interrupt Service Routine (ISR). For more information, refer to **Section 6. "Interrupts"** (DS70184).

Note:	The comparison required for generating interrupts is based on the current comparator state and the last read value of the comparator outputs. Reading the C1OUT, C2OUT and C3OUT bits in the CMSTAT register will update the values used for the interrupt generation.

54.5.1 Interrupt Operation During Sleep Mode

If a comparator is enabled and the dsPIC33F/PIC24H device is placed in Sleep mode, the comparator remains active. If the Comparator interrupt is enabled in the Interrupt module, it remains functional. Under these conditions, a comparator interrupt event will wake-up the device from Sleep mode.

Each operational comparator consumes additional current. To minimize power consumption in Sleep mode, turn off the comparators before entering Sleep mode by disabling the CON bit (CMxCON<15>). If the device wakes up from Sleep mode, the contents of the CMxCON register are not affected. For more information on Sleep mode, refer to **Section 9. "Watchdog Timer (WDT) and Power-Saving Modes"** (DS70196).

54.5.2 Interrupt Operation During Idle Mode

The comparator remains active in Idle mode. Comparator interrupt operation during Idle mode is controlled by the Comparator Idle Mode, CMSIDL (CMSTAT<15>). If CMSIDL = 0, normal interrupt operation continues. If CMSIDL = 1, the comparator continues to operate, but it does not generate interrupts.

The device enters Idle mode when CMSIDL = 1. The comparator will not wake the CPU from Idle mode. However, if an interrupt request (IRQ) occurs in this state, it will be queued, and only processed after the CPU wakes up from Idle. For more information on Idle mode, refer to **Section 9. "Watchdog Timer (WDT) and Power-Saving Modes"** (DS70196).

54.5.3 Effects of a Reset State

A device Reset forces the CMxCON register to its Reset state, causing the comparator modules to be turned off (CON = 0). However, the input pins multiplexed with analog input sources are configured as analog inputs by default on device Reset. The I/O configuration for these pins is determined by the setting of the ADxPCFGL or ADxPCFGH register. Therefore, device current is minimized when analog inputs are present at Reset time.

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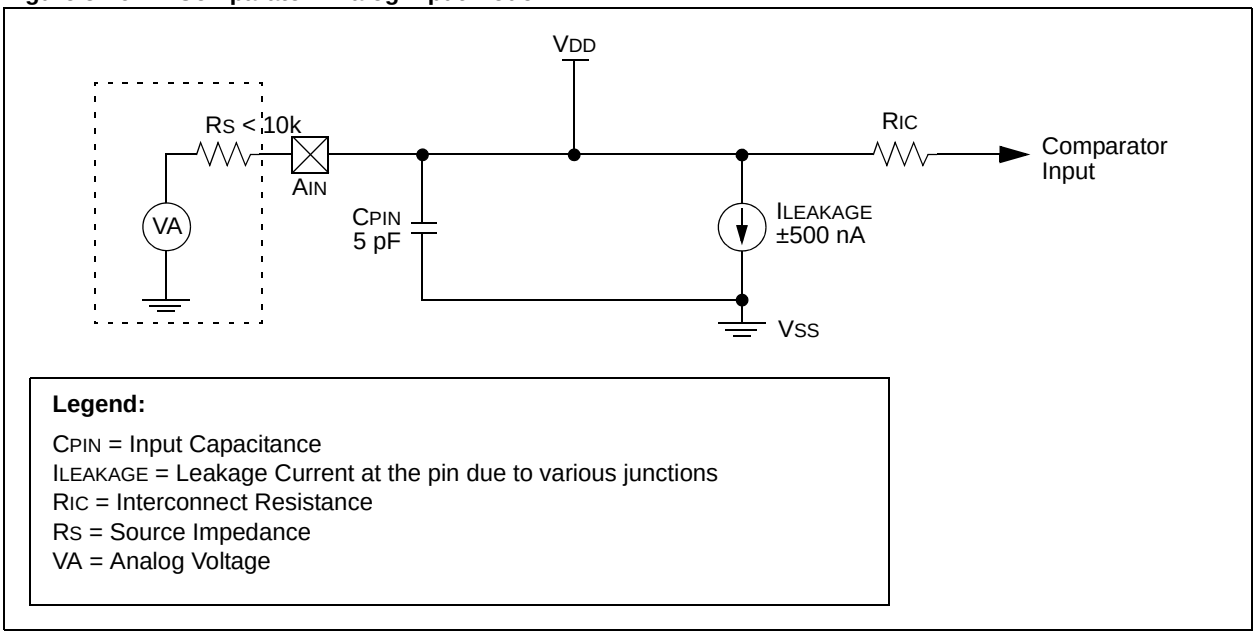
54.5.4 Analog Input Connection Considerations

A simplified circuit for an analog input is illustrated in Figure 54-6. A maximum source impedance of 10 kΩ is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have little leakage current.

Figure 54-6: Comparator Analog Input Model



Legend:

CPIN = Input Capacitance
ILEAKAGE = Leakage Current at the pin due to various junctions
RIC = Interconnect Resistance
RS = Source Impedance
VA = Analog Voltage

54.6 COMPARATOR VOLTAGE REFERENCE GENERATOR

The internal comparator voltage reference is derived from a 16-tap resistor ladder network that provides a selectable voltage level, as illustrated in Figure 54-7. This resistor network generates the internal voltage reference for the analog comparators.

This voltage generator network is managed by the CVRCON register (see Register 54-6) through these control bits:

- Comparator Voltage Reference Enable bit, CVREN (CVRCON<7>)

  This control bit enables the voltage reference circuit.

- Comparator Voltage Reference Output Enable bit, CVROE (CVRCON<6>)

  This control bit enables the reference voltage to be placed on the CVREF pin. When enabled, this bit overrides the corresponding TRIS bit setting.

- Voltage Reference Select bit, VREFSEL (CVRCON<10>)

  This control bit specifies whether the reference source is external (VREF+), or it is obtained from the 4-bit DAC output.

- Comparator Voltage Reference Source Selection bit, CVRSS (CVRCON<4>)

  This control bit specifies that the source (CVRSS) for the voltage reference circuit is either the device voltage supply (AVDD and AVSS) or an external reference (VREF+ and VREF-).

- Comparator Voltage Reference Range Selection bit, CVRR (CVRCON<5>)

  This control bit selects one of the two voltage ranges covered by the 16-tap resistor ladder network:

  - 0 CVRSRC to 0.67 CVRSRC
  - 0.25 CVRSRC to 0.75 CVRSRC

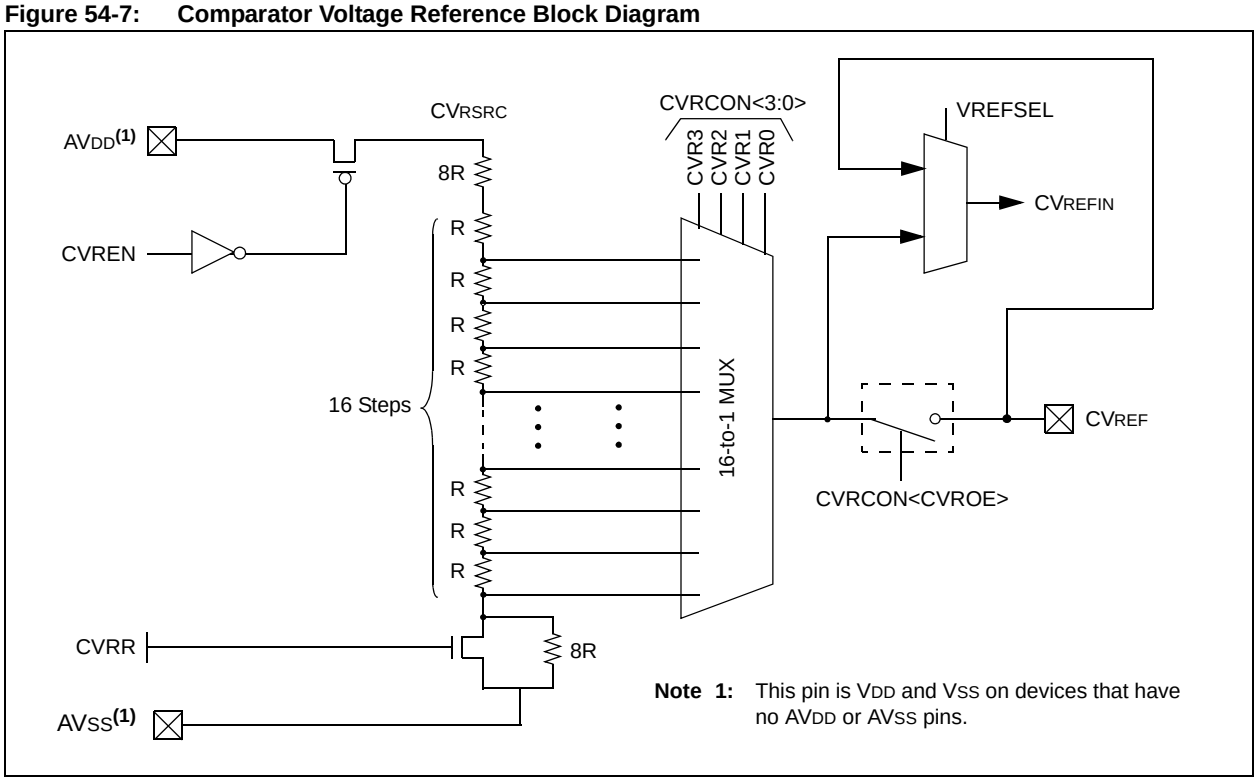
  The range selected also determines the voltage increments available from the resistor ladder taps (see **54.6.1 "Configuring the Comparator Voltage Reference"**).

- Comparator Voltage Reference Value Selection bits, CVR<3:0> (CVRCON<3:0>)

  These bits designate the resistor ladder tap position.

Table 54-1 lists the voltage at each tap for both ranges with CVRSRC = 3.3V.

Figure 54-7: Comparator Voltage Reference Block Diagram



Note 1: This pin is VDD and VSS on devices that have no AVDD or AVSS pins.

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Table 54-1: Typical Voltage Reference with CVRSRC = 3.3V

CVR<3:0>	Tap	Voltage Reference	
		CVRR = 0	CVRR = 1
0000	0	0.83V	0.00V
0001	1	0.93V	0.14V
0010	2	1.03V	0.28V
0011	3	1.13V	0.41V
0100	4	1.24V	0.55V
0101	5	1.34V	0.69V
0110	6	1.44V	0.83V
0111	7	1.55V	0.96V
1000	8	1.65V	1.10V
1001	9	1.75V	1.24V
1010	10	1.86V	1.38V
1011	11	1.96V	1.51V
1100	12	2.06V	1.65V
1101	13	2.17V	1.79V
1110	14	2.27V	1.93V
1111	15	2.37V	2.06V

54.6.1 Configuring the Comparator Voltage Reference

The voltage range selected by the CVRR bit (CVRCON<5>), determines the size of the steps selected by the CVR<3:0> bits (CVRCON<3:0>). One range (CVRR = 0) provides finer resolution by offering smaller voltage increments for each step. The equations used to calculate the comparator voltage reference are as follows:

If CVRR = 1:

Voltage Reference = ((CVR<3:0>)/24) (CVRSRC)*

If CVRR = 0:

*Voltage Reference = (CVRSRC/4) + ((CVR<3:0>)/32) * (CVRSRC)*

54.6.2 Voltage Reference Accuracy/Error

The full voltage reference range cannot be realized because the transistors on the top and bottom of the resistor ladder network, as illustrated in Figure 54-7, keep the voltage reference from approaching the reference source rails. The voltage reference is derived from the reference source; therefore, the voltage reference output changes with fluctuations in the reference source. For reference voltage accuracy, refer to **"Electrical Characteristics"** chapter in the specific device data sheet.

54.6.3 Operation During Sleep Mode

When the device wakes up from Sleep mode through an interrupt or a Watchdog Timer Time-out (WDTO), the contents of the CVRCON register are not affected. To minimize current consumption in Sleep mode, the voltage reference should be disabled.

54.6.4 Effects of a Reset

A device Reset has the following effects:

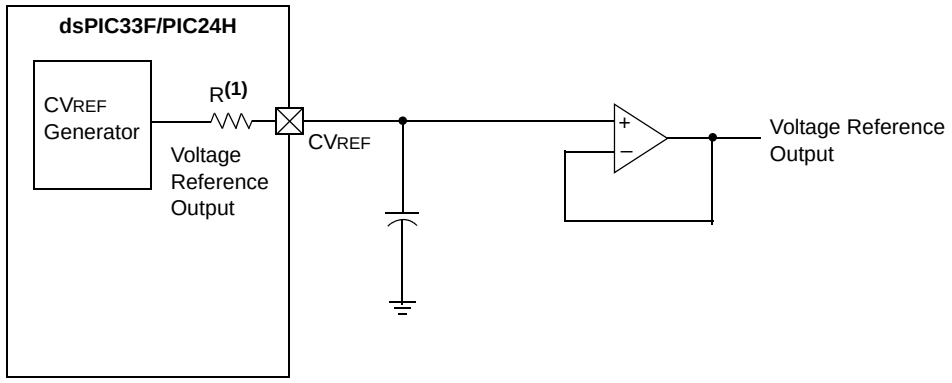
- Disables the voltage reference by clearing the CVREN bit (CVRCON<7>)
- Disconnects the reference from the CVREF pin by clearing the CVROE bit (CVRCON<6>)
- Selects the high-voltage range by clearing the CVRR bit (CVRCON<5>)
- Clears the CVR<3:0> value bits (CVRCON<3:0>)

54.6.5 Connection Considerations

The voltage reference generator operates independently of the Comparator with Blanking module. The output of the reference generator is connected to the CVREF pin, if the CVROE bit (CVRCON<6>) is set. Enabling the voltage reference output onto the I/O when it is configured as a digital input will increase current consumption. Configuring the port associated with CVREF as a digital output, with CVRSS enabled, will also increase current consumption.

The CVREF output pin can be used as a simple digital-to-analog output with limited drive capability. Due to this limited current drive capability, a buffer must be used on the voltage reference output for external connections to CVREF. Figure 54-8 illustrates a buffering technique example.

Figure 54-8: Comparator Voltage Reference Output Buffer Example



Note 1: 'R' is dependent upon the CVRR bit (CVRCON<5>) and CVR<3:0> value bits (CVRCON<3:0>).

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54.7 REGISTER MAP

A summary of the SFRs associated with the Comparator with Blanking module is provided in Table 54-2.

Table 54-2: Comparator Register Map

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMSTAT	CMSIDL	—	—	—	—	C3EVT	C2EVT	C1EVT	—	—	—	—	—	C3OUT	C2OUT	C1OUT	0000
CMxCON	CON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
CMxMSKSRC	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
CMxMSKCON	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CMxFLTR	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
CVRCON	—	—	—	—	—	VREFSEL	BGSEL<1:0>		CVREN	CVROE	CVRR	CVRSS	CVR<3:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Not all bits in these registers are available on all devices. Refer to the "Comparator" chapter in the specific device data sheet for availability.

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54.8 DESIGN TIPS

Question 1: ***Why is my voltage reference not what I expect?***

Answer: Any variation of the voltage reference source will translate directly onto the CVREF pin. Also, ensure that you have correctly calculated (specified) the voltage divider, which generates the voltage reference.

Question 2: ***Why is my voltage reference not at the expected level when I connect CVREF into a low-impedance circuit?***

Answer: The voltage reference module is not intended to drive large loads. A buffer must be used between the CVREF pin and the load of the dsPIC33F/PIC24H device (see Figure 54-8).

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54.9 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33F/PIC24H device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Comparator with Blanking module are:

Title	Application Note #
Make a Delta-Sigma Converter Using a Microcontroller's Analog Comparator Module	AN700
A Comparator Based Slope ADC	AN863

Note: Visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the dsPIC33F/PIC24H family of devices.

54.10 REVISION HISTORY

Revision A (December 2010)

This is the initial released version of the document

Revision B (June 2012)

This revision incorporates the following updates:

- Figures:
  - Updated Figure 54-1
- Notes:
  - Added Note 2 in Register 54-6
  - Added a note in Table 54-2
- Registers:
  - Updated the bit 1 and bit 0 value descriptions for bit 15, in Register 54-1
  - Updated the following in Register 54-6:
    - Changed the bit value 01 and bit value 00 description in the bit 9-8
    - Replaced bit 4, and changed the bit 4 description
- Sections:
  - Updated the following in **54.5.2 “Interrupt Operation During Idle Mode”**:
    - Updated any CMIDL references to CMSIDL
    - Updated the second paragraph
- Changes to text and formatting were incorporated throughout the document

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