Using XDMAC with QSPI on Arm Cortex-M7 MCUs Using MPLAB Harmony v3

AN3466

Introduction

This document describes how to use the Direct Memory Access Controller (XDMAC) with the Quad Serial Peripheral Interface (QSPI) on a Arm® Cortex®-M7 based MCU (SAM E70). It also describes the implementation of an application using the MPLAB® Harmony v3 software framework, and evaluating performance of QSPI read and write operations with or without XDMAC.

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1. Hardware and Software Requirements

1.1 SAM E70 Xplained Ultra Evaluation Kit

The SAM E70 Xplained Ultra Evaluation Kit is a development kit for evaluating the SAME70 microcontroller (MCU). The SAM E70 is based on the Cortex-M7 capable of running at 300 MHz. This ultra-evaluation kit includes an on-board Embedded Debugger, eliminating the need for external tools to program or debug the SAME70. The kit also offers external connectors to extend the features of the board and ease the development of custom designs.

The SAM E70 Xplained Ultra Evaluation Kit is available at Microchip Direct.

1.2 Logic Analyzer or Oscilloscope

A logic analyzer or scilloscope is required to analyze the GPIO pins which are configured to measure the performance of the QSPI read and write operations, with and without XDMAC.

1.3 MPLAB X IDE and MPLAB XC Compilers

The MPLAB X Integrated Development Environment (IDE) is an expandable, highly configurable software program that incorporates powerful tools to help discover, configure, develop, debug, and qualify embedded designs for most of the Microchip's microcontrollers.

The MPLAB X IDE is available for download at Microchip Website. This example describes MPLAB X IDE version 6.15. MPLAB XC compilers are available for download at Microchip Website. This example describes MPLAB XC32 version 4.30.

1.4 MPLAB Harmony v3

MPLAB Harmony v3 is a fully-integrated embedded software development framework that provides flexible and interoperable software modules that enable users to dedicate resources to creating applications for 32-bit PIC® and SAM devices, rather than dealing with device details, complex protocols and library integration challenges.

It includes the MPLAB Code Configurator (MCC), an easy-to-use development tool with a Graphical User Interface (GUI) that simplifies device set up, library selection, configuration and application development. The MCC is available as a plug-in that integrates with MPLAB X IDE and has a separate Java executable for stand-alone use with other development environments.

The examples described in this document use the following MPLAB Harmony v3 repositories. The user need to download the following repositories from GitHub:

- csp (MPLAB Harmony v3 Chip Support Package)
- dev_packs (MPLAB Harmony v3 Product Database)
- Core (MPLAB Harmony v3 Core)

or use the MCC Content Manager in MPLAB X IDE to download the repositories.

2. Introduction to QSPI

The Quad SPI Interface (QSPI) is a synchronous serial interface to communicate with external devices or memories. It is similar to the Serial Parallel Interface (SPI) protocol except that it has four data lines. Because the data is sent over multiple lines, it increases the bandwidth and performance compared to the standard SPI protocol.

The QSPI supports single, quad, or dual I/O based on the mode selected. The QSPI can be used in the following modes:

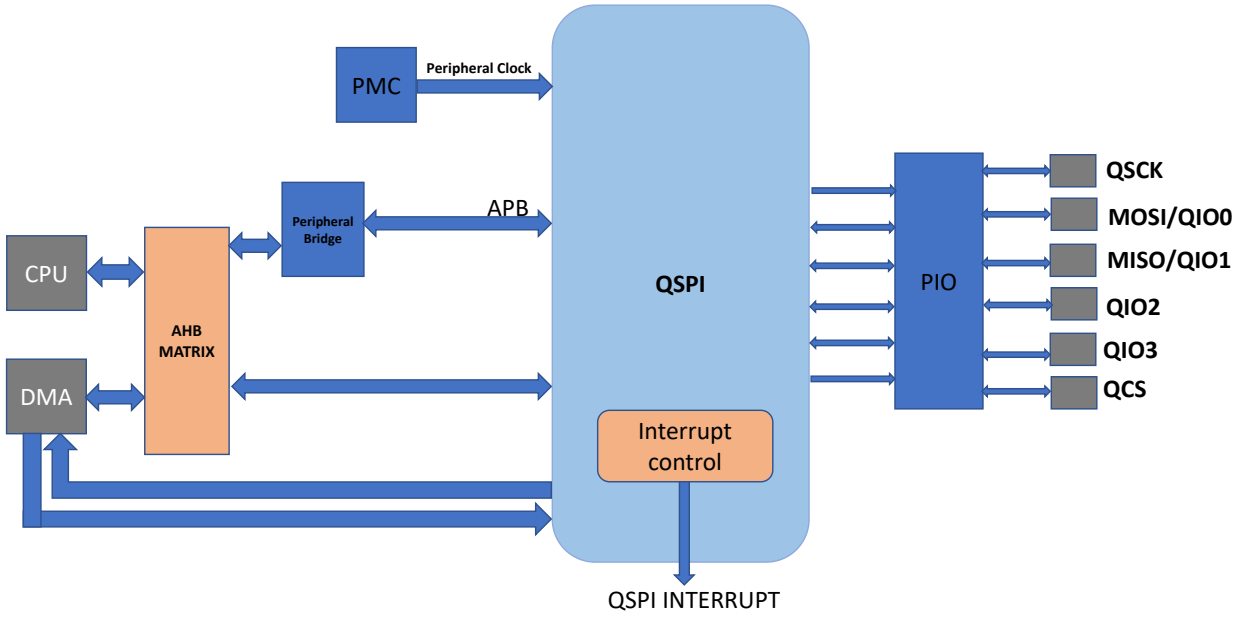
- **SPI mode:** Acts as a regular SPI Master mode. Interfaces to serial peripherals, such as ADCs, DACs, LCD controllers, CAN controllers, and sensors.

  Note: The scope of this document is limited to the QSPI serial memory mode. For a detailed description on the operation and configuration of the QSPI in SPI mode, refer to the product data sheet.
- **Serial Memory mode:** Interfaces to serial Flash memories.

The QSPI allows the system to use high-performance serial Flash memories, which are small and inexpensive, in place of larger and more expensive parallel Flash memories.

The following figure illustrates the block diagram of the QSPI.

Figure 2-1. QSPI Block Diagram

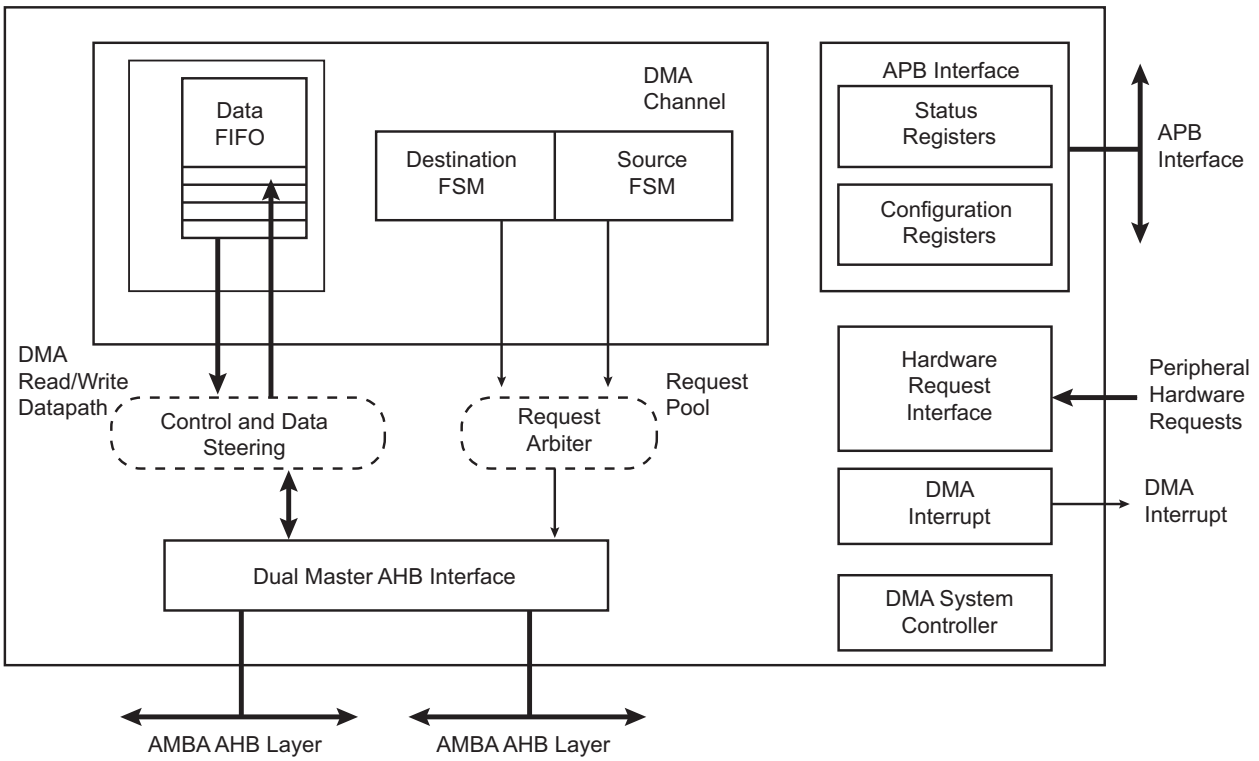


3. Direct Memory Access Controller

The Direct Memory Access Controller (XDMAC) is an AHB-protocol central direct memory access controller. It can transfer data between memories and peripherals, which allows these tasks to be offloaded from the CPU. It enables high data transfer rates with minimum CPU intervention and frees up CPU time. With access to all peripherals, the XDMAC can handle automatic data transfer between communication modules. The XDMAC has several DMA channels and each channel is fully programmable and provides both peripheral or memory-to-memory transfers.

The following figure illustrates the block diagram of the XDMAC controller.

Figure 3-1. XDMAC Controller Block Diagram



The XDMAC supports the following data transfers:

- Peripheral-to-memory transfer
- Memory-to-peripheral transfer
- Memory-to-memory transfer

3.1 Peripheral-to-Memory Transfer

The XDMAC transfers data from the source peripheral address and writes it to the destination memory location. This is a peripheral synchronized transfer, which mean the memory transaction is synchronized with the peripheral that generates the DMA request. It is also possible for software to initiate the DMA request.

Peripheral-to-memory transfer has five levels of data transactions: Master, Block, Microblock, Burst, and Chunk level transactions. Master, Block, Microblock, and Burst level transactions work same as explained in the memory-to-memory data transfer section. In peripheral-to-memory data transfer, the burst level transaction is further divided into chunk level data transaction to have a higher granularity.

3.2 Memory-to-Peripheral Transfer

The XDMAC transfers data from the source memory address and writes it to the destination peripheral location. This is also a peripheral synchronized transfer.

It has four levels of data transactions: Master, Block, Microblock, and Chunk level transactions. Master, Block, and Microblock level transactions work exactly the same way as explained in the memory-to-memory data transfer section. In the memory-to-peripheral data transfer, the burst level transaction is not present. The microblock is split into a chunk level data transaction.

3.3 Memory-to-Memory Transfer

The XDMAC reads data from the source memory location and writes it to the destination memory location. Memory-to-memory data transfer has four levels of data transactions: Master, Block, Microblock, and Burst level transactions.

XDMAC Master Transfer: The Master Transfer is a multi block data transfer, which is performed using a linked list of descriptors (blocks). Each descriptor in the linked list is configured to perform a block transfer. In multi block transfer mode, the XDMAC channel configuration parameters can be modified at the inter block boundary (between descriptors) and interrupts can be generated on a per block basis, or when the end of linked list event occurs.

- To configure the XDMAC Master Transfer mode, enable 'Use Linked List Mode' in the MCC under the XDMAC Configurations which will generate the code to configure the first descriptor control (XDMAC_CNDC) and address (XDMAC_CNDA) registers.
  Note: This application is not configured to use the XDMAC in Master Transfer mode.

XDMAC Block: An XDMAC block is composed of a programmable number of microblocks. The block length (number of microblocks) is configured in the BLEN field of the XDMAC Channel Block Control Register (XDMAC_CBCx).

- The MCC generates the XDMAC Block code by default.
  Note: This application does not use the XDMAC Block mode to transfer data between memory-to-memory.

XDMAC Microblock: A microblock is composed of programmable data. The microblock length is configured in the UBLEN field of the XDMAC Channel Microblock Control Register (XDMAC_CUBCx). The microblock length (UBLEN) indicates the amount of data (bytes, half words, or words based on the data width setting) present in a microblock. The XDMAC channel configuration parameters remain unchanged at the data boundary.

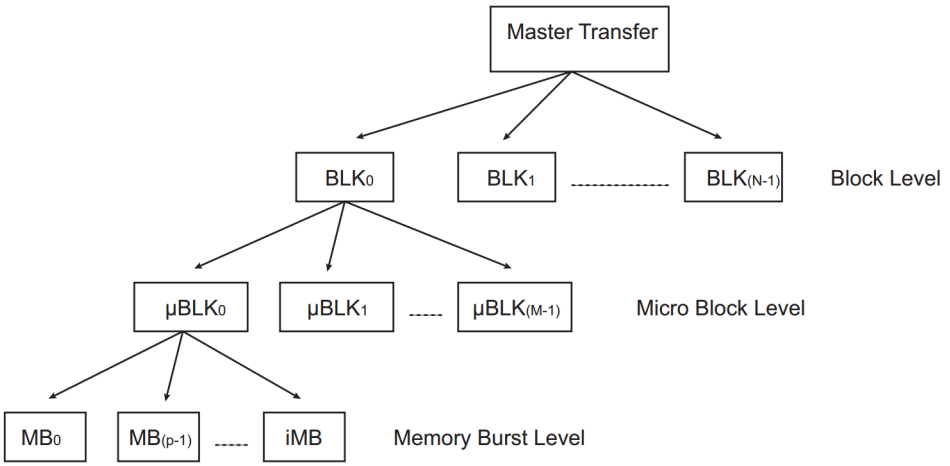
- The XDMAC Microblock mode is configured by setting the data width in the MCC under XDMAC Channel Settings. The data width can be 8, 16, or 32-bits.
  Note: The application is configured for a data width of 8-bit for writing, and 32-bit for reading.

XDMAC Burst and Incomplete Burst: To improve the overall performance when accessing the dynamic external memory, a burst access is mandatory. Each data unit of the microblock is considered a part of a memory burst. The programmable burst value indicates the largest memory burst allowed on a per channel basis. The burst size (in WORDS) is configured in the MBSIZE field of the XDMAC Channel Configuration Register (XDMAC_CCx). When the microblock length is not an integral multiple of the burst size, an incomplete burst is performed to read or write the last trailing bytes.

- The XDMAC Burst size is configured for memory-to-memory in the MCC under the XDMAC Channel Settings. The burst size can be 1, 4, 8, or 16 transfers per burst.
  Note: This application is configured for 1 transfer per burst for writing, and 16 transfers per burst for reading.

The following figure illustrates the Memory Transfer Hierarchy.

Figure 3-2. Memory Transfer Hierarchy



In the SAM E70 Xplained Ultra Evaluation Kit, the External Serial Flash (SST26VF032BA) is mapped to the QSPI memory region and the QSPI is configured to run in Serial Memory mode. The source (application buffer) and destination (Serial Flash) are memory types, therefore, the XDMAC transfer type is configured to memory-to-memory instead of peripheral-to-memory or memory-to-peripheral.

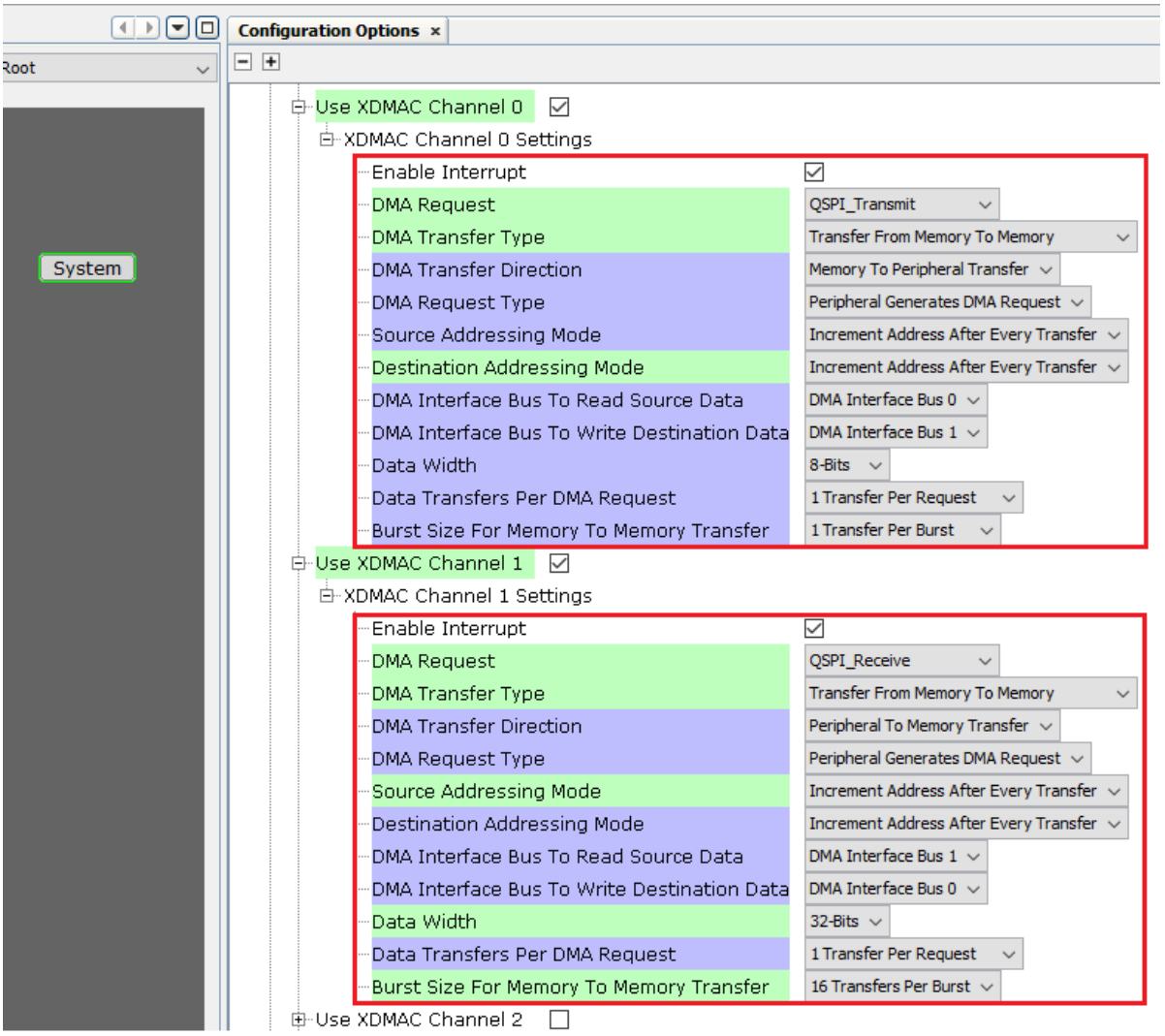
As mentioned previously, to increase the overall performance of the Read from External Serial Flash using the XDMAC, the data transaction level used for the Read operation is a XDMAC Microblock width size configured to 32-bits and a Burst Size to 16 transfers per burst, compared to the Write to External Serial Flash with the XDMAC Microblock width configured to 8-bits and the Burst Size to 1 transfer per burst. This is due to the slow write operation, which happens one page at a time. For additional information, refer to the SST26VF032BA document.

XDMAC Configurations:

The XDMAC can be configured by selecting the System module and traversing in tree view to DMA (XDMAC), then complete the XDMAC Transmit and Receive channel configurations in the Configuration Option window.

The figure below illustrates the XDMAC configurations for the QSPI Transmit and Receive channels in the MCC.

Figure 3-3. MPLAB Harmony v3 XDMAC QSPI Channel Configurations



XDMAC Channel Configurations: In the XDMAC write operation, the DMA transfers one byte from the application buffer to the QSPI memory address for each trigger, where in the read operation, one word is transferred from the application buffer to the QSPI memory address for each trigger, and the XDMAC holds the AHB bus till it finishes the 16 transfers in burst. This helps to increase the overall performance in the XDMAC Read operation.

- **Source and Destination Address Mode:** Select whether to increase the Source and Destination Address after every transfer.
  - Because it is a memory-to-memory transfer type, the Source and Destination Address mode are incremented after every transfer for both the QSPI Receive and Transmit channels.
- **Data Width:** Size of one transfer. The default value is 8 bits.
  - To increase the Read operation performance, the Data Width is configured to 32-bits.
- **DMA Interface Bus:** Configure the Source or Destination Interface Bus to Read or Write the data through the System bus.
  - If the trigger source is the QSPI transmit, then the DMA Interface Bus which reads the Source data is the *system bus interface 0* and the *system bus interface 1* writes the Destination data.

  - If the trigger source is the QSPI receive, then the DMA Interface Bus which reads the Source data is the *system bus interface 1* and the *system bus interface 0* writes the Destination data.

- **Memory Burst Size:** A fast data transfer mode. It can perform up to 16 transfers (beats) before releasing the control of the system bus back to the CPU. The value of burst length is configured to 16 transfers per burst to achieve better performance.

The DMA transfer direction, request type, and chunk size can be ignored if these configurations are applicable only to memory-to-peripheral transfer types or peripheral-to-memory transfer types.

4. MPU Configuration for QSPI

The Cortex-M7 processor features a Memory Protection Unit (MPU) allowing the division of the memory map into several regions with privilege permissions and access rules. It helps in providing fine grain memory control, enabling applications to utilize multiple privilege levels, separating and protecting code, data and stack on a task-by-task basis.

The SAM E70 devices manage up to 16 regions with the MPU for safety and critical applications. The following table summarizes the available MPU attributes in Cortex-M7.

Table 4-1. MPU Attributes

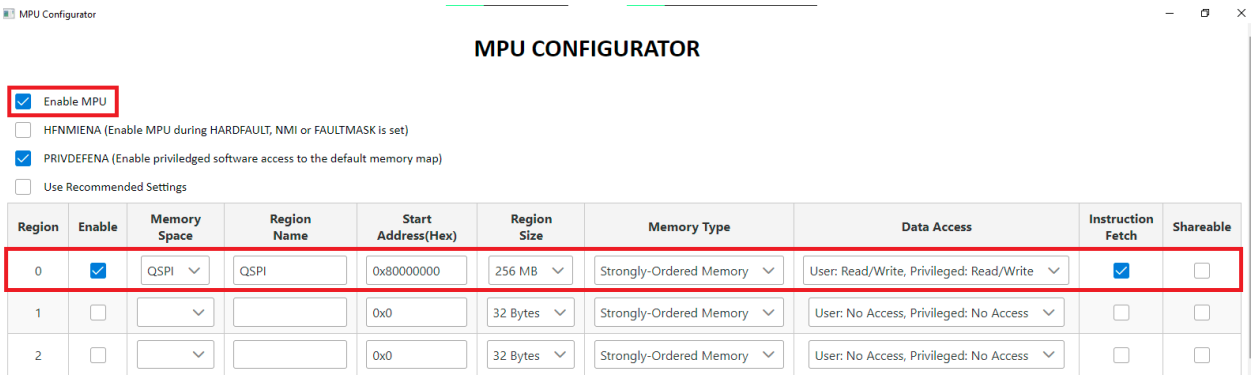
Memory type	Shareability	Attributes	Description
Strongly ordered	N/A	N/A	All access occurs in program order. No concurrent access can be done until the current access is completed.
Device	Shared	N/A	All access occurs in program order. Memory mapped peripheral shared by several masters.
	Non-shared	N/A	All access occurs in program order. Memory mapped peripheral shared by single master.
Normal	Shared	Non-cacheable Write-through cacheable Write-back Cacheable	Normal memory shared by several masters.
	Non-shared	Non-cacheable Write-through cacheable Write-back Cacheable	Normal memory shared by single master.

When the QSPI is accessed by the Cortex-M7 processor for programming operations, the QSPI memory space must be defined in the Cortex-M7 MPU.

For Programming operations, the QSPI memory space must be defined in the MPU with the attribute 'Device' or 'Strongly Ordered'. For Fetch/Read operations, the QSPI memory space must be defined in the MPU with the attribute 'Normal' to benefit from the internal cache.

The following figure shows the MPU configuration for the QSPI memory region using the “MPU Settings” window in the MCC.

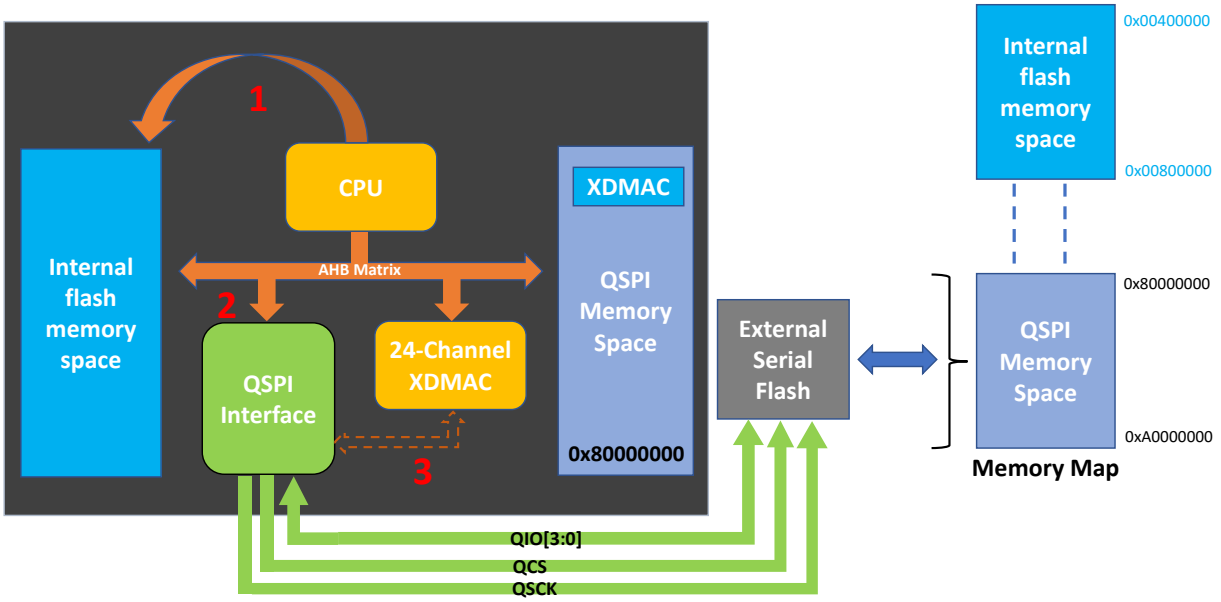
Figure 4-1. MPLAB Harmony v3 MPU Settings



5. Using XDMAC with QSPI on Cortex-M7 (SAM E70) Using MPLAB Harmony v3

To implement the XDMAC with QSPI using MPLAB Harmony v3, refer to the Hardware and Software Requirements section. The SAM E70 Xplained Ultra Board contains a 4-MB QSPI Flash (SST26VF032BA) interfaced to the QSPI lines. Refer to the SST26VF032BA data sheet to know which commands and instructions can be used to communicate to the serial Flash.

Figure 5-1. QSPI XDMAC Read Write Application Block Diagram



- **Initialization:** The CPU starts executing from the internal MCU Flash, and initializes the QSPI in Serial Memory mode, the XDMAC in memory-to-memory transfer mode, and configures the QSPI Transmit and Receive channels.
- **Without DMA:** In Serial Memory mode, the serial Flash mapped to 0x80000000, and appears as a memory address to the CPU. The CPU starts executing from the QSPI memory region (that is, 0x80000000). It Writes page by page into the QSPI memory region, which will in turn write to the External Serial Flash and read data from the same. The read/writes to the External Serial Flash requires the CPU to either poll or periodically monitor the completion of read/write transactions. Therefore, the CPU is kept consistently busy checking the status of the QSPI read/write operations.
- **With DMA:** The CPU sets up the QSPI and sends the read/write commands. The actual read/write operation is handled by the XDMAC, which off-loads these tasks from the CPU. It enables data transfer with minimal CPU intervention and notifies the application through a callback after the XDMAC read/write transfer is complete.

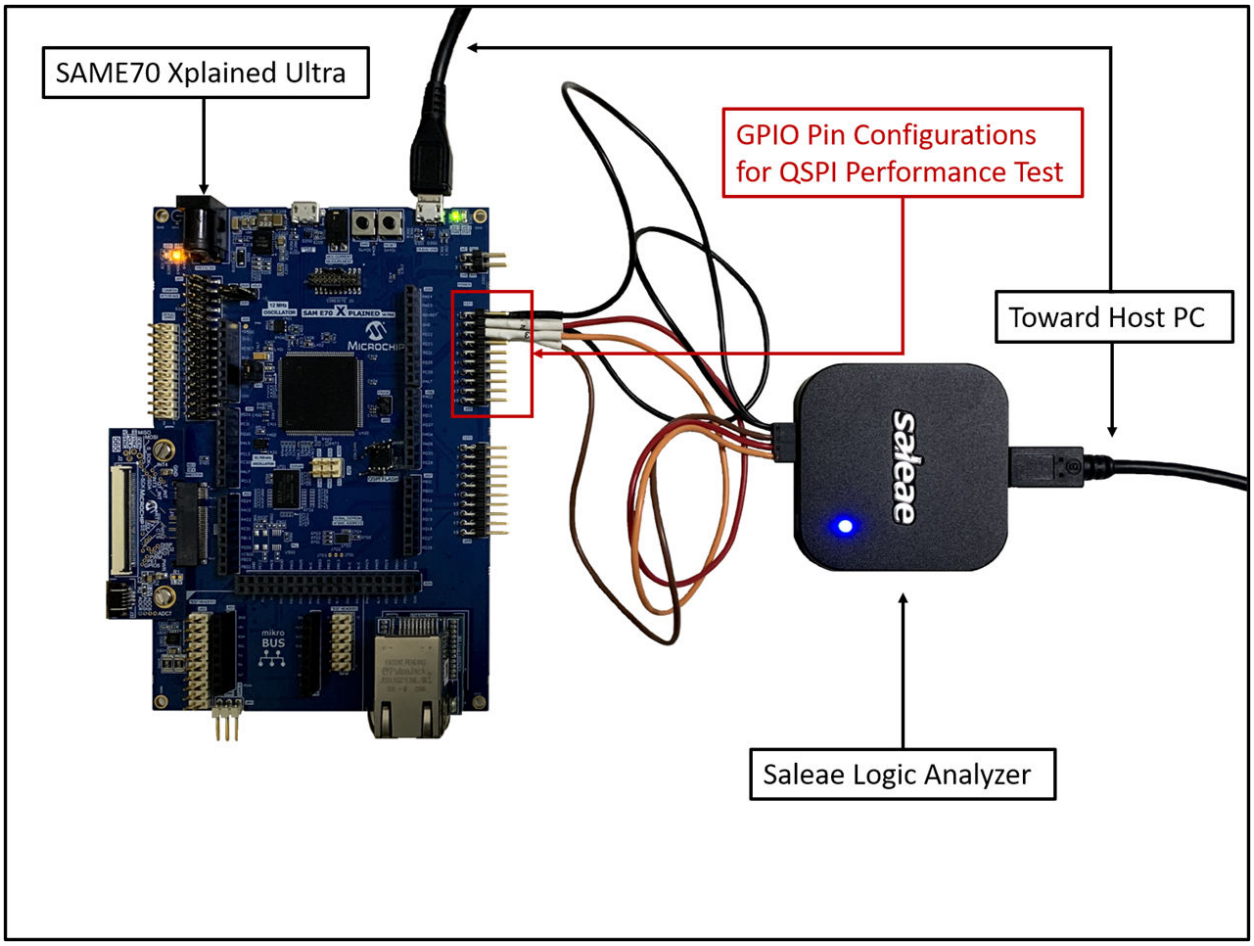
The application for using the XDMAC with the QSPI is available at qspi_xdmac_read_write, which is based on MPLAB Harmony v3.

5.1 QSPI XDMAC Read/Write MPLAB Harmony v3 Application

The QSPI XDMAC Read/Write application writes and reads 80 KB data into the External Serial Flash memory using the QSPI, with and without using XDMAC. The performance of the QSPI read/write is evaluated by comparing the time taken for the read/write to and from the External Serial Memory with or without using the XDMAC.

The following figure illustrates the hardware setup for the application.

Figure 5-2. QSPI XDMAC Read Write Hardware Setup



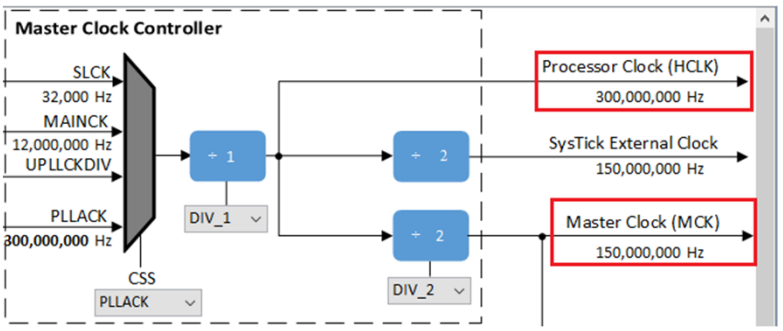
This application configures the following modules:

- Configure four GPIO pins to test the performance of the QSPI read/write operations:
  - Four separate GPIO pins are configured to measure the time taken for data transmission with and without the DMA. The pins are set before the read/write operations and are cleared after the read/write operations.
- The QSPI MPU memory region is strongly ordered which disables the cache.
- Configures the QSPI to Serial Memory Read mode to read/write from the serial Flash and set the QSPI Clock frequency to 50.0 MHz.
- Enable the XDMAC and configure the QSPI transmit and receive channels to perform read/write operations using the DMA.
- Enable the SysTick in interrupt mode to toggle the user LED1 every 500 ms. The LED is used to indicate the success or failure of the application.

Follow these steps to configure MCC for the QSPI XDMAC read/write application:

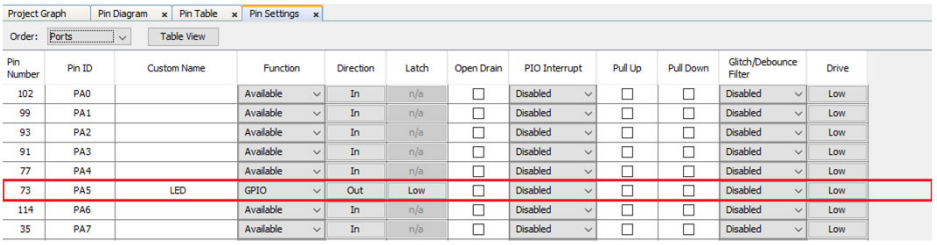
1. Configure the MPU for QSPI memory regions. The QSPI must be configured as 'Strongly ordered' for programming the operation as shown in MPLAB Harmony v3 MPU Settings.
2. Verify the Master and Processor clocks from the MCC **Clock Configuration** window.

Figure 5-3. QSPI XDMAC Read Write Clock Configurations



3. Configure the LED pin as a GPIO.

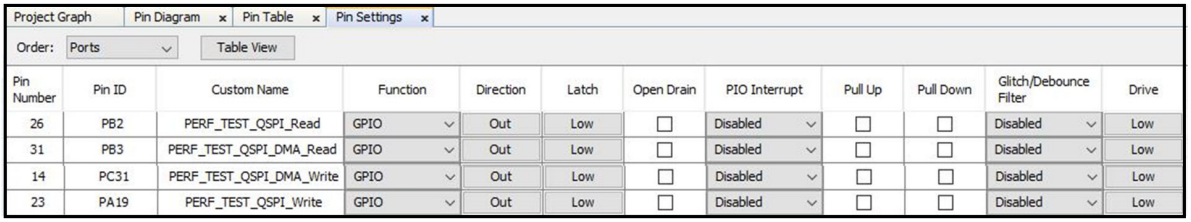
Figure 5-4. QSPI XDMAC Read/Write LED Pin Configuration



Pin Number	Pin ID	Custom Name	Function	Direction	Latch	Open Drain	PIO Interrupt	Pull Up	Pull Down	Glitch/Debounce Filter	Drive
102	PA0		Available	In	n/a	☐	Disabled	☐	☐	Disabled	Low
99	PA1		Available	In	n/a	☐	Disabled	☐	☐	Disabled	Low
93	PA2		Available	In	n/a	☐	Disabled	☐	☐	Disabled	Low
91	PA3		Available	In	n/a	☐	Disabled	☐	☐	Disabled	Low
77	PA4		Available	In	n/a	☐	Disabled	☐	☐	Disabled	Low
73	PA5	LED	GPIO	Out	Low	☐	Disabled	☐	☐	Disabled	Low
114	PA6		Available	In	n/a	☐	Disabled	☐	☐	Disabled	Low
35	PA7		Available	In	n/a	☐	Disabled	☐	☐	Disabled	Low

4. Click **Pin Settings** tab and then configure the GPIO pins (PB2, PB3, PC31 and PA19) for testing the QSPI performance:
   - PERF_TEST_QSPI_Read Pin: Used to set and clear the pin before and after the QSPI read without DMA.
   - PERF_TEST_QSPI_Write Pin: Used to set and clear the pin before and after the QSPI write without DMA.
   - PERF_TEST_QSPI_DMA_Read Pin: Used to set and clear the pin before and after the QSPI read with DMA.
   - PERF_TEST_QSPI_DMA_Write Pin: Used to set and clear the pin before and after the QSPI write with DMA.

Figure 5-5. QSPI XDMAC Read/Write GPIO PIN Configuration



Pin Number	Pin ID	Custom Name	Function	Direction	Latch	Open Drain	PIO Interrupt	Pull Up	Pull Down	Glitch/Debounce Filter	Drive
26	PB2	PERF_TEST_QSPI_Read	GPIO	Out	Low	☐	Disabled	☐	☐	Disabled	Low
31	PB3	PERF_TEST_QSPI_DMA_Read	GPIO	Out	Low	☐	Disabled	☐	☐	Disabled	Low
14	PC31	PERF_TEST_QSPI_DMA_Write	GPIO	Out	Low	☐	Disabled	☐	☐	Disabled	Low
23	PA19	PERF_TEST_QSPI_Write	GPIO	Out	Low	☐	Disabled	☐	☐	Disabled	Low

5. Configure the GPIO pins (QSCK, QCS, QIO [3:0]) for the QSPI peripheral from the MCC **Pin Settings** window.

Figure 5-6. QSPI XDMAC Read/Write QSPI Pin Configuration

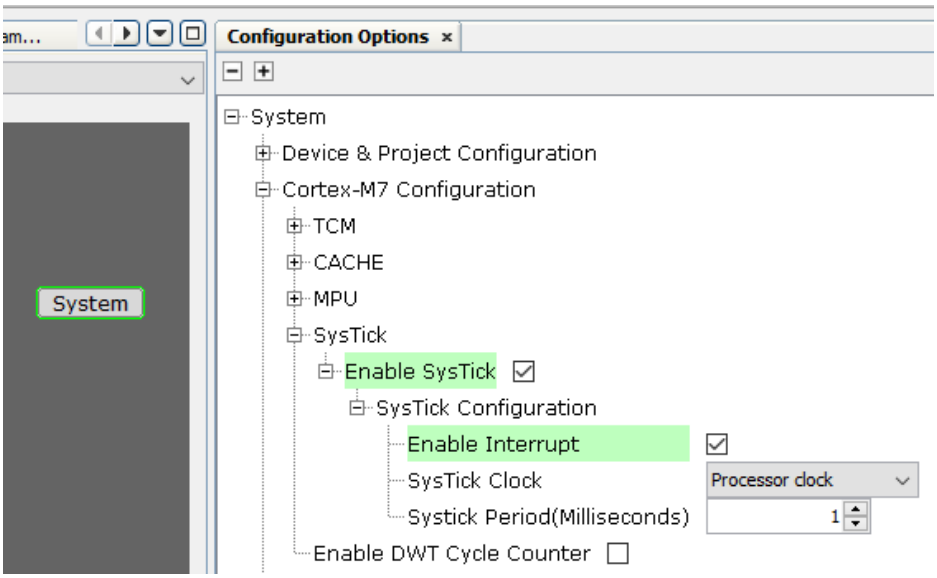
Kit Window | Start Page | MPLAB X Store | Project Graph | Clock Diagram | Pin Diagram | Pin Table | Pin Settings

Order: Ports | Table View

Pin Number	Pin ID	Custom Name	Function	Direction	Latch	Open Drain	PIO Interrupt	Pull Up	Pull Down	Glitch/Debounce Filter	Drive
64	PA11		QSPI_QCS	n/a	n/a		Disabled			Disabled	Low
68	PA12		QSPI_QIO1	n/a	n/a		Disabled			Disabled	Low
42	PA13		QSPI_QIO0	n/a	n/a		Disabled			Disabled	Low
51	PA14		QSPI_QSCK	n/a	n/a		Disabled			Disabled	Low
25	PA17		QSPI_QIO2	n/a	n/a		Disabled			Disabled	Low
2	PD31		QSPI_QIO3	n/a	n/a		Disabled			Disabled	Low

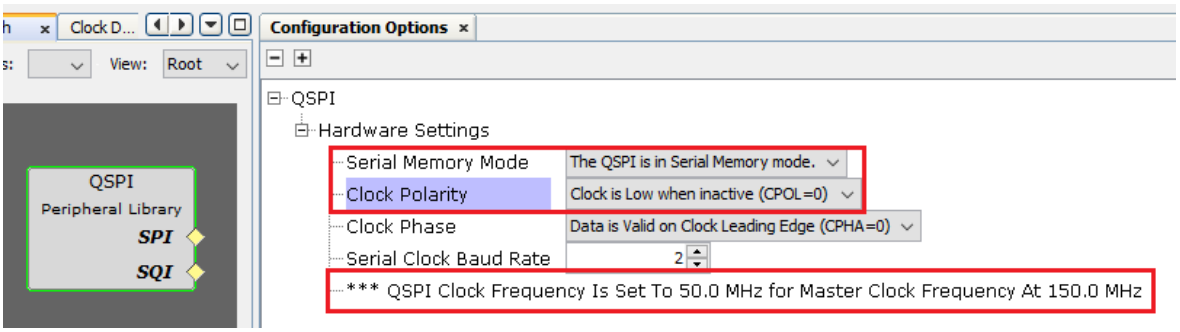
6. In the left Navigation bar select **System.** In the right Configuration Options section, click and expand **System > Cortex-M7 Configuration > SysTick**.
7. Select **Enable SysTick** and **Enable Interrupt** options as shown below.

Figure 5-7. QSPI XDMAC Read/Write CACHE and SysTick Configuration



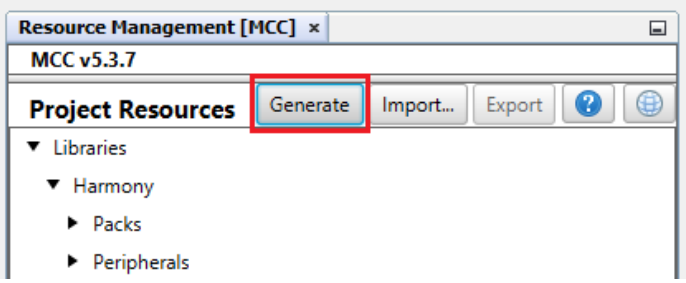
8. Select **QSPI Peripheral Library** and in the Configuration Options section, click and expand **QSPI > Hardware Settings**, and then configure Clock Polarity as shown below.

Figure 5-8. QSPI XDMAC Read/Write QSPI Configuration



9. Configure the XDMAC QSPI Transmit and Receive Channels in memory-to-memory mode. Refer to the MPLAB Harmony v3 XDMAC QSPI Channel Configurations for a detailed XDMAC configurations.
10. Click **Generate** to generate the MPLAB Harmony v3 code.

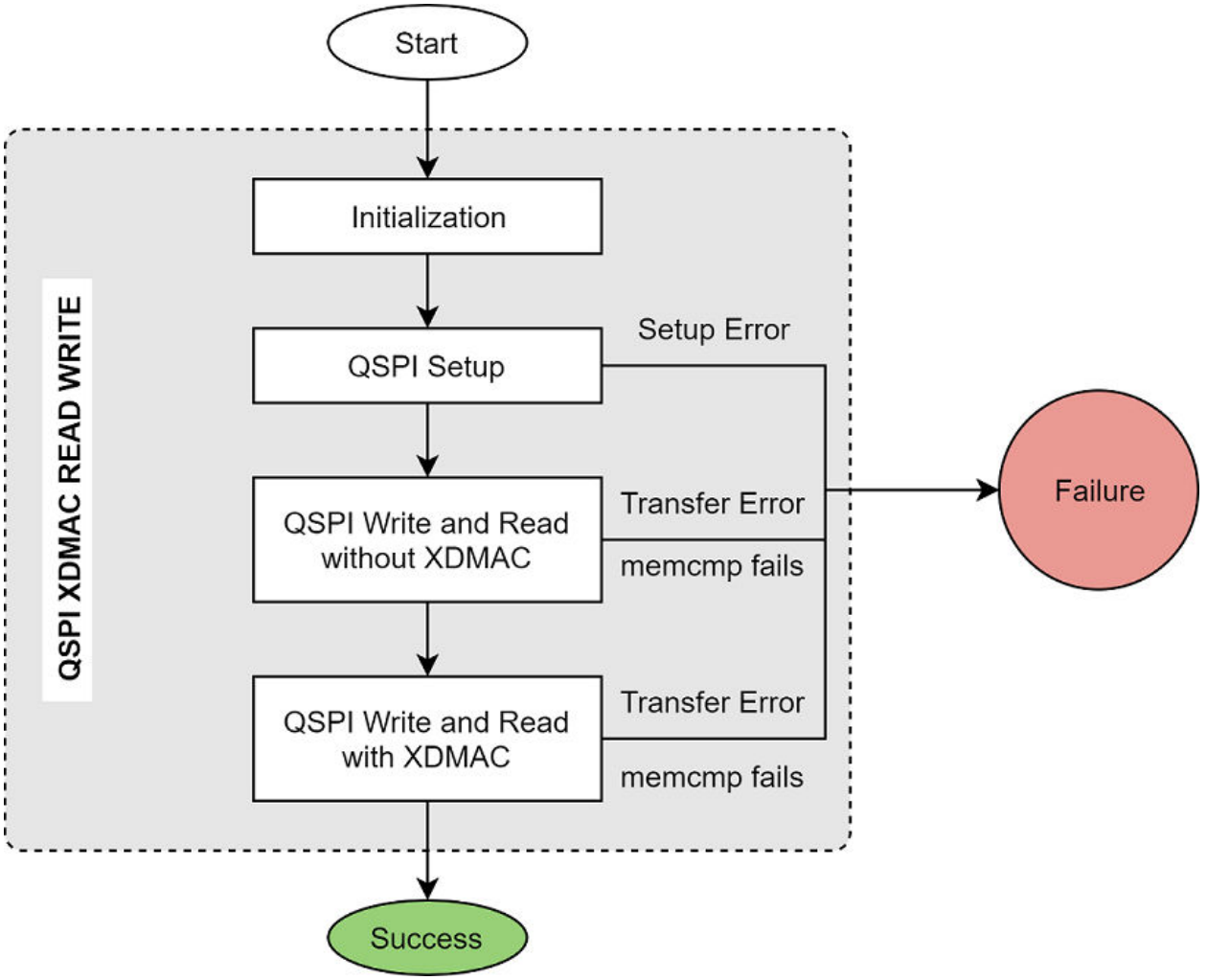
Figure 5-9. QSPI XDMAC Read/Write Generate Code



5.2 QSPI XDMAC Read/Write Application Flowchart

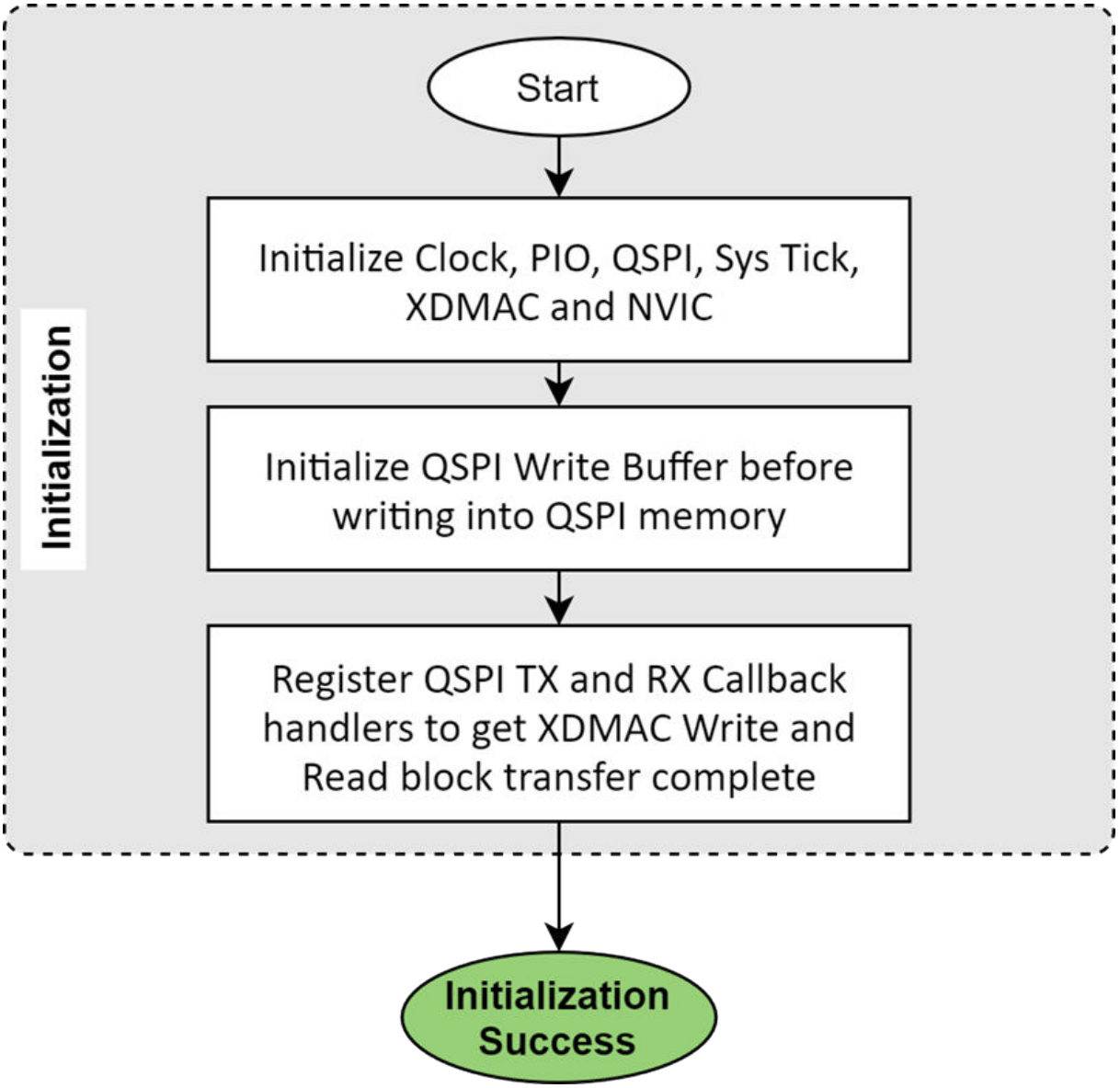
The QSPI XDMAC read/write application does the low-level initialization and setup of the QSPI peripheral before performing the read/write operation. The performance is evaluated with or without enabling the XDMAC. The following figure illustrates a high-level flowchart of the QSPI XDMAC read/write application.

Figure 5-10. QSPI XDMAC Read/Write Throughput Measurement Flowchart



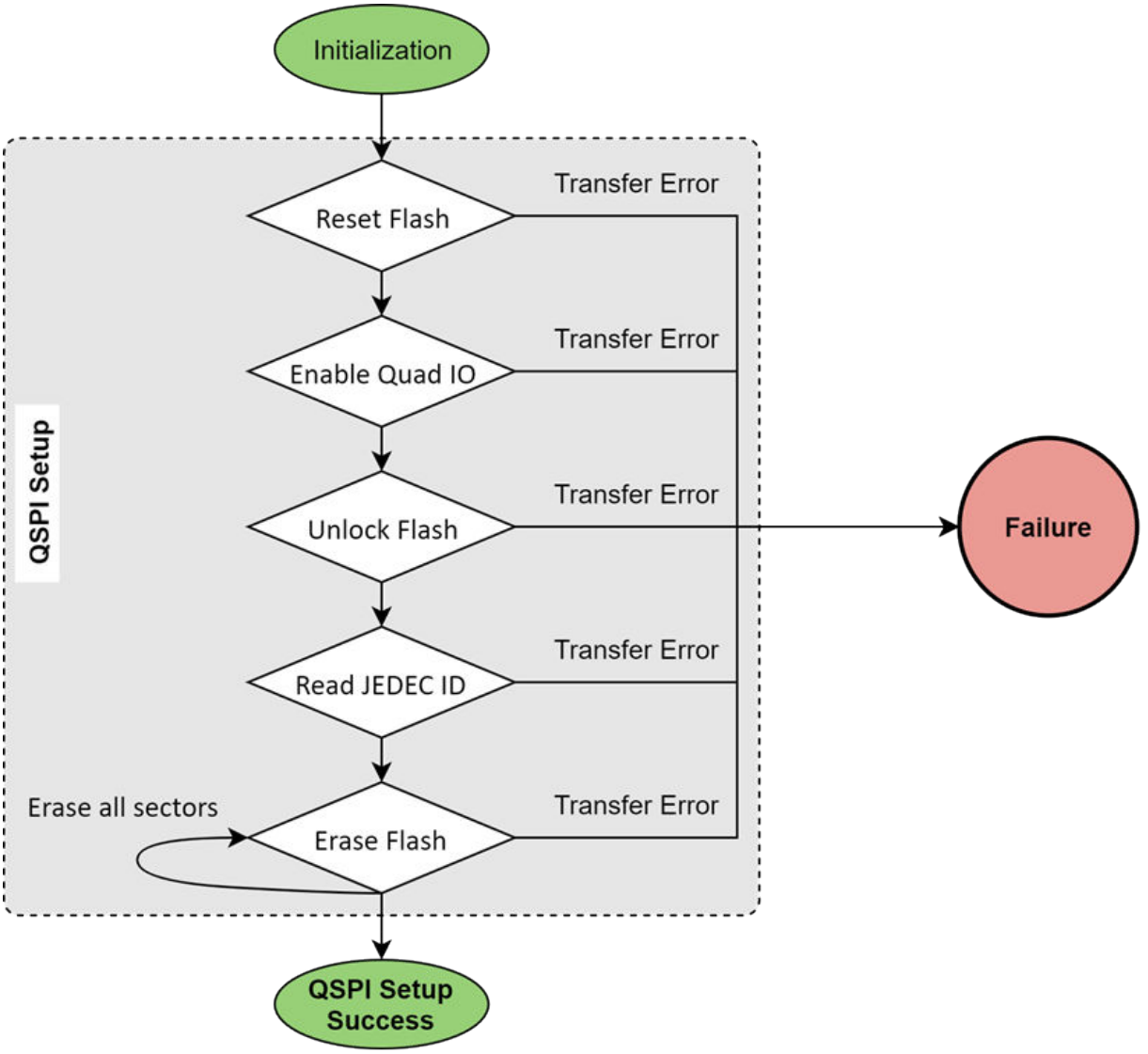
- **Initialization:** The application initializes low-level peripherals and registers to the QSPI RX/TX callback function to get the transfer complete status. The initialization sequence is shown in the following figure.

Figure 5-11. QSPI XDMAC Read/Write Initialization Flowchart



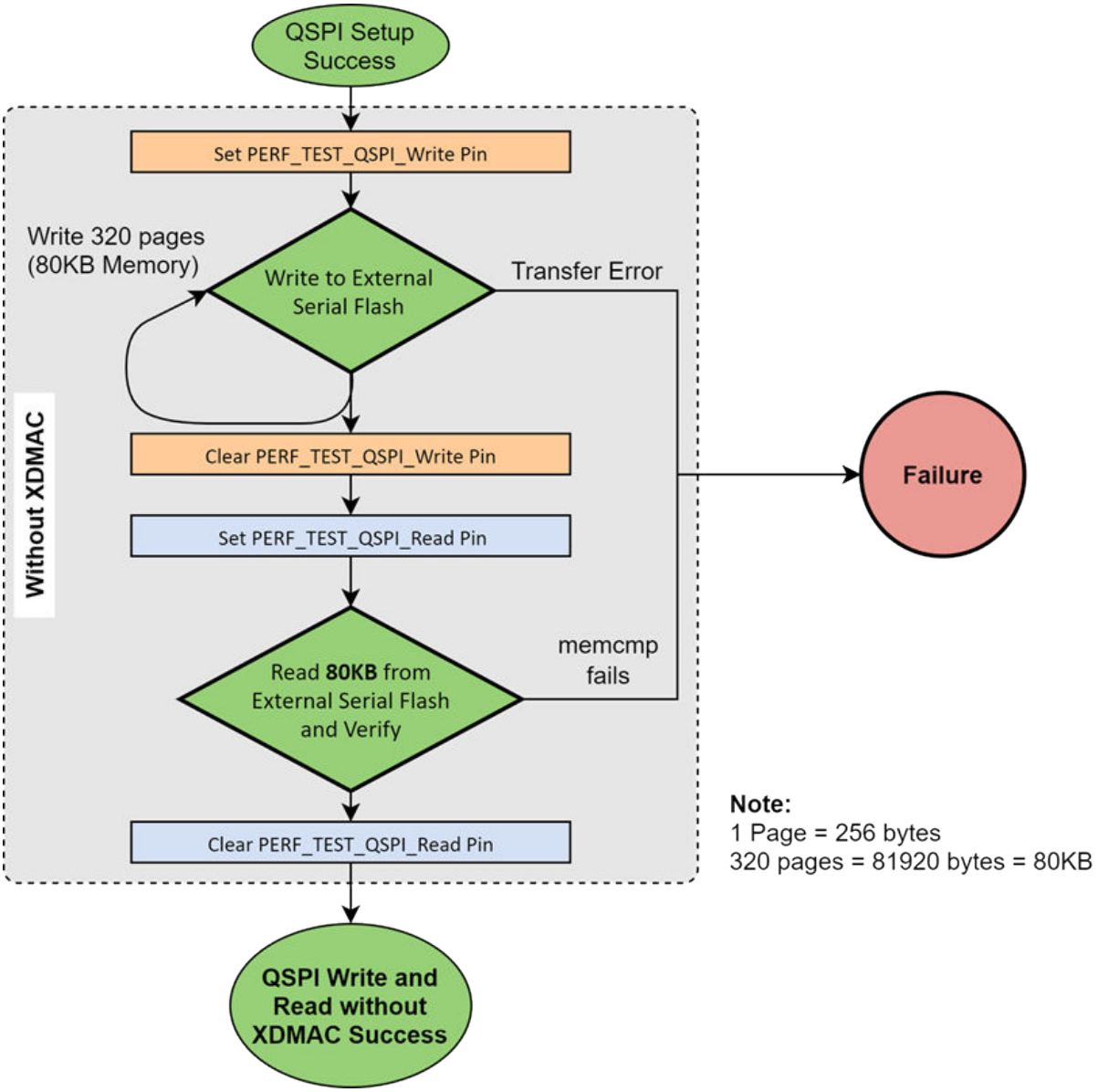
- **QSPI Setup:** The sequence of the QSPI setup includes Reset, Enable Quad I/O, Unlock, Read JEDEC ID, and Erase the Flash before proceeding with read/write operations.
  The following figure illustrates the QSPI XDMAC read/write setup flowchart.

Figure 5-12. QSPI XDMAC Read/Write Setup Flowchart



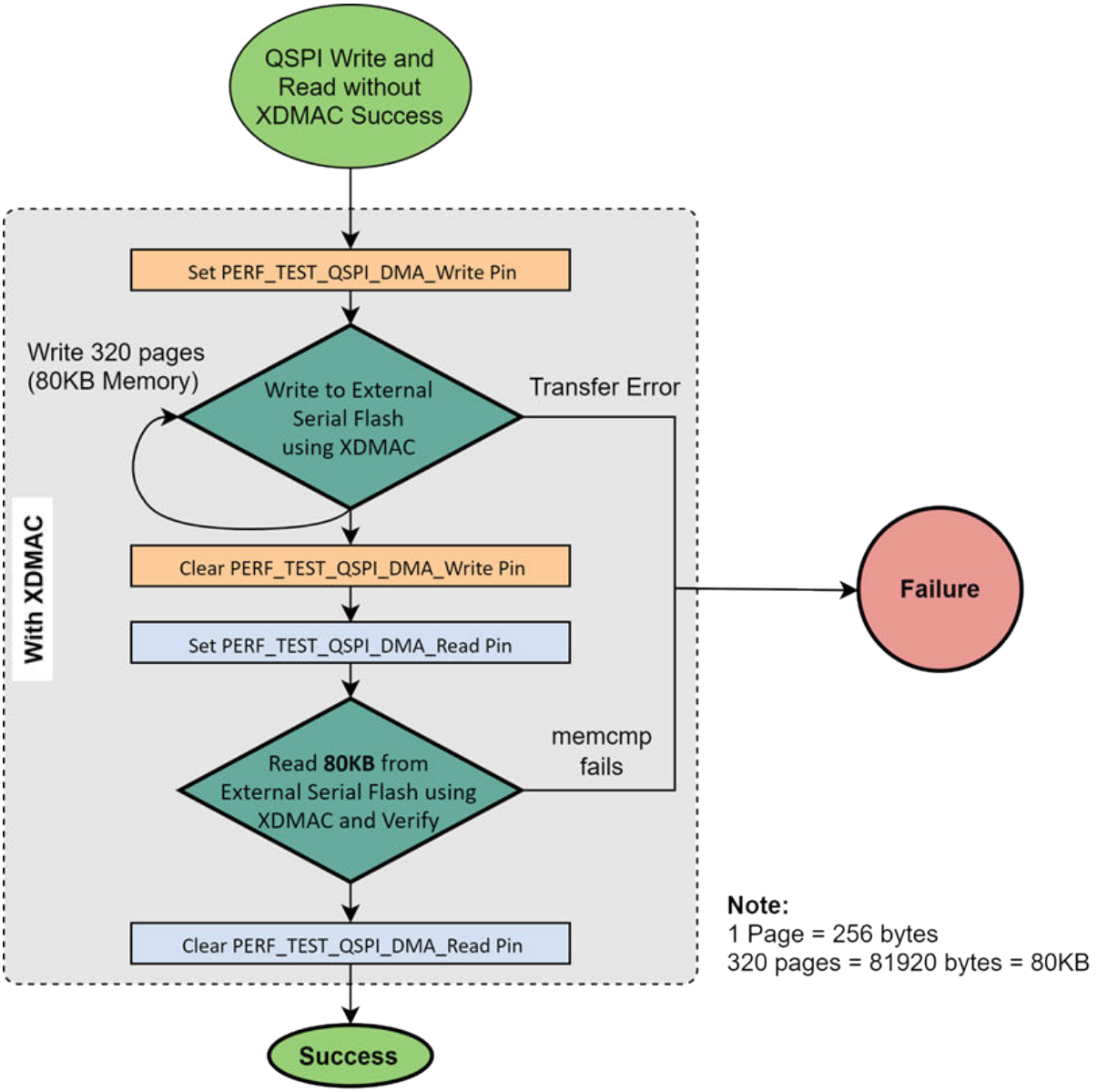
- **QSPI Read/Write without XDMAC:** The application sets the write pin before performing the data write to the external serial memory and it is cleared after a successful write operation. This is repeated for read operation. These pins are used as markers to evaluate the total time taken for the read/write operations without the XDMAC.
  The following figure illustrates the QSPI read/write without the XDMAC.

Figure 5-13. QSPI XDMAC Read/Write Without XDMAC Flowchart



- **QSPI Read/Write with XDMAC:** The application sets the write pin before performing the data write to the external serial memory using the XDMAC and it is cleared after successful write operation. This is repeated for the read with the XDMAC operation. These pins are used as markers to evaluate the total time taken for the read/write operations with the XDMAC. The following diagram illustrates the QSPI read/write with the XDMAC.

Figure 5-14. QSPI XDMAC Read/Write with XDMAC Flowchart



5.3 Running The QSPI XDMAC Read/Write Application

1. Perform the hardware setup as shown in the QSPI XDMAC Read Write Hardware Setup.
2. Connect the micro USB to the Host computer.
3. Connect the Saleae Logic Analyzer and establish a connection with the Host PC. Configure the following channels to measure the QSPI throughput as follows:
   - Channel 0 is PA19, which is configured to 'Set and Clear' the pin before and after the *QSPI Write without DMA*.
   - Channel 1 is PB2, which is configured to 'Set and Clear' the pin before and after the *QSPI Read without DMA*.
   - Channel 2 is PC31, which is configured to 'Set and Clear' the pin before and after the *QSPI Write with DMA*.
   - Channel 3 is PB3, which is configured to 'Set and Clear' the pin before and after the *QSPI Read with DMA* .

4. Open the QSPI XDMAC read/write project (*< downloaded folder > /qspi_xdmac_read_write/firmware/sam_e70_xult.X*) in the MPLAB X IDE.
5. Build the project using MPLAB X IDE and program it to the target.
6. Start capturing samples using the Logic Analyzer Software.
7. Reset the hardware to start the application run from the beginning.
8. Stop capturing the sample in the Logic Analyzer Software.
9. Toggling LED1 indicates that the QSPI read/write with or without the DMA is successful.
10. Check the above mentioned four GPIO pin waveforms and timestamps to see the QSPI performance with or without using the XDMAC. See QSPI Performance Evaluation for a detailed analysis.

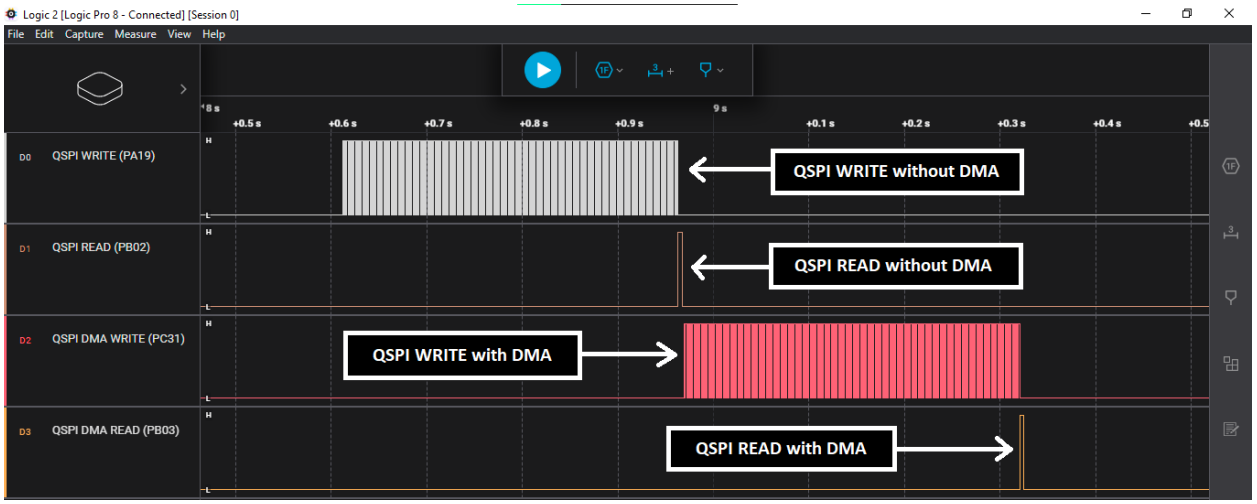
6. QSPI Performance Evaluation

The QSPI read/write performances are evaluated with or without the XDMAC. The following use cases are executed to capture the throughput of the QSPI running at 50 MHz. The time taken for the actual write or read from the External Serial Memory is captured by toggling the GPIO lines before performing the operation.

- Write 80 KB of data to external serial Flash without using the DMA
- Read 80 KB of data from the external serial Flash without using the DMA
- Write 80 KB of data to external serial Flash using the DMA
- Read 80 KB of data from the external serial Flash using the DMA

The following diagram shows these operations.

Figure 6-1. QSPI XDMAC Read/Write Throughput Measurement Overview



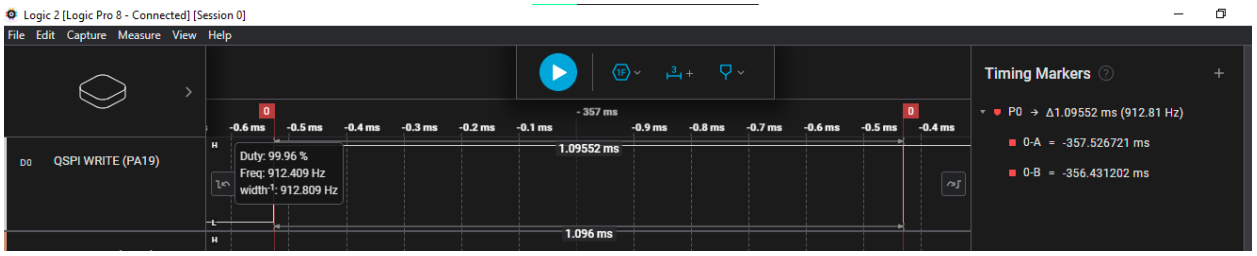
6.1 QSPI Write Without DMA

The time taken by the QSPI to write one page (256 bytes) without the DMA is 1.09552 ms.

The total time taken to write 80 KB (that is, 320 pages) of data: 320 * 1.09552 ms = 350.5664 ms.

The following figure shows the time taken to write one page into the serial external memory without DMA.

Figure 6-2. QSPI XDMAC Write Throughput Measurement Without DMA



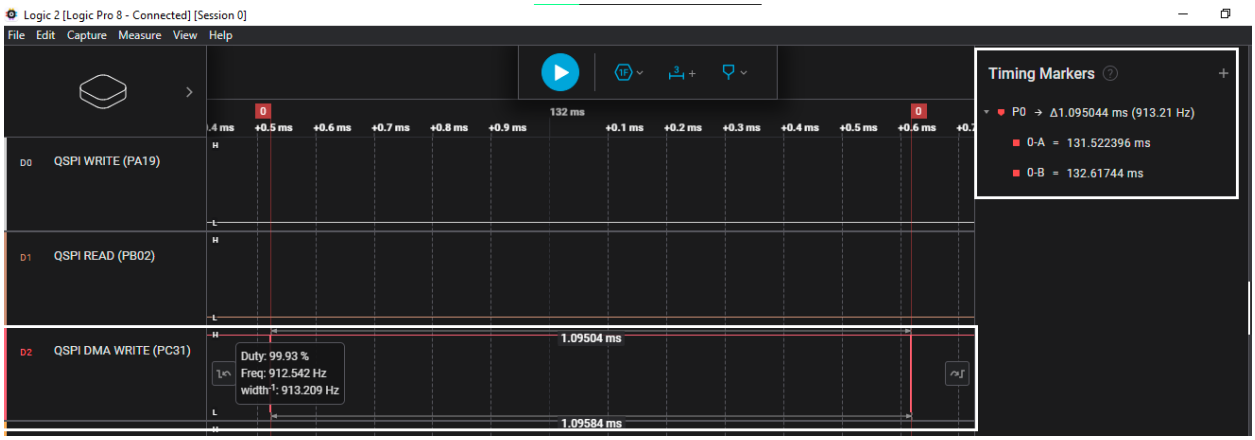
6.2 QSPI Write with DMA

The time taken by the QSPI to write one page (256 bytes) with the DMA is 1.095044 ms.

The total time taken to write 80 KB (that is, 320 pages) of data: 320 * 1.095044 ms = 350.41408 ms.

The following figure shows the time taken to write one page into serial external memory with DMA.

Figure 6-3. QSPI XDMAC Write Throughput Measurement with DMA



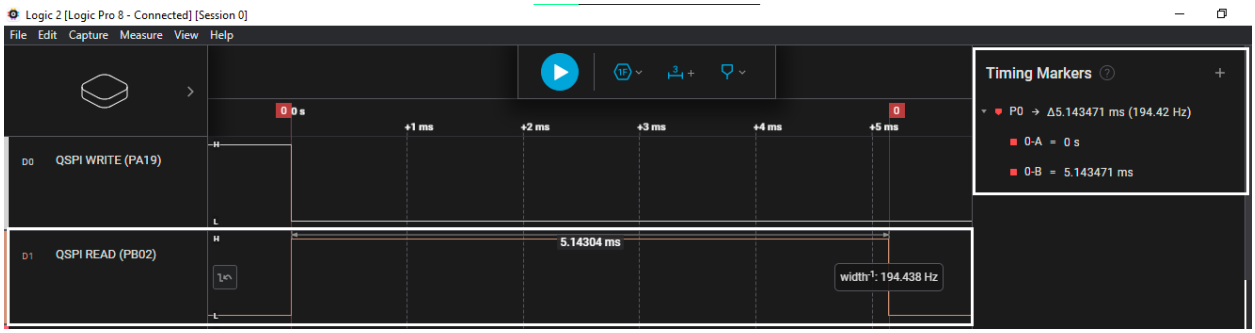
The time saved by using the XDMAC for the QSPI Write Operation: 350.5664 - 350.41408 = 0.15232 ms.

6.3 QSPI Read Without DMA

The time taken by the QSPI to read 80 KB of data without the DMA is 5.14304 ms.

The following figure shows the timestamp.

Figure 6-4. QSPI XDMAC Read Throughput Measurement Without DMA



6.4 QSPI Read With DMA

The time taken by the QSPI to read one 80 KB of data with the DMA is 3.99216 ms.

The time saved by using the DMA for the QSPI Read Operation: 5.14304 - 3.99216 = 1.15088 ms.

The following figure shows the timestamp.

Figure 6-5. QSPI XDMAC Read Throughput Measurement With DMA

7. Conclusion

The QSPI can be used in conjunction with the Direct Memory Access Controller (XDMAC) to reduce the processor overhead.

QSPI write with DMA: The performance evaluation test results show there is not much performance improvement in the QSPI write with the XDMAC. Because the QSPI is configured to run at high speed (that is, 50.0 MHz) and each write operation involves writing one page (that is, 256 bytes) at a time. Therefore, with the DMA there is not much improvement in the QSPI write throughput except that the CPU can off-load the write task to the XDMAC, which allows the CPU to execute other high-priority tasks.

QSPI read with DMA: The performance evaluation test results show a significant improvement in the QSPI read throughput when the XDMAC is used for reading the data from the external serial memory. Also, the CPU can off-load this task to the XDMAC and can execute other high-priority tasks.

8. References

The following documents are used as reference. For additional information, visit the Microchip website or contact a local Microchip sales office.

- Execute in place with QSPI using ASF:
  ww1.microchip.com/downloads/en/DeviceDoc/Atmel-44065-Execute-in-Place-XIP-with-Quad-SPI-Interface-SAM-V7-SAM-E7-SAM-S7_Application-Note.pdf
- AT17417: Usage of XDMAC on SAM S/SAM E/SAM V:
  ww1.microchip.com/downloads/en/DeviceDoc/Atmel-42761-Usage-of-XDMAC-on-SAMS-SAME-SAMV_ApplicationNote_AT17417.pdf
- Execute in place with QSPI using MPLAB Harmony 3
  ww1.microchip.com/downloads/en/Appnotes/Execute-In-Place%20_with_QSPI_on_%20Cortex-M7_MCUs_Using_MPLAB_Harmony_v3_DS00003443A.pdf
- SAM E70 Xplained Ultra User's Guide:
  ww1.microchip.com/downloads/en/DeviceDoc/SAM-E70-Xplained-Ultra-User-Guide-70005389A.pdf
- SAM E70/S70/V70/V71 Family Data Sheet:
  ww1.microchip.com/downloads/aemDocuments/documents/MCU32/ProductDocuments/DataSheets/SAM-E70-S70-V70-V71-Family-Data-Sheet-DS60001527.pdf
- For additional information about 32-bit Microcontroller Collaterals and Solutions, refer to:
  DS70005534: 32-bit Microcontroller Collateral and Solutions Reference Guide
- For other relevant information, refer to the Microchip web site

9. Revision History

Revision B - 08/2024

The following updates were performed for this revision:

- Throughout the document all references to the MHC were converted to the MCC
- Updated Software versions and website links for the following sections:
  - SAM E70 Xplained Ultra Evaluation Kit
  - MPLAB X Integrated Development Environment and XC Compilers
  - MPLAB Harmony v3
- Updated terminology, links and images in the following sections to reflect the tool update to the MCC:
  - Memory-to-Memory Transfer
  - MPU Configuration for QSPI
  - QSPI XDMAC Read/Write MPLAB Harmony v3 Application
  - QSPI Performance Evaluation
  - QSPI Write Without DMA
  - QSPI Write with DMA
  - QSPI Read Without DMA
  - QSPI Read With DMA
- Updated References with new links to reflect the tool update

Revision A - 05/2020

This is the initial release of the document.

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