UG0478
User Guide
IGLOO2 FPGA Evaluation Kit

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Power Matters.™

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 5.0

Updated all Microsemi links with Microchip links.

1.2 Revision 4.1

Libero SoC software license information was updated from Gold to Silver. For more information, see Software Settings, page 6.

1.3 Revision 4.0

The following is a summary of the changes in revision 3.0 of this document.

- Throughout the document, figures were updated in accordance with revision E of the IGLOO2 M2GL-EVAL-KIT.
- Information about jumper settings was updated. For more information, see Jumper Settings, page 6.
- Information about the LPDDR SDRAM interface was updated. For more information, see Mobile LPDDR SDRAM, page 12.
- Information about programming the device for the manufacturing test was updated. For more information, see FPGA Programming Using Embedded FlashPro5, page 49.

1.4 Revision 3.0

Updated LPDDR resolution changes (SAR 52540, SAR 57285, SAR 61490, SAR 53271).

1.5 Revision 2.0

Added the recommended cable (SAR 53759).

1.6 Revision 1.0

Updated Manufacturing Test, page 40 (SAR 52040).

2 Introduction

The RoHS-compliant IGLOO®2 FPGA Evaluation Kit (M2GL-EVAL-KIT) enables you to develop the following types of applications:

- Motor control
- System management
- Industrial automation
- High-speed serial I/O applications:
  - Peripheral component interconnect express (PCIe)
  - Serial-gigabit media independent interface (SGMII)
  - User-customizable serial interfaces

2.1 Kit Contents

The following table lists the contents of the IGLOO2 Evaluation Kit.

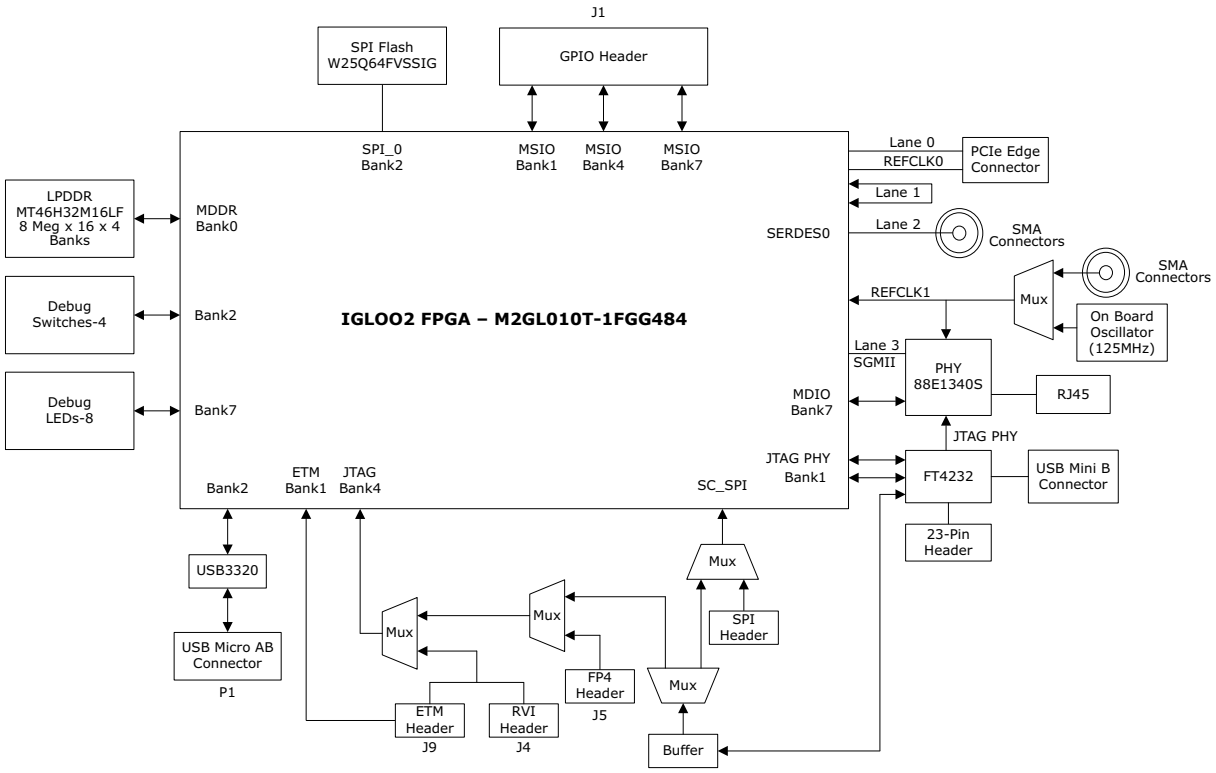
Table 1 • **Kit Contents**

Item	Quantity
IGLOO2 Evaluation Board with M2GL010T-1FGG484 device	1
FlashPro4 JTAG programmer for programming and debugging the IGLOO2 device	1
USB A male to mini-USB B male cable for UART/power interface (up to 1A) to PC	1
+12 V/2 A wall-mounted power supply	1
Quickstart card	1

2.2 Block Diagram

The following figure is the block diagram of the IGLOO2 FPGA Evaluation Kit.

Figure 1 • **IGLOO2 Evaluation Kit Block Diagram**



2.3 Web Resources

For more information about the M2GL-EVAL-KIT, see *https://www.microchip.com/en-us/development-tool/m2gl-eval-kit#Overview*.

2.4 Board Description

The IGLOO2 Evaluation Kit offers a full-featured evaluation board for IGLOO2 FPGAs. The kit integrates the following on a single chip:

- Reliable flash-based FPGA fabric
- Advanced security processing accelerators
- Digital signal processing (DSP) blocks
- Static random-access memory (SRAM)
- Embedded non-volatile memory (eNVM)
- High-performance communication interfaces

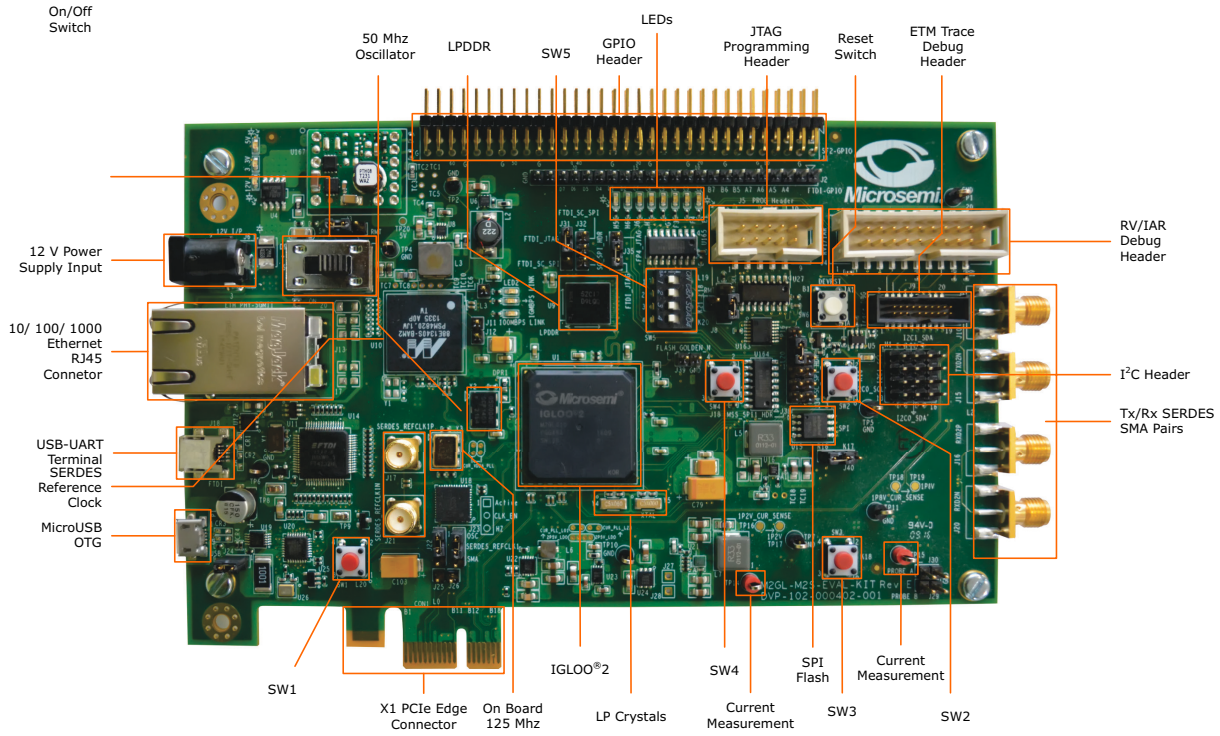
The board has several interfaces including an RJ45 connector for 10/100/1000 Ethernet, a full-duplex serializer/deserializer (SerDes) lane connected through Subminiature version A (SMA) connectors, a 64-bit GPIO header, and various connectors for SPI support.

The IGLOO2 memory management system supports 512 Mb on-board mobile LPDDR SDRAM memory and 64 Mb SPI flash memory. The SerDes block can be accessed either through the PCIe edge connector or using high-speed SMA connectors.

The printed circuit board (PCB) supports the M2GL010T device in an FGG484 package. The board has eight layers and is manufactured with FR4 dielectric material.

The following figure is a snapshot of the IGLOO2 Evaluation Board with its engineering silicon.

Figure 2 • **IGLOO2 FPGA Evaluation Kit Board**



Note: Microchip recommends using a 12-inch SMA male to SMA male Precision Cable using the RoHS-compliant PE-SR405FLJ coax with the IGLOO2 Evaluation Kit. For more information, see *http://www.pasternack.com/sma-male-sma-male-pe-sr405flj-cable-assembly-pe39429-12-p.aspx*.

2.5 Board Key Components

The following table lists key components of the IGLOO2 FPGA Evaluation Kit.

Table 2 • **IGLOO2 FPGA Evaluation Board Components**

Name	Description
M2GL010T-1FGG484	Microchip IGLOO2 FPGA
Mobile low-power DDR SDRAM	512 Mb (MT46H32M16LF – 8 Meg × 16 × 4 banks) for storing the data bits
SPI flash	64 Mb Winbond electronics W25Q64FVSSIG SPI flash connected to SPI port 0 of the IGLOO2 FPGA high-performance memory system (HPMS)
Ethernet	RJ45 connector (Ethernet jack with built-in magnetics) interfacing with Marvell 10/100/1000 BASE-T PHY chip 88E1340S in serial gigabit media independent interface (SGMII) mode, which, in turn, interfaces with the Ethernet port of the IGLOO2 FPGA (on-chip MAC and external PHY).
RVI header	RVI header for application programming and debugging from Keil ULINK or IAR J-Link
FP4 header	FlashPro4 programming header for programming and debugging the IGLOO2 FPGA using Microchip tools
Future Technology Devices International (FTDI) programmer	FTDI programmer interface (J18) to program the external SPI flash
Embedded trace macro (ETM) cell header	ETM header for debugging
GPIO header	General purpose input/output (GPIO) header for multi-standard I/O (MSIO) signals to be routed
PCIe edge connector	PCIe edge connector with one lane
Dual in-line package (DIP) switch	Debug switch for user applications
Light-emitting diodes (LEDs)	Eight active-low LEDs that are connected to some of the user I/Os for debug and three active-high LEDs that are used for power supply indication
Push-button reset	Push-button system reset for the IGLOO2 system
Push-button switches	Four push-button switches for test and navigation
USB interface	USB micro AB connector, interfacing with the high speed USB2.0 ULPI transceiver chip USB3320 which, in turn, interfaces with the FPGA pins of the IGLOO2 HPMS
OSC-125	125 MHz clock oscillator with differential output
OSC-50	50 MHz clock oscillator
OSC-32	32.768 KHz low-power oscillator

3 Installation and Settings

This section provides information about software and hardware settings required to run the pre-programmed demo design in the IGLOO2 Evaluation Kit.

3.1 Software Settings

1. Download and install the latest release of Microchip's Libero® SoC.
2. Generate your free Silver license at Microchip Portal.

The Libero SoC installer includes the required device programmer drivers. See the following references:

- For more information about the instructions about licensing and installing Libero SoC, see the Libero SoC Documentation.
- For more information about installing SoftConsole, see the SoftConsole page.
- For more information about downloading and installing Microchip's DirectCores on the Host PC where Libero SoC is installed, see the IP Core Tools.
- For more information about downloading and installing Microchip's firmware drivers on the Host PC where Libero SoC is installed, see the Firmware Catalog Documentation.

3.2 Hardware Settings

This section provides information about jumper settings, switches, LEDs, and DIP switches in the pre-programmed demo design.

3.2.1 Jumper Settings

Connect the jumpers with the settings specified in the following table to evaluate the pre-programmed demo design.

Table 3 • **Jumper Settings**

Jumper	Description	Pins	Default Setting
J23	Jumper to select switch-side MUX inputs of A or B to the line side	Pin 1-2 (input A to the line side) that is on board 125 MHz differential clock oscillator output will be routed to line side	Closed
		Pin 2-3 (input B to the line side) that is external clock required to source through SMA connectors to the line side	Open
J22	Jumper to select the output enable control for the line side outputs	Pin 1-2 (line-side output enabled)	Closed
		Pin 2-3 (line-side output disabled)	Open
J24	Jumper to provide the VBUS supply to USB when using in Host mode		Open
J8	JTAG selection jumper to select between RVI header or FP4 header for application debug	Pin 1-2 FP4 for SoftConsole/FlashPro	Closed
		Pin 2-3 RVI for Keil ULINK/IAR J-Link	Open
		Pin 2-4 for toggling JTAG_SEL signal remotely using the GPIO capability of the FT4232 chip	Open

Table 3 • Jumper Settings (continued)

J3	Jumper to select either the SW2 input or the ENABLE_FT4232 signal from the FT4232H chip	Pin 1-2 for manual power switching using the SW7 switch	Closed
		Pin 2-3 for remote power switch using the GPIO capability of the FT4232 chip	Open
J31	Jumper to select between FTDI JTAG programming and FTDI slave programming	Pin 1-2 for FlashPro FTDI JTAG programming	Closed
		Pin 2-3 for SPI slave programming	Open
J32	Jumper to select between FTDI SPI and SC_SCI header	Pin 1-2 for programming through FTDI SPI	Closed
		Pin 2-3 for programming through SC_SPI header	Open
J35	Jumper to select between FP4 Header and FTDI JTAG	Pin 1-2 for programming through FP4 header	Closed
		Pin 2-3 for programming through FTDI JTAG	Open

For the locations of various jumpers and test points on the IGLOO2 Evaluation Board, see Figure 18, page 37 and Figure 19, page 38.

3.2.2 LEDs

The following table lists the power supply and Ethernet LEDs in the pre-programmed demo design.

Table 4 • LEDs in Pre-Programmed Demo Design

LED	Comment
DS1 - Green	Indicates the 5 V rail
DS2 - Green	Indicates the 3.3 V rail
DS3 - Green	Indicates the 12 V power source
DS5 - Green	Connected to parallel LED output port 0 (P0_LED[0]) of Marvell PHY
DS4 - Green	Connected to parallel LED output port 0 (P0_LED[2]) of Marvell PHY
DS6 - Green	Connected to parallel LED output port 0 (P0_LED[3]) of Marvell PHY

3.2.3 Test Points

The following table lists the USB, ground, and other test points for the pre-programmed demo design.

Table 5 • Test Points for Pre-Programmed Demo Design

Test Point	Description
TP8	USB switch in/out for DP signal
TP9	USB switch in/out for DM signal
TP1, TP2, TP4, TP5, TP6, TP7, TP10, TP11	Ground
TP3	Test point for DDR_VTT
TP12	Test point to measure the voltage at TP12 with reference to ground
TP14	1.2 V current sensing test point

Table 5 • **Test Points for Pre-Programmed Demo Design**

TP15	1.8 V current sensing test point
TP16, TP17	Test points across current sense resistor 0.05 Ω for 1.2 V
TP18, TP19	Test points across current sense resistor 0.05 Ω for 1.8 V

3.3 Power Sources

All the power supply devices used in the IGLOO2 Evaluation Kit are Microchip devices. For more information about power supply devices, see Microchip's Power Management Devices.

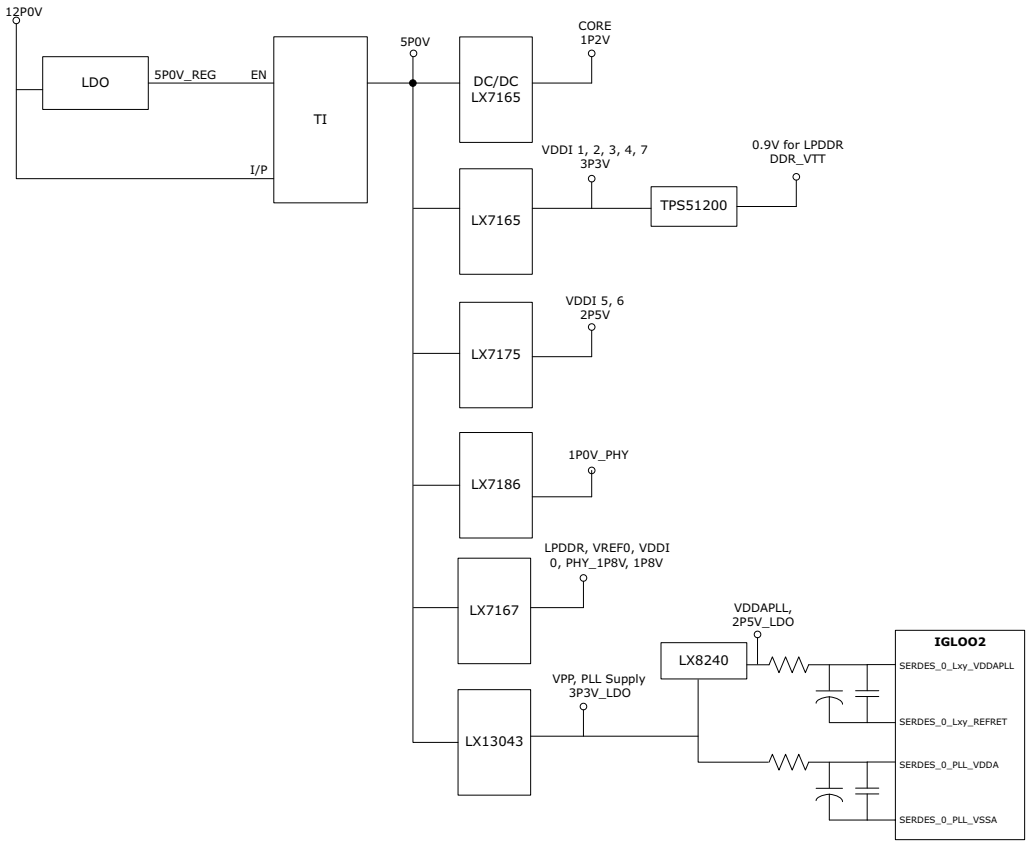
The following table lists the key power supplies required for normal operation of the IGLOO2 Evaluation Kit.

Table 6 • **I/O Voltage Rails**

IGLOO2 Bank	I/O Rail	Voltage
Bank 0	VDDI0	1.8 V
Bank 1	VDDI1	3.3 V
Bank 2	VDDI2	3.3 V
Bank 3	VDDI3	3.3 V
Bank 4	VDDI4	3.3 V
Bank 5	VDDI5	2.5 V
Bank 6	VDDI6	2.5 V
Bank 7	VDDI7	3.3 V

The following figure shows voltage rails (12 V, 5 V, 3.3 V, 2.5 V, 1.8 V, 1.5 V, and 1.0 V) available in the IGLOO2 Evaluation Kit.

Figure 3 • **Voltage Rails in the IGLOO2 FPGA Evaluation Kit**



3.4 Testing the Hardware

If the board is shipped directly from Microchip, it contains a test program that determines whether or not the board works properly. If you suspect that the board is damaged, you can rerun the manufacturing test to verify the key interfaces of the board functionality. For more information, see Manufacturing Test, page 40.

4 Key Components Description and Operation

This chapter describes the key component interfaces of the IGLOO2 Evaluation Kit. For device datasheets, go to IGLOO2 Documentation page.

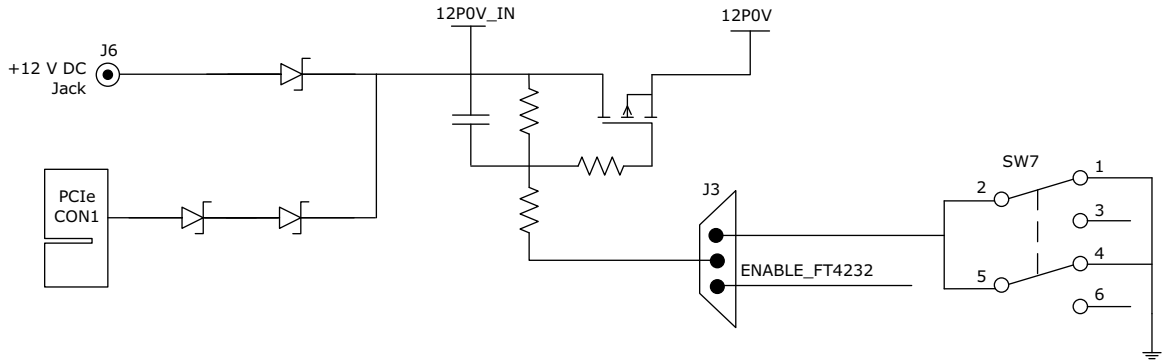
4.1 Powering Up the Board

The IGLOO2 Evaluation Board is powered by a 12 V power source using either of the two 12 V sources—the external +12 V/2 A DC jack or the PCIe connector, as shown in the following figure. Protection mechanism enables the external DC jack supply if both the sources are available simultaneously.

When both the power sources are ON, the board draws power from the external DC jack as diode D3 becomes reverse-biased and the path is let open for 12P0_PCIE. When external DC voltage is not present, the board can be powered up using the PCIe connector.

The following figure shows then power-up flow for the IGLOO2 Evaluation Board.

Figure 4 • **Powering Up the Board**



4.2 Current Measurement

This section provides information about current sensing for various modes.

4.2.1 1.2 V Current Sensing for Normal Operation

For applications that require current measurement, high-precision operational amplifier circuitry (U31 with gain 100) is placed on the board to measure the output voltage at test point TP14 with reference to the ground.

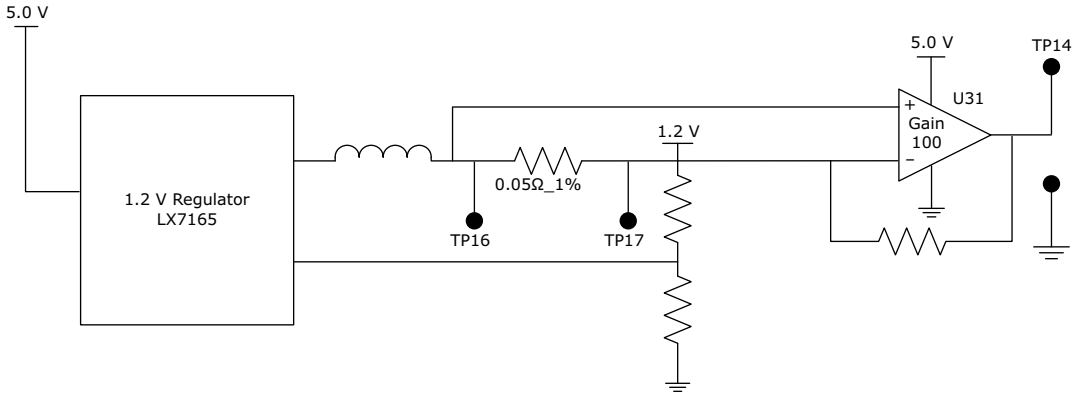
The following steps describe how to measure the core power:

1. Measure the output voltage (V_{OUT}) at TP14.
2. I = (V_{OUT}/5).
3. Core power consumed (P) = (1.2 V) × I.

For example, when the voltage measured across TP14 as 0.5 V, the core power consumed is 0.12 W.

The following figure shows the on-board core power measurement circuitry.

Figure 5 • **Core Power Measurement**



4.2.2 1.2 V Current Sensing for Flash*Freeze

The IGLOO2 device consumes very low power in Flash*Freeze mode. The voltage across the sense resistor (0.05 Ω) must be measured directly using a precision digital multimeter that can read sub-millivolts. Test points TP16 and TP17 can be used to directly measure voltage across the 1.2 V sense resistor.

To convert the voltage measured across a sense resistor to power, use the following equation:

$$\text{Power} = \left(\frac{\text{voltage\_in\_millivolts}}{0.05}\right) \times 1.2$$

4.2.3 1.8 V Current Sensing

For applications that require current measurement, high-precision operational amplifier circuitry (U32 with gain 100) is placed on the board to measure the output voltage at test point TP15 with reference to the ground.

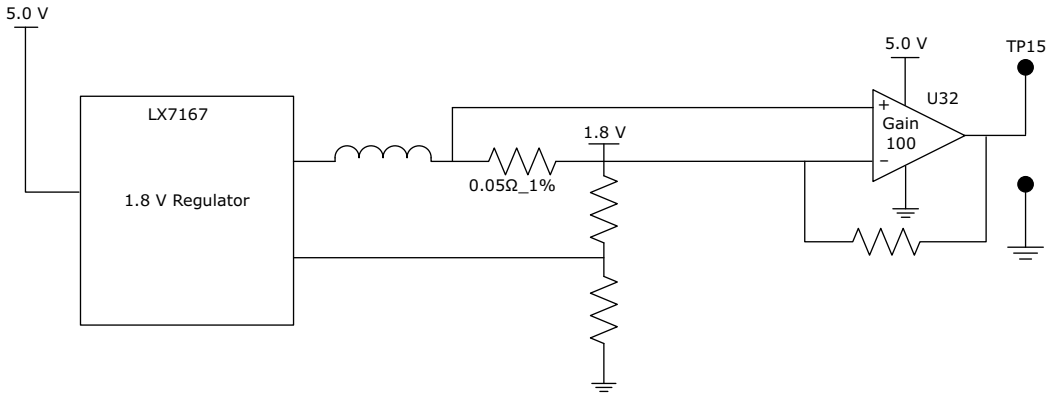
The following steps describe how to measure 1.8 V power:

1. Measure the output voltage (V_{OUT}) at TP15.
2. I = (V_{OUT}/5).
3. Power consumed (P)= (1.8 V) × I.

For example, when the voltage measured across TP15 as 0.5 V, the power consumed is 0.18 W.

The following figure shows the on-board 1.8 V power measurement circuitry.

Figure 6 • **1.8 V Power Measurement**

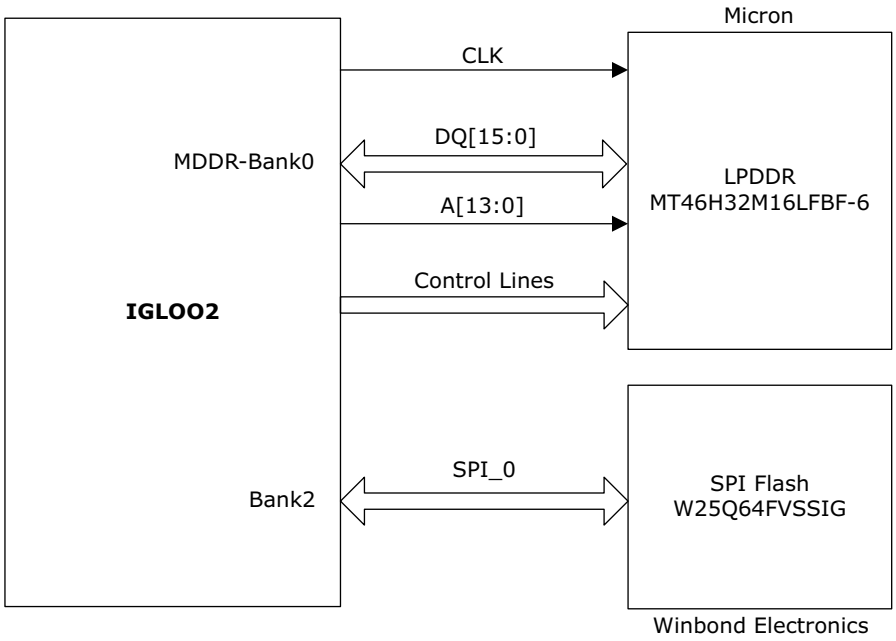


Note: Accuracy is ± 10%.

4.3 Memory Interface

Dedicated I/Os for HPMS DDR and fabric DDR are available in the IGLOO2 device. In addition to dedicated I/Os, regular I/Os can also be used to connect to other memory devices, as shown in the following figure.

Figure 7 • **IGLOO2 Memory Interface**



4.3.1 Mobile LPDDR SDRAM

An individual chip with 512 Mb LPDDR SDRAM memory is provided in the IGLOO2 device to serve as flexible volatile memory for user applications. The LPDDR interface is implemented in bank 0.

LPDDR SDRAM specifications for the IGLOO2 device are as follows:

- MT46H32M16LF: 8 Meg × 16 × 4 banks
- Density: 512 Mb
- Data rate: LPDDR 16-bit at 166 MHz clock rate

For more information, see the Board Level Schematics document (provided separately).

The IGLOO2 Evaluation Kit design uses the LPDDRI and LVCMOS18 standards for the LPDDR interface. The default board assembly available for the LPDDRI standard has RC terminations. The LVCMOS18 I/O standard has lower power characteristics than the LPDDRI (SSTL18) standard for LPDDR memories. To achieve low power characteristics (LPDDR in LVCMOS18 mode), change the I/O type in the design example to LVCMOS18.

4.3.2 SPI Serial Flash

SPI flash specifications for the IGLOO2 device are as follows.

- Density: 64 Mb
- Voltage: 2.7 V to 3.6 V
- Frequency: 104 MHz
- SPI mode support: Modes 0 and 3
- IGLOO2 HPMS: SPI0 interfaced to SPI flash

For more information, see the Board Level Schematics document (provided separately).

4.4 SERDES0 Interface

The SERDES0 has four lanes, connected as follows.

1. Lane 0 is directly routed to the PCIe connector.
   - TX pad > trace > AC coupling > trace > via (to bottom layer) > trace > PCIe connector pad
   - RX pad > trace > PCIe connector pad
2. Lane 1 is used for loopback testing. This path is routed between the TX and RX pads with a 6-inch trace and two vias.
   - TX pad via (to bottom layer) > trace > AC coupling > trace > via (to top layer) > RX pad
3. Lane 2 is routed to SMA connectors.
   - TX pad > trace > AC coupling > trace > SMA connector pad
   - RX pad > trace > via (to bottom layer) > trace > via (to top layer) > SMA connector pad
4. Lane 3 is routed to Marvell PHY 88E1340S.
   - TX pad > trace > AC coupling > trace > via > trace routed in sixth layer > via (to top layer) > Marvel PHY pin
   - RX pad > via > trace routed in sixth layer > via (to top layer) > trace > AC Coupling > trace > Marvel PHY pin

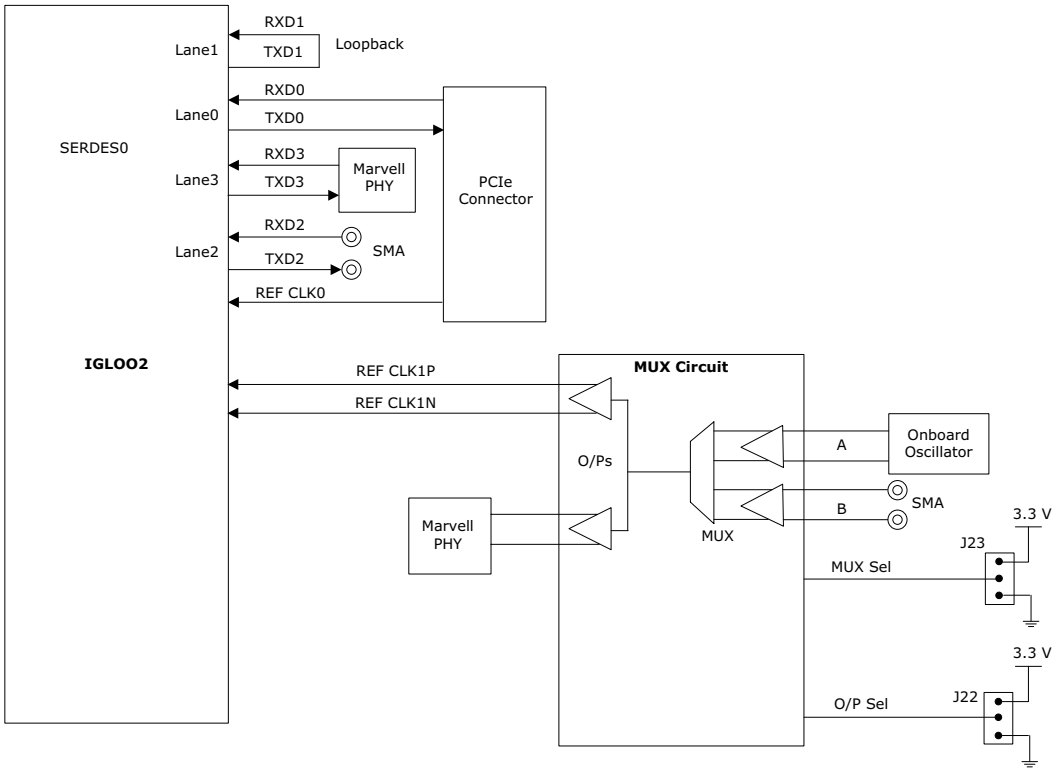
SERDES0 reference clock 0 is routed directly from the PCIe connector to IGLOO2 device. SERDES0 reference clock 1 is routed from the on-board 125 MHz clock oscillator and optionally routed from SMA connectors through LVDS MUX or buffer chip.

The expected SerDes reference clock specifications are as follows.

- Voltage level: 3.3 (± 0.3) V
- Differential LVDS
  - Symmetry: 50% (± 10%)
  - Rise/fall time: Maximum 1 ns @ 20% to 80% of supply (3.3 V)
  - Output voltage levels: 0 = 0.90 minimum, 1.10 typical; 1 = 1.43 typical, 1.60 maximum
  - Differential output voltage: 247 mV minimum, 454 mV maximum

The following figure shows the SERDES0 interface of the IGLOO2 Evaluation Board.

Figure 8 • **SERDES0 Interface**



For more information about **J22** and **J23** jumpers, see Table 3, page 6.

Notes:

- SERDES0 TXD pairs are capacitively coupled to the IGLOO2 device. Serial AC-coupling capacitors are used to provide common-mode voltage independence.
- AC-coupling capacitors are not provided for SERDES 0 RXD signals. The mating board must have the AC-coupling capacitors.

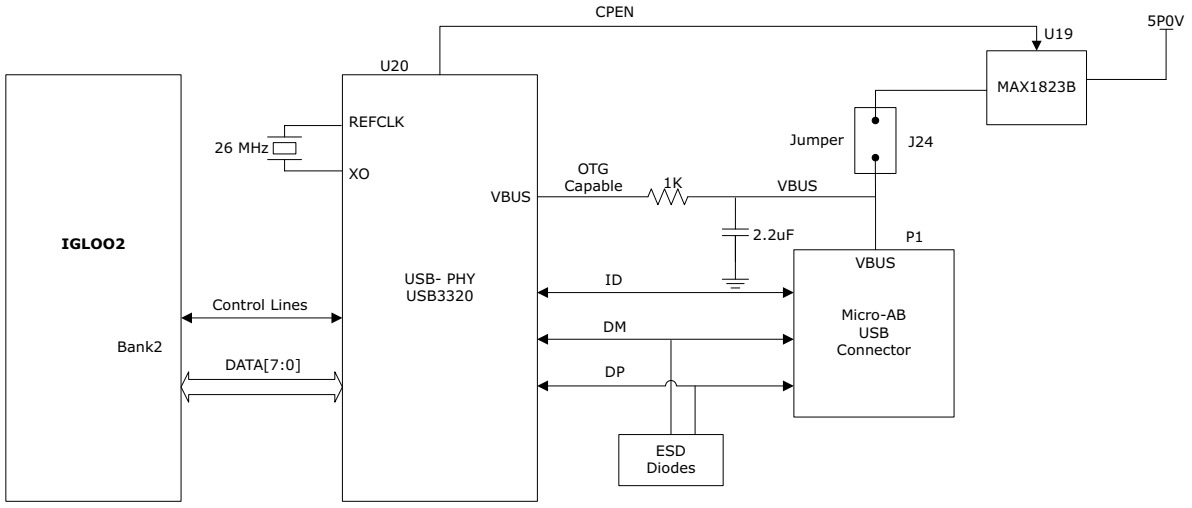
For more information, see the of Board Level Schematics document (provided separately).

4.5 USB Interface

The following figure shows the USB interface of the IGLOO2 Evaluation Board. The SMSC USB3320 shown in the figure is a high-speed USB 2.0 ULPI transceiver that supports the optional OTG protocol. CPEN is the external 5 V supply enable pin that controls the external VBUS power switch.

The following figure shows the USB interface of the IGLOO2 Evaluation Board.

Figure 9 • **USB Interface**



For more information, see the Board Level Schematics document (provided separately).

4.6 Marvell PHY (88E1340S)

The IGLOO2 Evaluation Kit uses the on-board Marvell Alaska physical layer (PHY) device (88E1340S) for Ethernet communications at 100 or 1000 Mbps. Device 88E1340S has four independent gigabit Ethernet transceivers; however, the board uses only one of the transceivers. Each transceiver performs all the physical layer functions for 100BASE-TX and 1000BASE-T full-duplex or half-duplex Ethernet on a CAT5 twisted-pair cable. The PHY device is connected to a user-provided Ethernet cable through an RJ45 connector with built-in magnetics.

Device 88E1340S supports Quad SGMII for direct connection to an IGLOO2 chip (see Figure 10, page 15). It is configured through the CONFIG [3:0] pins and the CLK_SEL [1:0] register.

The CLK_SEL [1:0] register is used to select the reference clock input option. On the board, the status of the CLK_SEL0 is *high* and the status of CLK_SEL1 is *low*. REF_CLK is the 125 MHz reference differential clock input. It consists of LVDS differential inputs with a 100Ω differential internal termination resistor.

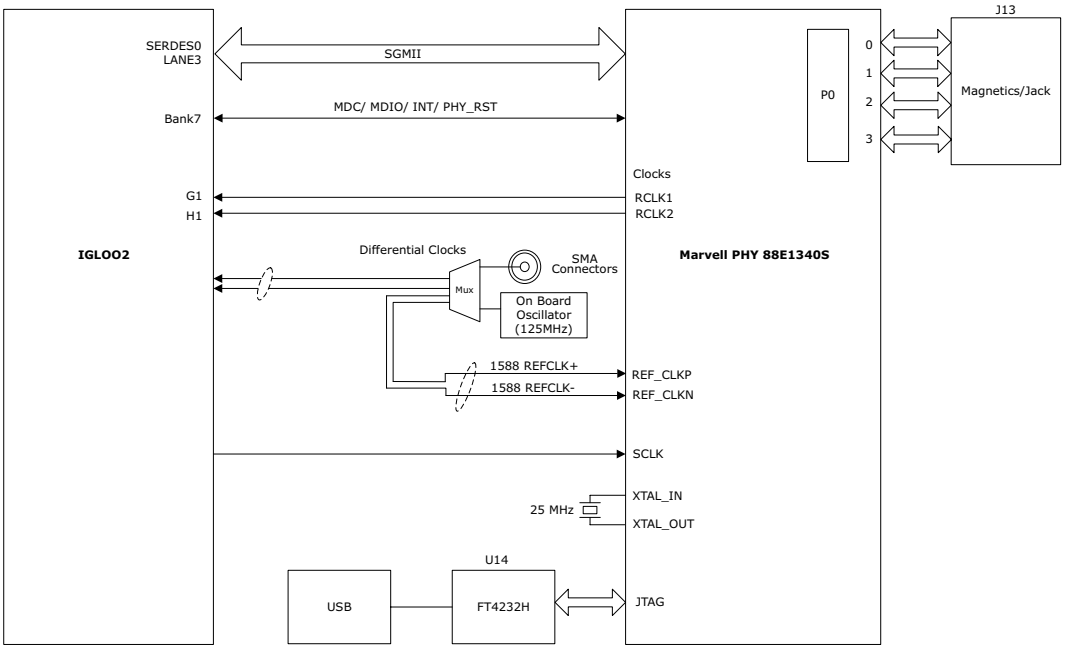
Key features of Marvell PHY 88E1340S are as follows:

- RCLK: Gigabit recovered clock
- SCLK: 25 MHz synchronous input reference clock

- Expected reference clock (REF_CLK) specifications:
  - Voltage level: 3.3 (± 0.3) V
  - Differential LVDS
    - Symmetry: 50% (± 10%)
    - Rise/fall time: Maximum 1 ns @ 20% to 80% of supply (3.3 V)
    - Output voltage levels: 0 = 0.90 minimum, 1.10 typical; 1 = 1.43 typical, 1.60 maximum
    - Differential output voltage: 247 mV minimum, 454 mV maximum

The following figure shows the IGLOO2 Marvell PHY interface.

Figure 10 • **Marvell PHY Interface**

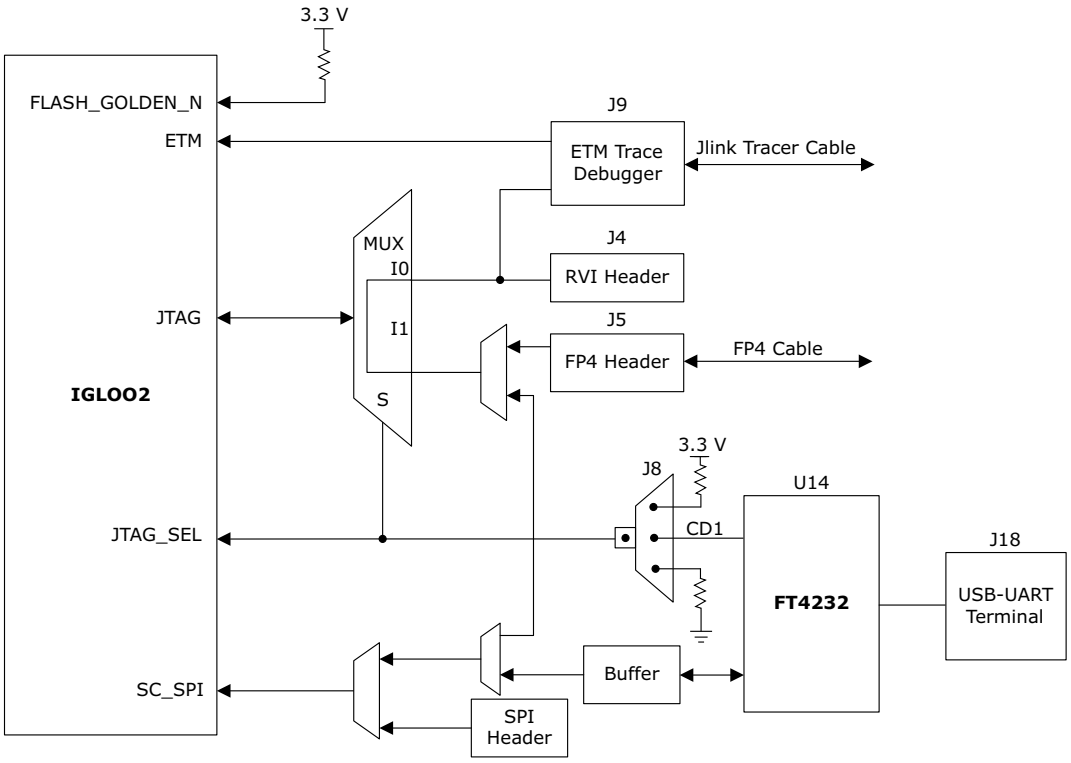


For more information, see the Board Level Schematics document (provided separately).

4.7 Programming

The IGLOO2 device can be programmed through the JTAG interface. The following figure shows various ways of programming the device.

Figure 11 • **IGLOO2 Programming Interface**



JTAG_SEL: JTAG_SEL is used to switch between the FlashPro4 header (high) and the RVI header or ETM header (low). For more information on the **J8** jumper, see Table 3, page 6.

RVI header: One 10 × 2 RVI header is provided on the board for debugging. This header allows plugging in the Keil ULINK debugger or IAR J-Link debugger.

FlashPro4 programming header: The IGLOO2 device in the evaluation kit can be programmed using the FlashPro4 programmer. FlashPro4 is also used for debugging the software using SoftConsole.

For more information, see the Board Level Schematics document (provided separately) and the *IGLOO2 and SmartFusion2 Programming User Guide*.

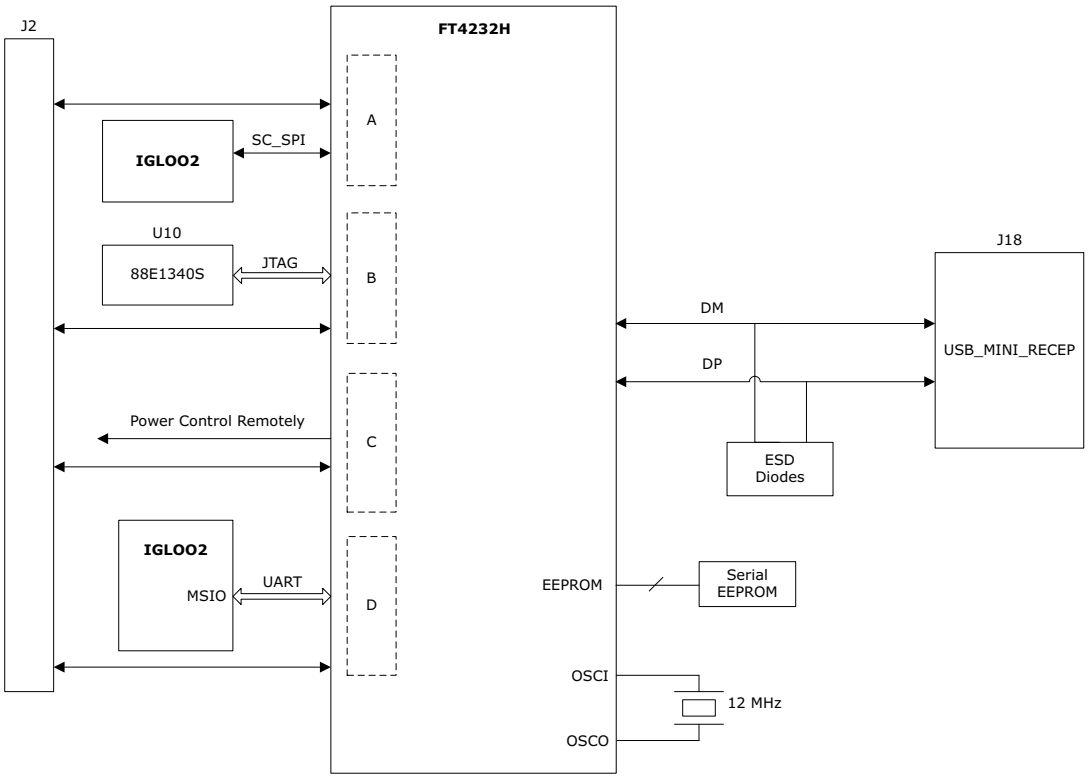
4.8 FTDI Interface

Key features of the FT4232H chip are as follows:

- USB 2.0 high-speed (480 Mbps) to UART/MPSSE IC
- Single-chip USB-to-quad serial ports with various configurations
- Entire USB protocol handled on the chip without requiring USB-specific firmware programming
- USB 2.0 high-speed (480 Mbps) and full-speed (12 Mbps) compatibility
- Two multi-protocol synchronous serial engines (MPSSE) on channel A and channel B to simplify synchronous serial protocol (USB to JTAG, I2C, SPI, or bit-bang) design
- Fully assisted hardware handshaking and X-On/X-Off software handshaking
- +1.8 V (chip core) and +3.3 V I/O interfacing with +5 V tolerance

The following figure shows the FTDI interface of the IGLOO2 Evaluation Board.

Figure 12 • **FTDI Interface**



For more information, see the Board Level Schematics document (provided separately).

4.9 I2C Port Header

The following table shows the two I2C ports routed to header H1:

Table 7 • **I2C Port Header**

Board Signal Name	IGLOO2 Pin Name	Pin Number	Header H1
I2C0_SCL	MSIO28NB1	G16	10, 14
I2C0_SDA	MSIO28PB1	G17	11, 15
I2C1_SCL	MSIO11NB2/CCC_NE0_CLKI2	R22	2, 6
I2C1_SDA	MSIO11PB2/CCC_NE0_CLKI1	P22	3, 7

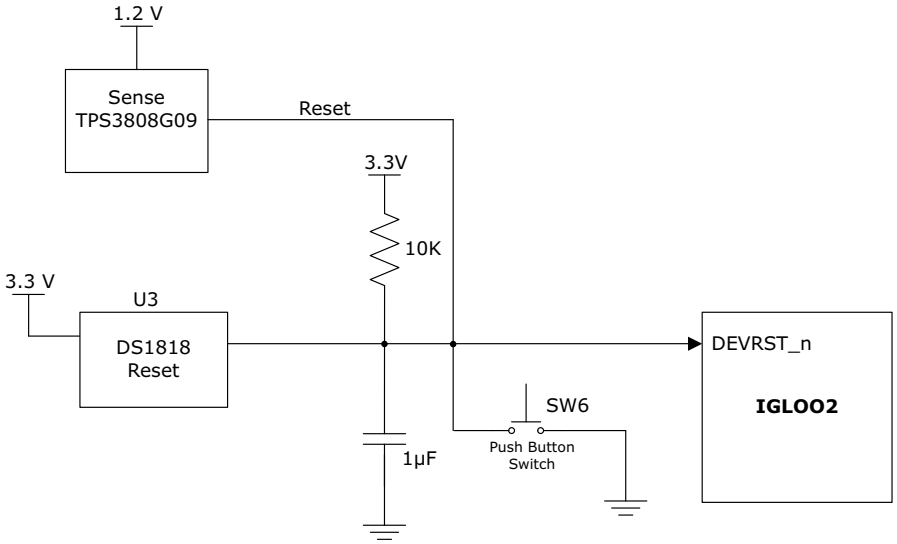
For more information, see the Board Level Schematics document (provided separately).

4.10 System Reset

DEVRST_N is an input-only reset pad that allows assertion of a full reset to the chip at any time. The DEVRST_N signal (active-low) is asserted in the following cases:

- When the **SW6** push-button switch is pressed
- When the 3.3 V or 1.2 V power supplies fall below the threshold level

Figure 13 • **System Reset Interface**



For more information, see the Board Level Schematics document (provided separately).

4.11 Clock Sources

This section provides information about the clock oscillator included in the IGLOO2 Evaluation Kit.

4.11.1 50 MHz Oscillator

A 50 MHz clock oscillator with +/-50 ppm is available on the board. This clock oscillator is connected to the FPGA fabric to provide a system reference clock.

An on-chip IGLOO2 PLL can be configured to generate a wide range of high-precision clock frequencies.

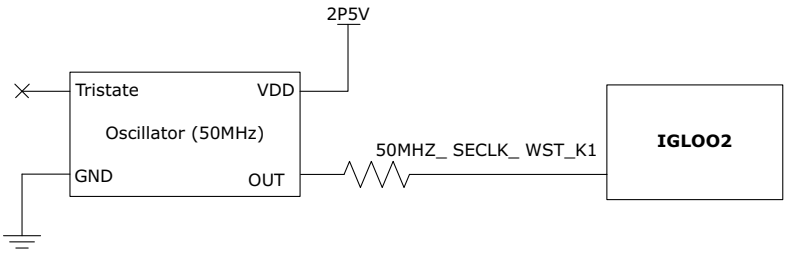
The following table provides package and pin details of the 50 MHz oscillator.

Table 8 • **50 MHz Clock**

IGLOO2 Evaluation Kit Pin Name	IGLOO2 Package Number	IGLOO2 Device Pin Name
50MHZ_ SECLK_ WST_K1	K1	MSIOD85PB6/CCC_NE1_CLKI1

The following figure shows the 50 MHz clock oscillator interface.

Figure 14 • **Clock Oscillator Interface**



For more information, see the Board Level Schematics document (provided separately).

4.11.2 Other Clock Sources

The following additional clock sources are used in the IGLOO2 Evaluation Kit:

- A 125 MHz clock oscillator for the SERDES0 interface. For more information, see SERDES0 Interface, page 13.
- 32.768 KHz crystal oscillators for the main and auxiliary oscillators of the IGLOO2 FPGA.

4.12 User Interface

The IGLOO2 Evaluation Board UI has user LEDs as well as push-button switches.

4.12.1 User LEDs

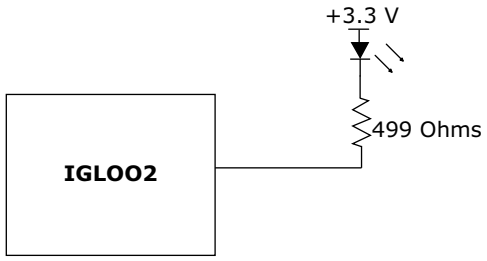
The board has eight active-low LEDs, which are connected to the IGLOO2 device for debugging applications. The following table lists the on-board debugging LEDs.

Table 9 • **LEDs**

IGLOO2 Evaluation Board Pin	IGLOO2 Package Pin Number	IGLOO2 Device Pin Name
LED0 - Yellow	E1	MSIO73PB7
LED1 – Yellow	F4	MSIO74NB7
LED2 – Green	F3	MSIO74PB7
LED3 – Green	G7	MSIO75NB7
LED4 – Red	H7	MSIO75PB7
LED5 – Red	J6	MSIO76NB7
LED6 – Blue	H6	MSIO76PB7
LED7 – Blue	H5	MSIO77NB7

The following figure shows the LED interface of the IGLOO2 Evaluation Board.

Figure 15 • **LED Interface**



For more information, see the Board Level Schematics document (provided separately).

4.12.2 Push-Button Switches

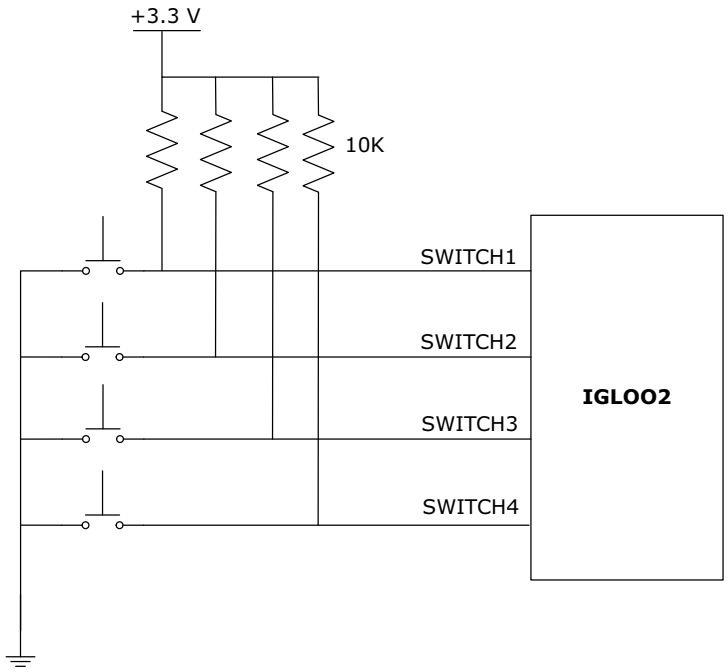
The IGLOO2 Evaluation Kit comes with five push-button tactile switches that are connected to the IGLOO2 device. The following table lists the on-board push-button switches.

Table 10 • **Push-Button Switches**

IGLOO2 Evaluation Board Pin	IGLOO2 Package Pin Number	IGLOO2 Device Pin Name
SWITCH1	L20	MSIO15NB2
SWITCH2	K16	MSIO19NB2
SWITCH3	K18	MSIO20PB2
SWITCH4	J18	MSIO20NB2
SW6	R15	DEVRST_N

The following figure shows the switches interface of the IGLOO2 Evaluation Board.

Figure 16 • **Switches Interface**



Note: For more information, see the Board Level Schematics document (provided separately).

4.12.3 Slide Switches (DPDT)

The **SW7** slide switch powers the device ON or OFF from +12 V DC external jack.

4.12.4 DIP Switches (SPST)

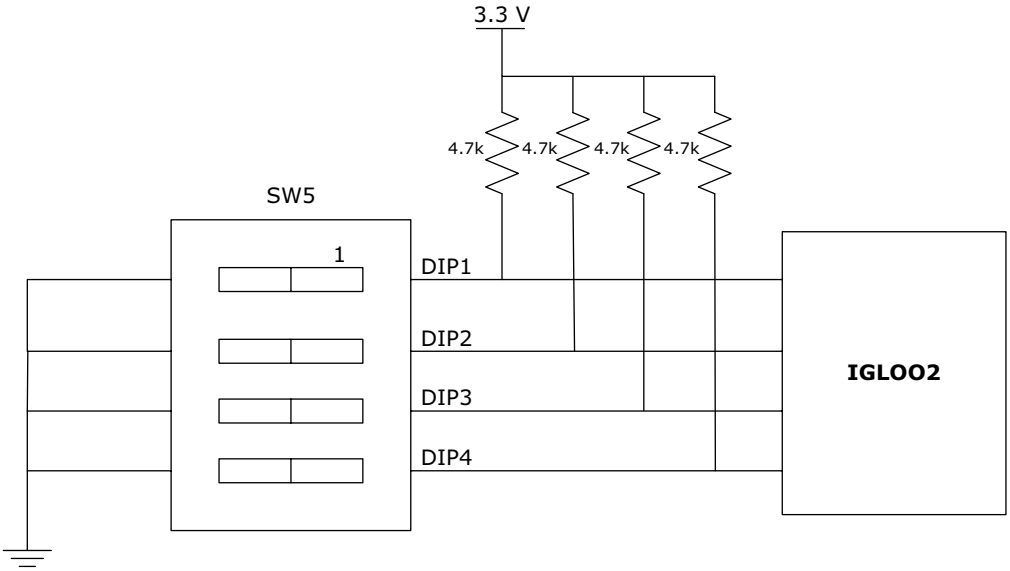
The **SW5** DIP switch has four connections to the IGLOO2 device. The following table lists the on-board DIP switches.

Table 11 • **DIP Switches**

IGLOO2 Evaluation Board Pin	IGLOO2 Package Pin Number	IGLOO2 Device Pin Name
DIP1	L19	MSIO16PB2
DIP2	L18	MSIO16NB2
DIP3	K21	MSIO17PB2
DIP4	K20	MSIO17NB2

The following figure shows the SPST interface of the IGLOO2 Evaluation Board.

Figure 17 • **SPST Interface**



For more information, see the Board Level Schematics document (provided separately).

4.13 GPIO Header Pin Out

Bank 4, bank 7, and bank 1 signals are routed to the GPIO header for user applications. The following table lists the GPIO header pinout details.

Table 12 • **GPIO Header Pin Out**

GPIO Header-J1	IGLOO2-U1		GPIO Header-J1	IGLOO2-U1	
Pin Number	**Package Number**	**Pin Name**	**Pin Number**	**Package Number**	**Pin Name**
1	AB15	MSIO110PB4	2		3P3V
3	AA15	MSIO110NB4	4		VSS
5		VSS	6	AA16	MSIO114PB4
7	AB18	MSIO118PB4	8	AA17	MSIO114NB4
9	AB19	MSIO118NB4	10		VSS
11		VSS	12	AB17	MSIO113PB4
13	Y18	MSIO117PB4	14	AA18	MSIO113NB4
15	Y19	MSIO117NB4	16		VSS
17		VSS	18	Y17	MSIO116PB4
19	W16	MSIO115PB4	20	W17	MSIO116NB4
21	V16	MSIO115NB4	22		VSS
23		VSS	24	U14	MSIO112PB4
25	C22	MSIO27PB1	26	U15	MSIO112NB4
27	B22	MSIO27NB1	28		VSS
29		VSS	30	V13	MSIO108PB4
31	Y15	MSIO111PB4	32	V14	MSIO108NB4
33	W15	MSIO111NB4	34		VSS
35		VSS	36	G5	MSIO66PB7
37	F5	MSIO67PB7	38	G6	MSIO66NB7
39	F6	MSIO67NB7	40		VSS
41		VSS	42	E4	MSIO70PB7
43	C4	MSIO64PB7	44	E5	MSIO70NB7
45	D5	MSIO64NB7	46		VSS
47		VSS	48	C3	MSIO65PB7
49	B2	MSIO69PB7	50	B3	MSIO65NB7
51	A2	MSIO69NB7	52		VSS
53		VSS	54	C1	MSIO71PB7
55	D1	MSIO72PB7	56	B1	MSIO71NB7
57	D2	MSIO72NB7	58		VSS
59		VSS	60	D3	MSIO68PB7
61		3P3V	62	D4	MSIO68NB7
63		3P3V	64		VSS

5 Pin List

The following table lists all the package pins in IGLOO2 M2GL010T-FGG484 devices.

Table 13 • **Pin List**

Package Pin	Device Pin Name
A1	VSS
A10	DDRIO51PB0/MDDR_DM_RDQS0
A11	DDRIO51NB0/MDDR_DQ4
A12	DDRIO48PB0/MDDR_DQ8
A13	DDRIO48NB0/MDDR_DQ9
A14	DDRIO44PB0/MDDR_DQ12
A15	DDRIO44NB0/MDDR_DQ13
A16	DDRIO39PB0/MDDR_CLK
A17	DDRIO39NB0/MDDR_CLK_N
A18	DDRIO38PB0/MDDR_BA0
A19	DDRIO38NB0/MDDR_BA1
A2	MSIO69NB7
A20	DDRIO34NB0/MDDR_ADDR6
A21	DDRIO31PB0/MDDR_ADDR10
A22	VSS
A3	DDRIO63NB0
A4	DDRIO63PB0
A5	DDRIO62NB0
A6	DDRIO59NB0/GB4
A7	DDRIO56PB0/MDDR_DQ_ECC1
A8	DDRIO56NB0/MDDR_DQ_ECC0
A9	DDRIO54NB0/MDDR_DQ1
AA1	VSS
AA10	NC
AA11	NC
AA12	NC
AA13	MSIO106PB4
AA14	VSS
AA15	MSIO110NB4
AA16	MSIO114PB4
AA17	MSIO114NB4
AA18	MSIO113NB4
AA19	VDDI4

Table 13 • **Pin List *(continued)***

Package Pin	Device Pin Name
AA2	SERDES_0_TXD0_N
AA20	VDD
AA21	XTLOSC_MAIN_EXTAL
AA22	JTAGSEL
AA3	VSS
AA4	SERDES_0_TXD1_N
AA5	VSS
AA6	SERDES_0_TXD2_N
AA7	VSS
AA8	SERDES_0_TXD3_N
AA9	VSS
AB1	VSS
AB10	NC
AB11	NC
AB12	VDDI4
AB13	MSIO105PB4/CCC_NE0_CLKI0
AB14	MSIO105NB4
AB15	MSIO110PB4
AB16	VSS
AB17	MSIO113PB4
AB18	MSIO118PB4
AB19	MSIO118NB4
AB2	SERDES_0_TXD0_P
AB20	VDD
AB21	XTLOSC_MAIN_XTAL
AB22	VSS
AB3	VSS
AB4	SERDES_0_TXD1_P
AB5	VSS
AB6	SERDES_0_TXD2_P
AB7	VSS
AB8	SERDES_0_TXD3_P
AB9	VSS
B1	MSIO71NB7
B10	VSS
B11	DDRIO52PB0/MDDR_DQS0
B12	VDDI0

Table 13 • **Pin List *(continued)***

Package Pin	Device Pin Name
B13	DDRIO46PB0/MDDR_DQS1
B14	VSS
B15	DDRIO41PB0/MDDR_CKE
B16	VDDI0
B17	DDRIO37NB0/MDDR_ADDR0
B18	VSS
B19	DDRIO34PB0/MDDR_ADDR5
B2	MSIO69PB7
B20	VDDI0
B21	DDRIO31NB0/MDDR_ADDR11
B22	MSIO27NB1
B3	MSIO65NB7
B4	VSS
B5	DDRIO62PB0
B6	DDRIO59PB0/GB0
B7	DDRIO58NB0/MDDR_DQS_ECC_N
B8	VDDI0
B9	DDRIO54PB0/MDDR_DQ0
C1	MSIO71PB7
C10	VDDI0
C11	DDRIO52NB0/MDDR_DQS0_N
C12	VSS
C13	DDRIO46NB0/MDDR_DQS1_N
C14	VDDI0
C15	DDRIO41NB0/MDDR_CS_N
C16	DDRIO37PB0/MDDR_BA2
C17	DDRIO35PB0/MDDR_ADDR3
C18	DDRIO35NB0/MDDR_ADDR4
C19	DDRIO33NB0/MDDR_ADDR7
C2	VDDI7
C20	DDRIO33PB0/MDDR_ODT
C21	VSS
C22	MSIO27PB1
C3	MSIO65PB7
C4	MSIO64PB7
C5	DDRIO61PB0
C6	VDDI0

Table 13 • **Pin List *(continued)***

Package Pin	Device Pin Name
C7	DDRIO58PB0/MDDR_DQS_ECC
C8	VSS
C9	DDRIO55NB0
D1	MSIO72PB7
D10	DDRIO50PB0/MDDR_DQ5
D11	DDRIO50NB0/MDDR_DQ6
D12	DDRIO47PB0/MDDR_DQ10
D13	DDRIO47NB0/MDDR_DQ11
D14	DDRIO43PB0/MDDR_DQ14
D15	VSS
D16	DDRIO36PB0/MDDR_ADDR1
D17	VDDI0
D18	DDRIO29PB0/MDDR_ADDR14
D19	VSS
D2	MSIO72NB7
D20	DDRIO30NB0/MDDR_ADDR13
D21[1]	MSI26NB1
D22	FLASH_GOLDEN_N
D3	MSIO68PB7
D4	MSIO68NB7
D5	MSIO64NB7
D6	DDRIO61NB0
D7	MDDR_IMP_CALIB_ECC
D8	DDRIO57NB0/MDDR_DM_RDQS_ECC
D9	DDRIO55PB0/CCC_NE0_CLKI3
E1	MSIO73PB7
E10	DDRIO53NB0/MDDR_DQ3
E11	VDDI0
E12	DDRIO49PB0/MDDR_DQ7
E13	DDRIO43NB0/MDDR_DQ15
E14	VSS
E15	DDRIO40PB0/MDDR_RESET_N
E16	DDRIO36NB0/MDDR_ADDR2
E17	DDRIO32PB0/MDDR_ADDR8
E18	DDRIO29NB0/MDDR_ADDR15
E19	DDRIO30PB0/MDDR_ADDR12
E2	MSIO73NB7

Table 13 • **Pin List *(continued)***

Package Pin	Device Pin Name
E20	VDDI1
E21	MSIO25NB1
E22	MSIO25PB1
E3	VSS
E4	MSIO70PB7
E5	MSIO70NB7
E6	VSS
E7	DDRIO60PB0/MDDR_TMATCH_ECC_OUT
E8	DDRIO57PB0/MDDR_TMATCH_ECC_IN
E9	VSS
F1	VDDI7
F10	DDRIO53PB0/MDDR_DQ2
F11	VSS
F12	DDRIO49NB0/MDDR_TMATCH_0_OUT
F13	VDDI0
F14	DDRIO42PB0/MDDR_RAS_N
F15	DDRIO40NB0/MDDR_CAS_N
F16	VSS
F17	DDRIO32NB0/MDDR_ADDR9
F18	MSIO24NB1
F19	MSIO24PB1
F2	NC
F20	MSIO23NB1
F21	MSIO23PB1
F22	VDDI1
F3	MSIO74PB7
F4	MSIO74NB7
F5	MSIO67PB7
F6	MSIO67NB7
F7	VDDI0
F8	DDRIO60NB0/CCC_NE1_CLKI3
F9	VDDI0
G1	MSIO78NB7
G10	VREF0
G11	VREF0
G12	DDRIO45PB0/MDDR_TMATCH_0_IN
G13	DDRIO45NB0/MDDR_DM_RDQS1

Table 13 • **Pin List *(continued)***

Package Pin	Device Pin Name
G14	DDRIO42NB0/MDDR_WE_N
G15	VREF0
G16	MSIO28NB1
G17	MSIO28PB1
G18	MSIO22NB1
G19	MSIO22PB1/GB6
G2	NC
G20	VSS
G21	NC
G22	NC
G3	NC
G4	VDDI7
G5	MSIO66PB7
G6	MSIO66NB7
G7	MSIO75NB7
G8	NC
G9	NC
H1	MSIO78PB7/GB2
H10	VDD
H11	VSS
H12	VDDI0
H13	VSS
H14	VDDI0
H15	CCC_NE0_PLL_VDDA
H16	MDDR_PLL_VDDA
H17	MDDR_PLL_VSSA
H18	VDDI1
H19	MSIO21NB1
H2	VSS
H20	MSIO21PB1/GB5
H21	NC
H22	NC
H3	NC
H4	MSIO77PB7
H5	MSIO77NB7
H6	MSIO76PB7
H7	MSIO75PB7

Table 13 • **Pin List *(continued)***

Package Pin	Device Pin Name
H8	NC
H9	VSS
J1	MSIO80PB7
J10	VSS
J11	VDD
J12	VSS
J13	VDD
J14	VSS
J15	CCC_NE0_PLL_VSSA
J16	CCC_NE1_PLL_VSSA
J17	CCC_NE1_PLL_VDDA
J18	MSIO20NB2
J19	NC
J2	MSIO80NB7
J20	NC
J21	VDDI1
J22	NC
J3	MSIO79PB7/GB1
J4	MSIO79NB7
J5	VSS
J6	MSIO76NB7
J7	VDDI7
J8	NC
J9	VDD
K1	MSIOD85PB6/CCC_NE1_CLKI1
K10	VDD
K11	VSS
K12	VDD
K13	VSS
K14	VDD
K15	MSIO18NB2
K16	MSIO19NB2
K17	MSIO19PB2
K18	MSIO20PB2
K19	VSS
K2	MSIOD85NB6
K20	MSIO17NB2

Table 13 • **Pin List *(continued)***

Package Pin	Device Pin Name
K21	MSIO17PB2
K22	NC
K3	VDDI6
K4	MSIOD82PB6
K5	MSIOD82NB6
K6	MSIO81PB7
K7	MSIO81NB7
K8	MSIOD83PB6
K9	VSS
L1	VSS
L10	VSS
L11	VDD
L12	VSS
L13	VDD
L14	VSS
L15	VPP
L16	MSIO18PB2
L17	VDDI2
L18	MSIO16NB2
L19	MSIO16PB2
L2	MSIOD86PB6
L20	MSIO15NB2
L21	MSIO15PB2
L22	VSS
L3	MSIOD86NB6
L4	MSIOD87PB6
L5	MSIOD87NB6
L6	VDDI6
L7	MSIOD84NB6
L8	MSIOD83NB6
L9	VDD
M1	MSIOD92NB6
M10	VDD
M11	VSS
M12	VDD
M13	VSS
M14	VDD

Table 13 • **Pin List *(continued)***

Package Pin	Device Pin Name
M15	VPPNVM
M16	NC
M17	NC
M18	NC
M19	NC
M2	MSIOD90NB6
M20	VDDI2
M21	MSIO14PB2
M22	MSIO14NB2
M3	MSIOD90PB6
M4	VSS
M5	MSIOD88PB6
M6	MSIOD88NB6
M7	MSIOD84PB6/CCC_NE1_CLKI2
M8	MSIOD95NB6
M9	VSS
N1	MSIOD92PB6
N10	VSS
N11	VDD
N12	VSS
N13	VDD
N14	VSS
N15	VSSNVM
N16	MSIO8PB2
N17	MSIO8NB2
N18	VSS
N19	MSIO12PB2/SPI_0_CLK
N2	VDDI6
N20	MSIO12NB2/SPI_0_SDI
N21	MSIO13PB2/SPI_0_SDO
N22	MSIO13NB2/SPI_0_SS0
N3	MSIOD91PB6
N4	MSIOD91NB6
N5	MSIOD89PB6
N6	MSIOD89NB6
N7	VSS
N8	MSIOD95PB6

Table 13 • **Pin List *(continued)***

Package Pin	Device Pin Name
N9	VDD
P1	MSIOD94PB6
P10	VDD
P11	VSS
P12	VDD
P13	VSS
P14	VDD
P15	VPP
P16	MSIO7NB2
P17	MSIO6PB2
P18	MSIO6NB2
P19	SC_SPI_SDO
P2	MSIOD94NB6
P20	SC_SPI_SS
P21	VSS
P22	MSIO11PB2/CCC_NE0_CLKI1
P3	MSIOD93NB6
P4	MSIOD93PB6
P5	VDDI6
P6	MSIOD96PB6
P7	MSIOD96NB6
P8	SERDES_0_VDD
P9	VSS
R1	MSIOD97NB6
R10	VSS
R11	VDD
R12	VSS
R13	VDD
R14	VSS
R15	DEVRST_N
R16	MSIO7PB2
R17	MSIO1PB2
R18	MSIO1NB2
R19	VDDI2
R2	MSIOD97PB6
R20	SC_SPI_CLK
R21	SC_SPI_SDI

Table 13 • **Pin List** ***(continued)***

Package Pin	Device Pin Name
R22	MSIO11NB2/CCC_NE0_CLKI2
R3	MSIOD98PB6
R4	MSIOD98NB6
R5	VSS
R6	NC
R7	NC
R8	SERDES_0_L01_VDDAIO
R9	VSS
T1	MSIOD100NB5/SERDES_0_REFCLK0_N
T10	SERDES_0_L23_VDDAIO
T11	NC
T12	NC
T13	MSIO107NB4
T14	VDDI4
T15	VSS
T16	NC
T17	VSS
T18	MSIO2PB2
T19	MSIO2NB2
T2	VSS
T20	MSIO5PB2
T21	MSIO5NB2
T22	VDDI2
T3	MSIOD99NB6
T4	MSIOD99PB6
T5	NC
T6	SERDES_0_PLL_VSSA
T7	NC
T8	SERDES_0_PLL_VDDA
T9	SERDES_0_VDD
U1	MSIOD100PB5/SERDES_0_REFCLK0_P
U10	NC
U11	NC
U12	VSS
U13	MSIO107PB4
U14	MSIO112PB4
U15	MSIO112NB4

Table 13 • **Pin List *(continued)***

Package Pin	Device Pin Name
U16	NC
U17	NC
U18	NC
U19	MSIO0PB2
U2	VDDI5
U20	VSS
U21	MSIO4NB2
U22	MSIO4PB2
U3	MSIOD101PB5/SERDES_0_REFCLK1_P
U4	MSIOD101NB5/SERDES_0_REFCLK1_N
U5	SERDES_0_L01_REXT
U6	SERDES_0_L01_REFRET
U7	SERDES_0_L01_VDDAPLL
U8	SERDES_0_L23_VDDAPLL
U9	VPP
V1	VSS
V10	VDDI4
V11	MSIO104PB4/GB3
V12	NC
V13	MSIO108PB4
V14	MSIO108NB4
V15	VSS
V16	MSIO115NB4
V17	NC
V18	NC
V19	MSIO0NB2
V2	VSS
V20	JTAG_TMS
V21	MSIO3NB2
V22	MSIO3PB2
V3	VSS
V4	VSS
V5	VSS
V6	VSS
V7	VSS
V8	SERDES_0_L23_REXT
V9	SERDES_0_L23_REFRET

Table 13 • **Pin List *(continued)***

Package Pin	Device Pin Name
W1	SERDES_0_RXD0_P
W10	MSIO103PB4/PROBE_A
W11	MSIO104NB4/GB7
W12	NC
W13	VDDI4
W14	MSIO109NB4
W15	MSIO111NB4
W16	MSIO115PB4
W17	MSIO116NB4
W18	VSS
W19	NC
W2	VSS
W20	JTAG_TCK
W21	VDDI3
W22	JTAG_TDI
W3	SERDES_0_RXD1_P
W4	VSS
W5	SERDES_0_RXD2_P
W6	VSS
W7	SERDES_0_RXD3_P
W8	VSS
W9	MSIO102PB4
Y1	SERDES_0_RXD0_N
Y10	MSIO103NB4/PROBE_B
Y11	VSS
Y12	NC
Y13	MSIO106NB4
Y14	MSIO109PB4
Y15	MSIO111PB4
Y16	VDDI4
Y17	MSIO116PB4
Y18	MSIO117PB4
Y19	MSIO117NB4
Y2	VSS
Y20	NC
Y21	JTAG_TDO
Y22	JTAG_TRSTB

Table 13 • **Pin List *(continued)***

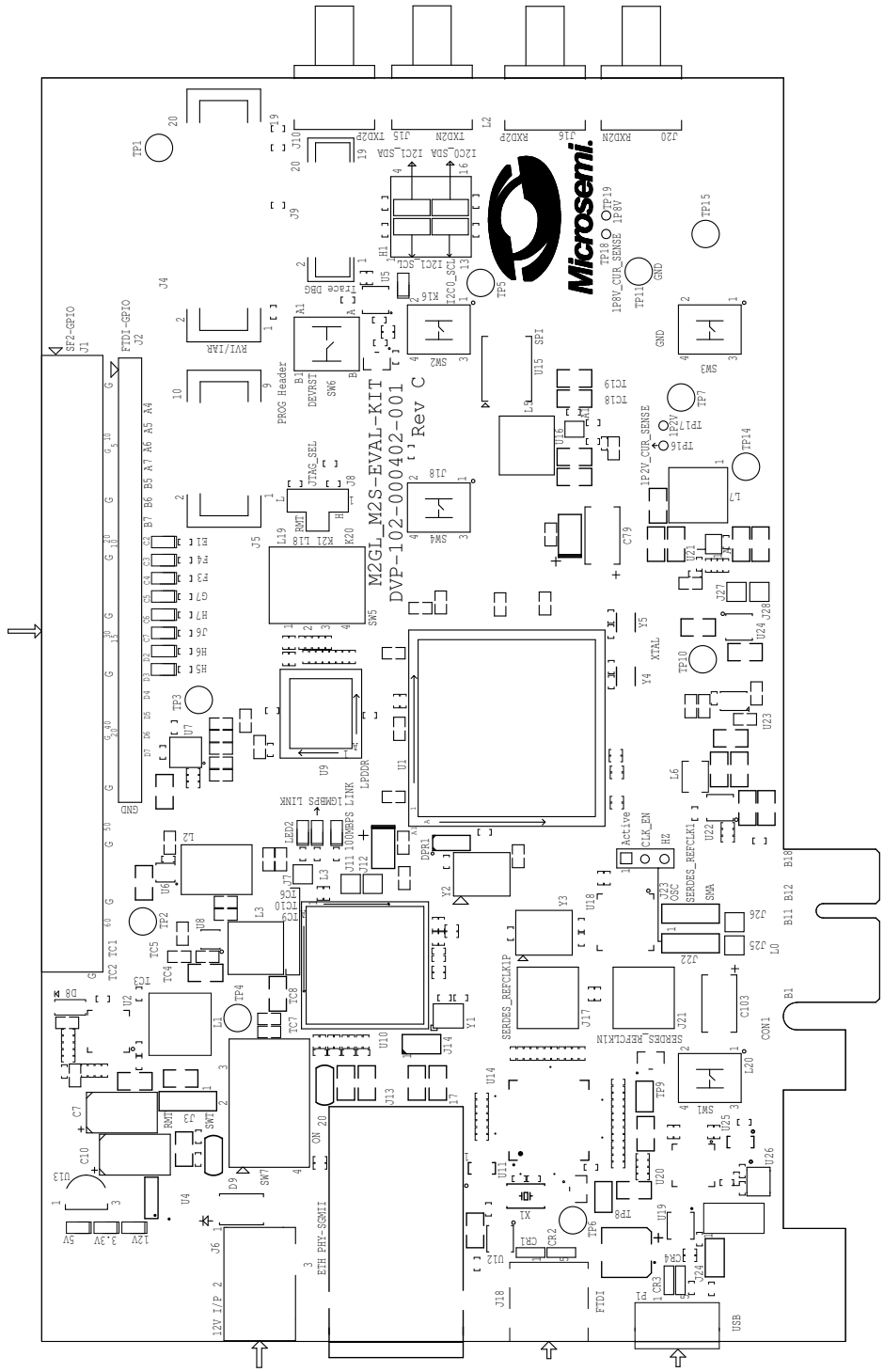
Package Pin	Device Pin Name
Y3	SERDES_0_RXD1_N
Y4	VSS
Y5	SERDES_0_RXD2_N
Y6	VSS
Y7	SERDES_0_RXD3_N
Y8	VSS
Y9	MSIO102NB4/CCC_NE1_CLKI0

1. This is an input-only pin and cannot be used as a fabric output.

6 Board Component Placement

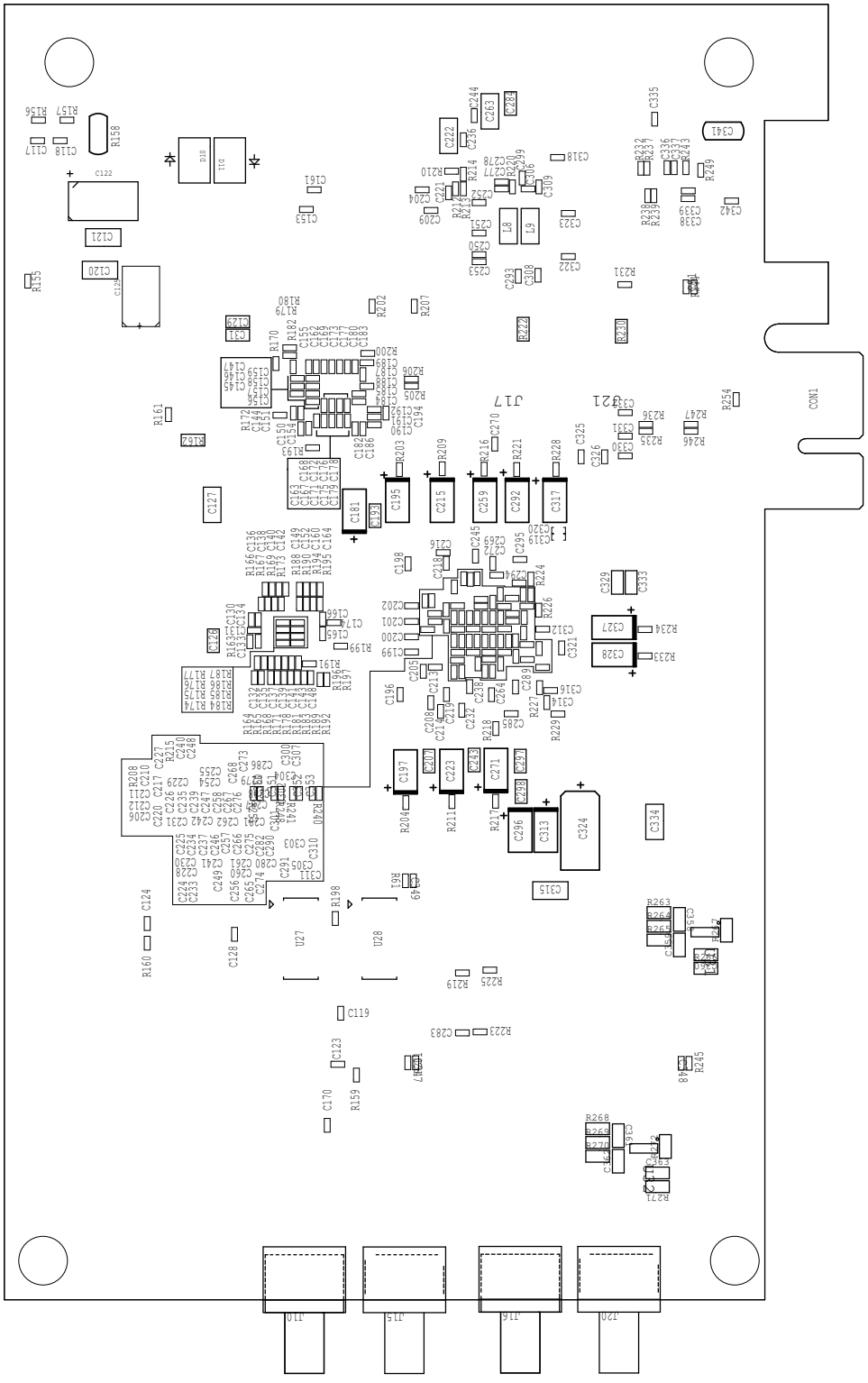
The following figure shows the placement of various components on the IGLOO2 Evaluation Kit silkscreen.

Figure 18 • **Silkscreen Top View**



The following figure shows the bottom view of the silkscreen.

Figure 19 • **Silkscreen Bottom View**



7 Demo Design

The IGLOO2 M2GL-EVAL-KIT comes with a preloaded PCIe control plane design to demonstrate key features of the IGLOO2 device, such as the PCIe interface, fabric interface, and GPIOs. These features can be used for rapid prototyping and validation of user designs.

For more information about how to run the demo design, see *Implementing PCIe Control Plane Design in IGLOO2 FPGA - Libero SoC v11.5 Tutorial.*

8 Manufacturing Test

The M2GL-EVAL-KIT contains a manufacturing test program that can be run to verify the functionality of the board. The test program contains various options that can be run as diagnostics for the SerDes, LPDDR, and SPI flash interfaces, and for debugging the LEDs and switches on the IGLOO2 Evaluation Board. One or more tests can then be selected from the list of available tests.

8.1 Board Setup

Before testing the IGLOO2 Evaluation Board:

- Download the `IGLOO2_MTD_top.stp`, `MTD_TESTER.exe` and `PMA_SERDES_CONFIGURATOR.exe` files from https://ww1.microchip.com/downloads/aemDocuments/documents/FPGA/SOCDesignFiles/IGLOO2_EVAL_KIT_MTD.zip.
- Download and install drivers from *http://www.ftdichip.com/Drivers/D2XX.htm*.

8.2 Loopback Test for SerDes Lanes

The following table shows the list of tests performed on the four SerDes lanes in EPCS mode.

Table 14 • **Loopback Tests for SerDes Lanes**

Lane	Loopback Test(s)
Lane 0	Internal loopback
Lane 1	Internal and external loopback
Lane 2	Internal loopback
Lane 3	Internal loopback

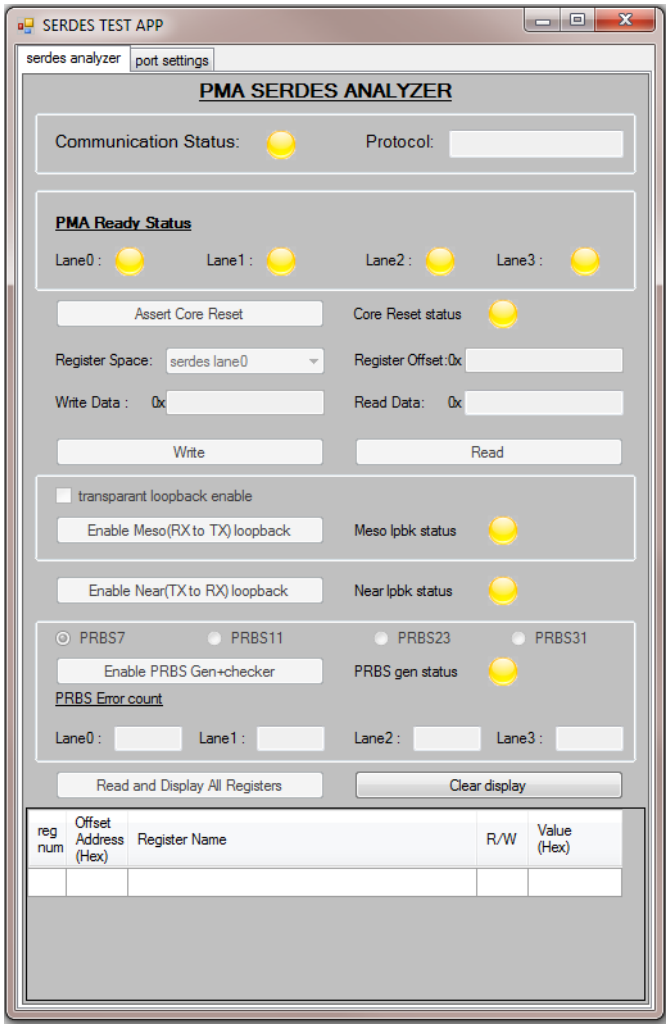
8.2.1 Internal Loopback Test

To perform an internal loopback test on the SerDes lanes:

1. Connect the **J18** jumper to the test PC using a mini-USB to Type-A USB cable. This is required for SerDes GUI UART communication.
2. Switch ON the **SW7** power supply switch.
3. Ensure that the board is programmed with the `IGLOO2_MTD_top.stp` file.
4. Double-click the `PMA_SERDES_CONFIGURATOR.exe` file to open the PMA SerDes Analyzer and test the board.

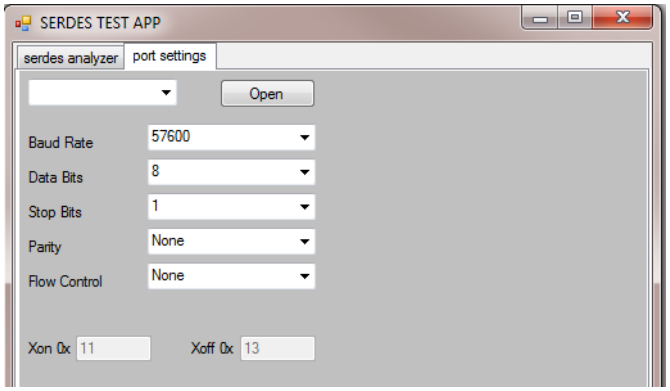
The **SERDES TEST APP** window appears, as shown in the following figure.

Figure 20 • **SERDES TEST APP Window**



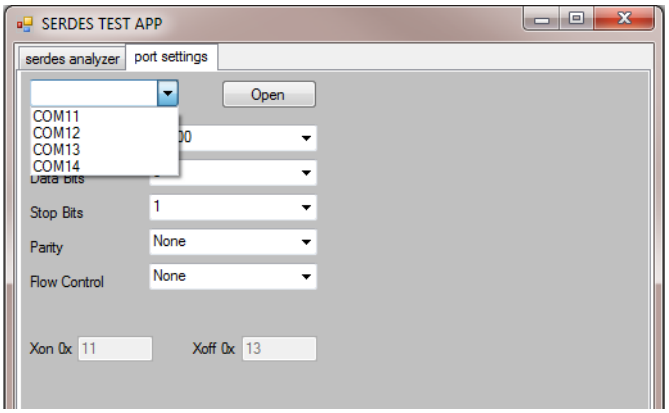
5. Click the **port settings** tab.

Figure 21 • **Port Settings Tab**



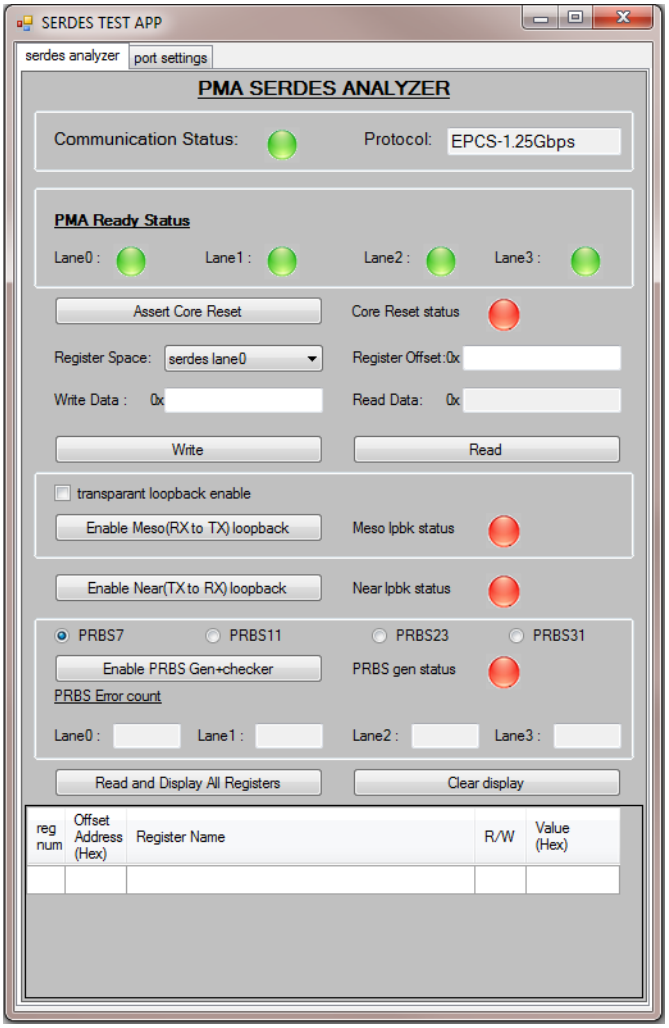
6. Select the highest COM port from the drop-down list, and click **Open** to establish connection with the test PC.

Figure 22 • **Selecting the COM Port**



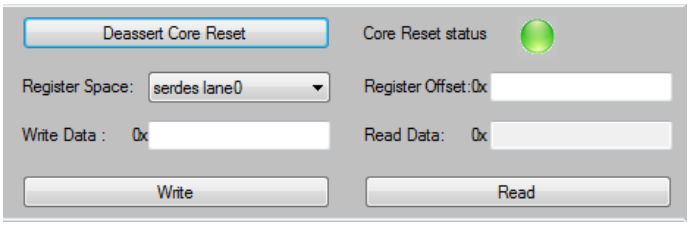
7. Click the **serdes analyzer** tab to verify the connection.

Figure 23 • **SERDES Analyzer Tab**



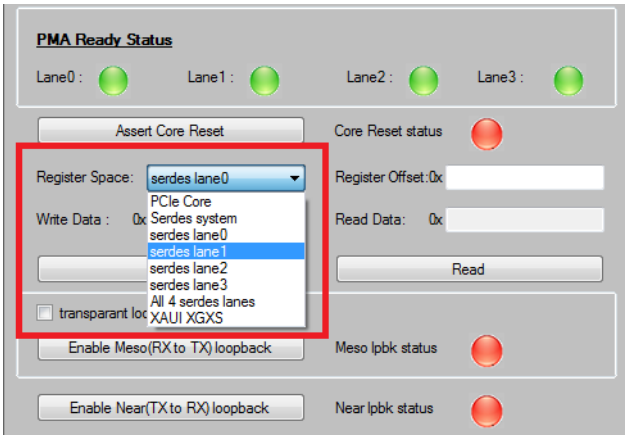
- Confirm that **Communication Status** indicator is green. A red indicator means that UART communication is not set up properly.
- Confirm that the **Core Reset status** indicator is red. If the indicator is green, click **Deassert Core Reset** to disable the core reset.

Figure 24 • **Deasserting Core Reset**



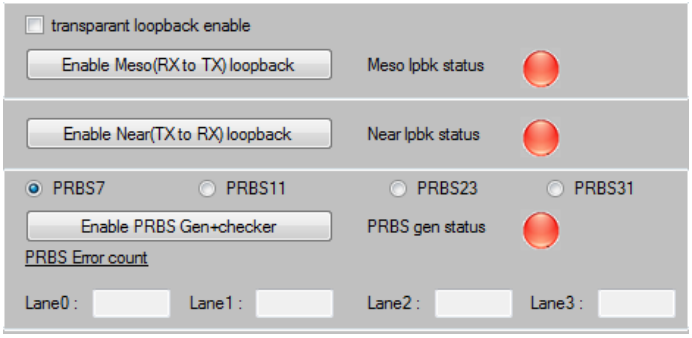
8. Select **serdes lane0** from the **Register Space** drop-down list.

Figure 25 • **Selecting Register Space**



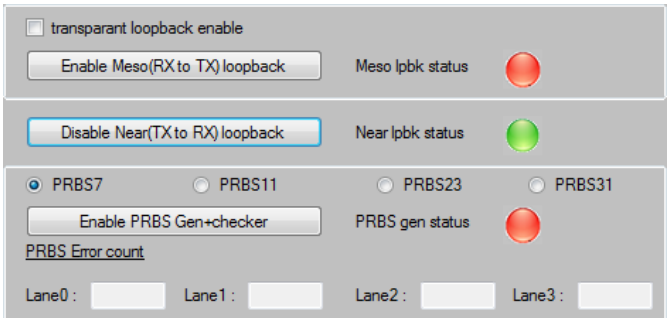
9. Click **Enable Near (TX to RX) loopback** to enable internal near-end loopback on SerDes lane 0.

Figure 26 • **Enabling Internal Loopback**



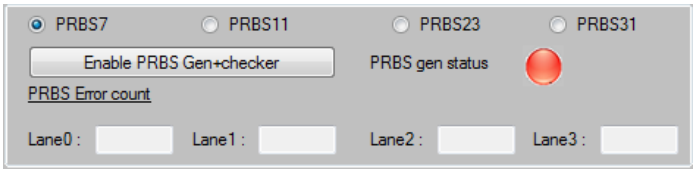
The **Near lpbk status** indicator turns green, as shown in the following figure.

Figure 27 • **Enabled Internal Loopback**



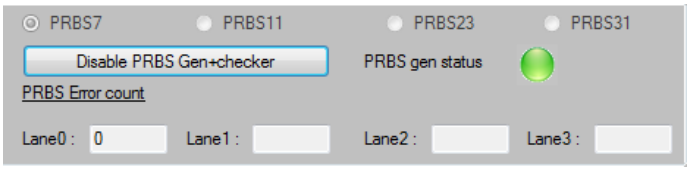
10. Click **Enable PRBS Gen+checker** to enable PRBS check.

Figure 28 • **Enabling PRBS Generator**



The **PRBS gen status** indicator turns green, as shown in the following figure.

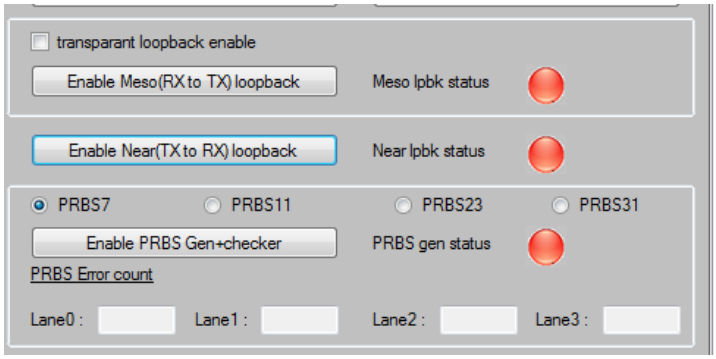
Figure 29 • **Enabling PRBS Pattern Generation**



After PRBS check is enabled, observe the PRBS error count for lane 0. The error count must be 0, indicating that the internal loopback test for SerDes lane 0 was successful. Any value other than 0 indicates that the internal loopback test had errors and was not successful.

11. Click **Disable PRBS Gen+checker** to stop packet transmission, and click **Disable Near (TX to RX) loopback** to disable loopback.
    The **Near lpbk status** and **PRBS gen status** indicators turn red, as shown in the following figure.

Figure 30 • **Disabling Internal Loopback**



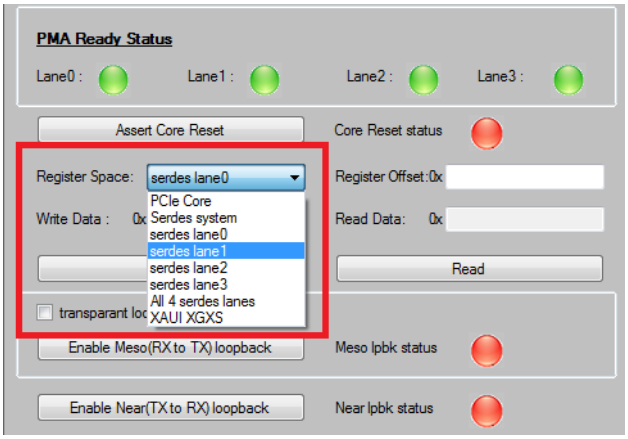
After testing internal loopback on SerDes lane 0, repeat the same test for other three SerDes lanes (lanes 1, 2, and 3).

8.2.2 External Loopback Test

External loopback can be performed on SerDes lane 1 only. To perform the external loopback test:

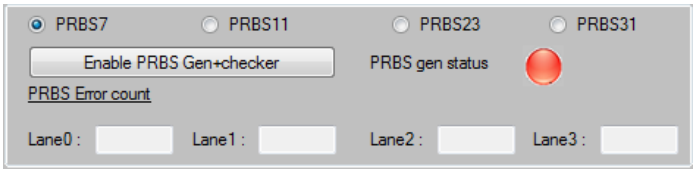
1. Select **serdes lane1** from the **Register Space** drop-down list.

Figure 31 • **Selecting SerDes Lane 1**



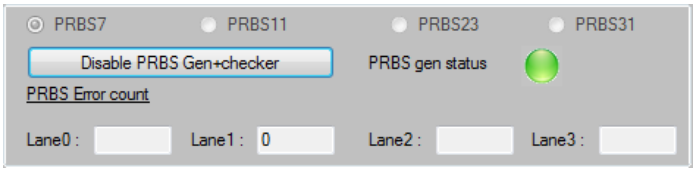
2. Click **Enable PRBS Gen+checker** to check the error count.

Figure 32 • **Enabling PRBS Generator**



The **PRBS gen status** indicator turns green, as shown in the following figure.

Figure 33 • **Enabling PRBS Pattern Generation**



After the PRBS check is enabled, observe the PRBS error count for lane 1. It must be 0, indicating that the external loopback test for SerDes lane 1 was successful. Any value other than 0 indicates that the external loopback test had errors and was not successful.

3. Close the **SerDes TEST APP** window after the test is completed.

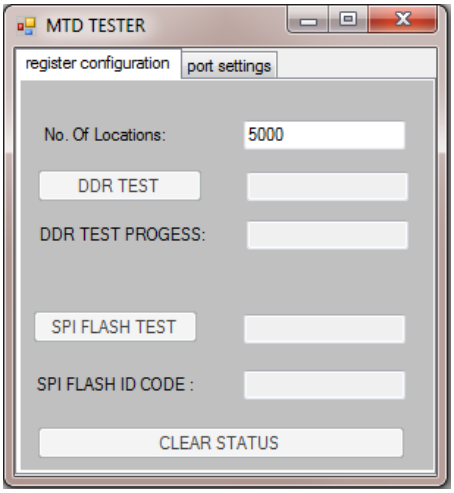
8.3 LPDDR and SPI Tests

To run the LPDDR and SPI tests on the IGLOO2 Evaluation Kit:

1. Connect the **J18** jumper to the test PC using a mini-USB to Type-A USB cable. This is required for SerDes GUI UART communication.
2. Switch ON the **SW7** power supply switch.
3. Ensure that the board is programmed with the `IGLOO2_MTD_top.stp` file.
4. Double-click the `MTD_TESTER.exe` file to open the MTD TESTER and test the evaluation board.

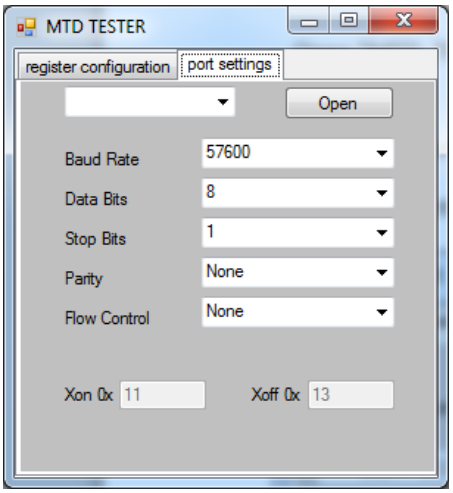
The **MTD TESTER** window appears, as shown in the following figure.

Figure 34 • **MTD TESTER Window**



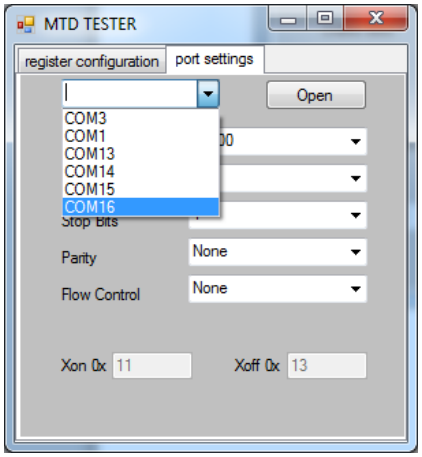
5. Click the **port settings** tab.

Figure 35 • **Port Setting Tab in MTD TESTER Window**



6. Select the highest COM port from the drop-down list, and click **Open** to establish the connection with the test PC.

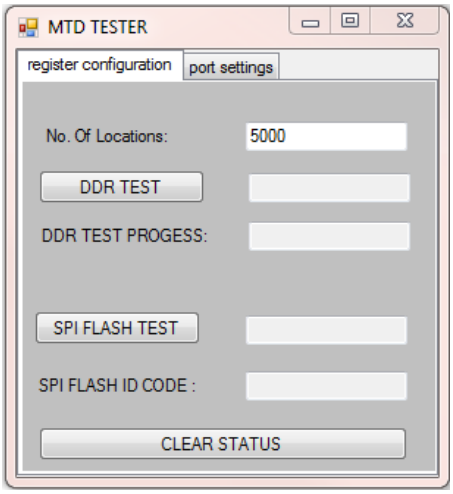
Figure 36 • **Selecting COM Port**



Note: When using the USB cable for UART communication, four COM ports are shown in the drop-down list.

7. Click the **register configuration** tab to find the LPDDR test and SPI flash test.

Figure 37 • **Register Configuration Tab**



8.3.1 LPDDR Test

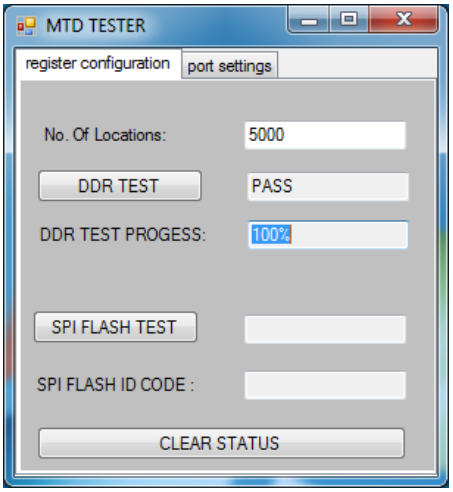
In the LPDDR test, you can test the board in multiple locations. To run the LPDDR test:

1. Enter the number of locations to be accessed on LPDDR memory.

Note: The default value is 5000.

2. Click **DDR TEST** to run the LPDDR write or read test.
   - While the test is in progress, the percentage of test completed is displayed.
   - If the LPDDR test fails, the number of locations where the test failed is displayed.
   - If the test is completed successfully, the test status shows as **PASS**, as shown in the following figure.

Figure 38 • **LPDDR Test Passed**

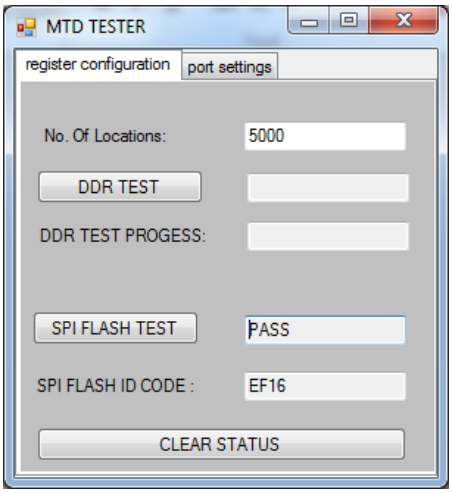


8.3.2 SPI Flash Test

To run the SPI flash test:

1. Click **SPI FLASH TEST** to start the SPI flash test.
   After the test is completed successfully, the test status shows the status as **PASS**, as shown in the following figure.

Figure 39 • **SPI Flash Test Passed**



2. After the test is completed, close the **MTD TESTER** window.
3. Click **Clear Status** to clear the status.

8.4 Switch and LED Tests

Use the following switches on the board to test the corresponding LEDs:

- When **SW1** is pressed, the **H5** LED must glow.
- When **SW3** is pressed, the **H6** LED must glow.
- When **SW4** is pressed, the **J6** LED must glow.
- When **SW2** is pressed, the **H7** LED must glow.

8.5 Board Debugging

If the board is not programmed successfully, check if all the power supplies, clocks, and reset signals are within the accepted range.

8.5.1 Power Supply Validation

To test and validate the power supply to the board:

1. Check for the default jumper settings as listed in Jumper Settings, page 6.

2. After power-on, measure the voltage at all the power supplies with respect to ground, and ensure that the voltages are within the ranges specified in the following table.

Table 15 • **Power Supply Ranges**

Power Rail	Probing Point	Accepted Voltage Range (in Volts)
1P2V	C95 pin 2	1.15 < VDD_REG < 1.25
5P0V	C16 pin 2	4.75 < 5P0V < 5.25
3P3V	C76 pin 2	3.15 < 3P3V < 3.46
2P5V	C107 pin 2	2.375 < 2P5V < 2.625
3P3V_LDO	C99 pin 1	3.135 < 3P3V_LDO < 3.465
2P5V_LDO	C100 pin 1	2.375 < 2P5V_LDO < 2.625
DDR_VTT	C22 pin 1	0.88 < DDR3_VTT < 0.92
1P0V_PHY	C36 pin 1	0.95 < 1P0V_PHY < 1.05
1P8V	C31 pin 1	1.78 < 1P8V < 1.82

3. Check to confirm that the LED (on the top left of board) corresponding to each power rail is glowing.
4. Check to ensure that the ripples on each power rail are within ±5% of the corresponding voltage rail.

8.5.2 Clock Measurement

Measure the clock signal at Y2 pin 3, and ensure that a stable 50 MHz signal is available.

8.5.3 Reset Measurement

Measure the reset signal at resistor R14, and ensure that the signal is 3.3 V, and held *high*.

8.6 FPGA Programming Using Embedded FlashPro5

The IGLOO2 M2GL-EVAL-KIT has an embedded FlashPro5 programmer; therefore, an external programmer is not required to program the IGLOO2 device. The device can be programmed using the embedded FlashPro5, provided the FlashPro software is installed in the host PC.

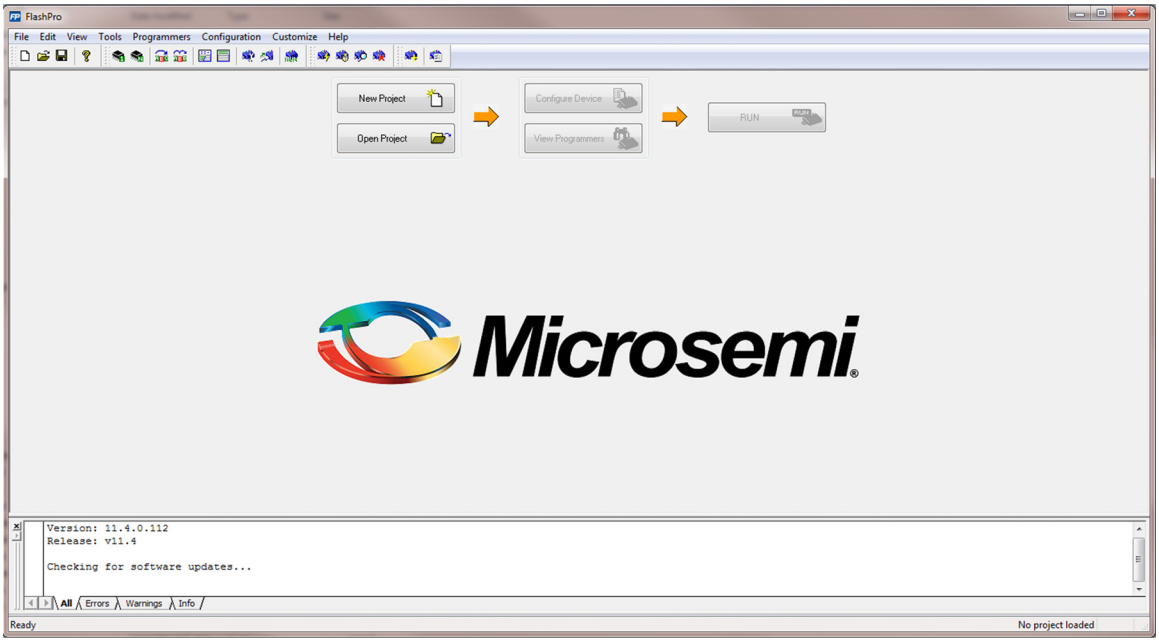
Note: The board can also be programmed using FlashPro4. To program the board using FlashPro4, connect the FlashPro4 header to the **J5** jumper and change the position of the **J35** jumper to pin 2-3.

To program the device using the embedded FlashPro5:

1. Connect one end of a mini-USB to Type-A USB cable to the **J18** jumper and the other end to the USB port of the host PC.

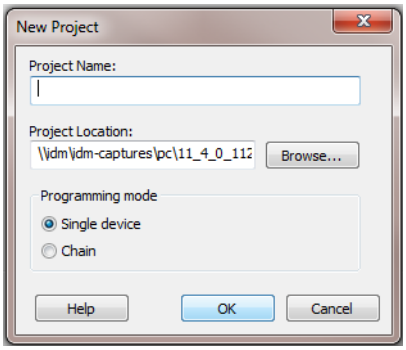
2. Launch the FlashPro software.

Figure 40 • **FlashPro Window**



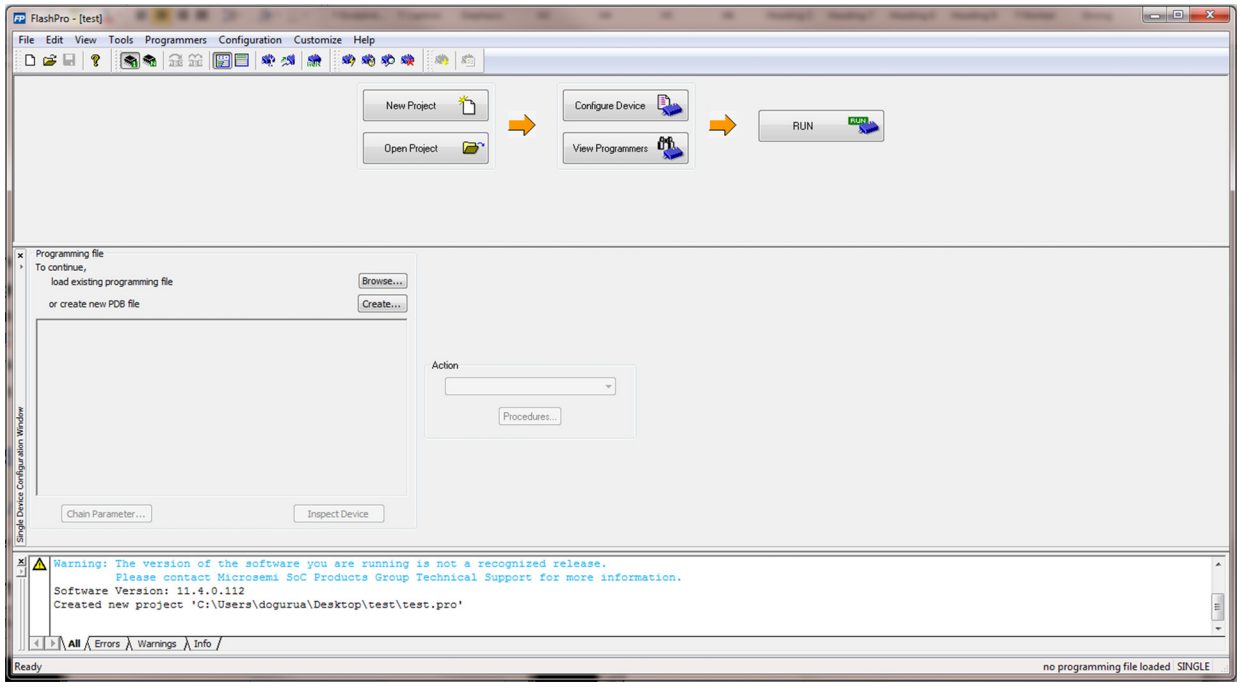
3. Click **New Project** to create a new project.
4. In the **New Project** window, do the following, and click **OK**:
   - Enter a project name.
   - Select **Single device** as the programming mode.

Figure 41 • **New Project Window**



5. Click **Configure Device**.

Figure 42 • **Configuring the Device**



6. Click **Browse**, and select the `SEC_KIT_MTD_top.stp` file from the **Load Programming File** window.
7. Click **Program** to program the device.
   When the device is programmed successfully, a **Run Program PASSED** status is displayed.