APPLICATION NOTE

Atmel AVR32715: AVR UC3B 32-bit Microcontroller Schematic Checklist

Atmel AVR UC3 32-bit Microcontroller

Features

- Power circuit
- Reset circuit
- Clocks and crystal oscillators
- USB connection
- JTAG and Nexus debug ports

Introduction

A good hardware design comes from a proper schematic. Since Atmel® AVR® UC3B series devices have a fair number of pins and functions, the schematic for these devices can be large and quite complex.

This application note describes a common checklist which should be used when starting and reviewing the schematics for an AVR UC3B series design.

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1. Power Circuit

1.1 Single 3.3V Power Supply

Figure 1-1. Single 3.3V power example schematic.

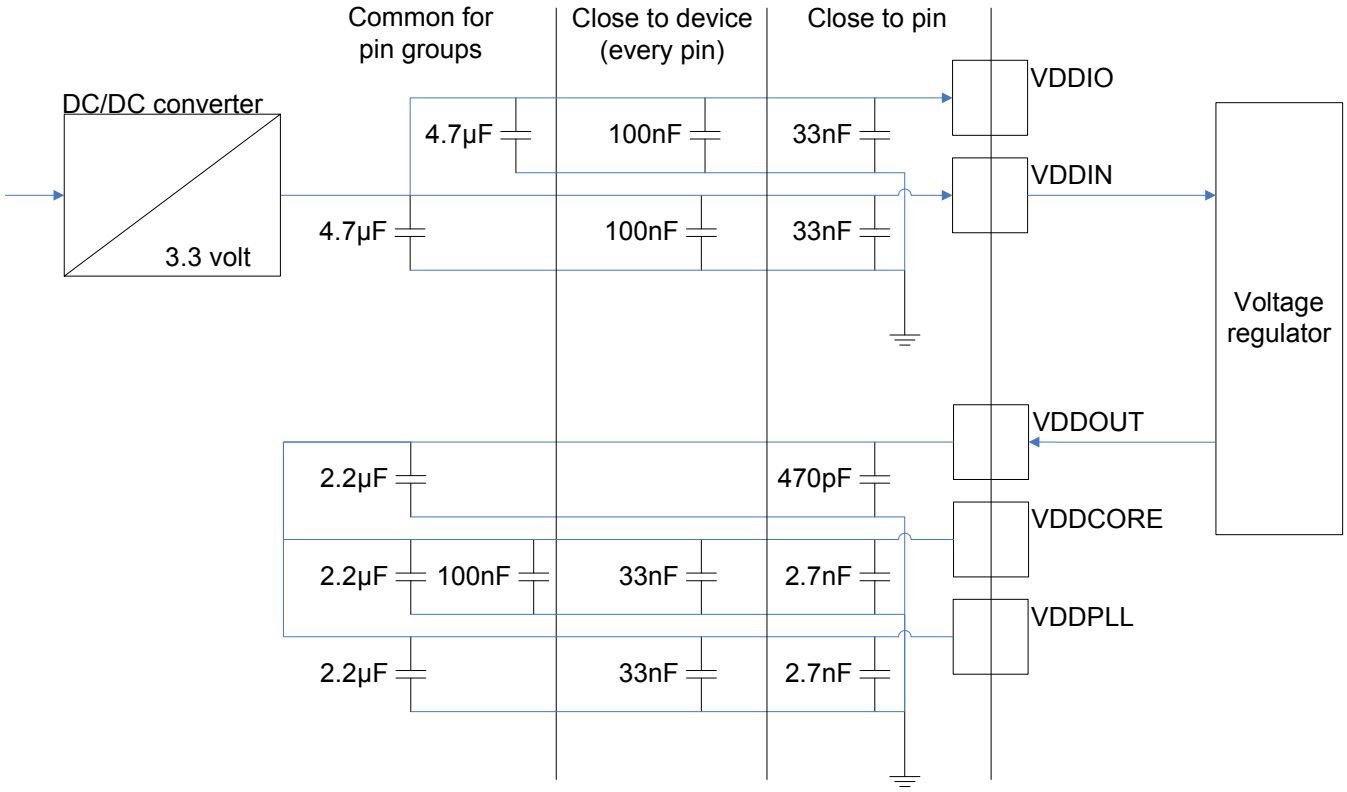


Table 1-1. Single 3.3V power supply checklist.

Signal name	Recommended pin connection	Description
VDDIO	3.0V to 3.6V Decoupling/filtering capacitors 33nF (1)(2), 100nF (1)(3) and 4.7µF (1)	Powers I/O lines and USB transceiver. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.
VDDIN	3.0V to 3.6V Decoupling/filtering capacitors 33nF (1)(2), 100nF (1)(3) and 4.7µF (1)	Powers on-chip voltage regulator. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.
VDDOUT	Decoupling/filtering capacitors 470pF (1)(2) and 4.7µF (1)	Output of the on-chip 1.8V voltage regulator. Decoupling/filtering capacitors must be added to guarantee 1.8V stability.
VDDCORE	1.65V to 1.95V Connected to VDDOUT Decoupling/filtering capacitors 2.7nF (1)(2), 33nF (1)(3), 100nF (1) and 4.7µF (1)	Powers device, flash logic and on-chip RC. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.

Signal name	Recommended pin connection	Description
VDDPLL	1.65V to 1.95V Connected to VDDOUT Decoupling/filtering capacitors 2.7nF (1)(2), 33nF (1)(3) and 4.7µF (1)	Powers the PLL. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.

Notes:
1. These values are given only as a typical example.
2. Decoupling capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.
3. Decoupling capacitor should be placed close to the device for each pin in the signal group.

1.2 Dual 3.3V and 1.8V Power Supply

Figure 1-2. Dual 3.3V and 1.8V power example schematic.

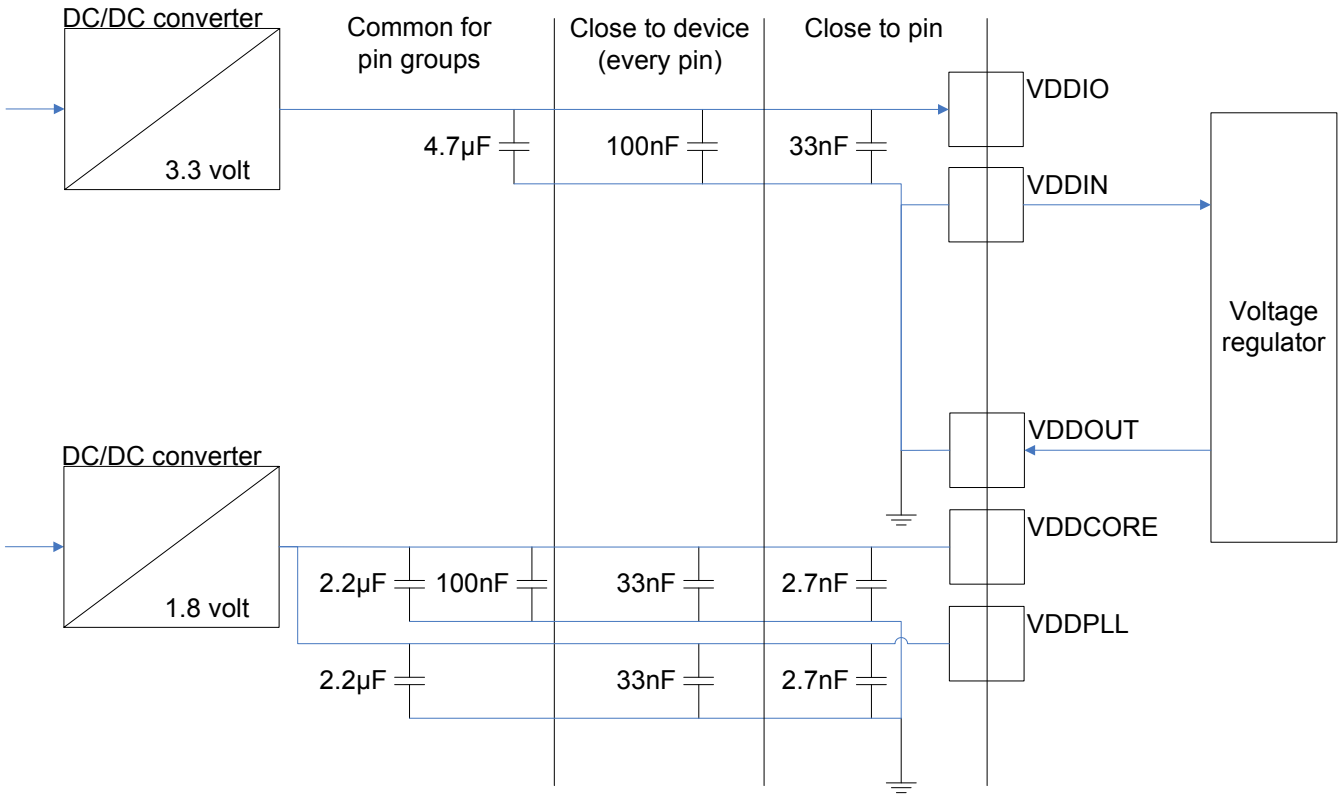


Table 1-2. Dual 3.3V and 1.8V power supply checklist.

Signal name	Recommended pin connection	Description
VDDIO	3.0V to 3.6V Decoupling/filtering capacitors 33nF (1)(2), 100nF (1)(3) and 4.7µF (1)	Powers I/O lines and USB transceiver. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.
VDDIN	Connected to ground.	On-chip voltage regulator not in use.
VDDOUT	Connected to ground.	On-chip voltage regulator not in use.

Signal name	Recommended pin connection	Description
VDDCORE	1.65V to 1.95V Decoupling/filtering capacitors 2.7nF (1)(2), 33nF (1)(3), 100nF (1) and 2.2µF (1)	Powers device, flash logic and on-chip RC. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.
VDDPLL	1.65V to 1.95V Decoupling/filtering capacitors 2.7nF (1)(2), 33nF (1)(3) and 2.2µF (1)	Powers the PLL. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.

Notes:
1. These values are given only as a typical example.
2. Decoupling capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.
3. Decoupling capacitor should be placed close to the device for each pin in the signal group.

1.3 ADC Reference Power Supply

The following schematic checklist is only necessary if the design is using the internal analog to digital converter.

Figure 1-3. ADC reference power supply example schematic.

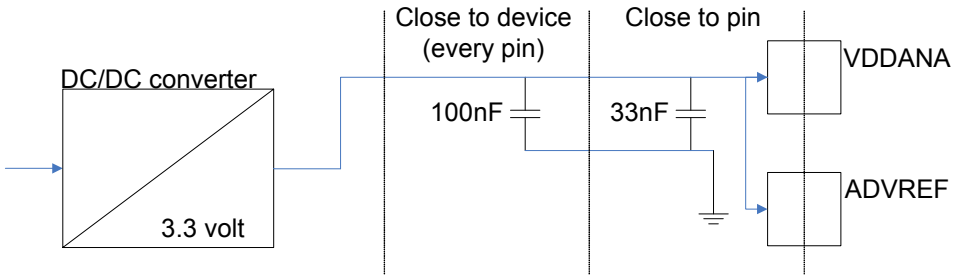


Table 1-3. ADC reference power supply checklist.

Signal name	Recommended pin connection	Description
VDDANA	3.0V to 3.6V Decoupling/filtering capacitors 33nF (1)(2) and 100nF (1)(3)	Powers on-chip ADC. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.
ADVREF	2.6V to VDDANA. Connect with VDDANA.	ADVREF is a pure analog input.

Notes:
1. These values are given only as a typical example.
2. Decoupling capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.
3. Decoupling capacitor should be placed close to the device for each pin in the signal group.

1.4 No ADC Power Supply

The following schematic checklist is only necessary if the design is not using the internal analog to digital converter.

Figure 1-4. No ADC power supply example schematic.

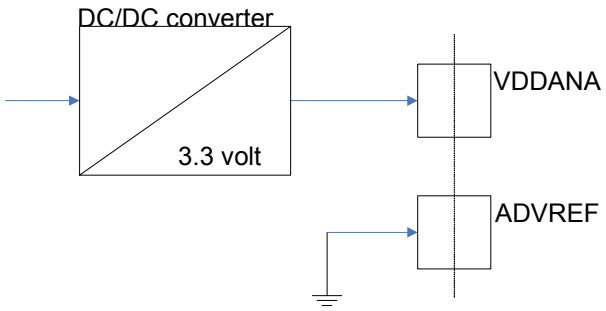


Table 1-4. No ADC power supply checklist.

Signal name	Recommended pin connection	Description
VDDANA	3.0V to 3.6V	
ADVREF	Connected to ground.	

2. Reset Circuit

Figure 2-1. Reset circuit example schematic.

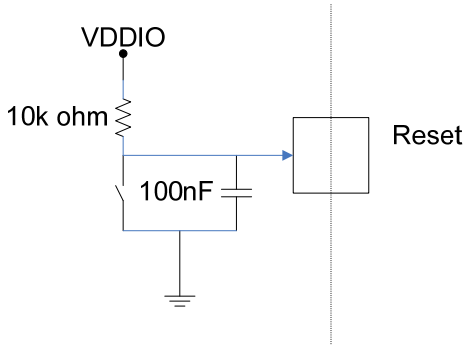


Table 2-1. Reset circuit checklist.

Signal name	Recommended pin connection	Description
RESET	Can be left unconnected in case no reset from the system needs to be applied to the product.	The RESET_N pin is a Schmitt input and integrates a permanent pull-up resistor to VDDIO.

3. Clocks and Crystal Oscillators

3.1 External Clock Source

Figure 3-1. External clock source schematic.

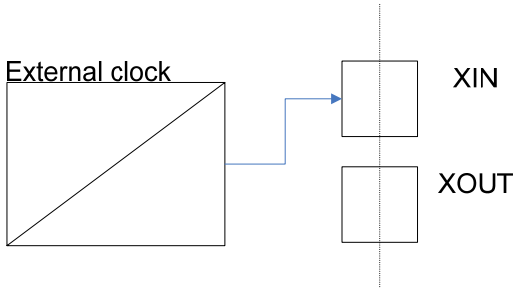


Table 3-1. External clock source checklist.

Signal name	Recommended pin connection	Description
XIN	Connected to clock output from external clock source.	Up to VDDIO volt square wave signal up to 50MHz.
XOUT	Can be left unconnected or used as GPIO.	

3.2 Crystal Oscillator

Figure 3-2. Crystal oscillator example schematic.

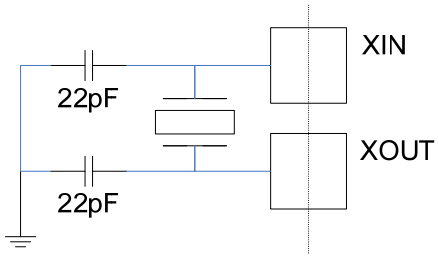


Table 3-2. Crystal oscillator checklist.

Signal name	Recommended pin connection	Description
XIN	Biasing capacitor 22pF (1)(2)	External crystal between 0.4MHz and 20MHz.
XOUT	Biasing capacitor 22pF (1)(2)	

Notes:
1. These values are given only as a typical example. The capacitance C of the biasing capacitors can be computed based on the crystal load capacitance C_L and the internal capacitance C_i of the MCU as follows: $C = 2 (C_L – C_i)$
   The value of C_L can be found in the crystal datasheet and the value of C_i can be found in the MCU datasheet.
2. Decoupling capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.

4. USB Connection

4.1 Not Used

When the USB interface is not used, D+ and D- should be connected to ground.

4.2 Device Mode, Powered from Bus Connection

Figure 4-1. USB in device mode, bus powered connection example schematic.

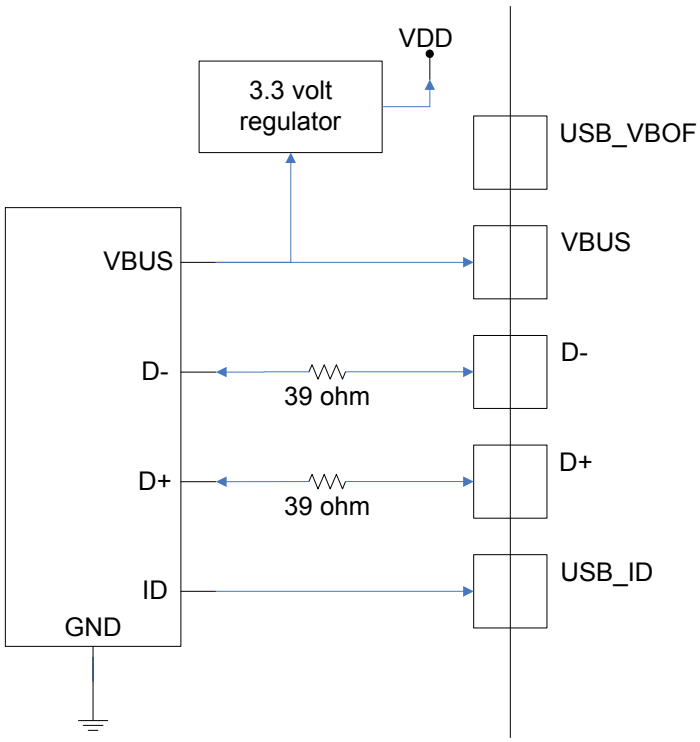


Table 4-1. USB bus powered connection checklist.

Signal name	Recommended pin connection	Description
USB_VBOF	Can be left unconnected.	USB power control pin.
VBUS	Directly to connector.	USB power measurement pin.
D-	39Ω series resistor. Placed as close as possible to pin.	Negative differential data line.
D+	39Ω series resistor. Placed as close as possible to pin.	Positive differential data line.
USB_ID	Can be left unconnected.	Mini connector USB identification pin.

4.3 Device Mode, Self Powered Connection

Figure 4-2. USB in device mode, self powered connection example schematic.

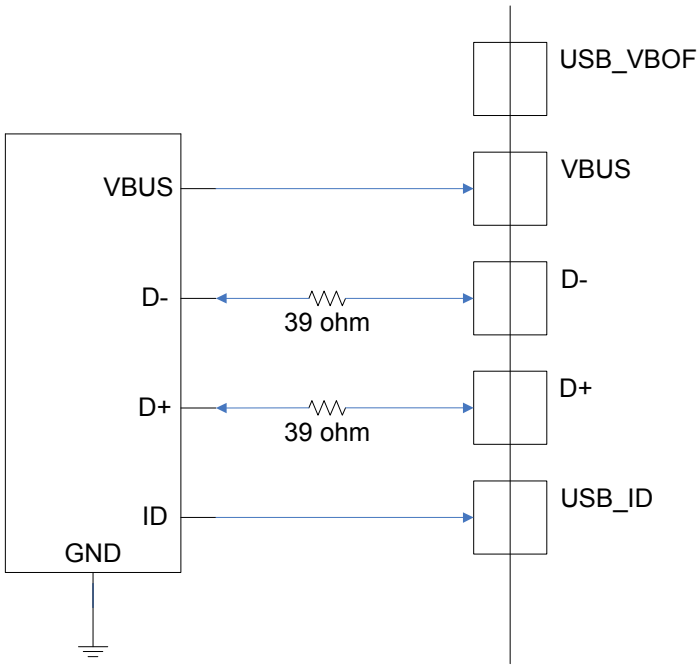


Table 4-2. USB self powered connection checklist.

Signal name	Recommended pin connection	Description
USB_VBOF	Can be left unconnected.	USB power control pin.
VBUS	Directly to connector.	USB power measurement pin.
D-	39Ω series resistor. Placed as close as possible to pin.	Negative differential data line.
D+	39Ω series resistor. Placed as close as possible to pin.	Positive differential data line.
USB_ID	Can be left unconnected.	Mini connector USB identification pin.

4.4 Host/OTG Mode, Power from Bus Connection

Figure 4-3. USB host and OTG powering connection example schematic.

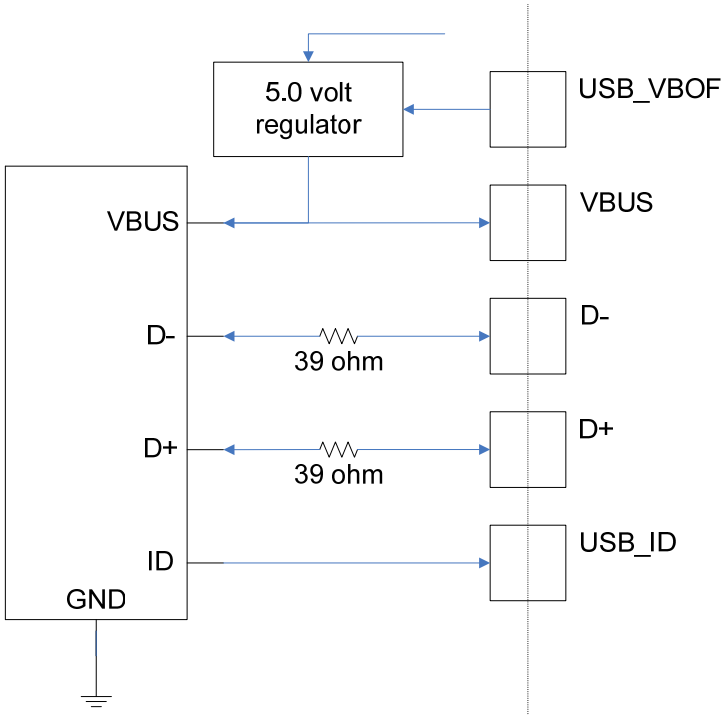


Table 4-3. USB host and OTG powering connection checklist.

Signal name	Recommended pin connection	Description
USB_VBOF	GPIO connected to VBUS 5.0V regulator enable signal.	USB power control pin.
VBUS	Directly to connector.	USB power measurement pin.
D-	39Ω series resistor. Placed as close as possible to pin.	Negative differential data line.
D+	39Ω series resistor. Placed as close as possible to pin.	Positive differential data line.
USB_ID	GPIO directly connected to connector, mandatory in OTG mode.	Mini connector USB identification pin. For OTG it will be tied to ground in host mode, and left floating in device mode. Pull-up on GPIO pin must be enabled.

5. JTAG and Nexus Debug Ports

5.1 JTAG Port Interface

Figure 5-1. JTAG port interface example schematic.

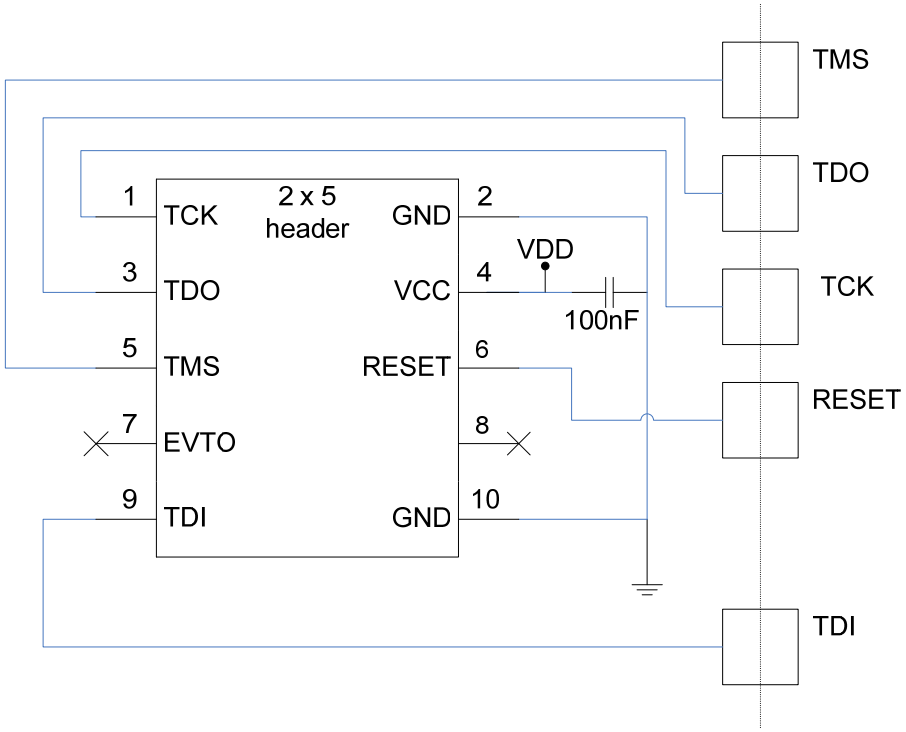


Table 5-1. JTAG port interface checklist.

Signal name	Recommended pin connection	Description
TMS		Test mode select, sampled on rising TCK.
TDO		Test data output, driven on falling TCK.
TCK		Test clock, fully asynchronous to system clock frequency.
RESET		Device external reset line.
TDI		Test data input, sampled on rising TCK.
EVTO		Event output, not used.

5.2 Nexus Port Interface

Figure 5-2. Nexus port interface example schematic.

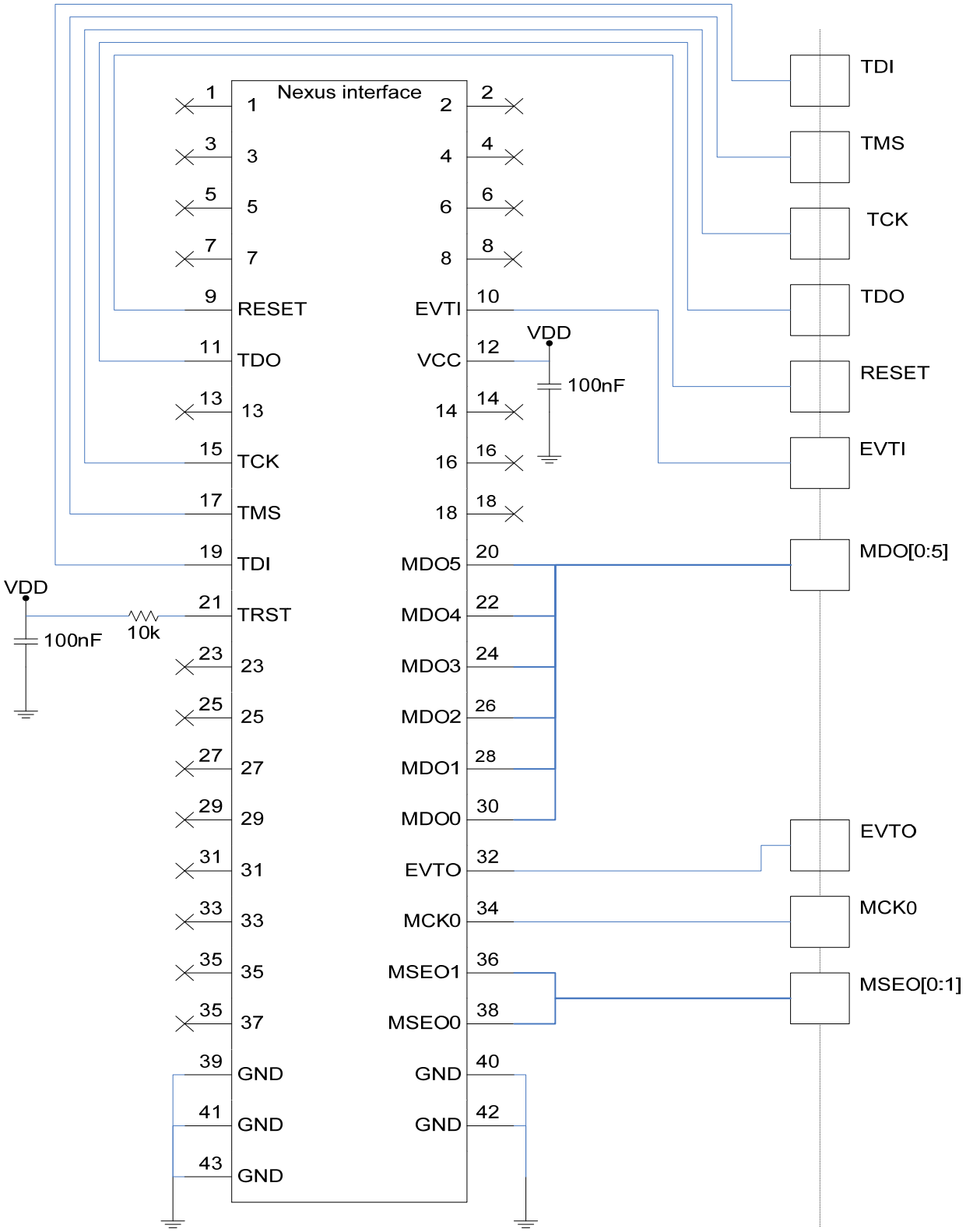


Table 5-2. Nexus port interface checklist.

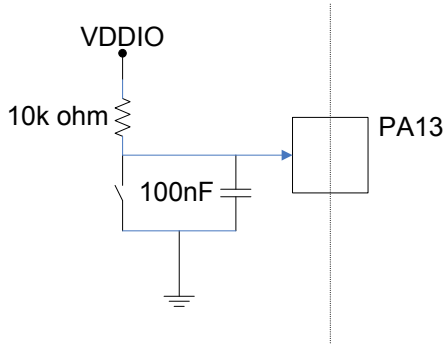
Signal name	Recommended pin connection	Description
TDI		Test data input, sampled on rising TCK.
TMS		Test mode select, sampled on rising TCK.
TCK		Test clock, fully asynchronous to system clock frequency.
TDO		Test data output, driven on falling TCK.
RESET		Device external reset line.
EVTI		Event input.
MDO[0:5]		Trace data output.
EVTO		Event output.
MCK0		Trace data output clock.
MSE[0:1]		Trace frame control.

6. GPIO Pin Used by Default USB DFU Bootloader

All AVR UC3B series devices are shipped with default USB DFU Bootloader. If this Bootloader is going to be used in the application, a pull up or pull down resistor (depending up on IO Pin Condition level in the user page configuration word) must be connected to specific GPIO pin. The logic level of this GPIO pin will be used as hardware condition to enter into the Bootloader mode.

The IO condition pin used in default USB DFU Bootloader (For UC3B Device) is **PA13**. By default, logic low condition is used to enter into Bootloader mode. Normally Push button in Atmel AVR UC3B Evaluation kits is used for this purpose. Following schematic is a typical example for this.

Figure 6-1. Bootloader GPIO pin – pull-up resistor typical example schematic.



To know more about the USB DFU Bootloader functionalities and its usage, please refer to the application note AVR32784: AVR UC3 USB DFU Bootloader.

7. Suggested Reading

7.1 Device Datasheet

The device datasheet contains block diagrams of the peripherals and details about implementing firmware for the device. The datasheet is available on http://www.atmel.com/products/microcontrollers/avr/default.aspx?tab=documents.

7.2 Evaluation Kit Schematic

The evaluation kit EVK1101 contains the full schematic for the board; it can be used as a reference design. The schematic is available on http://www.atmel.com/products/microcontrollers/avr/default.aspx?tab=tools.

Note that capacitors are soldered on the NEXUS trace data output lines on the EVK1101. This may cause speed limitations. In order to not have this limitation the capacitors has to be removed.

8. Revision History

Doc. rev.	Date	Comments
32095E	08/2013	New document template. Description for VDDPLL is corrected, external oscillator range is updated, and default bootloader pin is mentioned.
32095D	12/2008	New document template. Bugs fixed.
32095C	09/2008	XIN voltage corrected.
32095B	04/2008	Several updates.
32095A	01/2008	Initial document release.

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