REV	CHANGE DESCRIPTION	NAME	DATE
A	Release		1-26-16

DOCUMENT DESCRIPTION

Schematic Checklist for the LAN9355, 88-pin SQFN Package

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Document Number	Revision
SC471253	A

Schematic Checklist for LAN9355

Information Particular for the 88-pin SQFN Package

The LAN9355 is a full featured, 3 port 10/100 managed Ethernet switch designed for embedded applications where performance, flexibility, ease of integration and system cost control are required. The LAN9355 combines all the functions of a 10/100 switch system, including the Switch Fabric, packet buffers, Buffer Manager, Media Access Controllers (MACs), PHY transceivers, and serial management. IEEE 1588v2 is supported via the integrated IEEE 1588v2 hardware time stamp unit, which supports end-to-end and peer-to-peer transparent clocks. The LAN9355 complies with the IEEE 802.3 (full/half-duplex 10BASE-T and 100BASE-TX) Ethernet protocol, IEEE 802.3az Energy Efficient Ethernet (EEE) (100Mbps only), and 802.1D/802.1Q network management protocol specifications, enabling compatibility with industry standard Ethernet and Fast Ethernet applications. 100BASE-FX is supported via an external fiber transceiver.

The ten possible combinations for the 3 ports are illustrated in the following block diagram. This schematic checklist is organized such that checking a LAN9355 schematic should be very straight forward. Upon deciding the configuration required for each block as per the application, the sections that follow the block diagram outline each port. Each possible configuration is described in each of the port sections.

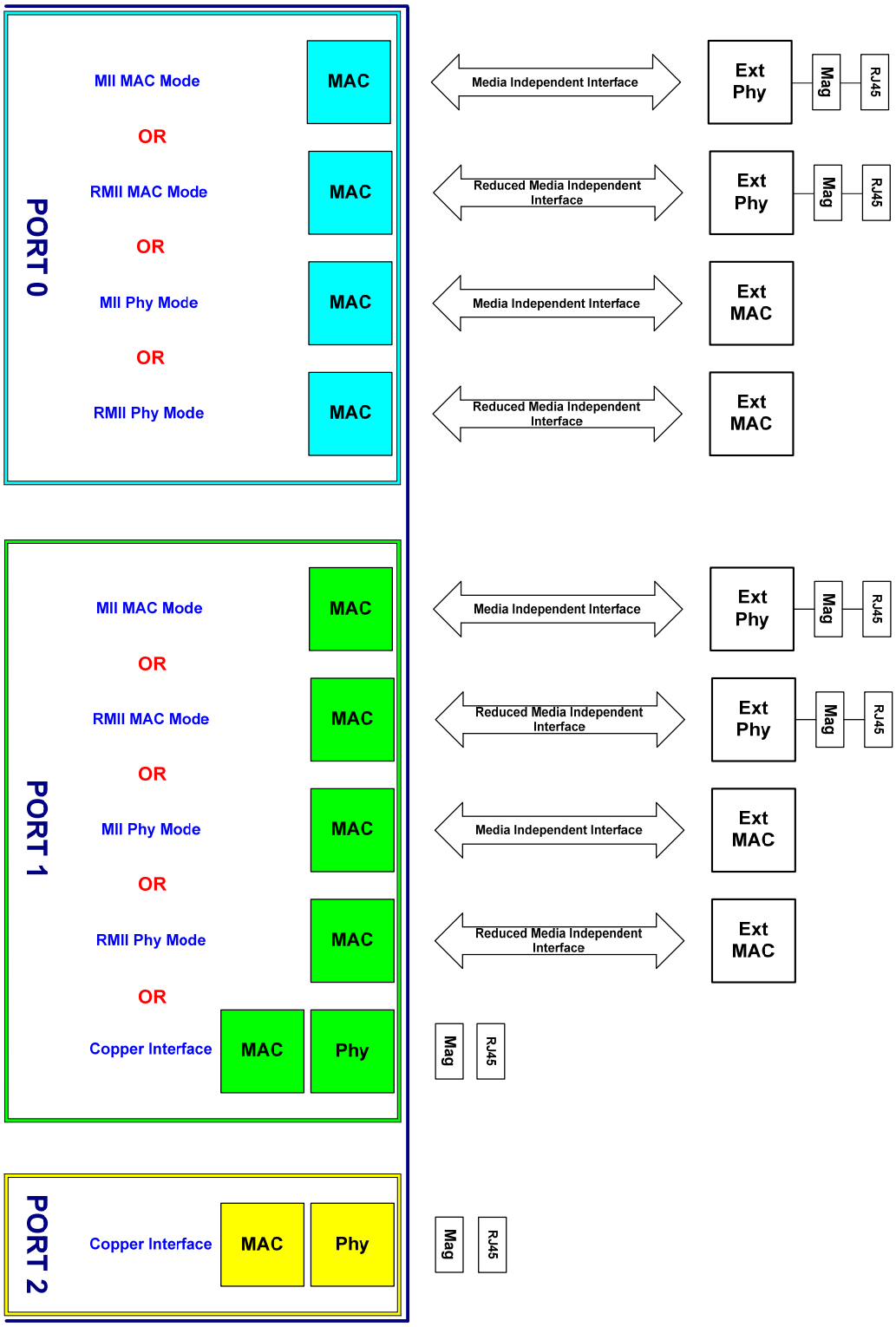


Figure 1 – Block Diagram

Port 0 Configurations

Port 0 Configuration Straps:

1. P0_MODE3, P0_MODE2, P0_MODE1, P0_MODE0 (pins 22, 32, 33 & 36), these four straps configure the mode of Port 0. These pins have weak internal pull-ups and can be driven low with an external 10.0K Ω resistor to digital ground. The possible modes for Port 0 are as follows:

Port 0 Mode Configuration Straps			
P0_MODE[3..0]	**Mode**	**Speed**	**Clock**
00xx	MII MAC Mode	100 Mbps	
010x	MII Phy Mode	100 Mbps	
0110	MII Phy Mode	200 Mbps	12 mA Output
0111	MII Phy Mode	200 Mbps	16 mA Output
100x	RMII MAC Mode	100 Mbps	Input
1010	RMII MAC Mode	100 Mbps	12 mA Output
1011	RMII MAC Mode	100 Mbps	16 mA Output
110x	RMII Phy Mode	100 Mbps	Input
1110	RMII Phy Mode	100 Mbps	12 mA Output
1111	RMII Phy Mode	100 Mbps	16 mA Output

2. P0_DUPLEX (pin 54), For MII MAC and RMII MAC Modes, this pin can be changed at any time (live value) and is typically tied to the duplex indication from the external PHY. It can be overridden by the Duplex Mode (VPHY_DUPLEX) bit in the Port 0 Port x Virtual PHY Basic Control Register (VPHY_BASIC_CTRL_x) by clearing the Auto-Negotiation (VPHY_AN) bit in the same register. The polarity of this pin is determined by the duplex_pol_strap_0. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

   Note: For MII PHY and RMII PHY Modes, this pin is **not** used.

3. P0_SPEED (pin 28), in RMII MAC Mode only, this pin can be changed at any time (live value) and is typically tied to the speed indication from the external PHY. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

   Note: For MII PHY and RMII PHY Modes, this pin is **not** used.

Port 0 MII MAC Mode:

The following diagram shows each of the pins on the Port 0 MII MAC Interface of the LAN9355. The design engineer should always double check his connections and make sure that outputs from the LAN9355 device are driving inputs on the target device. Also, check that inputs on the LAN9355 are being driven from outputs on the target device.

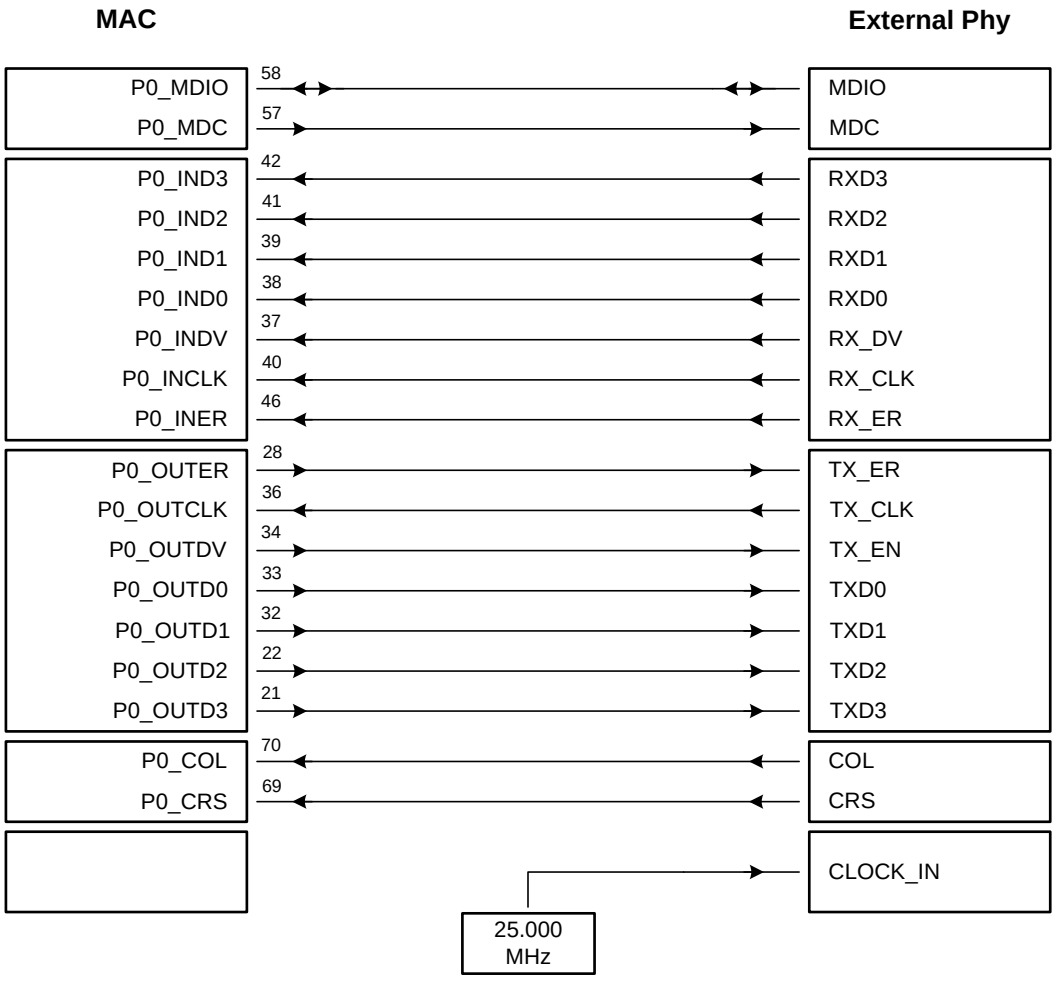


Figure 2 LAN9355 MII MAC Mode

The 25.000 MHz clock supplied to the external Phy provides the TX_CLK and RX_CLK clocks to the MAC in the LAN9355.

Port 0 MII Phy & MII Turbo Phy Mode:

The following diagram shows each of the pins on the Port 0 MII Phy Interface of the LAN9355 device. The design engineer should always double check his connections and make sure that outputs from the LAN9355 device are driving inputs on the target device. Also, check that inputs on the LAN9355 are being driven from outputs on the target device.

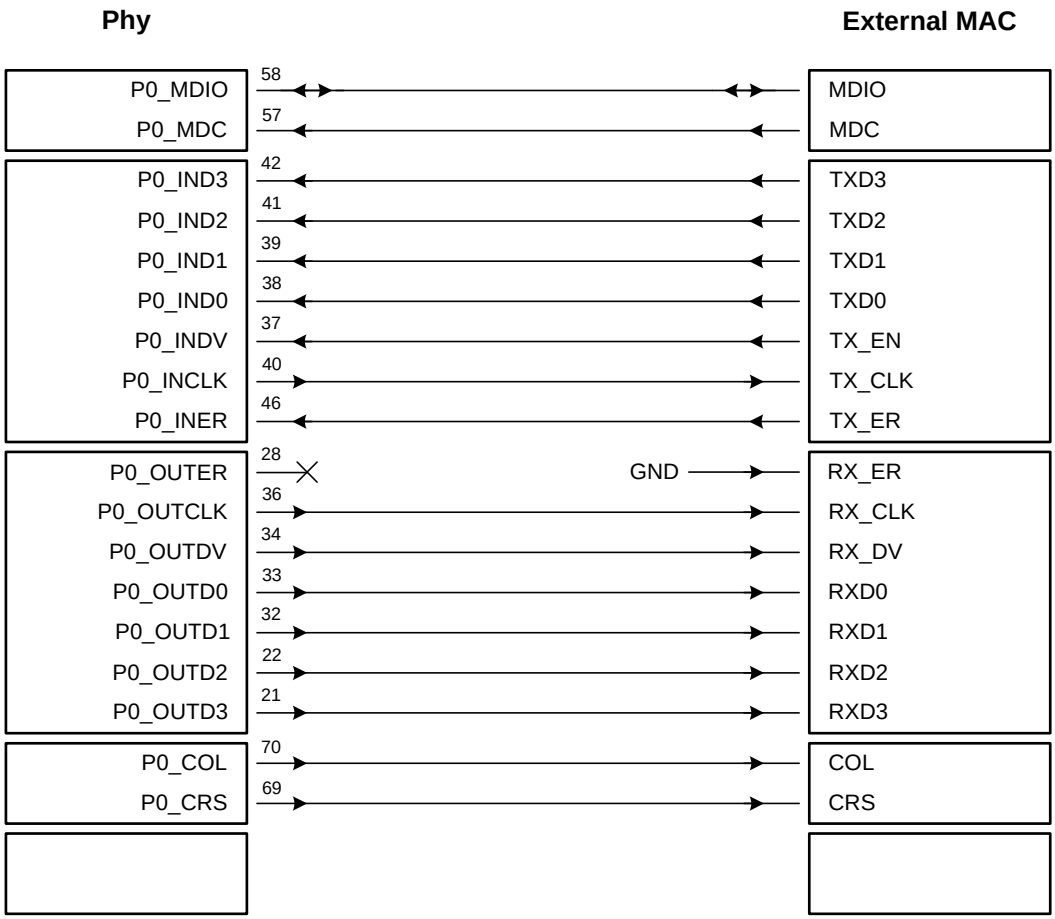


Figure 3 LAN9355 MII Phy Mode

The TX_CLK and RX_CLK clocks are supplied to the external MAC from the LAN9355.

Port 0 RMII MAC Mode:

The following diagram shows each of the pins on the Port 0 RMII MAC Interface of the LAN9355 device. The design engineer should always double check his connections and make sure that outputs from the LAN9355 device are driving inputs on the target device. Also, check that inputs on the LAN9355 are being driven from outputs on the target device.

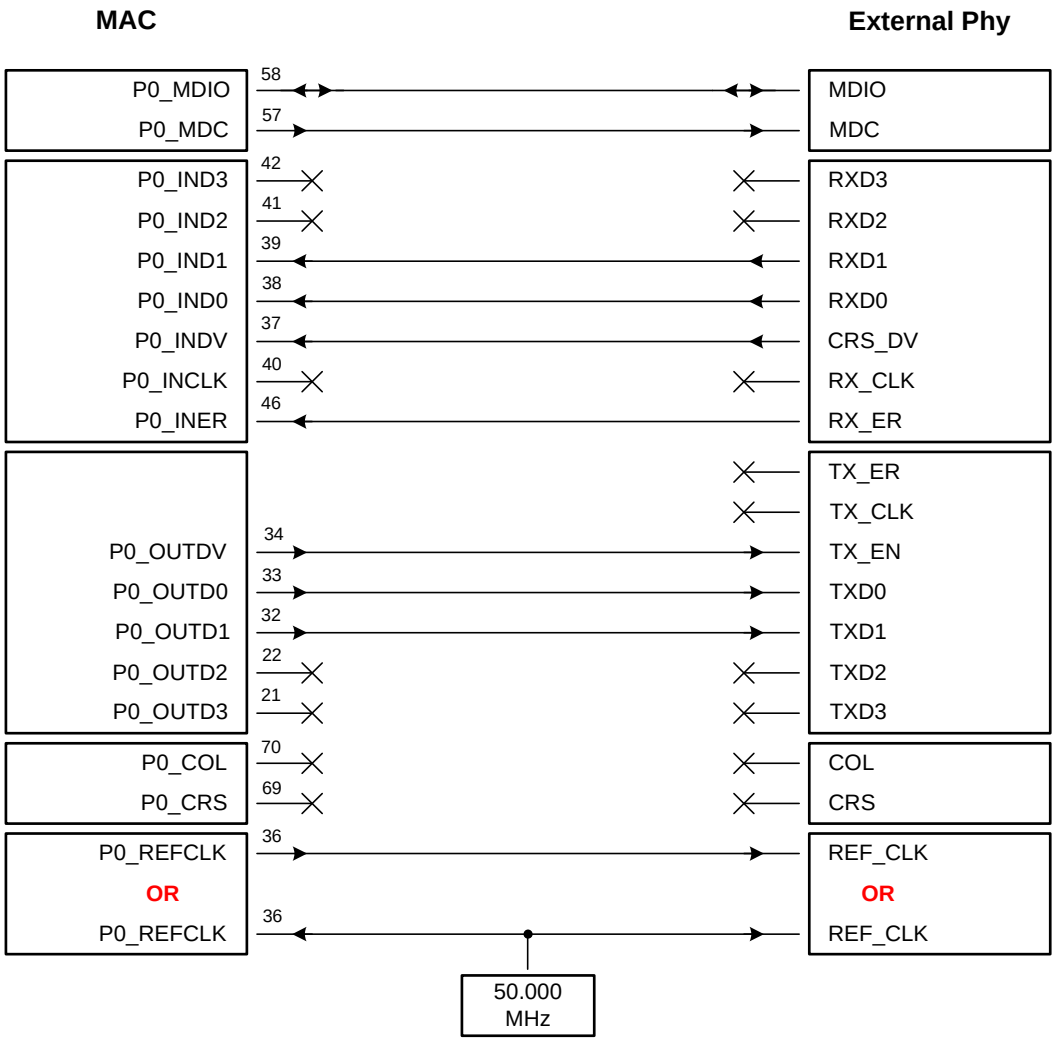


Figure 4 LAN9355 RMII MAC Mode

The 50.000 MHz RMII Reference Clock can be configured in one of two ways. An external 50.000 MHz clock oscillator can be supplied to both the LAN9355 and the target Phy. The other option is to have the LAN9355 output the 50.000 MHz Reference Clock to the target Phy.

Port 0 RMII Phy Mode:

The following diagram shows each of the pins on the Port 0 RMII Phy Interface of the LAN9355 device. The design engineer should always double check his connections and make sure that outputs from the LAN9355 device are driving inputs on the target device. Also, check that inputs on the LAN9355 are being driven from outputs on the target device.

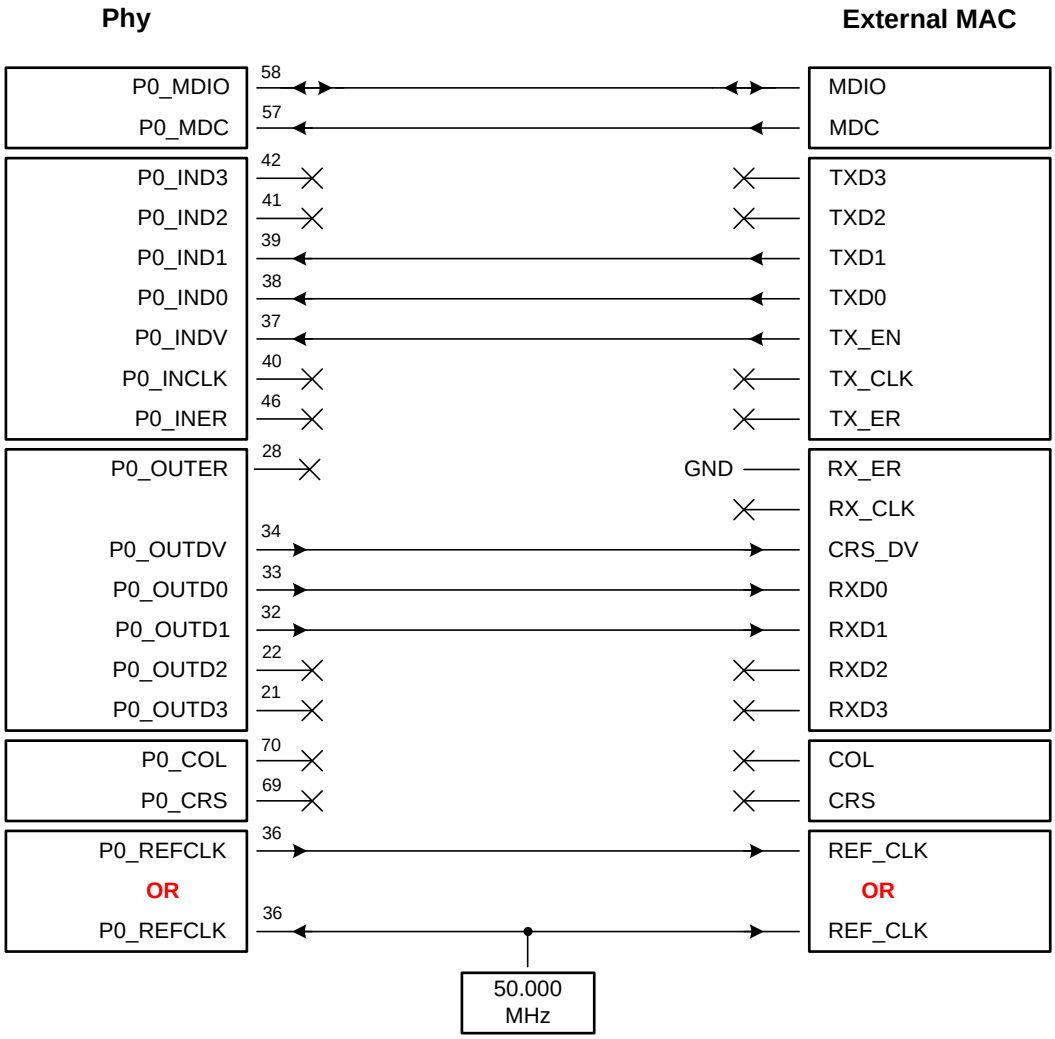


Figure 5 LAN9355 RMII Phy Mode

The 50.000 MHz RMII Reference Clock can be configured in one of two ways. An external 50.000 MHz clock oscillator can be supplied to both the LAN9355 and the target MAC. The other option is to have the LAN9355 output the 50.000 MHz Reference Clock to the target MAC.

Port 1 Configurations

Port 1 Configuration Straps:

1. P1_INTPHY, P1_MODE3, P1_MODE2, P1_MODE1, P1_MODE0 (pins 64, 49, 51, 52 & 50), these five straps configure the mode of Port 1. These pins have weak internal pull-ups and can be driven low with an external 10.0K Ω resistor to digital ground. The possible modes for Port 1 are as follows:

Port 1 Mode Configuration Straps			
P1_INTPHY P1_MODE[3..0]	**Mode**	**Speed**	**Clock**
0 00xx	MII MAC Mode	100 Mbps	
0 010x	MII Phy Mode	100 Mbps	
0 0110	MII Phy Mode	200 Mbps	12 mA Output
0 0111	MII Phy Mode	200 Mbps	16 mA Output
0 100x	RMII MAC Mode	100 Mbps	Input
0 1010	RMII MAC Mode	100 Mbps	12 mA Output
0 1011	RMII MAC Mode	100 Mbps	16 mA Output
0 110x	RMII Phy Mode	100 Mbps	Input
0 1110	RMII Phy Mode	100 Mbps	12 mA Output
0 1111	RMII Phy Mode	100 Mbps	16 mA Output
1 xxxx	Internal Phy Mode		

2. P1_DUPLEX (pin 71), For MII MAC and RMII MAC Modes, **t**his pin can be changed at any time (live value) and is typically tied to the duplex indication from the external PHY. It can be overridden by the Duplex Mode (VPHY_DUPLEX) bit in the Port 1 Port x Virtual PHY Basic Control Register (VPHY_BASIC_CTRL_x) by clearing the Auto-Negotiation (VPHY_AN) bit in the same register. The polarity of this pin is determined by the duplex_pol_strap_1. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

   Note: For MII PHY and RMII PHY Modes, **t**his pin is **not** used.

3. P1_SPEED (pin 44), in RMII MAC Mode only, this pin can be changed at any time (live value) and is typically tied to the speed indication from the external PHY. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

   Note: For MII PHY and RMII PHY Modes, this pin is **not** used.

Port 1 MII MAC Mode:

The following diagram shows each of the pins on the Port 1 MII MAC Interface of the LAN9355 device. The design engineer should always double check his connections and make sure that outputs from the LAN9355 device are driving inputs on the target device. Also, check that inputs on the LAN9355 are being driven from outputs on the target device.

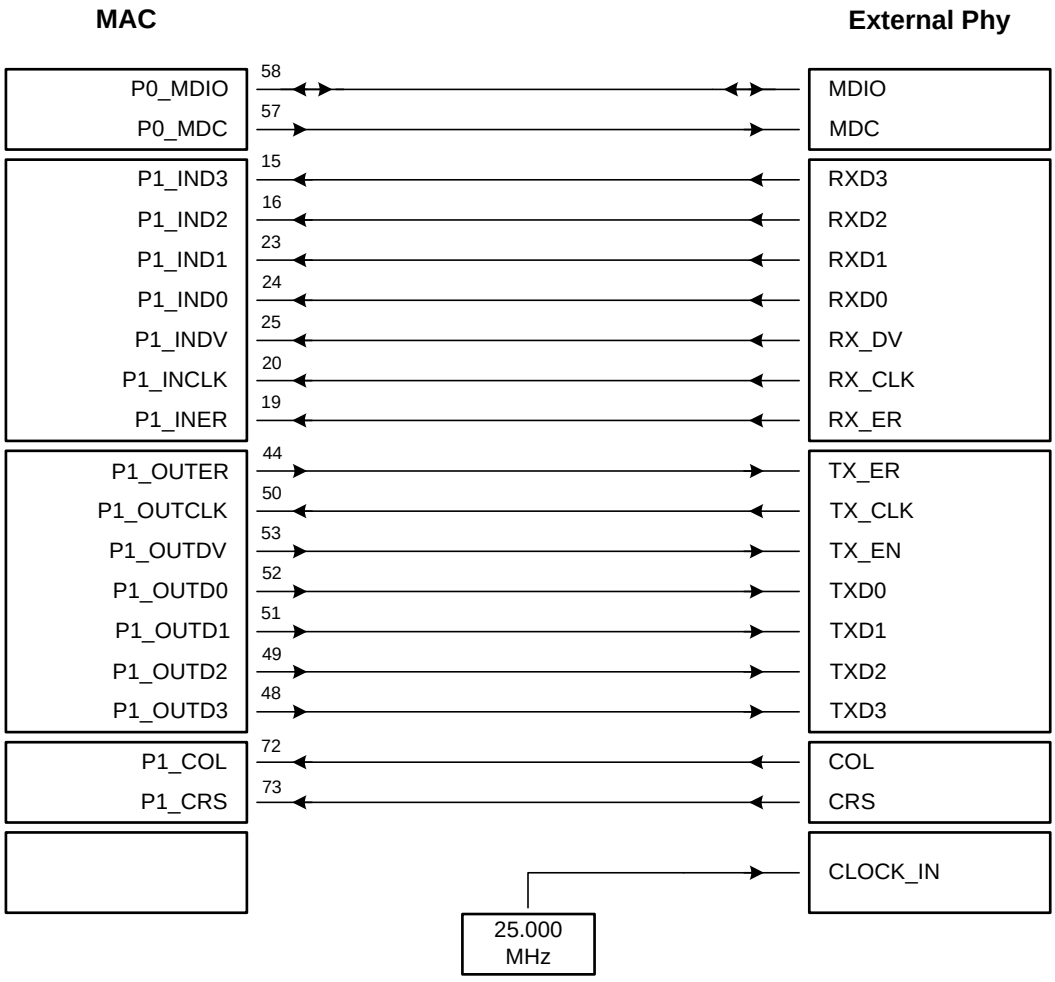


Figure 6 LAN9355 MII MAC Mode

The 25.000 MHz clock supplied to the external Phy provides the TX_CLK and RX_CLK clocks to the MAC in the LAN9355.

Port 1 MII Phy & MII Turbo Phy Mode:

The following diagram shows each of the pins on the Port 1 MII Phy Interface of the LAN9355 device. The design engineer should always double check his connections and make sure that outputs from the LAN9355 device are driving inputs on the target device. Also, check that inputs on the LAN9355 are being driven from outputs on the target device.

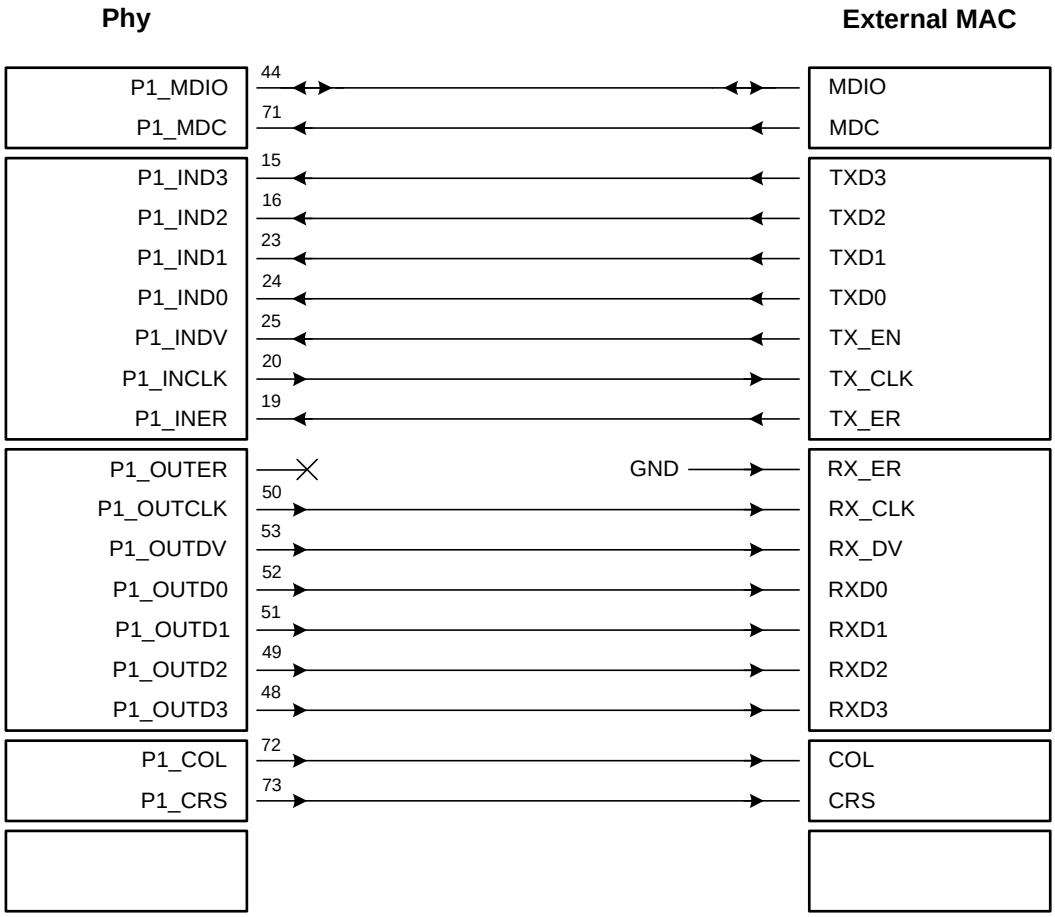


Figure 7 LAN9355 MII Phy Mode

The TX_CLK and RX_CLK clocks are supplied to the external MAC from the LAN9355.

Port 1 RMII MAC Mode:

The following diagram shows each of the pins on the Port 1 RMII MAC Interface of the LAN9355 device. The design engineer should always double check his connections and make sure that outputs from the LAN9355 device are driving inputs on the target device. Also, check that inputs on the LAN9355 are being driven from outputs on the target device.

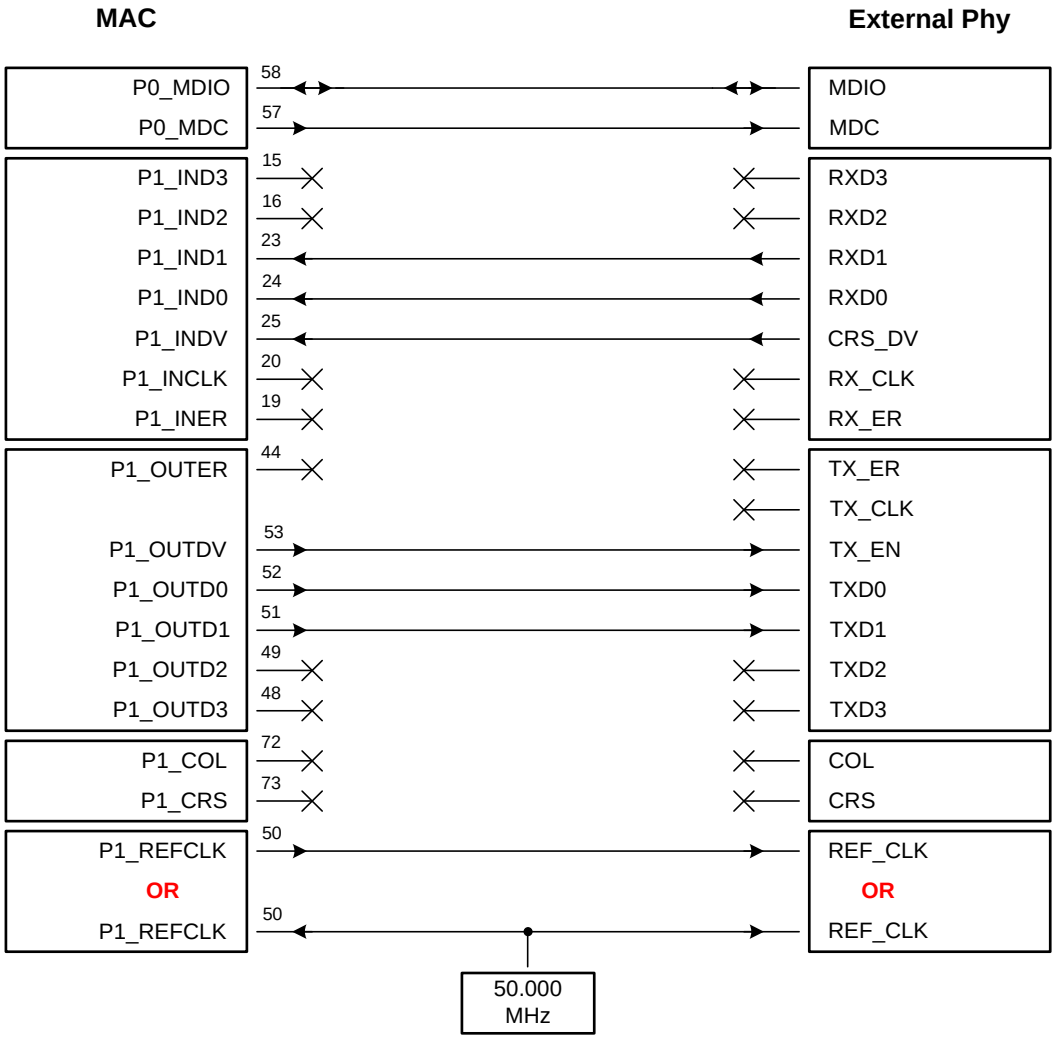


Figure 8 LAN9355 RMII MAC Mode

The 50.000 MHz RMII Reference Clock can be configured in one of two ways. An external 50.000 MHz clock oscillator can be supplied to both the LAN9355 and the target Phy. The other option is to have the LAN9355 output the 50.000 MHz Reference Clock to the target Phy.

Port 1 RMII Phy Mode:

The following diagram shows each of the pins on the Port 1 RMII Phy Interface of the LAN9355 device. The design engineer should always double check his connections and make sure that outputs from the LAN9355 device are driving inputs on the target device. Also, check that inputs on the LAN9355 are being driven from outputs on the target device.

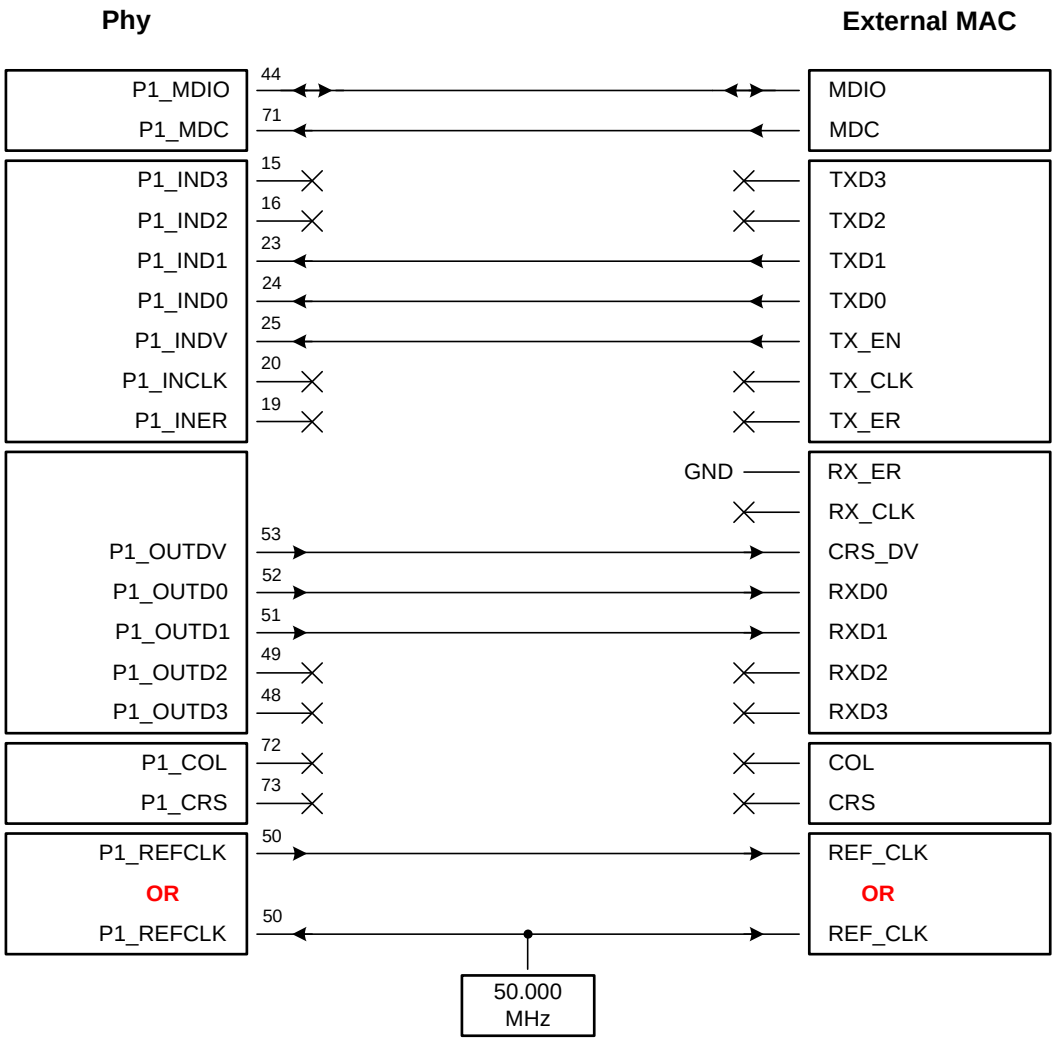


Figure 9 LAN9355 RMII Phy Mode

The 50.000 MHz RMII Reference Clock can be configured in one of two ways. An external 50.000 MHz clock oscillator can be supplied to both the LAN9355 and the target MAC. The other option is to have the LAN9355 output the 50.000 MHz Reference Clock to the target MAC.

LAN9355 SQFN Port A Copper Twisted Pair Phy Interface:

1. TXPA (pin 76); This pin is the transmit twisted pair output positive connection from the primary internal Phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33TXRX1 (created from +3.3V). This pin also connects to the transmit channel of the primary magnetics.

2. TXNA (pin 75); This pin is the transmit twisted pair output negative connection from the primary internal Phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33TXRX1 (created from +3.3V). This pin also connects to the transmit channel of the primary magnetics.

3. For Port A, Transmit Channel connection and termination details, refer to Figure 10.

4. RXPA (pin 78); This pin is the receive twisted pair input positive connection to the primary internal Phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33TXRX1 (created from +3.3V). This pin also connects to the receive channel of the primary magnetics.

5. RXNA (pin 77); This pin is the receive twisted pair input negative connection to the primary internal Phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33TXRX1 (created from +3.3V). This pin also connects to the receive channel of the primary magnetics.

6. For Port A, Receive Channel connection and termination details, refer to Figure 11.

7. For added EMC flexibility in a LAN9355 design, the designer should include four low valued capacitors on the TXPA, TXNA, RXPA & RXNA pins. Low valued capacitors (less than 22 ρF) can be added to each line and terminated to digital ground. These components can be added to the schematic and should be designated as Do Not Populate (DNP).

LAN9355 SQFN Port B Copper Twisted Pair Phy Interface:

1. TXPB (pin 85); This pin is the transmit twisted pair output positive connection from the secondary internal Phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33TXRX2 (created from +3.3V). This pin also connects to the transmit channel of the secondary magnetics.

2. TXNB (pin 86); This pin is the transmit twisted pair output negative connection from the secondary internal Phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33TXRX2 (created from +3.3V). This pin also connects to the transmit channel of the secondary magnetics.

3. For Port B, Transmit Channel connection and termination details, refer to Figure 10.

4. RXPB (pin 83); This pin is the receive twisted pair input positive connection to the secondary internal Phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33TXRX2 (created from +3.3V). This pin also connects to the receive channel of the secondary magnetics.

5. RXNB (pin 84); This pin is the receive twisted pair input negative connection to the primary internal Phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33TXRX2 (created from +3.3V). This pin also connects to the receive channel of the secondary magnetics.

6. For Port B, Receive Channel connection and termination details, refer to Figure 11.

7. For added EMC flexibility in a LAN9355 design, the designer should include four low valued capacitors on the TXPB, TXNB, RXPB & RXNB pins. Low valued capacitors (less than 22 ρF) can be added to each line and terminated to digital ground. These components can be added to the schematic and should be designated as Do Not Populate (DNP).

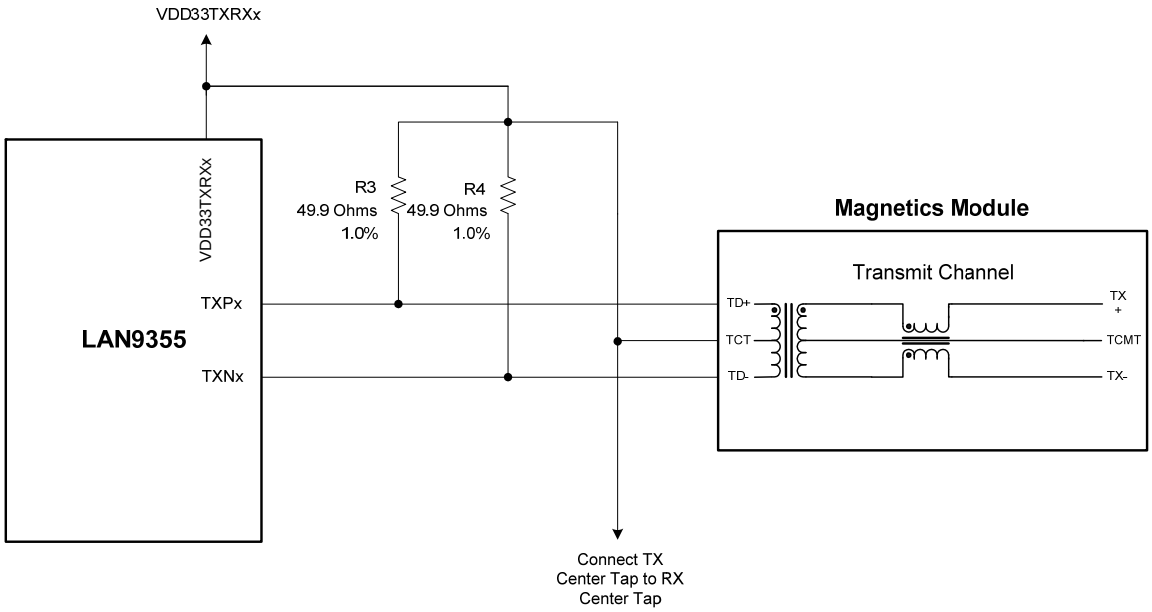


Figure 10 – Transmit Channel Connections and Terminations

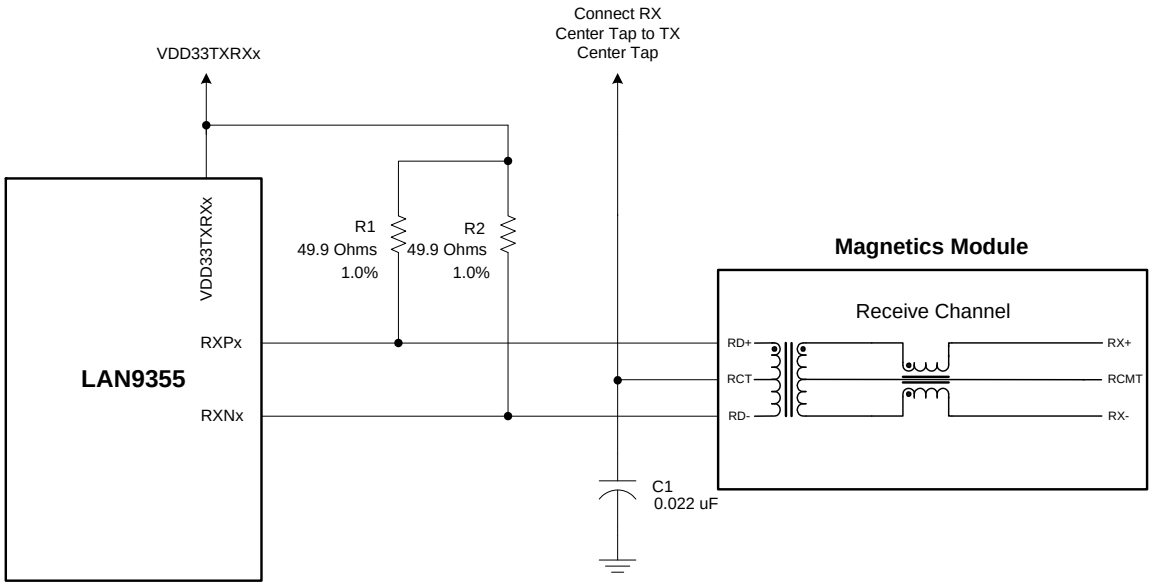


Figure 11 - Receive Channel Connections and Terminations

LAN9355 SQFN Port A Copper Twisted Pair Phy Magnetics:

1. The center tap connection on the LAN9355 side for the transmit channel must be connected to VDD33TXRX1 (created from +3.3V) directly. The transmit channel center tap of the magnetics also connects to the receive channel center tap of the magnetics.

2. The center tap connection on the LAN9355 side for the receive channel is connected to the transmit channel center tap on the primary magnetics. In addition, a 0.022 μF capacitor is required from the receive channel center tap of the primary magnetics to digital ground.

3. The center tap connection on the cable side (RJ45 side) for the primary transmit channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

4. The center tap connection on the cable side (RJ45 side) for the primary receive channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

5. Only one 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground is required. It is shared by both TX & RX center taps.

6. Assuming the design of an end-point device (NIC), pin 1 of the RJ45 is TX+ and should trace through the magnetics to TXPA (pin 76) of the LAN9355 SQFN.

7. Assuming the design of an end-point device (NIC), pin 2 of the RJ45 is TX- and should trace through the magnetics to TXNA (pin 75) of the LAN9355 SQFN.

8. Assuming the design of an end-point device (NIC), pin 3 of the RJ45 is RX+ and should trace through the magnetics to RXPA (pin 78) of the LAN9355 SQFN.

9. Assuming the design of an end-point device (NIC), pin 6 of the RJ45 is RX- and should trace through the magnetics to RXNA (pin 77) of the LAN9355 SQFN.

10. When using the LAN9355 in the HP Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module is required. Please refer to the Reference Material section of this document for proper magnetics.

LAN9355 SQFN Port B Copper Twisted Pair Phy Magnetics:

1. The center tap connection on the LAN9355 side for the transmit channel must be connected to VDD33TXRX2 (created from +3.3V) directly. The transmit channel center tap of the magnetics also connects to the receive channel center tap of the magnetics.

2. The center tap connection on the LAN9355 side for the receive channel is connected to the transmit channel center tap on the secondary magnetics. In addition, a 0.022 μF capacitor is required from the receive channel center tap of the secondary magnetics to digital ground.

3. The center tap connection on the cable side (RJ45 side) for the secondary transmit channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

4. The center tap connection on the cable side (RJ45 side) for the secondary receive channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

5. Only one 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground is required. It is shared by both TX & RX center taps.

6. Assuming the design of an end-point device (NIC), pin 1 of the RJ45 is TX+ and should trace through the magnetics to TXPB (pin 85) of the LAN9355 SQFN.

7. Assuming the design of an end-point device (NIC), pin 2 of the RJ45 is TX- and should trace through the magnetics to TXNB (pin 86) of the LAN9355 SQFN.

8. Assuming the design of an end-point device (NIC), pin 3 of the RJ45 is RX+ and should trace through the magnetics to RXPB (pin 83) of the LAN9355 SQFN.

9. Assuming the design of an end-point device (NIC), pin 6 of the RJ45 is RX- and should trace through the magnetics to RXNB (pin 84) of the LAN9355 SQFN.

10. When using the LAN9355 in the HP Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module is required. Please refer to the Reference Material section of this document for proper magnetics.

Copper Twisted Pair RJ45 Connectors Ports A & B:

1. Pins 4 & 5 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 ρF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:

    a) Pins 4 & 5 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 ρF, 2KV capacitor (C_{rjterm}).

    b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 ρF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.

2. Pins 7 & 8 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 ρF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:

    a) Pins 7 & 8 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 ρF, 2KV capacitor (C_{rjterm}).

    b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 ρF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.

3. The RJ45 shield should be attached directly to chassis ground.

LAN9355 SQFN Port A Fiber Phy (100BASE-FX) Interface:

1. TXPA (pin 76); This pin is the Port A Fiber transmit positive output pin. This low voltage PECL output pin should connect to the external fiber transceiver in the design.

2. TXNA (pin 75); This pin is the Port A Fiber transmit negative output pin. This low voltage PECL output pin should connect to the external fiber transceiver in the design.

3. For Port A, Fiber Transmit Channel connection details, refer to Figure 13.

4. RXPA (pin 78); This pin is the Port A Fiber receive positive input pin. This analog input pin should connect to the external fiber transceiver in the design.

5. RXNA (pin 77); This pin is the Port A Fiber receive negative input pin. This analog input pin should connect to the external fiber transceiver in the design.

6. For Port A, Fiber Receive Channel connection details, refer to Figure 14.

7. FXSDA (pin 9); Port A Fiber Signal Detect. When FX-LOS mode is not selected, this pin functions as the Signal Detect input from the external fiber transceiver. A level above 2 V (typ.) indicates valid signal. When FX-LOS mode is selected, the input buffer is disabled.

8. FXLOSA (pin 9); Port A Fiber Loss of Signal. When FX-LOS mode is selected, this pin functions as the Loss of Signal input from the external transceiver. A high indicates LOS while a low indicates valid signal. When FX-LOS mode is not selected, the input buffer and pull-up are disabled.

9. **Architecture Note:** 100BASE-FX is a version of Fast Ethernet over optical fiber. It uses a 1300 nm near-infrared (NIR) light wavelength transmitted via two strands of optical fiber, one for receive(RX) and the other for transmit(TX). Maximum length is 412 metres (1,350 ft) for half-duplex connections (to ensure collisions are detected), and 2 kilometres (6,600 ft) for full-duplex over multi-mode optical fiber. 100BASE-FX uses the same 4B5B encoding and NRZI line code that 100BASE-TX does. 100BASE-FX should use SC, ST, LC, MTRJ or MIC connectors with SC being the preferred option.

LAN9355 SQFN Port B Fiber Phy (100BASE-FX) Interface:

1. TXPB (pin 85); This pin is the Port B Fiber transmit positive output pin. This low voltage PECL output pin should connect to the fiber transceiver in the design.

2. TXNB (pin 86); This pin is the Port B Fiber transmit negative output pin. This low voltage PECL output pin should connect to the fiber transceiver in the design.

3. For Port B, Fiber Transmit Channel connection details, refer to Figure 13.

4. RXPB (pin 83); This pin is the Port B Fiber receive positive input pin. This analog input pin should connect to the fiber transceiver in the design.

5. RXNB (pin 84); This pin is the Port B Fiber receive negative input pin. This analog input pin should connect to the fiber transceiver in the design.

6. For Port B, Fiber Receive Channel connection details, refer to Figure 14.

7. FXSDB (pin 10); Port B Fiber Signal Detect. When FX-LOS mode is not selected, this pin functions as the Signal Detect input from the external fiber transceiver. A level above 2 V (typ.) indicates valid signal. When FX-LOS mode is selected, the input buffer is disabled.

8. FXLOSB (pin 10); Port B Fiber Loss of Signal. When FX-LOS mode is selected, this pin functions as the Loss of Signal input from the external transceiver. A high indicates LOS while a low indicates valid signal. When FX-LOS mode is not selected, the input buffer and pull-up are disabled.

9. **Architecture Note:** 100BASE-FX is a version of Fast Ethernet over optical fiber. It uses a 1300 nm near-infrared (NIR) light wavelength transmitted via two strands of optical fiber, one for receive(RX) and the other for transmit(TX). Maximum length is 412 metres (1,350 ft) for half-duplex connections (to ensure collisions are detected), and 2 kilometres (6,600 ft) for full-duplex over multi-mode optical fiber. 100BASE-FX uses the same 4B5B encoding and NRZI line code that 100BASE-TX does. 100BASE-FX should use SC, ST, LC, MTRJ or MIC connectors with SC being the preferred option.

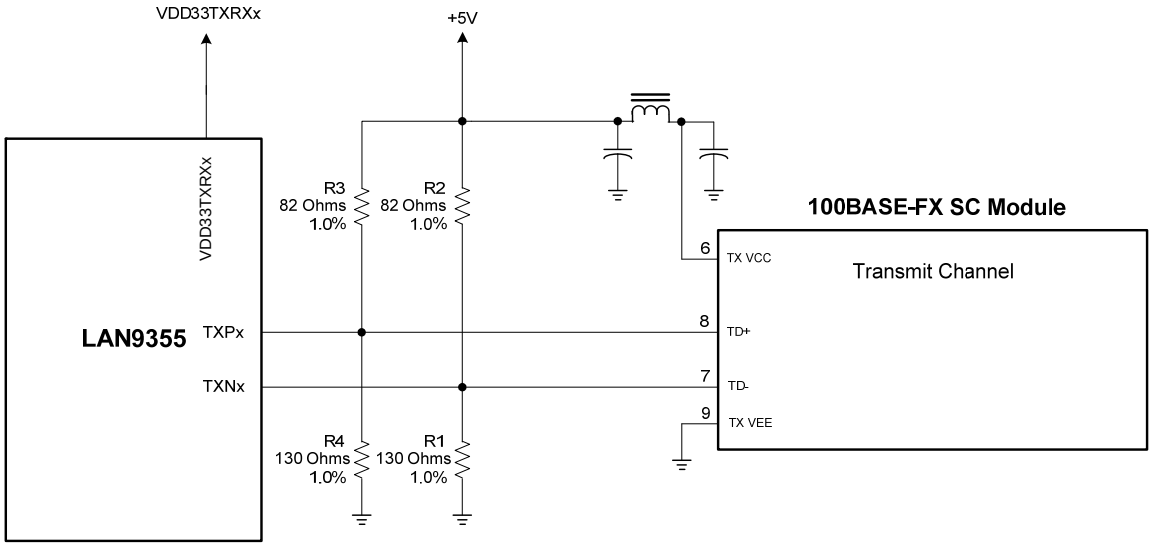


Figure 13 – Fiber Transmit Channel Connections

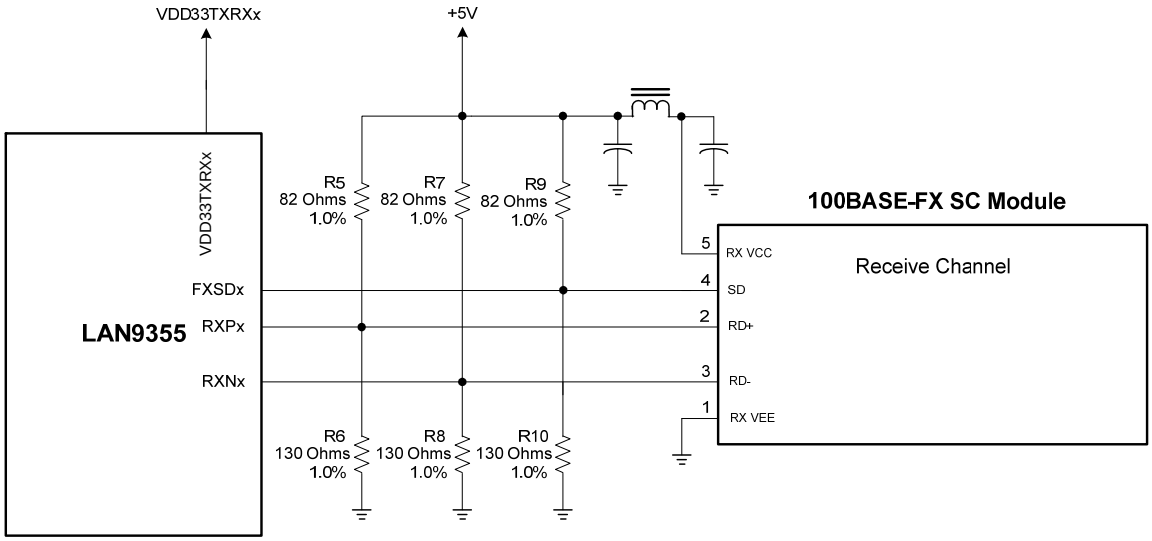


Figure 14 – Fiber Receive Channel Connections

CTP / FX-SD / FX-LOS Configuration Pins:

1. FXLOSEN (pin 8) is a tri-level configuration strap input that selects between FX-LOS and FX-SD / Copper Twisted Pair mode. The voltage levels are as follows:

   Below +1 V = Selects FX-SD / Copper Twisted Pair for Ports A and B, further determined by FXSDENA and FXSDENB.

   +1.5 V = Selects FX-LOS for Port A and FXSD / copper twisted pair for Port B, further determined by FXSDENB.

   Above +2 V = Selects FX-LOS for Ports A and B.

   A pull-up / pull-down resistor value of 10K is recommended in order to attain the required high / low voltage levels listed above. A voltage divider of two 10K resistors can be used for the middle, +1.5 V level listed above.

2. FXSDENA (pin 9), when FX-LOS mode is not selected, this configuration strap input selects between FX-SD and Copper Twisted Pair mode. When FX-LOS mode is selected, this input configuration strap is disabled.

   Below +1V = Selects Copper Twisted Pair mode for Port A.

   Above +1 V = Selects FX-SD fiber mode for Port A.

   A pull-up / pull-down resistor value of 10K is recommended in order to attain the required high / low voltage levels listed above.

3. FXSDENB (pin 10), when FX-LOS mode is not selected, this configuration strap input selects between FX-SD and Copper Twisted Pair mode. When FX-LOS mode is selected, this input configuration strap is disabled.

   Below +1V = Selects Copper Twisted Pair mode for Port B.

   Above +1 V = Selects FX-SD fiber mode for Port B.

   A pull-up / pull-down resistor value of 10K is recommended in order to attain the required high / low voltage levels listed above.

+3.3V Power Supply Connections:

1. The supply for the two internal regulators on the LAN9355 SQFN is pin 5 (VDD33). This pin requires a connection to +3.3V. **Note:** +3.3V must be supplied to this pin even if the internal regulators are disabled.

2. The VDD33 power pin should have one .01 μF (or smaller) capacitor to decouple the LAN9355. The capacitor size should be SMD_0603 or smaller.

3. The analog supply (VDD33TXRX1) pin on the LAN9355 SQFN is pin 74. It requires a connection to +3.3V through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

4. The VDD33TXRX1 pin should have one .01 μF (or smaller) capacitor to decouple the LAN9355. The capacitor size should be SMD_0603 or smaller.

5. The analog supply (VDD33TXRX2) pin on the LAN9355 SQFN is pin 87. It requires a connection to +3.3V through a second ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

6. The VDD33TXRX2 pin should have one .01 μF (or smaller) capacitor to decouple the LAN9355. The capacitor size should be SMD_0603 or smaller.

7. VDD33BIAS (pin 81), this pin serves as the master bias voltage supply for the LAN9355. This pin requires a connection to +3.3V through a third ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

8. The VDD33BIAS pin should have one .01 μF (or smaller) capacitor to decouple the LAN9355. The capacitor size should be SMD_0603 or smaller.

+1.8V to +3.3V Variable I/O Power Supply Connections:

1. The variable I/O supply (VDDIO) pins on the LAN9355 SQFN are 17, 30, 43, 55 & 65. They require an externally supplied voltage supply between +1.8V and +3.3V.

2. Each VDDVARIO pin should have one .01 μF (or smaller) capacitor to decouple the LAN9355. The capacitor size should be SMD_0603 or smaller.

VDDCR:

1. VDDCR (pins 6, 35 & 56), these three pins are used to provide bypassing for the +1.2V core regulator. Each pin requires a 0.01 μF decoupling capacitor. Each capacitor should be located as close as possible to its pin without using vias. In addition, pin 6 requires a bulk capacitor placed as close as possible to pin 6. The bulk capacitor must have a value of at least 1.0 μF, and have an ESR (equivalent series resistance) of no more than 2.0 Ω. Microchip recommends a very low ESR ceramic capacitor for design stability. In addition, pin 6 also requires a 470 pF bypass capacitor. Other values, tolerances & characteristics are not recommended.

Caution: This +1.2V supply is for internal logic only. **Do Not** power other external circuits or devices with this supply.

2. VDD12TX1 (pin 79) and VDD12TX2 (pin 82), these pins supply power for the two Ethernet blocks. These two pins must be tied together. These two pins must be connected to VDDCR through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

3. The VDD12TX1 and VDD12TX2 pins should each have one .01 μF (or smaller) capacitor to decouple the LAN9355. The capacitor size should be SMD_0603 or smaller.

Ground Connections:

1. All grounds, the digital ground pins (GND), the core ground pins (GND_CORE) and the analog ground pins (VSS_A) on the LAN9355 SQFN, are all connected internally to the exposed die paddle ground (VSS). The EDP Ground pad on the underside of the LAN9355 must be connected directly to a solid, contiguous digital ground plane.

2. On the PCB, we recommend one Digital Ground. We do not recommend running separate ground planes for any of our LAN products.

Crystal Connections:

1. A 25.000 MHz crystal must be used with the LAN9355 SQFN. For exact specifications and tolerances refer to the latest revision LAN9355 data sheet.

2. OSCI (pin 1) on the LAN9355 SQFN is the clock circuit input. This pin requires a 27 – 33 ρF capacitor to digital ground. One side of the crystal connects to this pin.

3. OSCO (pin 2) on the LAN9355 SQFN is the clock circuit output. This pin requires a matching 27 – 33 ρF capacitor to ground and the other side of the crystal.

4. Since every system design is unique, the capacitor values are system dependant. The PCB design, the crystal selected, the layout and the type of caps selected all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, the stability and the voltage level of the circuit to guarantee that the circuit meets all design criteria as put forth in the data sheet.

5. For proper operation, the additional external 1.0M Ω resistor across the crystal is no longer required. The necessary resistance has been designed-in internally on the LAN9355 SQFN.

6. OSCVDD12 (pin 3), this pin is supplied by one of the internal +1.2V regulators of the LAN9355 and can be left as a no-connection in this mode (REGEN = high). When REGEN = low, this pin must be supplied by an external +1.2V power supply.

7. OSCVSS (pin 4), this pin should be connected directly to digital ground for all applications.

8. **Design Verification Tip:** Microchip recommends taking advantage of the Clock Output Test Mode in the LAN9355. In order to facilitate system level validation and debug, the crystal clock can be enabled onto the IRQ pin by setting the IRQ Clock Select (IRQ_CLK_SELECT) bit of the Interrupt Configuration Register (IRQ_CFG). The IRQ pin should be set to a push-pull driver by using the IRQ Buffer Type (IRQ_TYPE) bit for the best result. Be sure to include a test pin on the IRQ pin (pin 44) and a ground pin close to the test pin. Using a high-quality, precise frequency counter with 8-digits or better will accurately determine the frequency of the 25.000 MHz in the design. Adjusting the crystal circuit load caps slightly will fine tune the frequency of the circuit.

RBIAS Resistor:

1. RBIAS (pin 80) on the LAN9355 SQFN should connect to digital ground through a 12.1K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the embedded 10/100 Ethernet Physical device.

Required External Pull-ups/Pull-downs:

1. IRQ (pin 62) may require an external pull-up resistor to VDDIO if configured as an Open Drain type.

2. When using the MII / RMII of the LAN9355, a pull-up resistor on P0_MDIO (pin 58) is required. If Port 1 RMII is being used, a pull-up resistor on P1_MDIO (pin 44) is also required. A pull-up resistor of 1.5KΩ to VDDIO is required for this application.

GPIO[7:0] pins:

1. GPIO[7:0] (pins 13, 14, 26, 27, 47, 63, 64, 66) These pins are configurable to operate as general purpose GPIOs. Each pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input by writing the General Purpose I/O Configuration Register (GPIO_CFG) and the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR).

LED pins:

1. LED5 (pin 26) This pin is configured to operate as an LED when the LED 5 Enable bit of the LED Configuration Register (LED_CFG) is set. The buffer type depends on the setting of the LED Function 2-0 (LED_FUN[2:0]) field in the LED Configuration Register (LED_CFG) and is configured to be either a push-pull or open-drain/open-source output. When selected as an open-drain/open-source output, the polarity of this pin depends upon the **PHYADD** strap value sampled at reset.

2. LED4 (pin 27) This pin is configured to operate as an LED when the LED 4 Enable bit of the LED Configuration Register (LED_CFG) is set. The buffer type depends on the setting of the LED Function 2-0 (LED_FUN[2:0]) field in the LED Configuration Register (LED_CFG) and is configured to be either a push-pull or open-drain/open-source output. When selected as an open-drain/open-source output, the polarity of this pin depends upon the **1588EN** strap value sampled at reset.

3. LED3 (pin 47) This pin is configured to operate as an LED when the LED 3 Enable bit of the LED Configuration Register (LED_CFG) is set. The buffer type depends on the setting of the LED Function 2-0 (LED_FUN[2:0]) field in the LED Configuration Register (LED_CFG) and is configured to be either a push-pull or open-drain/open-source output. When selected as an open-drain/open-source output, the polarity of this pin depends upon the **EEEEN** strap value sampled at reset.

4. LED2 (pin 63) This pin is configured to operate as an LED when the LED 2 Enable bit of the LED Configuration Register (LED_CFG) is set. The buffer type depends on the setting of the LED Function 2-0 (LED_FUN[2:0]) field in the LED Configuration Register (LED_CFG) and is configured to be either a push-pull or open-drain/open-source output. When selected as an open-drain/open-source output, the polarity of this pin depends upon the **E2PSIZE** strap value sampled at reset.

5. LED1 (pin 64) This pin is configured to operate as an LED when the LED 1 Enable bit of the LED Configuration Register (LED_CFG) is set. The buffer type depends on the setting of the LED Function 2-0 (LED_FUN[2:0]) field in the LED Configuration Register (LED_CFG) and is configured to be either a push-pull or open-drain/open-source output. When selected as an open-drain/open-source output, the polarity of this pin depends upon the **P1_INTPHY** strap value sampled at reset.

6. LED0 (pin 66) This pin is configured to operate as an LED when the LED 0 Enable bit of the LED Configuration Register (LED_CFG) is set. The buffer type depends on the setting of the LED Function 2-0 (LED_FUN[2:0]) field in the LED Configuration Register (LED_CFG) and is configured to be either a push-pull or open-drain/open-source output. When selected as an open-drain/open-source output, the polarity of this pin depends upon the **MNGT0** strap value sampled at reset.

I^2C Management pins:

1. I2CSDA (pin 60) This pin is the I^2C serial data input/output from/to the external I^2C master. **Note:** This pin must be pulled-up by an external resistor at all times.

2. I2CSCL (pin 61) This pin is the I^2C clock input from the external I^2C master. **Note:** This pin must be pulled-up by an external resistor at all times.

I^2C EEPROM pins:

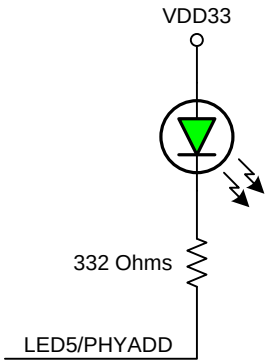
1. EESDA (pin 60) When the device is accessing an external EEPROM, this pin is the I^2C serial data input/open-drain output. **Note:** This pin must be pulled-up by a 10K ohm external resistor at all times.

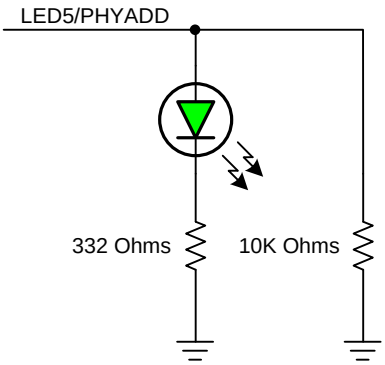
2. EESCL (pin 61) When the device is accessing an external EEPROM this pin is the I^2C clock open-drain output. **Note:** This pin must be pulled-up by a 10K ohm external resistor at all times.

Dedicated Configuration Strap Pins:

1. PHYADD (pin 26) Each individual PHY is assigned a default PHY address via the phy_addr_sel_strap configuration strap as shown below. Virtual PHYs 0 and 1 use the same address since they are on separate management interfaces. In addition, the addresses for Physical PHY A and B can be changed via the PHY Address (PHYADD) field in the PHY x Special Modes Register (PHY_SPECIAL_MODES_x). For proper operation, the addresses for Virtual PHY 0 and Physical PHYs A and B must be unique. No check is performed to assure each PHY is set to a different address.

phy_addr_sel_strap	Virtual Phy 0 and Virtual Phy 1 Default Address Value	Phy A Default Address Value	Phy B Default Address Value
0	0	1	2
1	1	2	3





PHYADD Bit = 1

LED Output Signal from LAN9355 is Active Low

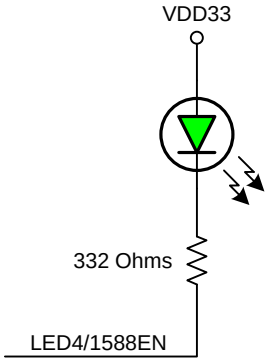
phy_addr_sel_strap = 1

PHYADD Bit = 0

LED Output Signal from LAN9355 is Active High

phy_addr_sel_strap = 0

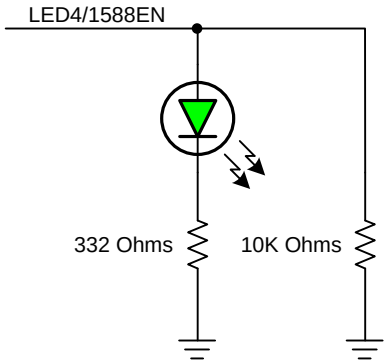
2. 1588EN (pin 27) This strap configures the default value of the 1588 Enable (1588_ENABLE) bit in the 1588 Command and Control Register (1588_CMD_CTL).
Note: The defaults of the 1588 register set are such that the device will perform End-to-End Transparent Clock functionality without further configuration. Writing a one to this bit will enable the 1588 unit.



1588EN Bit = 1

LED Output Signal from LAN9355 is Active Low

1588_enable_strap = 1

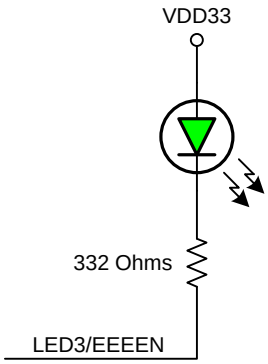


1588EN Bit = 0

LED Output Signal from LAN9355 is Active High

1588_enable_strap = 0

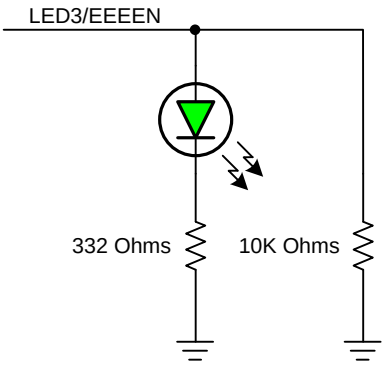
3. EEEEN (pin 47) When set, this bit enables Energy Efficient Ethernet (EEE) operation in the PHY. When cleared, EEE operation is disabled.



EEEEN Bit = 1

LED Output Signal from LAN9355 is Active Low

EEE_enable_strap_1 = 1

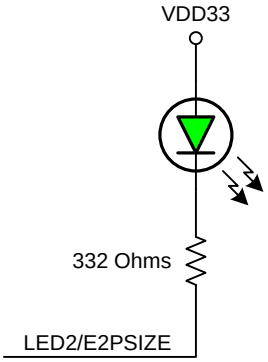


EEEEN Bit = 0

LED Output Signal from LAN9355 is Active High

EEE_enable_strap_1 = 0

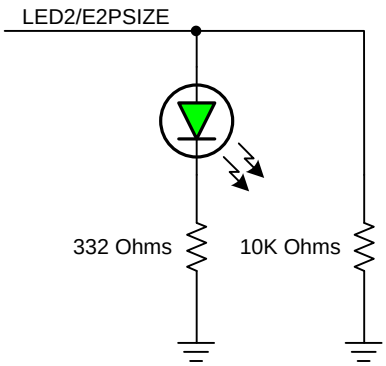
4. E2PSIZE (pin 63), this strap pin configures the I^2C EEPROM size. When latched low, EEPROM sizes 128 x 8-bit (1K) through 2048 x 8-bit (16K) are supported. When latched high, EEPROM sizes 4096 x 8-bit (32K) through 64K x 8-bit (512K) are supported. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.



E2PSIZE Bit = 1

LED Output Signal from LAN9355 is Active Low

32K – 512K EEPROMs Supported

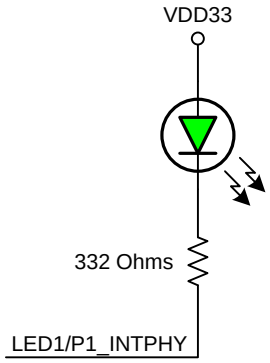


E2PSIZE Bit = 0

LED Output Signal from LAN9355 is Active High

1K – 16K EEPROMs Supported

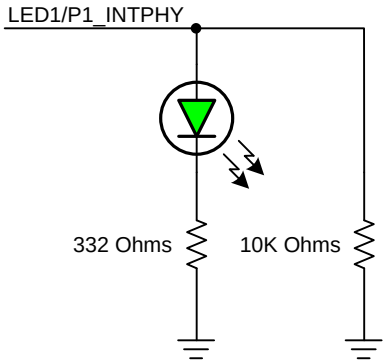
5. P1_INTPHY (pin 64) This configuration strap determines the operating mode of Port 1 on the switch. When P1_INTPHY is latched high, Port 1 is set for Copper Mode. When P1_INTPHY is latched low, Port 1 is set for MII / RMII Mode.



P1_INTPHY Bit = 1

LED Output Signal from LAN9355 is Active Low

Port 1 Set For Copper Mode

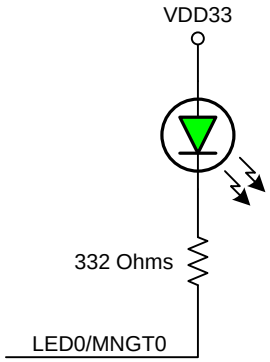


P1_INTPHY Bit = 0

LED Output Signal from LAN9355 is Active High

Port 1 Set For MII / RMII Mode

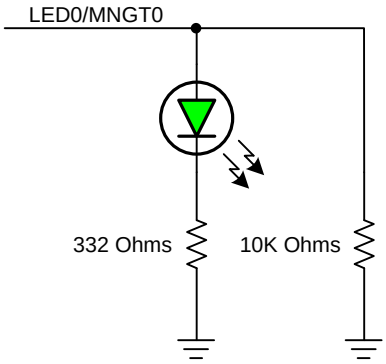
6. MNGT0 (pin 66) This pin configures the serial management mode of the LAN9355. When latched high, the switch is configured for I^2C Managed Mode. When this bit is latched low, the switch is configured for SMI Managed Mode.



MNGT0 Bit = 1

LED Output Signal from LAN9355 is Active Low

I^2C Managed Mode



MNGT0 Bit = 0

LED Output Signal from LAN9355 is Active High

SMI Managed Mode

Miscellaneous:

1. RST# (pin 12), As an input, this active low signal allows external hardware to reset the device. The device also contains an internal power-on reset circuit. Thus this signal may be left unconnected if an external hardware reset is not needed. When used this signal must adhere to the reset timing requirements as detailed in the Section 20.0, "Operational Characteristics," on page 502.

2. REG_EN (pin 7), this pin enables / disables the two +1.2V internal regulators of the LAN9355. Refer to the latest revision of the data sheet for additional information. Connecting this pin to +3.3V will enable the regulators. Connecting this pin to digital ground will disable both regulators. This pin has no internal terminations and must be strapped accordingly.

3. The LAN9355 has an IEEE 1149.1 compliant JTAG Boundary Scan interface. This test interface can be utilized to accomplish board level testing to ensure system functionality and board manufacturability. For details, see the LAN9355 data sheet.

4. TESTMODE (pin 59) This input pin must be tied to VSS to ensure proper operation.

5. In order to take advantage of the JTAG interface, the TESTMODE pin must be driven high. Then, for normal operation, the TESTMODE pin must be driven low. This pin has an internal pull-down to ensure normal operation as a no-connect.

6. IRQ (pin 62) Interrupt request output. The polarity, source and buffer type of this signal is programmable via the Interrupt Configuration Register (IRQ_CFG).

7. There are (8) No-Connect pins (pin 11, 18, 29, 31, 45, 67, 68 & 88) on the LAN9355 and must be left as a no-connects to ensure proper operation of the switch.

8. Incorporate a large SMD resistor (SMD_1210) to connect the chassis ground to the digital ground. This will allow some flexibility at EMI testing for different grounding options. Leave the resistor out, the two grounds are separate. Short them together with a zero ohm resistor. Short them together with a cap or a ferrite bead for best performance.

9. Be sure to incorporate enough bulk capacitors (4.7 - 22μF caps) for each power plane.

10. Configuration strap values are typically latched on power-on reset and system reset. Microchip will guarantee that the proper high / low level will be latched in on any device pin with an internal pull-up or pull-down where the device pin is a true no-connect. However, when the configuration strap pin (typically an output pin) is connected to a load, the input leakage current associated with the input load may have an adverse effect on the high / low level ability of the internal pull-up / pull-down. In this case, it is Microchip's recommendation to include an external resistor to augment the internal pull-up / pull-down to ensure the proper high / low level for configuration strap values. Lower VDDIO voltages will further exacerbate this condition

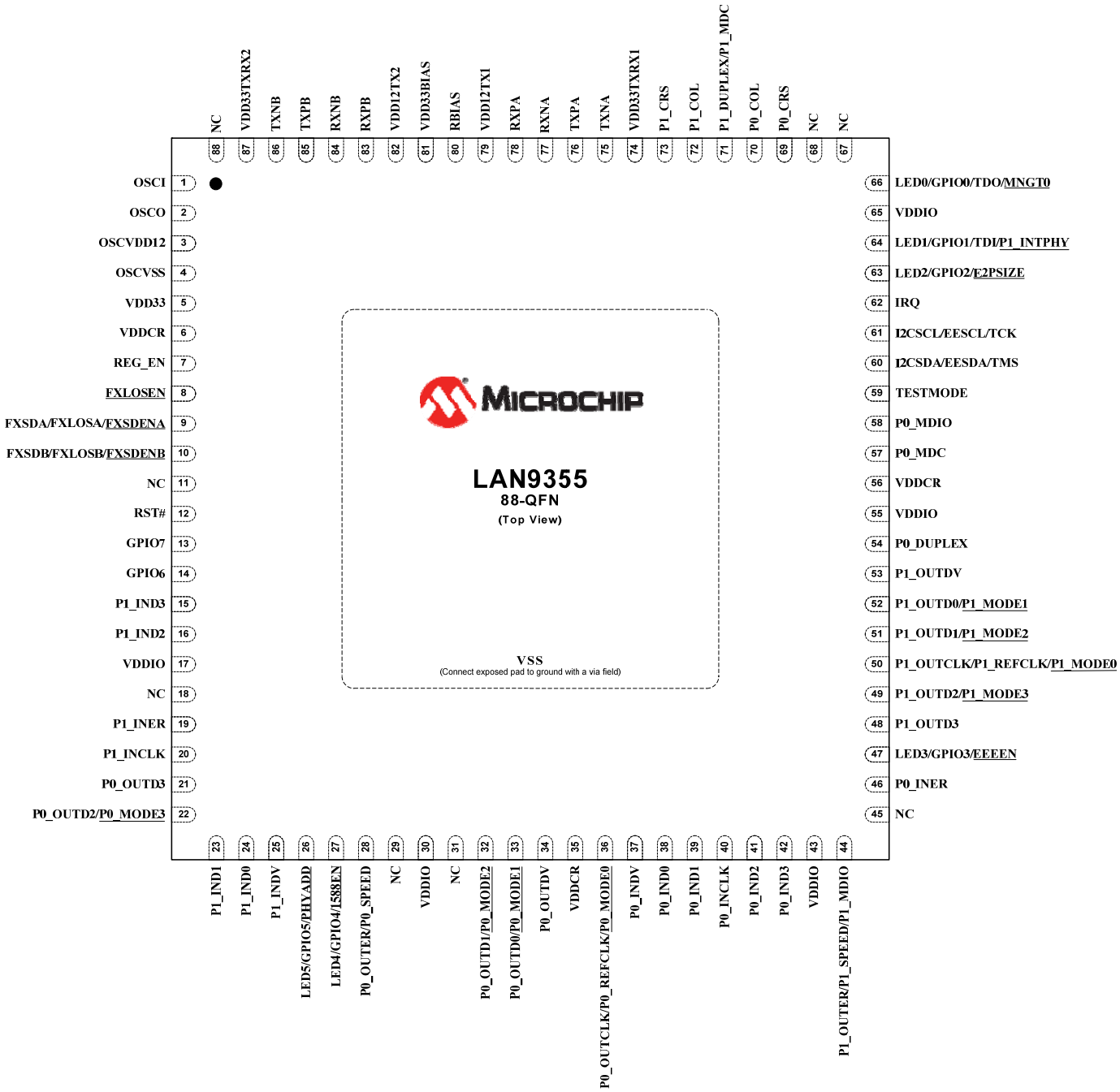
LAN9355 SQFN QuickCheck Pinout Table:

Use the following table to check the LAN9355 SQFN shape in your schematic.

LAN9355 SQFN			
Pin No.	Pin Name	Pin No.	Pin Name
1	OSCI	45	NC
2	OSCO	46	P0_INER
3	OSCVDD12	47	LED3 / GPIO3 / EEEEN
4	OSCVSS	48	P1_OUTD3
5	VDD33	49	P1_OUTD2 / P1_MODE3
6	VDDCR	50	P1_OUTCLK / P1_REFCLK / P1_MODE0
7	REG_EN	51	P1_OUTD1 / P1_MODE2
8	FXLOSEN	52	P1_OUTD0 / P1_MODE1
9	FXSDA / FXLOSA / FXSDENA	53	P1_OUTDV
10	FXSDB / FXLOSB / FXSDENB	54	P0_DUPLEX
11	NC	55	VDDIO
12	RST#	56	VDDCR
13	GPIO7	57	P0_MDC
14	GPIO6	58	P0_MDIO
15	P1_IND3	59	TESTMODE
16	P1_IND2	60	I2CSDA / EESDA / TMS
17	VDDIO	61	I2CSCL / EESCL / TCK
18	NC	62	IRQ
19	P1_INER	63	LED2 / GPIO2 / E2PSIZE
20	P1_INCLK	64	LED1 / GPIO1 / TDI / P1_INTPHY
21	P0_OUTD3	65	VDDIO
22	P0_OUTD2 / P0_MODE3	66	LED0 / GPIO0 / TDO / MNGT0
23	P1_IND1	67	NC
24	P1_IND0	68	NC
25	P1_INDV	69	P0_CRS
26	LED5 / GPIO5 / PHYADD	70	P0_COL
27	LED4 / GPIO4 / 1588EN	71	P1_DUPLEX / P1_MDC
28	P0_OUTER / P0_SPEED	72	P1_COL
29	NC	73	P1_CRS
30	VDDIO	74	VDD33TXRX1
31	NC	75	TXNA
32	P0_OUTD1 / P0_MODE2	76	TXPA
33	P0_OUTD0 / P0_MODE1	77	RXNA
34	P0_OUTDV	78	RXPA
35	VDDCR	79	VDD12TX1
36	P0_OUTCLK / P0_REFCLK / P0_MODE0	80	RBIAS
37	P0_INDV	81	VDD33BIAS
38	P0_IND0	82	VDD12TX2
39	P0_IND1	83	RXPB
40	P0_INCLK	84	RXNB
41	P0_IND2	85	TXPB
42	P0_IND3	86	TXNB
43	VDDIO	87	VDD33TXRX2
44	P1_OUTER / P1_SPEED /P1_MDIO	88	NC
89		**EDP Ground Connection Exposed Die Paddle Ground Pad on Bottom of Package**	

Notes:

LAN9355 SQFN Package Drawing:



Note: Exposed pad **(VSS)** on bottom of package must be connected to ground with a via field.

Reference Material:

1. Microchip LAN9355 Data Sheet; check web site for latest revision.
2. Microchip LAN9355 Reference Design, check web site for latest revision.
3. Microchip Reference Designs are schematics only; there are no associated PCBs.
4. EVB-LAN9355 Customer Evaluation Board & Schematics