ANTC206

Differential Clock Translation

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INTRODUCTION

Considering that each available clock logic type (LVPECL, HCSL, CML, and LVDS) operates with a different common-mode voltage and swing level than the next (see Table 1), it is necessary to design clock logic translation between the driver side and receiver side for any given system design. This application note details how to translate one differential clock into other types of differential logics by adding attenuation resistors and bias circuits between them to attenuate the swing level and re-bias the common-mode for the input of the receiver.

TABLE 1: COMMON-MODE VOLTAGE AND SWING LEVELS OF DIFFERENT CLOCK LOGIC TYPES

Spec.	LVPECL	LVDS	CML[1]	HCSL
V_{CM}	V_{CC}-1.4V	1.2V	V_{CC}-0.2V	350 mV
V_{SWING_SE}	800 mV	325 mV	400 mV	700 mV
V_{OH}	V_{CC}-1V	1.3625V	V_{CC}	700 mV
V_{OL}	V_{CC}-1.8V	1.0375V	V_{CC}-0.400V	0V
Reference	V_{CC}	Ground	V_{CC}	Ground

Note 1: Terminated 50Ω to V_{CC}.

INPUT/OUTPUT STRUCTURE OF EACH DIFFERENTIAL CLOCK LOGIC

Prior to designing the logic translation circuit, an examination of the input/output structures of each logic type — LVPECL, HCSL, CML, and LVDS — is required as each logic type features a different common-mode voltage and swing level.

Low-Voltage, Positive-Reference, Emitter-Coupled Logic (LVPECL)

Low-voltage, positive-referenced, emitter-coupled logic (LVPECL) originates from emitter-coupled logic (ECL), adopting a positive power supply.

The LVPECL input is a current-switching differential pair with high input impedance (see Figure 1). The input common-mode voltage should be approximately V_{CC} – 1.3V for the purpose of having operating headroom, either from internal self-biasing or external biasing.

The LVPECL output consists of a differential pair amplifier which drives a pair of emitter followers (or open emitters) as illustrated in Figure 1. The output emitter followers should operate in the “active” region with DC current at all times. The output pins of OUT+ and OUT– are typically connected to differential transmission lines (Z_0 = 100Ω) or a single-ended transmission line (Z_0 = 50Ω) for impedance matching. The proper termination for LVPECL output is 50Ω to V_{CC} – 2V and OUT+/OUT– will typically be V_{CC} – 1.3V, resulting in an approximate DC current flow of 14 mA.

Another way to terminate LVPECL output is to apply 142Ω to GND, which provides a DC-biasing for LVPECL output and a DC current path to GND. Because the LVPECL output common-mode is at V_{CC} – 1.3V, the DC-biasing resistor can be selected by assuming a DC current of 14 mA (R = V_{CC} – 1.3V / 14 mA), resulting in R = 142Ω (150Ω also works) for V_{CC} – 3.3V.

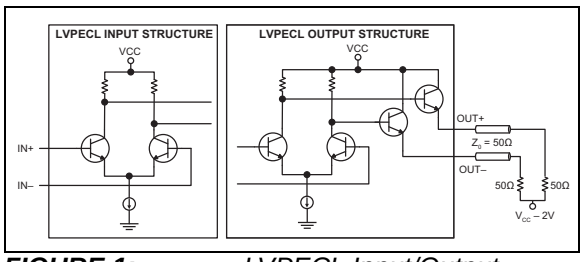

FIGURE 1: *LVPECL Input/Output Structure.*

Low-Voltage Differential Signaling (LVDS)

Low-voltage differential signaling (LVDS) input requires a 100Ω termination resistor across the pins of IN+ and IN– with a common-mode voltage of approximately 1.2V (see Figure 2). If the 100Ω termination is not included on-chip, it must be included on the printed circuit board (PCB).

The LVDS output driver consists of a 3.5 mA current source which is connected to differential outputs through a switching network. The output pins of OUT+ and OUT– are typically connecting to differential trans-

mission lines (Z_0 = 100Ω) or a single-ended transmission line (Z_0 = 50Ω) for impedance matching, which are terminated with a 100Ω resistor across the receiver inputs, resulting in 350 mV swing for LVDS logic (Figure 2).

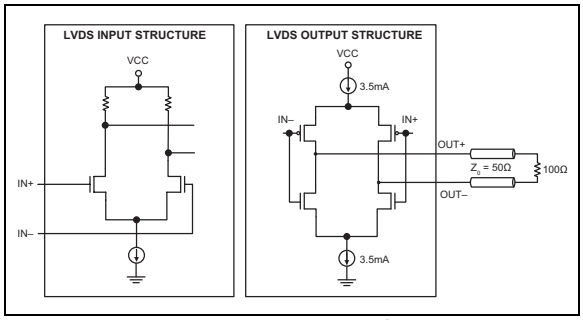

FIGURE 2: *LVDS Input/Output Structure.*

Current-Mode Logic (CML)

Most current-mode logic (CML) input structures have a 50Ω resistor to V_{CC} on-chip (see Figure 3). If not, then one must be applied to V_{DD} on both inputs of IN+ and IN– on the PCB. The input transistors are emitter followers which drive a differential-pair amplifier.

The CML output consists of a differential pair of common-emitter transistors with 50Ω collector resistors as the CML output structure illustrated in Figure 3 shows. The outputs of OUT+ and OUT– are typically connecting to differential transmission lines (Z_0 = 100Ω) or a single-ended transmission line (Z_0 = 50Ω) for impedance matching (Figure 3). The signal swing is provided by switching the current in a common-emitter differential BJT. Assuming the current source is 16 mA (typical) and the CML output is loaded with a 50Ω resistor that is pulled-up to V_{CC}, this will result in an output voltage swing from V_{CC} to V_{CC} – 0.4V with a common-mode voltage (V_{CC} – 0.2V).

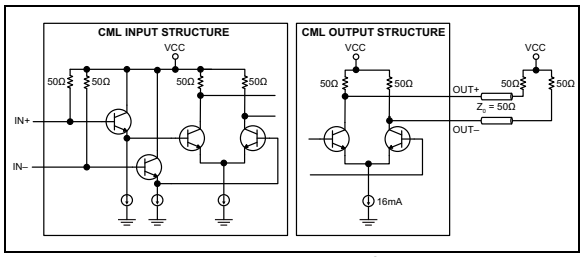

FIGURE 3: *CML Input/Output Structure.*

High-Speed Current-Steering Logic (HCSL)

The high-speed current-steering logic (HCSL) input requires the single-ended swing of 700 mV on both input pins of IN+ and IN– with a common-mode voltage of approximately 350 mV (see Figure 4).

A typical HCSL driver is a differential logic with open-source outputs, where each of the output pins switches between 0 and 14 mA. When one output pin is low (0), the other is high (driving 14 mA). The output pins of OUT+ and OUT– are typically connecting to differential transmission lines (Z_0 = 100Ω) or a single-ended transmission line (Z_0 = 50Ω), which requires an external termination resistor (50Ω to GND), resulting in a 700 mV swing level for HCSL input structures (Figure 4).

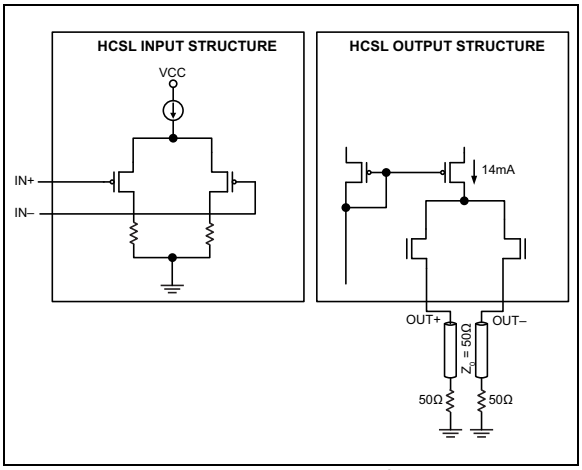

FIGURE 4: *HCSL Input/Output Structure.*

LVPECL-TO-CML TRANSLATION

As shown in Figure 5, placing a 150Ω resistor to GND at LVPECL driver output is essential for the open emitter to provide the DC-biasing as well as a DC current path to GND. In order to attenuate the 800 mV LVPECL swing to 400 mV CML swing, place a 50Ω attenuating resistor (R_A) after the 150Ω resistor to attenuate half of the LVPECL swing level. Additionally, self-biasing inside the CML receiver input must be confirmed. If the self-biasing at the input of CML is not present, a 50Ω termination resistor to V_{CC} must be placed on the PCB for CML biasing and transmission line termination.

Microchip's ultra-low-jitter crystal oscillators and clock generators (i.e., MX55, MX57, SM802xxx, SM803xxx, MX85xxx) can provide <0.3 ps RMS phase jitter with any type of output logics, except CML logic. With the below translation circuit, it is easy to achieve CML output from LVPECL logic.

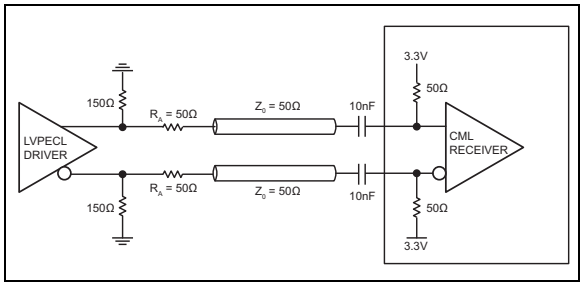

FIGURE 5: *LVPECL-to-CML Translation.*

LVPECL-TO-LVDS TRANSLATION

Placing a 150Ω resistor to GND at LVPECL driver output is essential for the open emitter to provide the DC-biasing as well as a DC current path to GND (Figure 6). In order to attenuate the 800 mV LVPECL swing to a 325 mV LVDS swing, a 70Ω attenuating resistor must be applied after the 150Ω resistor. A 10 nF AC-coupled capacitor should be placed in front of the LVDS receiver to block DC level coming from the LVPECL driver. After the AC-coupled capacitor, re-biasing is required for the LVDS input and can be done by placing 8.7 kΩ resistor to 3.3V and 5 kΩ resistor to GND to achieve 1.2V DC level for the input common-mode of LVDS receiver. If the LVDS receiver already has integrated a 100Ω resistor across the differential input pins, the external 100Ω resistor is not required.

When Microchip's LVPECL fanout buffers (i.e., SY89831) have been qualified and adopted by customers—but some of the outputs require LVDS logics for the following receivers—this LVPECL-to-LVDS translation circuit is very helpful to achieve the target.

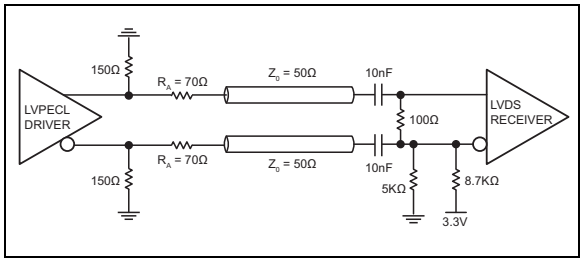

FIGURE 6: *LVPECL-to-LVDS Translation.*

LVPECL-TO-HCSL TRANSLATION

As shown in Figure 7, placing a 150Ω resistor to GND at LVPECL driver output is essential for the open emitter to provide the DC-biasing as well as a DC current path to GND. In order to attenuate an 800 mV LVPECL swing to a 700 mV HCSL swing, an attenuating resistor (R_A = 8Ω) must be placed after the 150Ω resistor. A 10 nF AC-coupled capacitor should be placed in front of the HCSL receiver to block DC level coming from the LVPECL driver. After the AC-coupled capacitor is placed, re-biasing is required for the HCSL input and can be done by placing 470Ω resistor to 3.3V and 56Ω resistor to GND to achieve 350 mV DC level for the input common-mode of HCSL receiver.

When Microchip's LVPECL fanout buffers (i.e., SY89831) have been qualified and adopted by customers—but some of the outputs require HCSL logics for the following receivers—this LVPECL-to-HCSL translation circuit is very helpful to achieve the target.

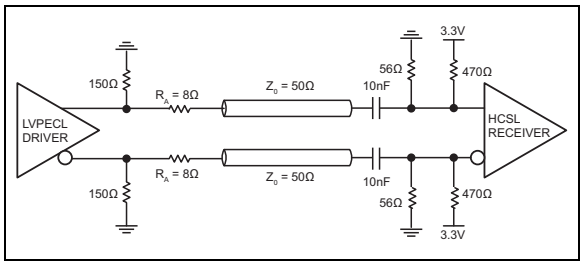

FIGURE 7: *LVPECL-to-HCSL Translation.*

HCSL-TO-LVDS TRANSLATION

In Figure 8, each of HCSL output pins switches between 0 and 14 mA. When one output pin is low (0), the other is high (driving 14 mA). The equivalent loading for HCSL driver is 48Ω parallel to 50Ω, which equates 23.11Ω. The swing level on the LVDS input is 14 mA × 23.11Ω = 323 mV. A 10 nF AC-coupled capacitor should be placed in front of the LVDS receiver to block DC level coming from the HCSL driver. After the AC-coupled capacitor is placed, re-biasing is required for the LVDS input and can be done by placing 8.7 kΩ resistor to 3.3V and 5 kΩ resistor to GND to achieve 1.2V DC level for the input common-mode of LVDS Receiver. If the LVDS receiver already has integrated a 100Ω resistor across the differential input pins, the external 100Ω resistor is not required.

When Microchip's HCSL fanout buffers (i.e., SY75576L, SY75578L) have been qualified and adopted by customers—but some of the outputs require LVDS logics for the following receivers—this HCSL-to-LVDS translation circuit is very helpful to achieve the target.

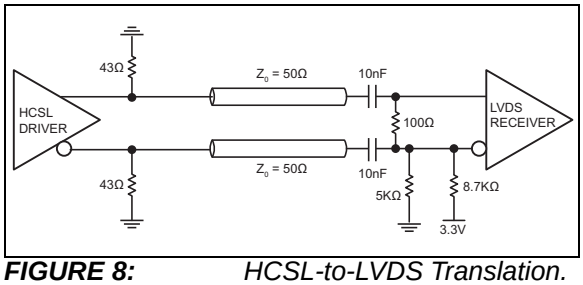

FIGURE 8: *HCSL-to-LVDS Translation.*

HCSL-TO-CML TRANSLATION

In Figure 9, each of HCSL output pins switches between 0 and 14 mA. When one output pin is low (0), the other is high (driving 14 mA). The equivalent loading for HCSL driver is 68Ω parallel to 50Ω, which equates 28.81Ω. The swing level on the CML input is 14 mA × 28.81Ω = 403 mV. A 10 nF AC-coupled capacitor should be placed in front of the CML receiver to block DC level coming from the HCSL driver. Additionally, self-biasing inside the CML receiver input must be confirmed. If the self-biasing at the input of CML is not present, a 50Ω termination resistor to V_{CC} must be placed on the PCB for CML biasing and transmission line termination.

Microchip's ultra-low-jitter crystal oscillators and clock generators (i.e., MX55, MX57, SM802xxx, SM803xxx, MX85xxx) can provide <0.3 ps RMS phase jitter with any type of output logics, except CML logic. With the translation circuit below, it is easy to achieve CML output from HCSL logic.

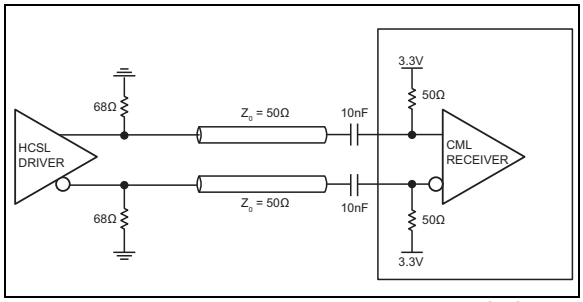

FIGURE 9: *HCSL-to-CML Translation.*

LVDS-TO-CML TRANSLATION

LVDS output drives a ±3.5 mA current through the termination of 100Ω resistor, resulting in a 350 mV swing level in front of the CML receiver (Figure 10). Confirmation that the CML receivers are capable of receiving a 350 mV swing is required because the standard swing of CML is 400 mV. Additionally, self-biasing inside the CML receiver input must also be confirmed. If the self-biasing at the input of CML is not present, a 50Ω termination resistor to V_{CC} must be placed on the PCB for CML biasing and transmission line termination.

Microchip's ultra-low-jitter crystal oscillators and clock generators (i.e., MX55, MX57, SM802xxx, SM803xxx, MX85xxx) can provide <0.3 ps RMS phase jitter with any type of output logics, except CML logic. With the below translation circuit, it is easy to achieve CML output from LVDS logic.

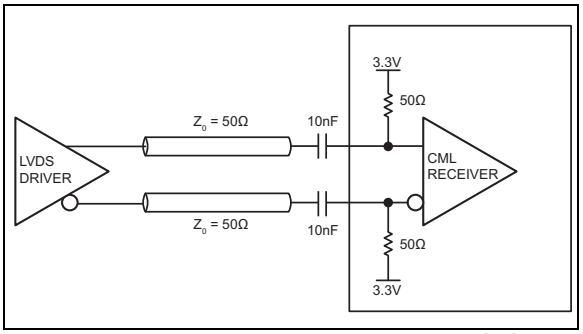

FIGURE 10: *LVDS-to-CML Translation.*

SUMMARY

This application note presents how to translate different clock logics. With the proper signal level attenuation and self-biasing circuit in front of the receiver side, a translation circuit can be easily achieved with fewer external components.

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