Silicon Errata and Data Sheet Clarifications

ATmega48A/PA/88A/PA/168A/PA/328/P

Introduction

The ATmega48A/PA/88A/PA/168A/PA/328/P devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002061), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATmega48A/PA/88A/PA/168A/PA/328/P devices.

Note:

- This document summarizes all the silicon errata issues from all silicon revisions, previous and current

1. Silicon Issue Summary

Legend

-	Erratum is not applicable.
X	Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision								
		ATmega48A/PA		ATmega88A/PA		ATmega168A/PA		ATmega328/P		
		Rev. D (1)	Rev. E	Rev. F (1)	Rev. G	Rev. E (1)	Rev. L	Rev. A	Rev. B	Rev. D
System Clock and Clock Options	2.2.1. Unstable 32 kHz Oscillator	-	-	-	-	-	-	X	X	-
TWI	2.3.1. TWI Data Setup Time Can Be Too Short	X	X	X	X	X	X	-	-	X
Analog Comparator	2.4.1. Analog MUX Can Be Turned Off When Setting the ACME Bit	X	X	X	X	X	X	X	X	X

Note:

1. This revision is the initial release of the silicon.

The following silicon revisions were never released to production:

- ATmega168A/PA
  - Rev. F-K
- ATmega328/P
  - Rev. C

2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 System Clock and Clock Options

2.2.1 Unstable 32 kHz Oscillator

The 32 kHz oscillator does not work as a system clock and if it used as an asynchronous timer, it is inaccurate.

Work around

None.

Affected Silicon Revisions

ATmega48A/PA	
Rev. D	Rev. E
-	-

ATmega88A/PA	
Rev. F	Rev. G
-	-

ATmega168A/PA	
Rev. E	Rev. L
-	-

ATmega328/P		
Rev. A	Rev. B	Rev. D
X	X	-

2.3 TWI - Two-Wire Interface

2.3.1 TWI Data Setup Time Can Be Too Short

When running the device as a TWI slave with a system clock above 2 MHz, the data setup time for the first bit after ACK may, in some cases, be too short. This may cause a false start or stop condition on the TWI line.

Work around

Insert a delay between setting TWDR and TWCR.

Affected Silicon Revisions

ATmega48A/PA	
Rev. D	Rev. E
X	X

ATmega88A/PA	
Rev. F	Rev. G
X	X

ATmega168A/PA	
Rev. E	Rev. L

.....continued

ATmega168A/PA	
X	X

ATmega328/P		
Rev. A	Rev. B	Rev. D
-	-	X

2.4 AC - Analog Comparator

2.4.1 Analog MUX Can Be Turned Off When Setting the ACME Bit

If the ACME (Analog Comparator Multiplexer Enabled) bit in ADCSRB is set while MUX3 in ADMUX is '1' (ADMUX[3:0]=1xxx), all MUXs are turned off until the ACME bit is cleared.

Work around

Clear the MUX3 bit before setting the ACME bit.

Affected Silicon Revisions

ATmega48A/PA	
Rev. D	Rev. E
X	X

ATmega88A/PA	
Rev. F	Rev. G
X	X

ATmega168A/PA	
Rev. E	Rev. L
X	X

ATmega328/P		
Rev. A	Rev. B	Rev. D
X	X	X

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (www.microchip.com/DS40002061).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 System Clock and Clock Options for ATmega328P

3.1.1 Low-Power Crystal Oscillator

A clarification has been made to *Table 9-4 Start-Up Times for the Low-Power Crystal Oscillator Clock Selection*, where 14 CK in the column *Additional Delay from Reset (V_{CC} = 5.0V)* has been replaced by **19 CK**. Functional changes are shown in **bold**.

Table 9-4. Start-Up Times for the Low-Power Crystal Oscillator Clock Selection

Oscillator Source/Power Conditions	Start-Up Time from Power-Down and Power-Save	Additional Delay from Reset (V_{CC} = 5.0V)	CKSEL0	SUT[1:0]
Ceramic resonator, fast rising power	258 CK	**19 CK** + 4 ms(1)	0	00
Ceramic resonator, slowly rising power	258 CK	**19 CK** + 65 ms(1)	0	01
Ceramic resonator, BOD enabled	1K CK	**19 CK**(2)	0	10
Ceramic resonator, fast rising power	1K CK	**19 CK** + 4 ms(2)	0	11
Ceramic resonator, slowly rising power	1K CK	**19 CK** + 65 ms(2)	1	00
Crystal Oscillator, BOD enabled	16K CK	**19 CK**	1	01
Crystal Oscillator, fast rising power	16K CK	**19 CK** + 4 ms	1	10
Crystal Oscillator, slowly rising power	16K CK	**19 CK** + 65 ms	1	11

Notes:

1. These options should only be used when not operating close to the maximum device frequency and only if frequency stability at start-up is not important for the application. These options are not suitable for crystals.
2. These options are intended for use with ceramic resonators and will ensure frequency stability at start-up. They can also be used with crystals when not operating close to the maximum device frequency and if frequency stability at start-up is unimportant for the application.

3.1.2 Full Swing Crystal Oscillator

A clarification has been made to *Table 9-6 Start-Up Times for the Full Swing Crystal Oscillator Clock Selection*, where 14 CK in the column *Additional Delay from Reset (V_{CC} = 5.0V)* has been replaced by **19 CK**. Functional changes are shown in **bold**.

Table 9-6. Start-Up Times for the Full Swing Crystal Oscillator Clock Selection

Oscillator Source/Power Conditions	Start-Up Time from Power-Down and Power-Save	Additional Delay from Reset (V_{CC} = 5.0V)	CKSEL0	SUT[1:0]
Ceramic resonator, fast rising power	258 CK	**19 CK** + 4.1 ms(1)	0	00
Ceramic resonator, slowly rising power	258 CK	**19 CK** + 65 ms(1)	0	01
Ceramic resonator, BOD enabled	1K CK	**19 CK**(2)	0	10
Ceramic resonator, fast rising power	1K CK	**19 CK** + 4.1 ms(2)	0	11
Ceramic resonator, slowly rising power	1K CK	**19 CK** + 65 ms(2)	1	00
Crystal Oscillator, BOD enabled	16K CK	**19 CK**	1	01

.....continued				
Oscillator Source/Power Conditions	Start-Up Time from Power-Down and Power-Save	Additional Delay from Reset (V_{CC} = 5.0V)	CKSEL0	SUT[1:0]
Crystal Oscillator, fast rising power	16K CK	**19 CK** + 4.1 ms	1	10
Crystal Oscillator, slowly rising power	16K CK	**19 CK** + 65 ms	1	11

Notes:

1. These options should only be used when not operating close to the maximum device frequency and only if frequency stability at start-up is not important for the application. These options are not suitable for crystals.
2. These options are intended for use with ceramic resonators and will ensure frequency stability at start-up. They can also be used with crystals when not operating close to the maximum device frequency and if frequency stability at start-up is unimportant for the application.

3.1.3 Low-Frequency Crystal Oscillator

A clarification has been made to *Table 9-9 Start-Up Times for the Low-Frequency Crystal Oscillator Clock Selection - SUT Fuses*, where 14 CK in the column *Additional Delay from Reset (V_{CC} = 5.0V)* has been replaced by **19 CK**. Functional changes are shown in **bold**.

Table 9-9. Start-Up Times for the Low-Frequency Crystal Oscillator Clock Selection - SUT Fuses

SUT[1:0]	Additional Delay from Reset (V_{CC} = 5.0V)	Recommended Usage
00	**19 CK**	Fast rising power or BOD enabled
01	**19 CK** + 4.1 ms	Slowly rising power
10	**19 CK** + 65 ms	Stable frequency at start-up
11	Reserved	

3.1.4 Calibrated Internal RC Oscillator

A clarification has been made to *Table 9-12 Start-Up Times for the Calibrated Internal RC Oscillator Clock Selection - SUT*, where 14 CK in the column *Additional Delay from Reset (V_{CC} = 5.0V)* has been replaced by **19 CK**. Functional changes are shown in **bold**.

Table 9-12. Start-Up Times for the Calibrated Internal RC Oscillator Clock Selection - SUT

Power Conditions	Start-Up Time from Power-Down and Power-Save	Additional Delay from Reset (V_{CC} = 5.0V)	SUT[1:0]
BOD enabled	6 CK	**19 CK**(1)	00
Fast rising power	6 CK	**19 CK** + 4 ms	01
Slow rising power	6 CK	**19 CK** + 65 ms(2)	10
Reserved			11

Notes:

1. If the RSTDISBL fuse is programmed, this start-up time will be increased to **19 CK** + 4 ms to ensure the programming mode can be entered.
2. The device is shipped with this option selected.

3.1.5 128 kHz Internal Oscillator

A clarification has been made to *Table 9-14 Start-Up Times for the 128 kHz Internal Oscillator*, where 14 CK in the column *Additional Delay from Reset (V_{CC} = 5.0V)* has been replaced by **19 CK**. Functional changes are shown in **bold**.

Table 9-14. Start-Up Times for the 128 kHz Internal Oscillator

Power Conditions	Start-Up Time from Power-Down and Power-Save	Additional Delay from Reset	SUT[1:0]
BOD enabled	6CK	**19 CK**(1)	00
Fast rising power	6CK	**19 CK** + 4 ms	01
Slowly rising power	6CK	**19 CK** + 65 ms	10
Reserved			11

Note:

1. If the RSTDISBL fuse is programmed, this start-up time will be increased to **19 CK** + 4 ms to ensure the programming mode can be entered.

3.1.6 External Clock

A clarification has been made to *Table 9-16 Start-Up Times for the External Clock Selection*, where 14 CK in the column *Additional Delay from Reset (V_{CC} = 5.0V)* has been replaced by **19 CK**. Functional changes are shown in **bold**.

Table 9-16. Start-Up Times for the External Clock Selection

Power Conditions	Start-Up Time from Power-Down and Power-Save	Additional Delay from Reset (V_{CC} = 5.0V)	SUT[1:0]
BOD enabled	6 CK	**19 CK**(1)	00
Fast rising power	6 CK	**19 CK** + 4.1 ms	01
Slow rising power	6 CK	**19 CK** + 65 ms(2)	10
Reserved			11

Notes:

1. If the RSTDISBL fuse is programmed, this start-up time will be increased to **19 CK** + 4 ms to ensure the programming mode can be entered.
2. The device is shipped with this option selected.

3.2 Ordering Information

A clarification has been made to tables titled 'Package Type' for all devices documented in the data sheet:

- A note to the 32M1-A row was added informing that the package type can be delivered in two different styles

Package Type	
32A	32-lead, (1.0 mm) Plastic Thin Quad Flat Package (TQFP)
28M1	28-pad, 4 x 4 x 1.0 body, Lead Pitch 0.45 mm Very Thin Plastic Quad Flat No-Lead (VQFN)
32M1-A(1)	32-pad, 5 x 5 x 1.0 body, Lead Pitch 0.50 mm Thin Plastic Quad Flat No-Lead (VQFN)
28P3	28-lead, 0.300" Wide, Skinny Plastic Dual Inline Package (SPDIP)

1. **This package type can be delivered with two different styles with reference numbers 'C04-21400' (punched) and 'C04-21395' (sawn) as shown in section 3.2.1 - 32M1-A. For PCB layouts, it is recommended to take both *recommended land patterns* into consideration.**

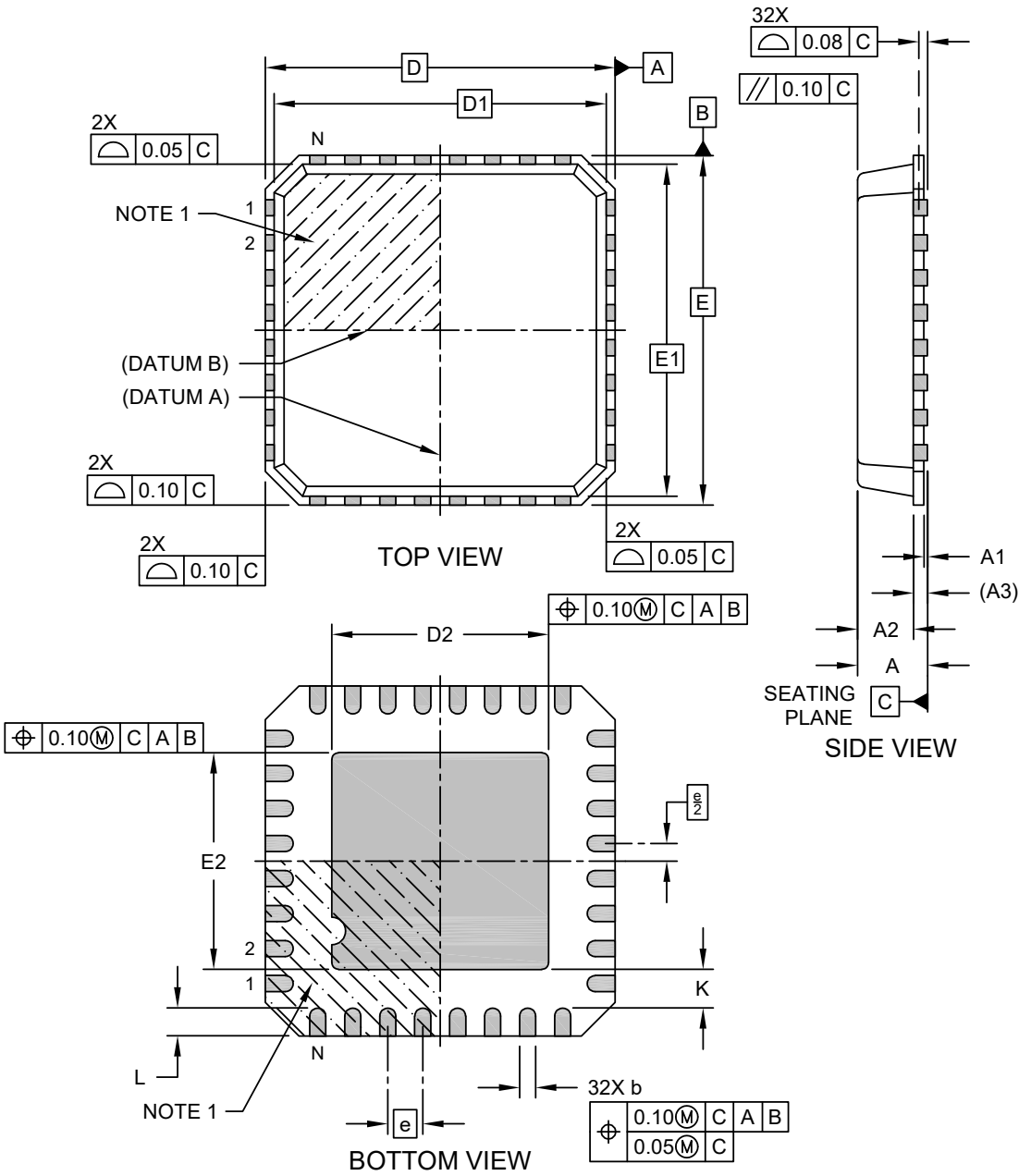
3.3 Package Information

A clarification about the other package style available for package type 32M1-A has been added to the 32M1-A section.

3.3.1 32M1-A

32-Lead Thin Plastic Quad Flat, No Lead Package (S4B) - 5x5 mm Body [VQFN] Punch Singulated; 3.10x3.10 mm Exposed Pad

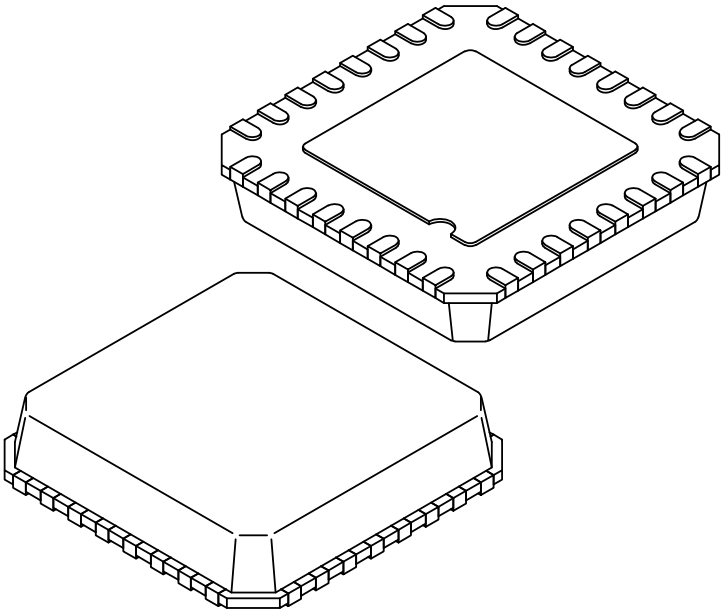
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21400 Rev B Sheet 1 of 2

32-Lead Thin Plastic Quad Flat, No Lead Package (S4B) - 5x5 mm Body [VQFN] Punch Singulated; 3.10x3.10 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		32	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	1.00
Standoff	A1	0.00	0.02	0.05
Mold Cap Thickness	A2	-	0.65	0.70
Terminal Thickness	A3		0.20 REF	
Overall Length	D		5.00 BSC	
Mold Cap Length	D1		4.75 BSC	
Exposed Pad Length	D2	2.95	3.10	3.25
Overall Width	E		5.00 BSC	
Mold Cap Width	E1		4.75 BSC	
Exposed Pad Width	E2	2.95	3.10	3.25
Terminal Width	b	0.18	0.23	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

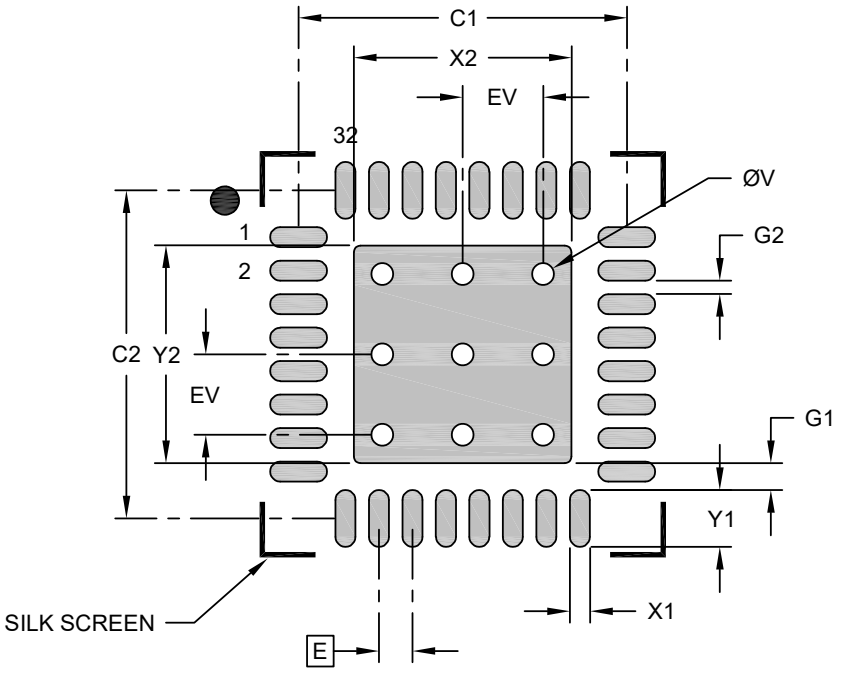
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is punch singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21400 Rev B Sheet 2 of 2

32-Lead Thin Plastic Quad Flat, No Lead Package (S4B) - 5x5 mm Body [VQFN] Punch Singulated; 3.10x3.10 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			3.25
Optional Center Pad Length	Y2			3.25
Contact Pad Spacing	C1		4.90	
Contact Pad Spacing	C2		4.90	
Contact Pad Width (X32)	X1			0.30
Contact Pad Length (X32)	Y1			0.85
Contact Pad to Center Pad (X32)	G1	0.40		
Contact Pad to Contact Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

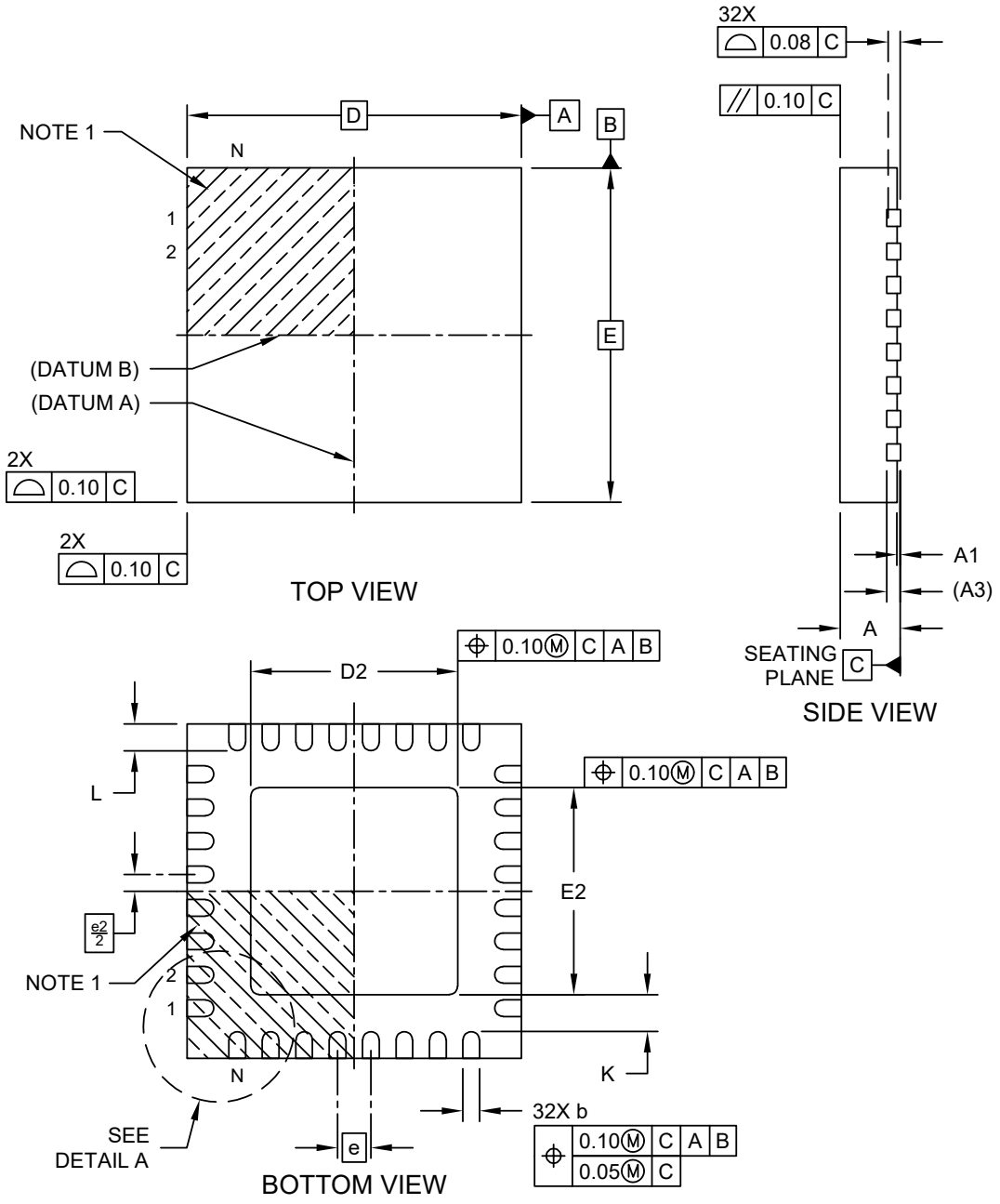
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23400 Rev B

32-Lead Very Thin Plastic Quad Flat, No Lead Package (UBB) - 5x5x0.9 mm Body [VQFN] With 3.1x3.1 mm Exposed Pad; Atmel Legacy Global Package Code ZMF

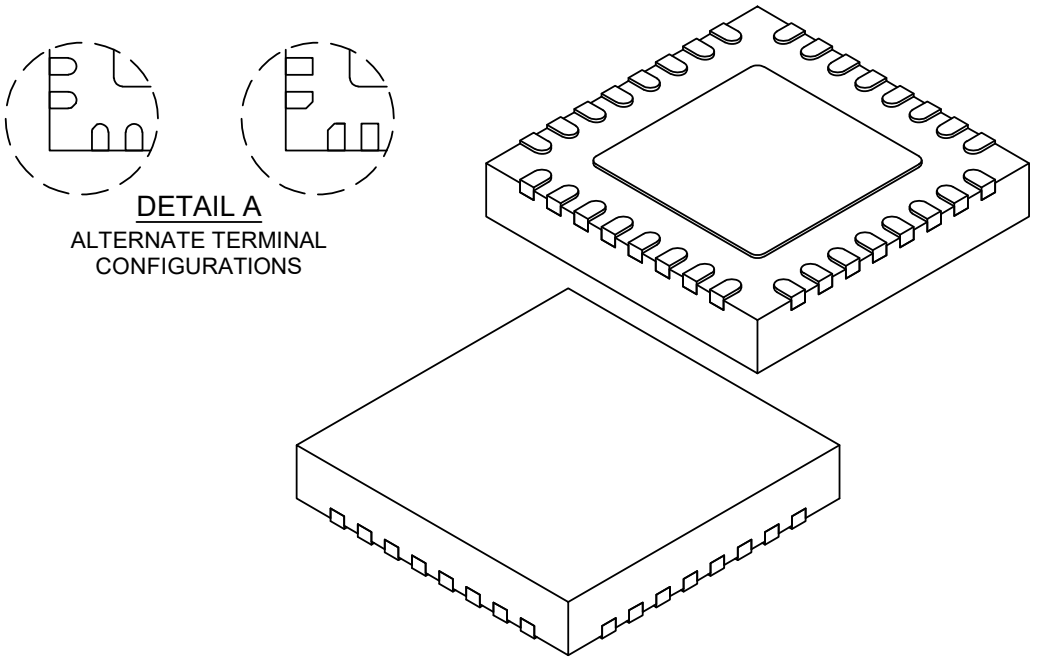
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21395-UBB Rev C Sheet 1 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (UBB) - 5x5x0.9 mm Body [VQFN] With 3.1x3.1 mm Exposed Pad; Atmel Legacy Global Package Code ZMF

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		32	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.00	3.10	3.20
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.00	3.10	3.20
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

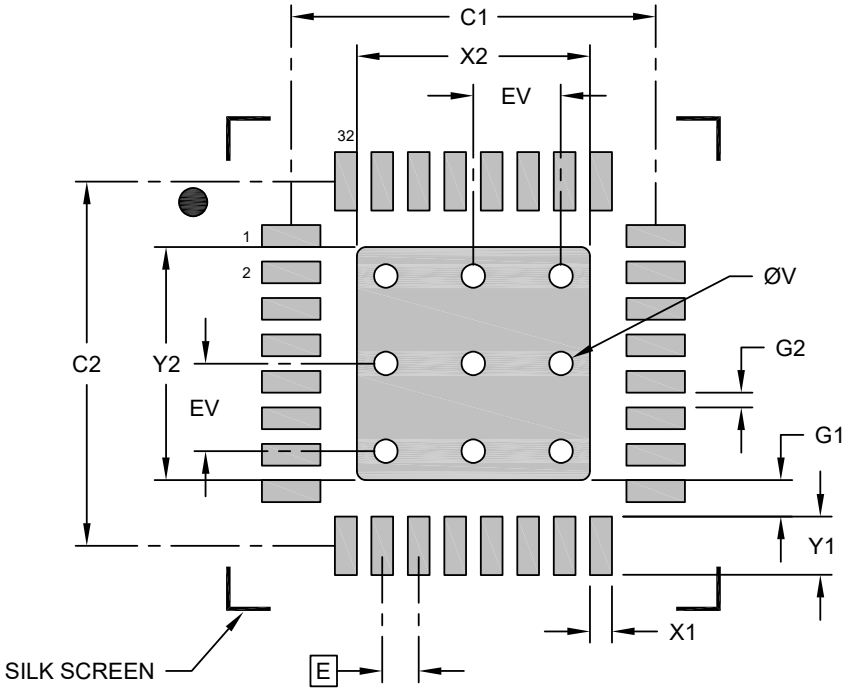
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21395-UBB Rev C Sheet 2 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (UBB) - 5x5x0.9 mm Body [VQFN] With 3.1x3.1 mm Exposed Pad; Atmel Legacy Global Package Code ZMF

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Center Pad Width	X2			3.20
Center Pad Length	Y2			3.20
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X32)	X1			0.30
Contact Pad Length (X32)	Y1			0.80
Contact Pad to Center Pad (X32)	G1	0.20		
Contact Pad to Contact Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23395-UBB Rev C

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc Rev.	Date	Comments
C	04/2024	• Document: – Editorial updates • Added new data sheet clarifications: – System Clock and Clock Options: • 3.1.1. Low-Power Crystal Oscillator • 3.1.2. Full Swing Crystal Oscillator • 3.1.3. Low-Frequency Crystal Oscillator • 3.1.4. Calibrated Internal RC Oscillator • 3.1.5. 128 kHz Internal Oscillator • 3.1.6. External Clock
B	11/2021	Added data sheet clarifications: • Ordering Information • Package Information
A	09/2020	Initial document release. • Content moved from the data sheet and restructured to the new document template • Updated the die revision list to reflect die revisions in production

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