Servicing Peripheral Interrupts While Writing Flash

TB3344

Introduction

Author: Henrik M. Arnesen, Egil Rotevatn, Microchip Technology Inc.

The Microchip AVR® EA Family of microcontrollers features Flash memory where the Flash is divided into one Read While Write (RWW) section and one Non Read While Write (NRWW) section, enabling the CPU to continue running instructions from the NRWW section while erasing or writing to the RWW section. Since the erase/write operations to Flash is timed in the order of milliseconds, the RWW functionality enables the user to utilize this time and not having to wait for it to finish. The purpose of this document is to describe how to use the NRWW Flash section to write to the RWW Flash section on AVR EA devices and why this is beneficial.

This technical brief explains the concept of RWW/NRWW and its implementation on the AVR EA Family of microcontrollers with the following use case:

Servicing Peripheral Interrupts While Writing Flash

- This example showcases the benefits of being able to write to RWW from NRWW Flash memory
- Different device pins are continuously toggled to show important events in the Erase/Write cycle
- The pins represent periodic interrupts, page buffer status, and Flash statuses
- The events have different occurrences when erasing and writing a program page in either NRWW or RWW areas

Note: For the use case described in this document, two code examples are set up, one made using Microchip Code Configurator (MCC) in MPLAB® and one bare metal example developed using Microchip Studio on AVR® EA. Both can be found on Microchip Discover:

- Example code for Microchip Studio
- Example code for MPLAB X

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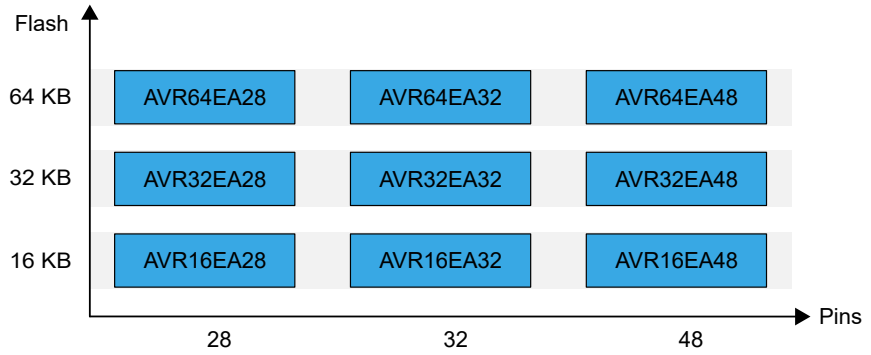
1. Relevant Devices

This section lists the relevant devices for this document. The following figures show the different family devices, laying out pin count variants and memory sizes:

- Vertical migration upwards is possible without code modification, as these devices are pin-compatible and provide the same or more features
- Horizontal migration to the left reduces the pin count and, therefore, the available features
- Devices with different Flash memory sizes typically also have different SRAM and EEPROM

Figure 1-1. AVR® EA Family Overview



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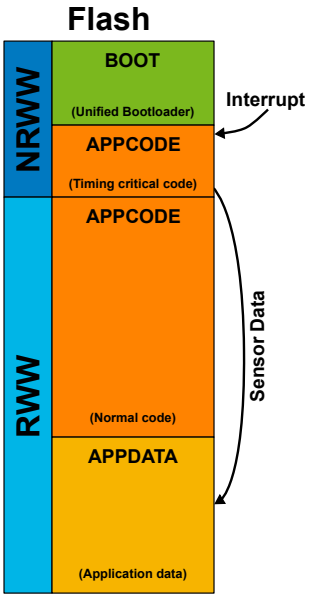
2. Overview

Flash memory is organized into pages consisting of several words. In general for AVR, a word is 2 bytes or 16 bits. For the AVR EA, the page size is 128 bytes. Independent of page size, the Flash is split into two physical sections: Non Read-While-Write (NRWW) and Read-While-Write (NRWW). The NRWW section starts at the start of the Flash and, by that, overlaps the BOOT section and the APPCODE/APPDATA section, depending on the fuse settings. It's important to note that writing to the same section as the code is running from is impossible. In the example where the NRWW overlaps the boundary between the BOOT/APPCODE or BOOT/APPDATA sections, the uninterrupted code needs to be placed in the BOOT section to run while an erase/write cycle is underway in APPCODE/APPDATA. If configuring to have BOOT/APPCODE/APPDATA, the uninterrupted code can also be in the NRWW part of the APPCODE section to program APPDATA without halting the CPU.

Figure 2-1. RWW Memory Flow



The syntax "RWW section" refers to which section is being programmed (erased or written) and not the one read. Only code located inside the NRWW Flash is accessible by either executing a CPU instruction or reading data while programming the RWW section.

It follows that the main differences between the NRWW and RWW sections are:

1. When erasing or writing to a page located inside the RWW section using code running from the NRWW section, code and data can continue to be run and read from the NRWW section, enabling the continuous operation of the CPU while the program memory operation is running.
2. When erasing or writing to a page in the NRWW section, the CPU is halted during the operation. An exception to this is when writing from the BOOT section to the APPCODE or APPDATA section that overlaps with the NRWW section.

An application, leveraging the NRWW/RWW program memory split of AVR EA, prevents the CPU from blocking while the program memory is written to.

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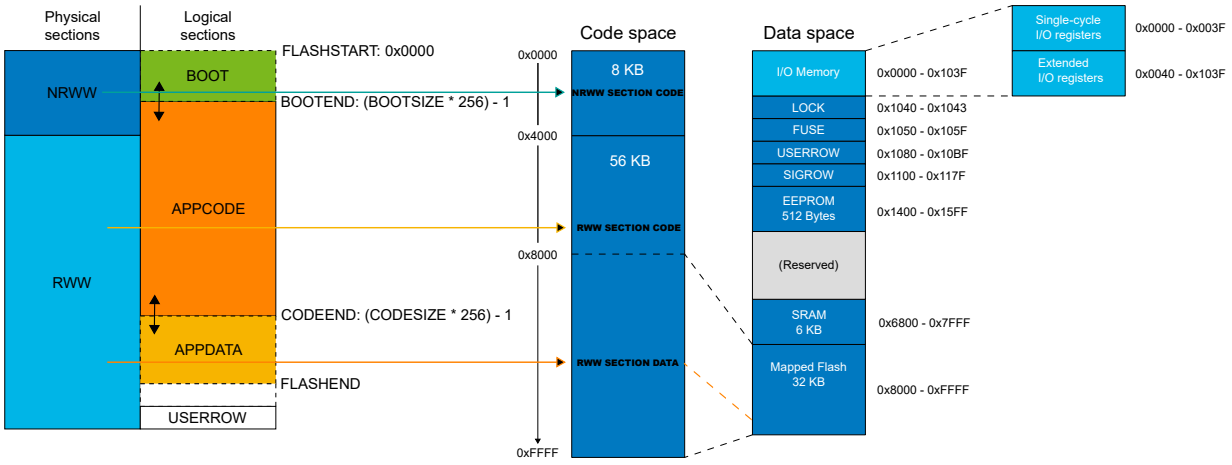
- One example is a Bootloader scenario where the CPU acts upon commands received via a communication peripheral (I^2C/USART) from the Host while simultaneously programming the APPCODE/APPDATA sections in program memory
- Another use case is a data logging scenario in which an analog peripheral interrupts CPU operation when data that at once must to be saved to program memory, becomes available

Both scenarios highlight the need for the CPU not to be blocked while the Nonvolatile Memory Controller (NVMCTRL) peripheral is erasing/writing to the program memory. By ensuring that the code that needs to run while an erase/write cycle is in progress is in the NRWW section, we can ensure that commands or interrupts are handled as they arrive and not after the Flash erase/write cycle.

To understand how to implement the Read-While-Write (RWW) feature on AVR EA, it helps to look at the program memory from a Physical, Logical, and Code/Data Space point of view. Physically, the program memory is designed with fixed NRWW and RWW sections. These are non-changeable and depend on the part number - see the "Memory Overview" section in the data sheet. Store the code and data in the respective physical sections to use the RWW use case.

The Logical sections are BOOT, APPCODE and APPDATA. These sections can be adjusted through the BOOTSIZE and CODESIZE fuses, as shown in the image below. Note - depending on the fuse configuration, the physical NRWW section can be used for both BOOT and APPCODE/APPDATA. See the data sheet in the NVMCTRL peripheral *Memory Organization* section for a detailed explanation. Note that you can access the code space via the data space through the Flash mapping feature, available on devices with a program memory exceeding 32kB. See the data sheet in the NVMCTRL peripheral *Memory Access* section for a detailed explanation.

Figure 2-2. AVR64EA48 Flash Sections



To implement this allocation, linker-named attributes with assigned addresses are given as linker options, and the named attributes are used when declaring both functions and data.

The RWW_DATA_SECTION attribute is used for data stored by the page write. These data can be written from either *BOOT* or *APPCODE* sections. The code snippet below shows the placement of an array in the APPDATA section. Define the .rww_data address in the Linker settings before compiling.

```
// the .rww_data section is at address 0x2000 (word address 0x1000)
#define RWW_DATA_SECTION __attribute__((used, section(".rww_data")))

const RWW_DATA_SECTION uint8_t rww_array[DATA_SIZE] = {0};
```

Use the NRWW_PROG_SECTION attribute for routines that **can be** executed in conjunction with Flash programming or erase (e.g., interrupts, app code Flash page write or erase, and boot loader

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host communication driver). In the code snippet below, a function called FillBuffer is placed in the NRWW section so that it can be called by interrupts running while writing to the Flash. Once again, the Linker settings must define the .nrww_program address.

```
// the .nrww_program section is at address 0x0400 (word address 0x0200)
#define NRWW_PROG_SECTION __attribute__((section(".nrww_program")))

void NRWW_SECTION_CODE FillBuffer(void);
```

Use the RWW_PROG_SECTION attribute for routines that **will not** execute during Flash programming or erase. These are blocking and must be placed in the physical RWW section. Examples of these are the setup routines.

Below is an example of the use of attribute sections.

If using a bootloader in the project, the bootloader code is placed first, from the Flash start (0x0000) until the BOOTEND (BOOTSIZE *256 -1). The BOOTSIZE fuse settings determine the BOOT section size. The Application code (App code) is placed after the BOOT (as long as CODESIZE > BOOTSIZE), which means that the application code may reside both in NRWW and RWW, making it possible to move functions into the NRWW section. Functions or interrupts placed in the NRWW section can run while erasing/writing the RWW section. However, take steps to ensure there are no interrupts or jumps to code located inside the RWW while operation on the RWW is ongoing, leading to the software ending up in an unknown state.

Table 2-1. Read-While-Write Scenarios

Flash Section Erased/Written	Flash Section Accessed	CPU
NRWW section	NRWW section	Halted
RWW section	NRWW section	Running
NRWW section	RWW section	Halted
RWW section	RWW section	Halted

Find the Flash memory size and the NRWW/RWW sections in the AVR EA's data sheet.

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3. Servicing Peripheral Interrupts While Writing Flash

This example shows the advantage of writing to the RWW Flash section from the NRWW Flash section. It is easy to get an overview of code flow and how it works with an oscilloscope or logic analyzer by using device pins for interrupt events and different memory statuses.

Testing

The program memory is divided into smaller pieces called pages. Each page is written and erased separately and consists of several bytes. The Flash has page granularity for the AVR EA, meaning it will perform an erase and/or write for every byte in the page whenever a change is necessary. In comparison, the EEPROM memory has byte granularity and can erase and write single bytes at a time.

The code works by first erasing the pages where data will be saved, filling up a buffer, and then performing a page write using the buffer values. A periodic timer interrupt continuously populate the buffer.

When the ring buffer is filled with new data >= `PROGMEM_PAGE_SIZE`, it copies the `PROGMEM_PAGE_SIZE` number of bytes from the ring buffer to the Flash page buffer and starts a Flash page write. It repeats this process a second time.

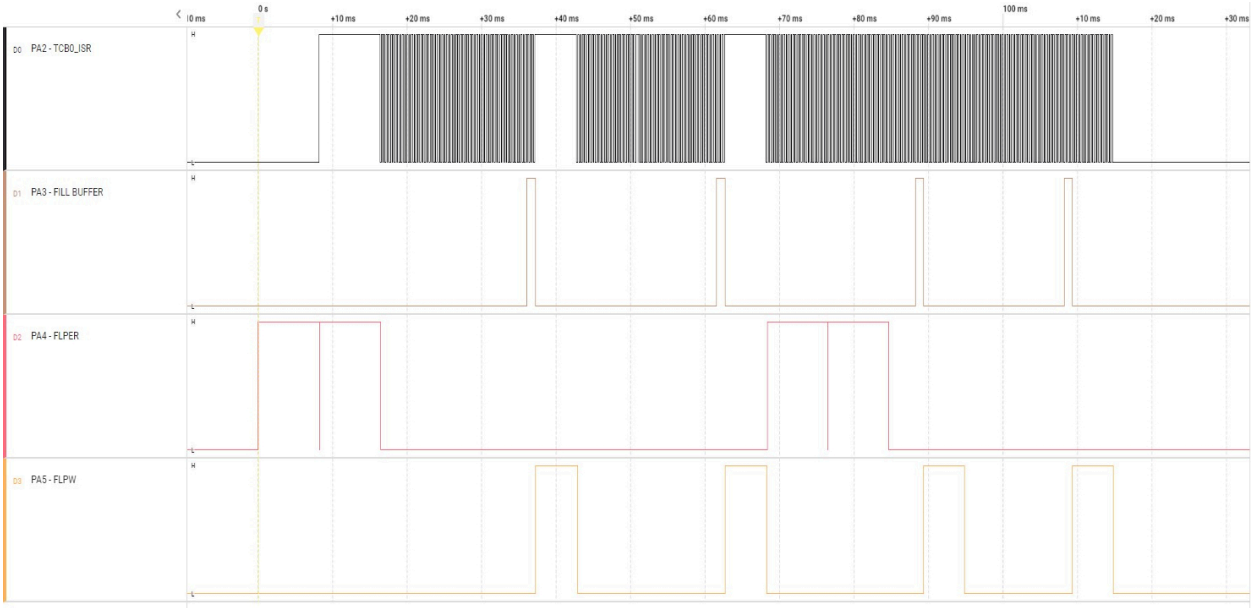
Writing to the Capture/Compare (CCMP) register in the TCB timer/counter changes the ISR period.

The code toggles some status pins, which makes it possible to scope the program flow:

- `PA2_ISR` toggles every time the TCB0 periodic interrupt ISR is handled
- `PA3_Buffer` is high when the Flash page buffer is being loaded
- `PA4_FLPER` is high while the Flash page erase is ongoing
- `PA5_FLPW` is high while the Flash page write is ongoing

As the application runs through its state machine, these pins will toggle, as seen in the image below. A more detailed description of this flow can be seen in the examples “README” file.

Figure 3-1. Pin Toggling Capture



Understanding The Code

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The linked code examples come in two flavors - an MPLAB X studio using MCC to generate drivers and a bare-metal project created in Microchip Studio. The projects have the same code flow and are divided into the following parts:

- Main file and function
- Timer 0 - Filling buffer
- Timer 1 - Switch debounce
- NVM controller

In addition to the parts above, to define the size of the BOOT and APPDATA sections set the fuses as shown below.

```
FUSES =
{
    .SYSCFG0 = FUSE_SYSCFG0_DEFAULT,
    .SYSCFG1 = FUSE_SYSCFG1_DEFAULT,

    .WDTCFG = FUSE_WDTCFG_DEFAULT,
    .BODCFG = FUSE_BODCFG_DEFAULT,
    .OSCCFG = FUSE_OSCCFG_DEFAULT,

    .BOOTSIZE = 31,     // 0x0000 -> 0x1F00 : BOOT Section
    .CODESIZE = 1,      // 0x01F00 -> FLASH_END : APPDATA Section
};
```

Most fuses are set to their default value, except BOOTSIZE, which is set to 31 blocks of 256 bytes and CODESIZE. As CODESIZE is set to 1, the program memory is logically split between the BOOT and APPDATA section.

Main file and setup

The main file of the system contains the initialization and main structure of the examples. The important things to notice are how the RWW/NRWW sections are defined and that the interrupt vector table is moved to the start of the BOOT section. Lastly, the mapped program memory points to the first section (the location of the .nrww_program, .nrww_data, and .rww_data sections). These initializations ensures that running code only exists in the program memory's NRWW section and that there exists memory addresses both in RWW and NRWW sections for data.

Timer 0

```
// TCB with capture interrupt
TCB0.INTCTRL = TCB_CAPT_bm;
TCB0.CCMP = TOP_VALUE;
TCB0.CTRLA = TCB_CLKSEL_DIV1_gc;
```

This timer is set up as a periodic interrupt that will trigger on capture when active. Note that the initialization does not enable the timer. The interrupt routine fills up the data buffer when called, as seen below.

```
// TCB0 capture interrupt
FillBuffer();
// Clear intflag
TCB0.INTFLAGS = TCB_CAPT_bm;
```

Timer 1

```
// TCB with periodic interrupt
TCB1.INTCTRL = TCB_CAPT_bm;
TCB1.CCMP = TCB1_TOP_VALUE;
TCB1.CTRLA = TCB_CLKSEL_DIV1_gc | TCB_ENABLE_bm;
```

The second timer is also set up to run periodic interrupts but is enabled all the time. The interrupt then runs the debounce function to avoid unwanted triggers.

```
// TCB1 capture interrupt
DebounceSW0();
```


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```
// Clear intflag
TCB1.INTFLAGS = TCB_CAPT_bm;
```

Erasing the Program Memory

```
NRWW_DATA_last_addr = ((((uint16_t) &nrww_array) & 0x7FFF) + MAPPED_PROGMEM_START +
DATA_SIZE);

while ((uint16_t)nrwwFlashPointer < NRWW_DATA_last_addr)
{
    _PROTECTED_WRITE_SPM(NVMCTRL.CTRLA, NVMCTRL_CMD_NOCMD_gc);

    // Perform a dummy write to this address to update the address register in NVMCTL
    *nrwwFlashPointer = 0;

    _PROTECTED_WRITE_SPM(NVMCTRL.CTRLA, NVMCTRL_CMD_FLPER_gc);

    while (NVMCTRL.STATUS & NVMCTRL_FLBUSY_bm)
    {
        ; // wait for Flash erase to complete
    }
    SCOPE_PORT.OUTCLR = SCOPE_FLPER_bm;

    nrwwFlashPointer = nrwwFlashPointer + PROGMEM_PAGE_SIZE;
}
```

The Flash erase operation for NRWW and RWW data sections is the same. It begins by setting the Flash page buffer to the area that will be erased. The FLPER pin is driven HIGH, so it's possible to see on the scope when the Flash erase operation is about to start. It sends NOCMD instructions to the NVM Controller to clear the previous NVM command to avoid a command collision error and is followed by a dummy write/store. The page erase command is sent to the NVM Controller. FLPER pin is driven LOW once the NVMCTRL.STATUS register shows that the Flash is not busy and the address of the next erase is incremented by a page size. The Flash erase operation is complete once the data section has been written to.

Writing the Program Memory

```
// Check if we have a full page to fill
if ((writeIndex - readIndex) >= PROGMEM_PAGE_SIZE)
{
    _PROTECTED_WRITE_SPM(NVMCTRL.CTRLA, NVMCTRL_CMD_NOCMD_gc);

    for (uint8_t i = 0; i < PROGMEM_PAGE_SIZE; i++)
    {
        *nrwwFlashPointer++ = buffer[readIndex++];
    }
    SCOPE_PORT.OUTCLR = SCOPE_BUFFER_bm;
    SCOPE_PORT.OUTSET = SCOPE_FLPW_bm;

    // Write the Flash page
    _PROTECTED_WRITE_SPM(NVMCTRL.CTRLA, NVMCTRL_CMD_FLPW_gc);
    while (NVMCTRL.STATUS & NVMCTRL_FLBUSY_bm)
    {
        ; // wait Flash write page operation to complete
    }
}
```

The Flash programming operation for NRWW and RWW data sections is the same. It begins by checking if enough data are available to write to a full Flash page. If not, it will wait until enough data have been generated. If yes, it sends NOCMD instructions to the NVM Controller to clear the previous NVM command to avoid a command collision error. Afterward, the BUFFER pin is driven HIGH, so it's possible to use the scope to see when the buffer load operation is about to start. Data is being read from the data buffer and stored in the Flash page buffer. When the equivalent of a complete page has been read and stored, the BUFFER pin is driven LOW. The FLPW pin is driven HIGH, and the page write command is sent to the NVM Controller. FLPW pin is driven LOW once the NVMCTRL.STATUS register shows that the Flash is not busy and the address of the next page write is incremented by a page size. The Flash write operation is complete once the data section has been written to.

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For the erase and write functions above, the code snippets are from the bare metal example and will be formatted differently for the MCC example. However, the functionality will be the same for each example.

Filling the buffer

```
void FillBuffer(void)
{
    // Fill the buffer with some data
    SCOPE_PORT.OUTTGL = SCOPE_ISR_bm;
    buffer[writeIndex++] = (data >> 2);
    data++;

    // Check if we have a buffer overflow
    if (writeIndex == readIndex)
    {
        // Overflow
        SCOPE_PORT.OUTTGL = SCOPE_OVERFLOW_bm;
    }
}
```

The FillBuffer function is triggered by the periodic interrupt on timer 0 when the timer compare counter reaches the set TOP value. The ISR pin toggles and the buffer is filled with data. OVERFLOW toggles if the buffer overflows.

SW0 Operation and Debouncing

The erase and write operation for both the NRWW and RWW data sections is started by a SW0 press. Subsequent SW0 presses will trigger the same process. The value of the last data location in the RWW data section is used as a seed for the new data. Due to this behavior, when SW0 is pressed and the program memory read, the user can observe a change in NRWW and RWW data sections. As a confirmation that SW0 has been pressed, LED0 lights up. It is necessary to trigger the whole operation of the example by a button press, as one needs to set up the external instruments (oscilloscope and/or logic analyzer) that can capture the toggling of the instrumentation pins. A simple debounce algorithm has been chosen and implemented. TCB1 is being employed for this purpose. Software debouncing the physical switch SW0 prevents the unwanted triggering of the erase and write operations. Please note that the programming Flash has a limited erase/write endurance beyond which operation is not guaranteed (consult the device's electrical characteristics for further information and details).

Moving the interrupt vector table

The vector interrupt placement depends on the Interrupt Vector Select (IVSEL) bit value in the Control A (CPUINT.CTRLA) register. If using no interrupt source, regular program code may be placed in these locations. By writing 1 to the IVSEL, the interrupt vector is placed at the start of the BOOT section of the Flash, enabling the interrupts to run as normal while an erase/write operation in the RWW section is running. As stated in the overview section, the syntax "RWW section" refers to which section is being programmed (erased or written) and not the one read. Only code located inside the NRWW Flash can be accessed by either executing a CPU instruction or reading data while the RWW section is being programmed.

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4. Get Code Examples from MPLAB Discover

MPLAB Discover bundles the available resources from multiple sources into one portal.

The MPLAB Discover webpage: MPLAB Discover

Code Examples

- Example code for Microchip Studio
- Example code for MPLAB X

You can download code examples as a `.zip` file directly from MPLAB Discover. Repositories ending with "*studio*" can be opened in Microchip Studio. Repositories ending with "*mplab-mcc*" can be opened in MPLAB X.

When the code example is hosted on GitHub, MPLAB Discover provides a link "*Open with Github*". There you can download the example code or use the `git` tool on your PC to create a local repository clone.

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5. Revision History

Document Revision	Date	Comments
A	10/2023	Initial document release

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