

NAND Flash Support on AT91SAM7SE Microcontrollers



AT91 ARM Thumb Microcontrollers

Application Note

1. Scope

The purpose of this document is to introduce NAND Flash memory technology and describe hardware and software requirements to interface NAND Flash with the Atmel® AT91SAM7SE family of ARM® Thumb®-based microcontrollers.

The AT91SAM7SE microcontroller family features an External Bus Interface (EBI) providing NAND Flash protocol support via the Static Memory Controller (SMC) and integrated logic circuitry. It also contains an Error Corrected Code Controller (ECC) which performs data error identification and single bit correction.

The associated zip file, *AN-NAND_FLASH_SAM7SE_software_example.zip*, provides code examples.

2. NAND Flash Overview

2.1 General Overview

Embedded systems have in the past widely used NOR Flash for nonvolatile memory but current designs are moving to NAND Flash to take advantage of its higher density.

NAND Flash nonvolatile memory provides low capacity (4 GB or less) storage for embedded systems such as portable and handheld devices intended for multimedia applications (pictures, audio, video, etc..). Low power consumption, pricing, memory capacity, weight, size and mechanical robustness make NAND Flash a very well suited cost effective alternative to hard drives.

2.2 Internal Array Architecture

The NAND Flash array is organized in a series of blocks which are divided in several pages. Data is stored either in byte (8 bits) or half-word (16 bits) format depending on the device type. Each page is constituted of a main storage area and a spare area (physically similar) typically used for data error identification and correction, wear levelling etc...

One particularity of NAND Flash devices is that they may contain a percentage of invalid blocks in the memory array. Before delivering the chip, these blocks are identified and marked as "Invalid Blocks" in the first or second page of each block. The existence of bad blocks does not affect the good ones because each block is independent and individually isolated from the bit lines by block select transistors.

Because NAND Flash devices have a finite lifetime (approximately 100 000 write/erase cycles), additional invalid blocks may develop while being used. Storing data requires bad-block management and data error identification and correction. Refer to [Section 3. "Invalid Block Management and Error Corrected Code \(ECC\)"](#).

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2.3 Basic Operation Principle

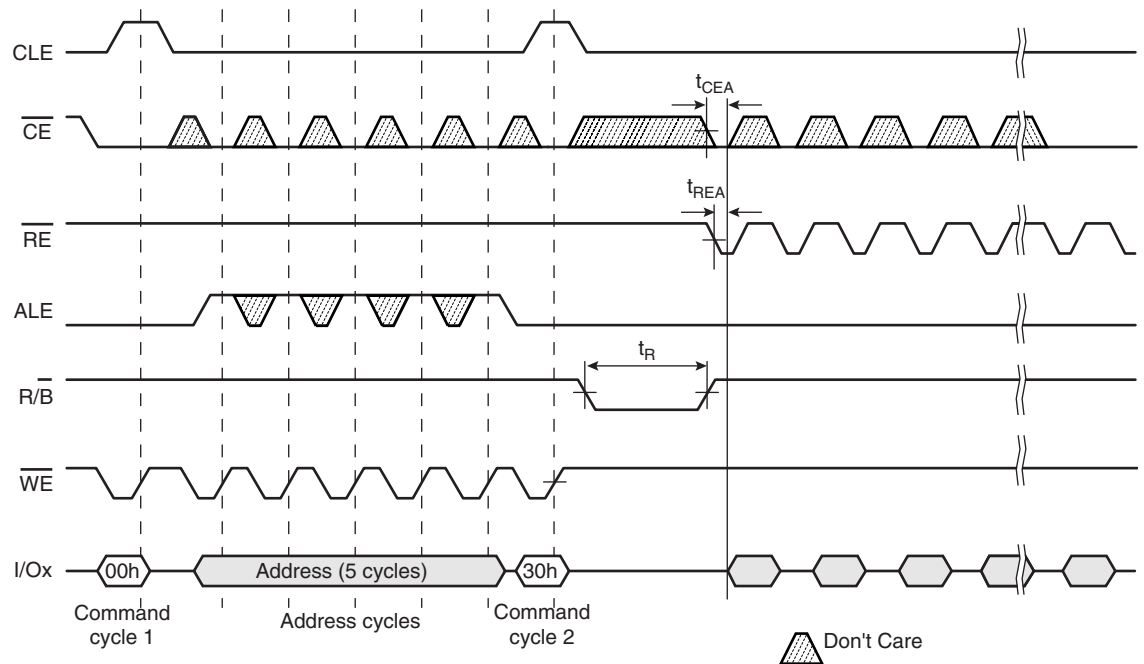
NAND Flash operations are fully controlled through a multiplexed I/O interface and additional control signals. Commands, addresses and data are transferred through the external input/output bus (8-bit or 16-bit) to the dedicated internal registers. In 16-bit devices, commands, addresses and data use the lower 8 bits (7 - 0), the upper 8 bits are only used during data-transfer cycles.

Read and program operations are performed on a per page basis whereas erase operations are performed on a block basis. To read or write from NAND Flash, a command sequence is issued to select a block and a page. After this selection, the entire page can be read or written.

The command sequence normally consists of a Command Latch Cycle, an Address Latch Cycle and a Data Cycle — either read or write.

The waveforms shown in Figure 2-1 depict the successive accesses: Command Latch, Address Latch and Data Output. Notice that no command can be sent to the NAND Flash during t_R due to its busy-state period.

Figure 2-1. Page READ Operation



Please refer to the NAND Flash manufacturer's datasheet for command sets and full operation description.

2.4 Hardware Interface

The NAND Flash hardware interface requires a maximum of 24 pins for 16-bit devices.

Table 2-1. NAND Flash Device Typical Hardware Interface

Pin Symbol	Pin Description	Pin description
$\overline{\text{CE}}$	Chip Enable	$\overline{\text{CE}}$ is active when asserted LOW to enable or select the device. $\overline{\text{CE}}$ pin must remain LOW during busy periods in order to prevent the device from entering standby mode and stopping the read operation in mid cycle. A subset of NAND Flash devices supports the $\overline{\text{CE}}$ “Don’t Care” option which allows deselecting the device without terminating the operation in progress. Other devices on the same memory bus can then be accessed while the NAND Flash is busy with internal operations.
$\overline{\text{WE}}$	Write Enable	The $\overline{\text{WE}}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{\text{WE}}$ pulse.
$\overline{\text{RE}}$	Read Enable	$\overline{\text{RE}}$ enables the output data buffers.
CLE	Command Latch Enable	When CLE is HIGH, commands are latched into the NAND Flash command register on the rising edge of the $\overline{\text{WE}}$ signal.
ALE	Address Latch Enable	When ALE is HIGH, addresses are latched into the NAND Flash address register on the rising edge of the $\overline{\text{WE}}$ signal.
I/O[7:0] or I/O[15:0]	Input/output Bus	The I/O pins are used for input commands, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled. I/O8 - I/O15 are used only in an X16 organization device. Since command input and address input are X8 operations, I/O8 - I/O15 are not used to input command and address. I/O8 - I/O15 are used only for data input and output.
$\overline{\text{WP}}$	Write Protect	The $\overline{\text{WP}}$ pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{\text{WP}}$ pin is active low.
R/ $\overline{\text{B}}$	Ready/Busy	If the NAND Flash device is busy with an ERASE, PROGRAM, or READ operation, the R/ $\overline{\text{B}}$ signal is asserted LOW. The R/ $\overline{\text{B}}$ signal is an open drain output and requires a pull-up resistor to be correctly read.
PRE	Power-on read enable (used for system boot)	The PRE pin controls auto read operations executed during power on. The power-on auto read is enabled when the PRE pin is tied to high level.

2.5 NAND Flash Design Benefits and Constraints

The main benefits of using NAND Flash are fast sequential write speed and erase time which respectively exceed 5 MB/s for a sustained write (on a page basis) and around 2 ms for a 128K block erase.

The key constraint to be taken into account is that NAND Flash devices are not suited for random accesses since it takes 25 μs for the first byte access and 0.03 μs for each following byte in the same page.

2.6 NAND Flash Device Example

The Samsung® K9F2G08U0M is a 256-Mbyte NAND Flash device arranged as 2048 blocks divided in 64 pages of 2048 bytes main area + 64 bytes spare area. This device is mounted on the AT91SAM7SE-EK evaluation kit.

The K9F2G08U0M NAND Flash device interfaced with AT91SAM7SE microcontrollers will be considered as a reference example through the rest of this document.

Figure 2-2 illustrates the memory organization of this device.

Figure 2-2. K9F2G08U0M Memory Array Organization

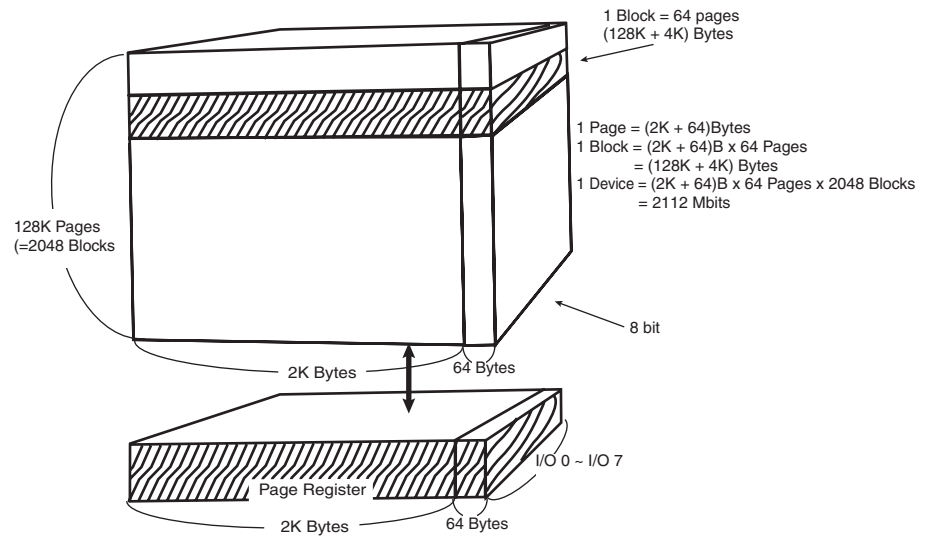
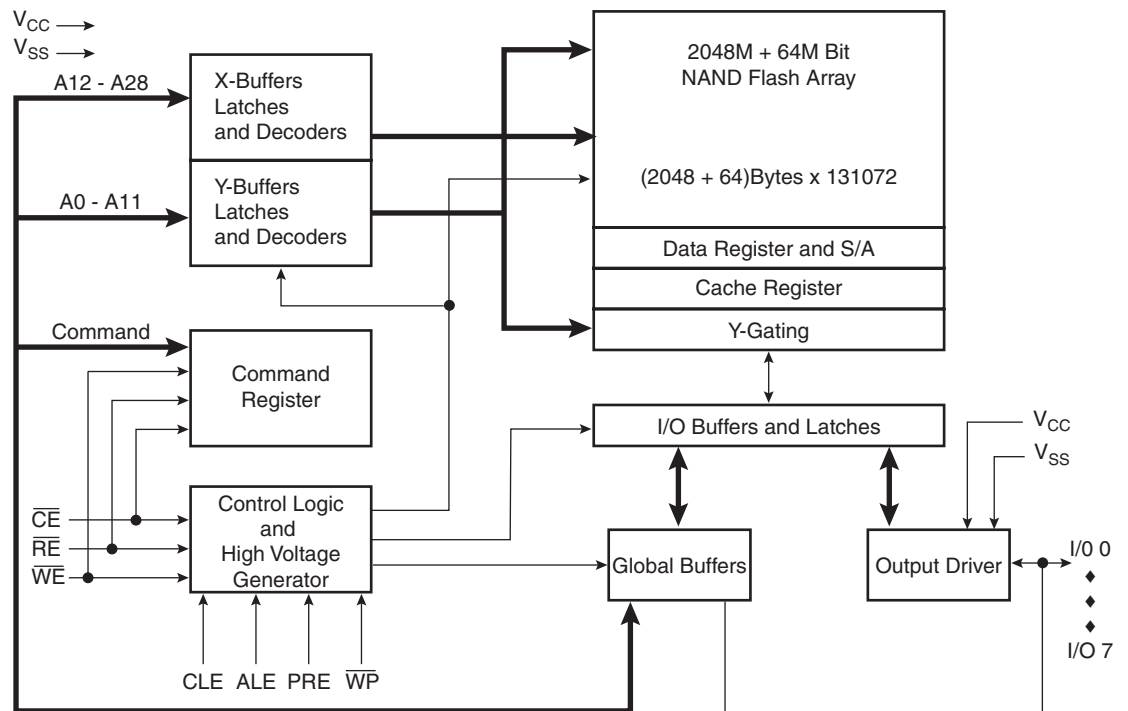


Figure 2-3 illustrates the internal architecture of the K9F2G08U0M device.

Figure 2-3. K9F2G08U0M Functional Block Diagram



Please refer to the manufacturer's datasheet for a full product description.

3. Invalid Block Management and Error Corrected Code (ECC)

3.1 Invalid Block Definition

As mentioned in [Section 2.2 on page 1](#), NAND flash devices contain a certain percentage of invalid blocks at the end of the production process. Invalid blocks are defined as blocks that contain one or more invalid bits.

3.2 Invalid Block Identification

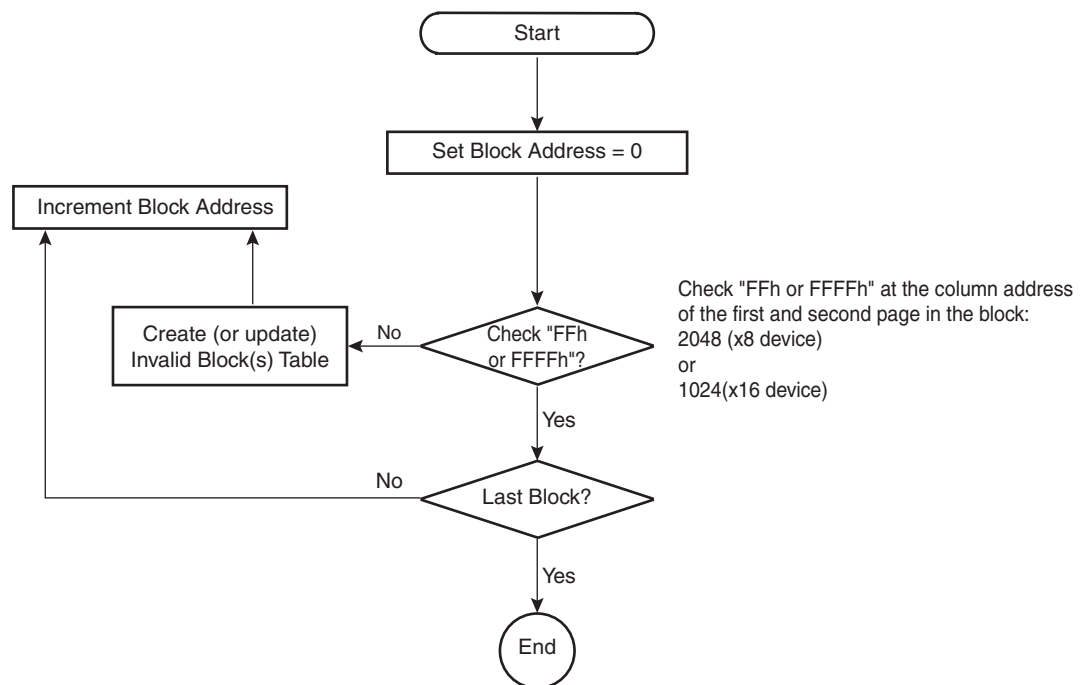
Before shipping, every NAND flash device is tested with specific test patterns under different voltage and temperature conditions in order to identify memory locations containing errors. When errors are detected, the block to which the invalid memory location belongs is marked as an "Invalid Block".

All device locations are erased (FFh for 8-bit devices, FFFFh for 16-bit devices) except locations where the invalid block information is written. The invalid block status is defined by the first byte (8-bit devices) or first half word (16-bit devices) in the spare area. Manufacturers make sure that either the first or second page of every invalid block has non-FFh (8-bit devices) or non-FFFFh (16-bit devices) data at the column address of 2048 (8-bit devices) or 1024 (16-bit devices).

Since invalid block information (located in the spare area) written by the manufacturer is not write/erase protected, it can be lost and will be almost impossible to recover. In order to prevent losing this information, it is highly recommended to proceed to a block status mapping before any write or erase operation.

The flow chart below describes how this can be done by software.

Figure 3-1. Bad Block Identification Flow Chart



Important Note: Any intentional erasure of the original invalid block information is prohibited.

3.3 Error Checking and Correction (ECC)

NAND devices are subject to data failures that occur during device operation. To ensure data read/write integrity, system error checking and correction (ECC) algorithms should be implemented. AT91SAM7SE microcontrollers provide ECC hardware support. The embedded ECC controller is capable of single bit error correction and 2-bit random detection. Please refer to the [AT91SAM7SE](#) product datasheet for a full operation description of the ECC Controller.

4. AT91SAM7SE NAND Flash Support

AT91SAM7SE microcontrollers feature an External Bus Interface (EBI) which provides external NAND Flash interface support via the Static Memory Controller (SMC) and integrated logic circuitry. Both 8-bit and 16-bit NAND flash devices can be accessed through the EBI without memory size restrictions.

The NAND Flash logic is driven by the Static Memory Controller (SMC) on the NCS3 address space. Programming the CS3A field in the EBI_CSA Register to the appropriate value enables the NAND Flash logic (Please refer to the “EBI Chip Select Assignment Register” in the [AT91SAM7SE](#) product datasheet).

Access to an external NAND Flash device is then made by accessing the address space reserved to NCS3 (i.e., between 0x40000000 and 0x4FFFFFFF). Please note that NCS3 address space does not represent the external NAND Flash address space since accesses are performed by a programming sequence. **Hence, the 256 MB (2 Gbits) allocated to NCS3 do not impose a limitation for addressing greater NAND Flash memories.**

The NAND Flash logic drives the read and write command signals of the SMC on the NANDOE and NANDWE signals when the NCS3 signal is active. NANDOE and NANDWE are invalidated as soon as the transfer address fails to lie in the NCS3 address space.

Figure 4-1. NAND Flash Signal Multiplexing on EBI Pins

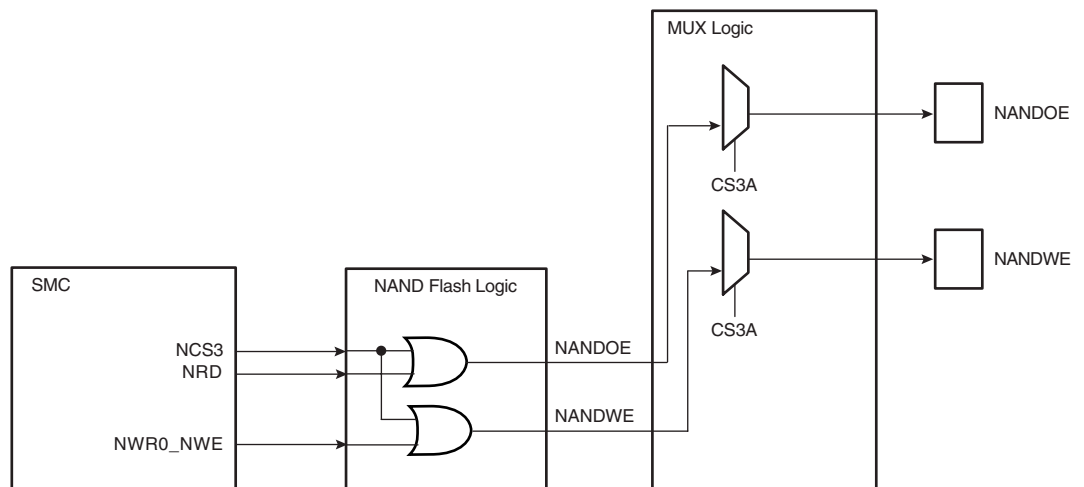


Table 4-1. AT91SAM7SE EBI NAND Flash Support signals

Name	Function	Type	Active Level
NCS3/NANDCS	NAND Flash Chip Select Line	Output	Low
NANDOE	NAND Flash Output Enable	Output	Low
NANDWE	NAND Flash Write Enable	Output	Low
A22/NANDCLE	Command Latch Enable	Output	High
A21/NANDALE	Address Latch Enable	Output	High

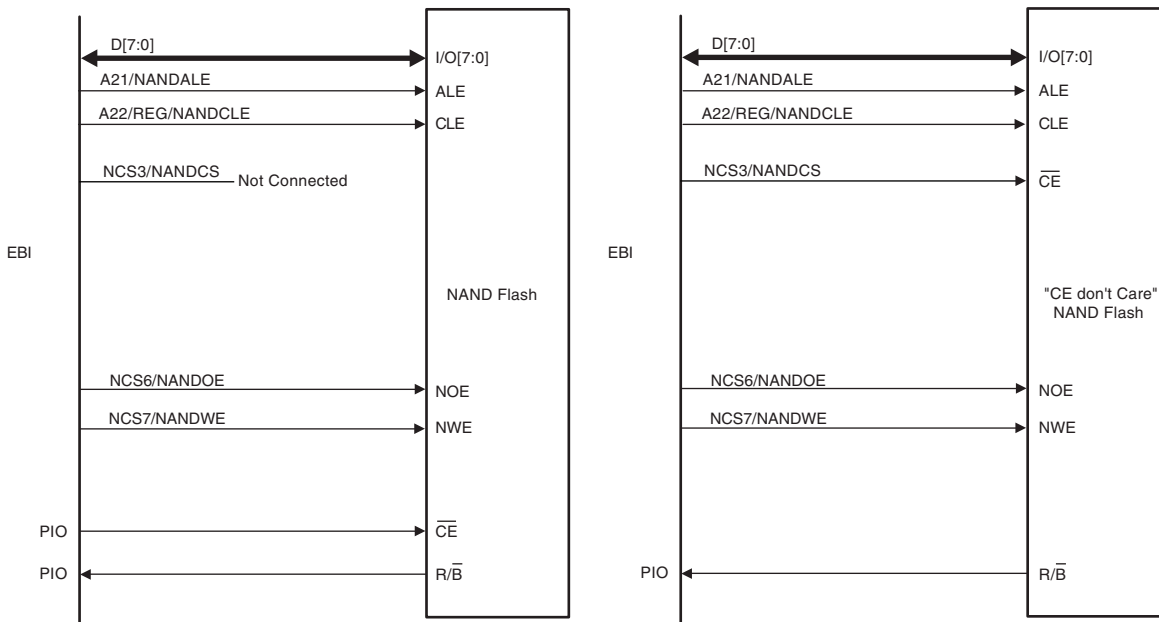
The NANDCS output signal should be used in accordance with the external NAND Flash device type. As mentioned in [“Section 2.4 ”Hardware Interface”](#), two types of CE behavior exist depending on the NAND flash device.

Standard NAND Flash devices require that the $\overline{CE}$ pin remains asserted Low continuously during the read busy period to prevent the device from returning to standby mode. Since the AT91SAM7SE Static Memory Controller (SMC) asserts the NCS3/NANDCS signal High, it is necessary to connect the $\overline{CE}$ pin of the NAND Flash device to a GPIO line in order to hold it low during the busy period preceding data read out.

This restriction has been removed for “CE don’t care” NAND Flash devices, in this case the AT91SAM7SE NCS3/NANDCS signal can be directly connected to the $\overline{CE}$ pin of the NAND Flash device.

Figure 4-2 illustrates the two types of topologies.

Figure 4-2. “CE don’t care” and Standard NAND Flash Application Examples



A GPIO line is dedicated to read the Ready/Busy# ($\overline{R/B}$) signal provided by the NAND Flash device.

In case of interfacing a Standard NAND Flash, a GPIO line is dedicated to drive the $\overline{CE}$ signal.

Please note that a particular constraint exists when interfacing 16-bit “CE don’t care” NAND Flash devices with the AT91SAM7SE. Since data line D15 is multiplexed with the NCS3/NANDCS, it is compulsory to dedicate a GPIO line to drive the $\overline{CE}$ signal when interfacing a 16-bit “CE don’t care” NAND Flash device.

Table 4-2. GPIO Requirements

AT91SAM7SE	NAND Flash	Function	Type	Active Level
PIOx	$\overline{CE}$	Chip Enable ⁽¹⁾ ⁽²⁾	Output	Low
PIOy	RDY/ $\overline{BSY}$	Ready/Busy# ⁽¹⁾	Input	Low

Notes: 1. Any free PIO can be used for this purpose.
2. For standard NAND and 16-bit devices.

The Address Latch Enable (ALE) and Command Latch Enable (CLE) signals on the NAND Flash device are respectively driven by address bits A21/NANDALE and A22/NANDCLE of the EBI address bus.

The command, address and data values must be written at address locations respecting certain restrictions to comply with NCS3 address space and ALE/CLE signal management.

The table below summarizes the address locations that can be written

Table 4-3. ALE/CLE Management

A22/NANDCLE	A21/NANDALE	AT91SAM7SE Memory Address Offset	NAND Register Selected
0	0	0x4X0XXXXX 0x4X1XXXXX 0x4X8XXXXX 0x4X9XXXXX	DATA register
0	1	0x4X2XXXXX 0x4X3XXXXX 0x4XAXXXXX 0x4XBXXXXX	ADDRESS register
1	0	0x4X4XXXXX 0x4X5XXXXX 0x4XCXXXXX 0x4XDXXXXX	COMMAND register

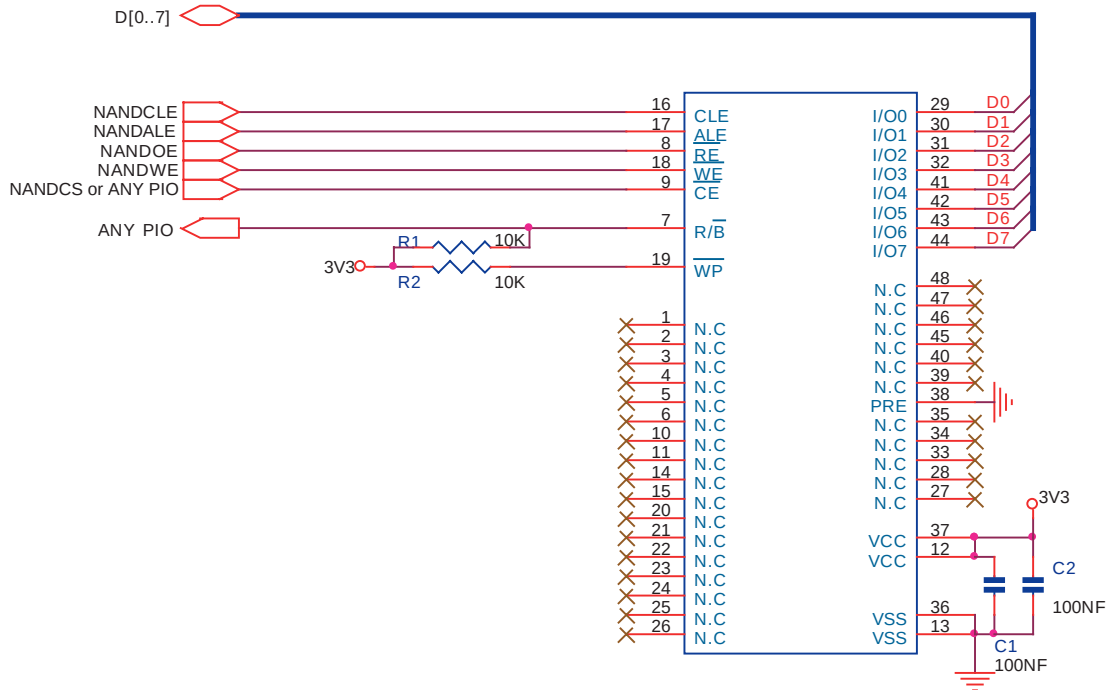
All the other address locations are prohibited to be used for accessing the NAND Flash device.

5. NAND Flash Connection Example on AT91SAM7SE

The AT91SAM7SE microcontrollers support 8-bit and 16-bit NAND Flash devices on one chip select area (NCS3).

5.1 8-bit NAND Flash Connection

5.1.1 Hardware Configuration



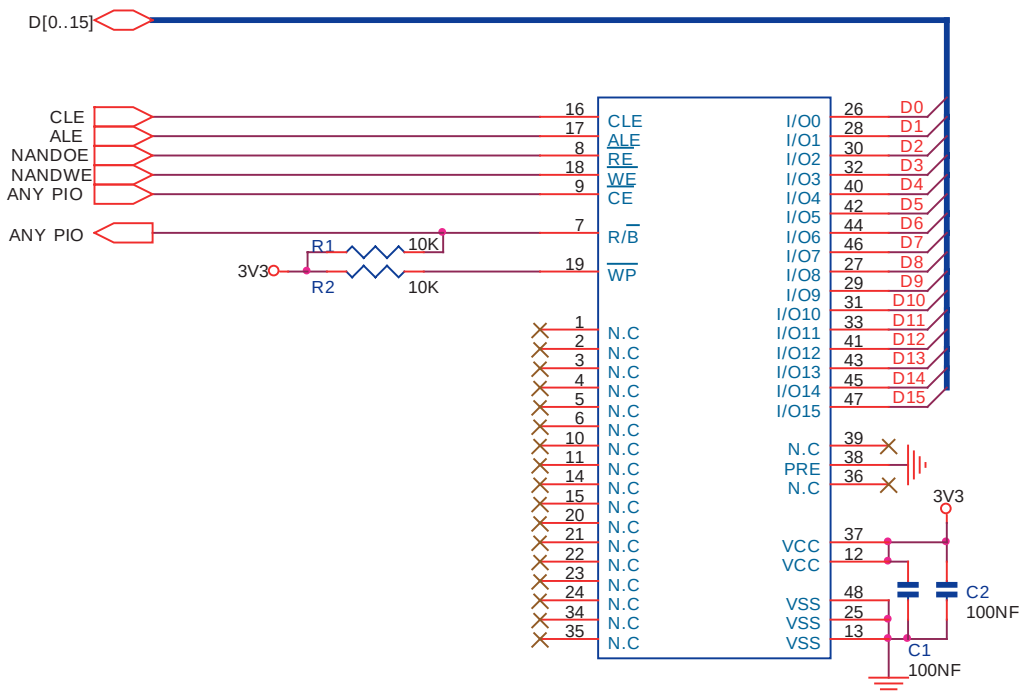
5.1.2 Software Configuration

The following configuration must be carried out:

- Setup Master clock through power management controller registers.
- Assign the EBI CS3 to the NAND Flash by setting the bit EBI_CS3A in the EBI Chip Select Assignment Register (EBI_CSA @0xFFFF FF80).
- A21/NANDALE, A22/NANDCLE, NANDOE, NANDWE, NANDCS (for CE don't care devices) and data lines D[0:7] are multiplexed with PIO lines and thus dedicated PIOs must be programmed in peripheral mode in the PIO controller.
- Configure a PIO line as an input and enable the clock of this PIO to manage the Ready/Busy signal. Enable the internal pull up resistor assigned to this pin by programming PIO_PUER register.
- Configure a PIO line as an output to control the NAND Flash device $\overline{CE}$ pin (In case of Standard NAND Flash device). Enable the internal pull up resistor assigned to this pin by programming PIO_PUER register.
- Configure the SMC_CSR3 register depending on NAND Flash device timings.

5.2 16-bit NAND Flash

5.2.1 Hardware Configuration



5.2.2 Software Configuration

The software configuration is the same as for 8-bit NAND Flash, except for the data bus width programmed in the SMC_CSR3 register and the assignment of the PIOs.

Note: When interfacing a Standard or “CE don’t care” NAND flash 16-bit device, it is compulsory to use a dedicated PIO line to drive the $\overline{CE}$ signal.

6. AT91SAM7SE System Initialization for a K9F2G08U0M Device

6.1 Samsung K9F2G08U0M Timing Parameters

Table 6-1 summarizes Samsung K9F2G08U0M timing parameters for SMC Chip Select register software settings.

Table 6-1. Samsung K9F2G08U0M Timings

Parameter	Symbol	Min	Max
CLE Setup Time	t_{CLS}	10	-
ALE Setup Time	t_{ALS}	10	-
$\overline{CE}$ Setup Time	t_{CS}	15	-
Data Setup Time	t_{DS}	10	-
Data Hold Time	t_{DH}	5	-
$\overline{CE}$ Access Time	t_{CEA}	-	23
$\overline{RE}$ Access Time	t_{REA}	-	18
Ready to $\overline{RE\#}$ Low	t_{RR}	20	-
CLE Hold Time	t_{CLH}	5	-
ALE Hold Time	t_{ALH}	5	-
$\overline{CE}$ Hold Time	t_{CH}	5	-
$\overline{RE}$ High to Output HI-Z	t_{RHZ}	30	-
$\overline{CE}$ High to Output HI-Z	t_{CHZ}	20	-
$\overline{RE}$ High Hold Time	t_{REH}	10	-
$\overline{WE}$ Pulse Width	t_{WP}	15	-
$\overline{RE}$ Pulse Width	t_{RP}	15	-
Write Cycle Time	t_{WC}	30	-
Read Cycle Time	t_{RC}	30	-

Figure 6-1 and Figure 6-2 illustrate respectively, Command Latch and Address Latch Cycle write sequences.

Figure 6-1. Samsung K9F2G08U0M Command Latch Cycle

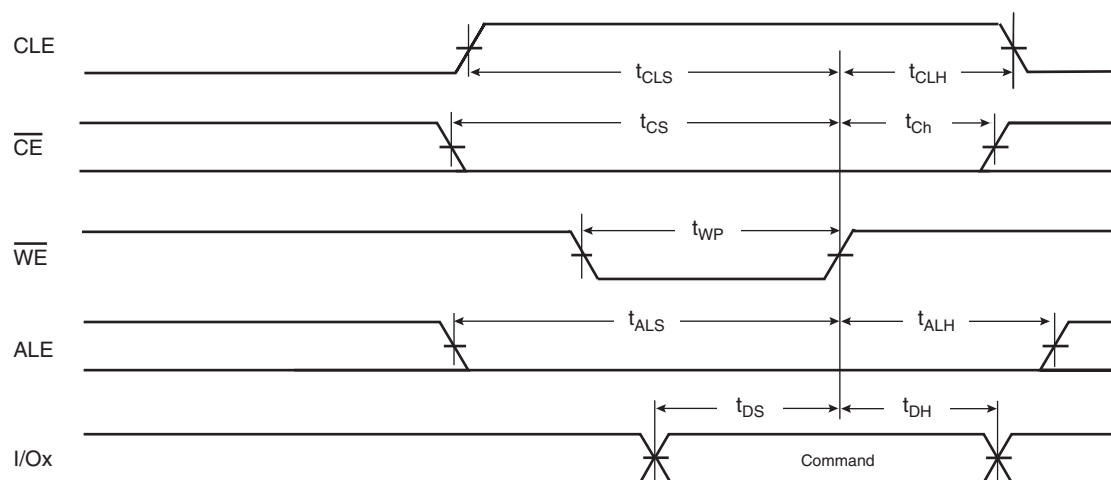


Figure 6-2. Samsung K9F2G08U0M Address Latch Cycle

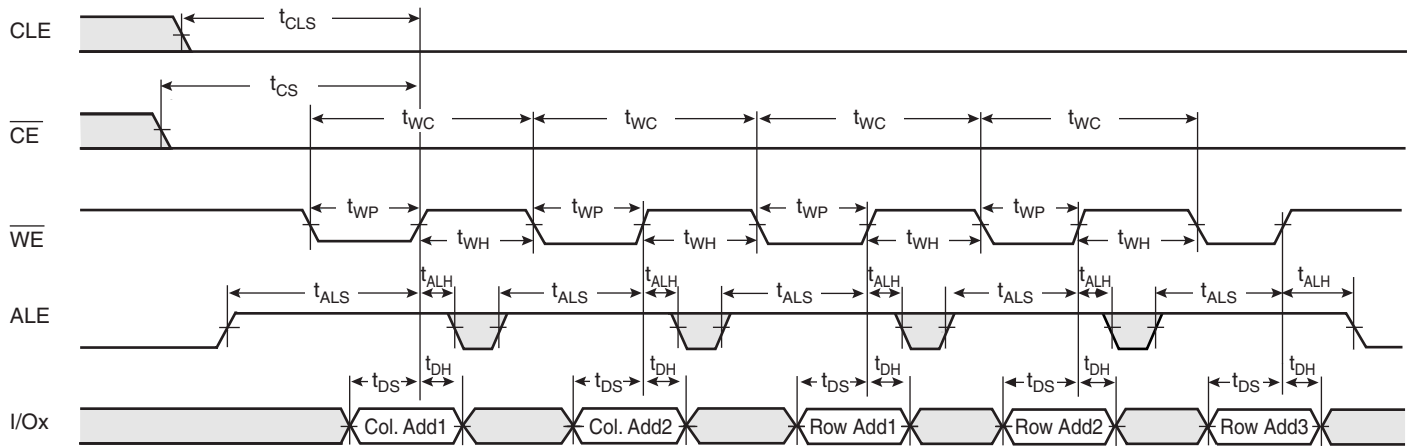


Figure 6-3 and Figure 6-4 illustrate respectively, Read Operation and Serial Access Cycle after Read sequences.

Figure 6-3. Samsung K9F2G08U0M Read Operation

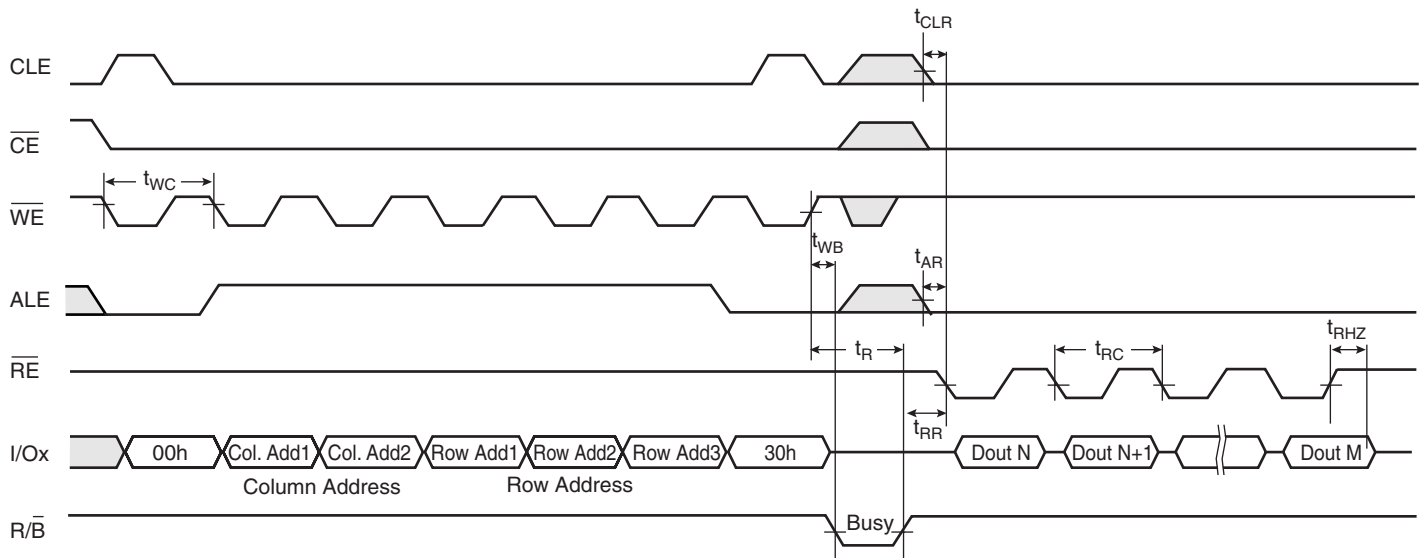
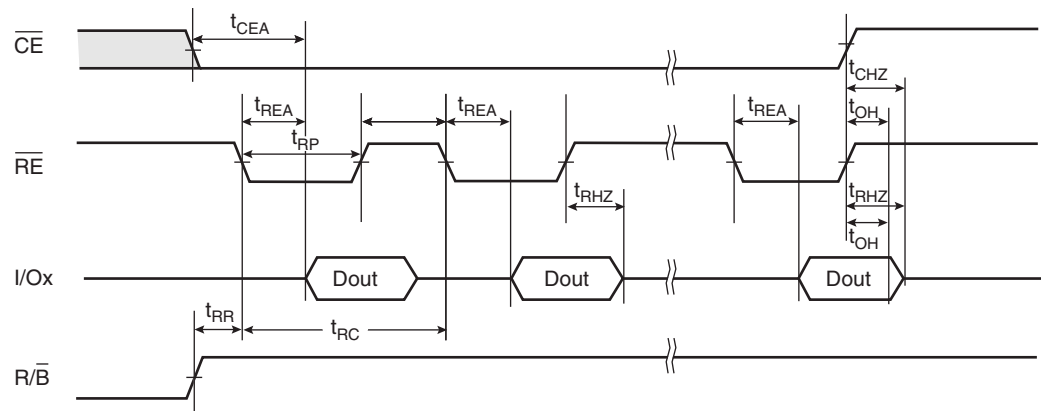


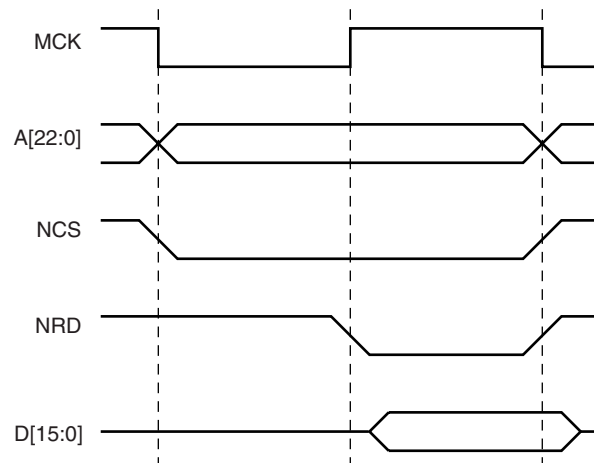
Figure 6-4. Samsung K9F2G08U0M Serial Access Cycle after Read



6.2 SMC Timings

Figure 6-5, Figure 6-6, Figure 6-7 and Figure 6-8 give the significant SMC read and write waveforms.

Figure 6-5. Standard Read Protocol



Please note that only ALE/A21 and CLE/A22 are concerned with address bus state changes.

Figure 6-6. Early Read Protocol

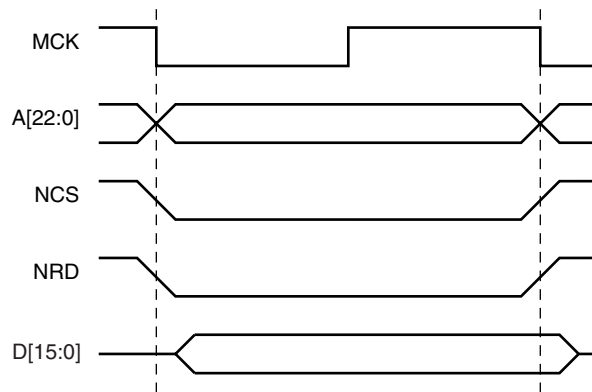


Figure 6-7. Write Access with 0 wait State

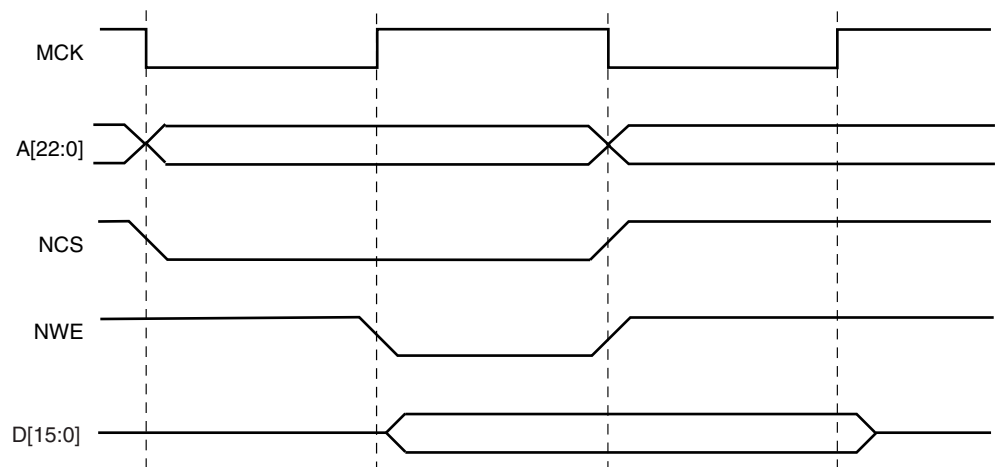
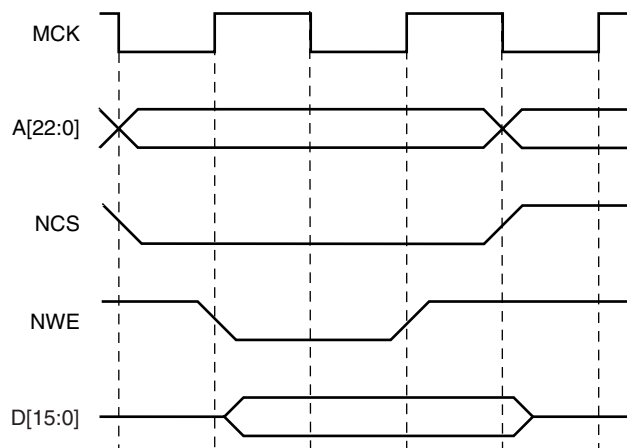


Figure 6-8. Write Access with 1 wait State



6.3 SMC Chip Select Register Parameters

The SMC_CSR3 register fields must be programmed with the appropriate values in accordance with the NAND Flash device timings.

The main parameters to program are as follows:

- Number of Wait States (NWS): defined as the read and write signal pulse length (from 1 to 128 cycles)
- Wait State Enable (WSEN): disable/enable the number of wait states programmed
- Data Float Time (TDF): represents the minimum time allowed for the data to go to high impedance after the memory is disabled
- Byte Access Type (BAT): defines the number of devices (in case of 16-bit data bus)
- Data bus Width (DBW): defines the data bus width
- Data Read Protocol (DRP): selects the standard or early read protocol
- Address to Chip Select Setup (ACSS): selects the number of cycles between assertion of the address and chip select
- Read and Write Signal Setup Time (RWSETUP): defines the number of cycles between the assertion of NCS signal and NWR or NRD activation.
- Read and Write Signal Hold Time (RWHOLD): defines the number of cycles between deactivation of NRD or NWR signals and the address/data change

It is assumed that the master clock frequency of the system is running at 48 MHz, hence one clock cycle is equal to 20.8 ns.

The first step to achieve is to determine whether the standard or the early read protocol has to be used. By comparison, it is deduced that the SMC standard read protocol waveform ([Figure 6-5](#)) matches with the Samsung K9F2G08U0M read operation ([Figure 6-3](#)) and serial access cycle after read waveforms ([Figure 6-4](#)).

Since the SMC asserts high at the same time as the NANDCS and NANDOE signals, the data float time (TDF) corresponds to the time referenced as t_{RHZ} in [Table 6-1](#). The TDF register is programmed with a value of 2 cycles, minimum.

The data bus width (DBW) is given by the NAND Flash device type. The K9F2G08U0M has an 8-bit data width.

As concerns the K9F2G08U0M command latch cycle ([Table 6-1](#)) and address latch cycle waveforms ([Table 6-2](#)), there are no time constraints between the assertion of address lines (ALE and CLE) and the chip select ($\overline{CE}$). Hence the Address to Chip Select Setup (ACSS) is programmed to standard.

[Table 6-2](#) below gives an overview of K9F2G08U0M timing requirements versus SMC programmable parameters.

Table 6-2. Samsung K9F2G08U0M Timing Requirements Versus SMC Programmable Parameters

Samsung K9F2G08U0M Parameter	Symbol	SMC Related Parameter
CLE Setup Time	t_{CLS}	NWR Setup + NWR Pulse
ALE Setup Time	t_{ALS}	NWR Setup + NWR Pulse
$\overline{CE}$ Setup Time	t_{CS}	NWR Setup + NWR Pulse
Data Setup Time	t_{DS}	Data Out Valid Before NWR High

Table 6-2. Samsung K9F2G08U0M Timing Requirements Versus SMC Programmable Parameters (Continued)

Samsung K9F2G08U0M Parameter	Symbol	SMC Related Parameter
Data Hold Time	t_{DH}	NWR Hold
$\overline{CE}$ Access Time	t_{CEA}	NRD Pulse + 1/2 Cycle - Data Setup before NRD High
$\overline{RE}$ Access Time	t_{REA}	NRD Pulse - Data Setup before NRD High
Ready to $\overline{RE}$ Low	t_{RR}	Managed by software
CLE Hold Time	t_{CLH}	NWR Hold
ALE Hold Time	t_{ALH}	NWR Hold
$\overline{CE}$ Hold Time	t_{CH}	NWR Hold
$\overline{RE}$ High to Output HI-Z	t_{RHZ}	TDF (if $\overline{RE}$ and $\overline{CE}$ asserted at the same time)
$\overline{CE}$ High to Output HI-Z	t_{CHZ}	TDF (if $\overline{CE}$ asserted High after $\overline{RE}$)
$\overline{RE}$ High Hold Time	t_{REH}	NRD Hold + NRD Setup
$\overline{WE}$ Pulse Width	t_{WP}	NWR Pulse
$\overline{RE}$ Pulse Width	t_{RP}	NRD Pulse
Write Cycle Time	t_{WC}	NWR Pulse + NWR Setup + NWR Hold
Read Cycle Time	t_{RC}	NRD Pulse + NRD Setup + NRD Hold

The K9F2G08U0M $\overline{WE}$ pulse width (t_{WP}) and the $\overline{RE}$ pulse width (t_{RP}) given in [Table 6-1](#) are both equal to 15 ns. They respectively define the NWR pulse length and the NRD pulse length SMC requirements.

[Table 6-3](#) summarizes the SMC NRD pulse length and NWR pulse length in accordance with the number of wait states.

Table 6-3. SMC NRD Pulse Length and NWR Pulse Length

Number of Wait States	NWS field	NRD Pulse Length	NWR Pulse Length
0 ⁽¹⁾	Don't Care	1/2 cycle ⁽²⁾	1/2 cycle
1	0	1 + 1/2 cycles	1 cycle
2	1	2 + 1/2 cycles	2 cycles
X + 1	Up to X = 127	X + 1 + 1/2 cycles	X + 1 cycle

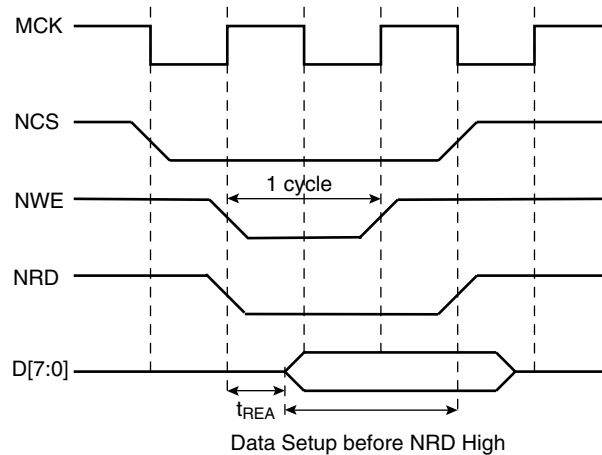
Notes: 1. Assuming WSEN Field = 0.
2. In Standard Read Protocol.

At 48 MHz, 1 cycle is equal to 20.8 ns. According to [Table 6-3](#) above, 1 wait state is required to comply with the K9F2G08U0M $\overline{WE}$ pulse width (t_{WP}) and the $\overline{RE}$ Pulse Width (t_{RP}) requirements.

With 1 wait state, the NRD pulse length is equal to 31.25ns (1 + 1/2 cycles) and the NWR pulse length is equal to 20.8 ns (1 cycle).

The figure below illustrates the time constraints related to the NAND Flash data read access time and the AT91SAM7SE data setup before the NRD signal goes High.

Figure 6-9. NAND Read and AT91SAM7SE Setup Constraints before NRD



The “Data Setup Before NRD High” and the “Data Out Valid Before NWR High” parameters as given in the [AT91SAM7SE](#) product datasheet (refer to the SMC signals in the Electrical Characteristics section) are respectively equal to 41.1 ns (Number of Wait States $\times t_{\text{CYCLE}} - 0.5$) and 22.2 ns.

The K9F2G08U0M $\overline{\text{RE}}$ data access time (t_{REA}) is given as 18 ns maximum, while Data Setup Before NRD High is given as 22.2 ns minimum, therefore it is required to extend the NRD pulse by programming the NWS field with at least two wait states.

With 2 wait states programmed, the SMC Data Out Valid before NWR High is equal to 41.1 ns. Since it is greater than the K9F2G08U0M data setup time (t_{DS}), there is no need to extend the NWR Pulse.

The NWS field is programmed according to [Table 6-3](#) in order to obtain 2 SMC Wait State waveforms.

Assuming the SMC is generating 2 Wait State waveforms at 48 MHz with a standard read protocol, the following timings are obtained:

- NRD Setup Min = 10.4 ns
- NWR Setup Min = 10.4 ns
- NRD Hold Min = 0 ns
- NWR Hold Min = 10.4 ns
- NRD Pulse = 52 ns
- NWR Pulse = 41.6 ns

According to [Table 6-2](#), RWSETUP and RWHOLD fields should be left at zero since all the K9F2G08U0M timing constraints are satisfied.

Referring to the [AT91SAM7SE](#) product datasheet, the ECC Controller requires at least one RWHOLD cycle to compute data properly. RWHOLD field is then programmed consequently.

6.4 NAND Flash Support Initialization on the AT91SAM7SE-EK

6.4.1 Clocks

The system is running at 48 MHz.

Table 6-4. System Configuration

Description	Settings	Register/field	Value
Crystal Frequency Oscillator	18.432 MHz		
PLL output frequency	96 MHz	CKGR_PLLR	0x1048100E
Processor / Master Clock	48 MHz	PMC_MCKR	0x00000007

6.5 EBI and SMC configuration

The EBI NCS3 has to be assigned for NAND Flash support.

[Table 6-5](#) gives EBI and SMC register configurations, other fields keep the reset values.

Table 6-5. SMC NCS3 Configuration

Description	Register/Field	Settings	Value
EBI Chip Select Assignment	EBI_CSA	NAND Flash support	0x8
SMC Chip Select Register 3	SMC_CSR3		
Number of Wait States	NWS	2 cycles	0x1
Wait State Enable	WSEN	Enabled	0x1
Data Float Time	TDF	2 cycles	0x2
Byte Access Type	BAT	8-bit wide device	0x0
Data Bus Width	DBW	8-bit bus width	0x2
Data Read Protocol	DRP	Standard	0x0
Address to Chip Select Setup	ACSS	Standard	0x0
Read and Write Signal Setup Time	RWSETUP	1/2 cycle	0x0
Read and Write Signal Hold Time	RWHOLD	1/2 cycle	0x1

7. Software Example Description

The software example associated with this document has been developed under IAR4.31 environment for running on the [AT91SAM7SE-EK board](#). The software example allows the user to perform low level basic operations such as:

- Block erase
- Data read from a specified location (page/block)
- Data write to a specified location (page/block)

Once downloaded and running on the AT91SAM7SE chip, the following operations are performed:

- PMC configuration
- PIO controller configuration
- EBI chip select assignment
- SMC controller configuration
- NAND Flash device initialization
- Bad block table creation

Communication with the [AT91SAM7SE-EK board](#) is performed through the DBGU port (115200 bauds, 1 start, 1 stop, 8 bits, no parity, hardware handshaking: none).

The user is able to control software operations by sending command characters through any serial COM port-compatible application.

Table 7-1. Software Function

Function Name	Input Parameters	Output Parameters	Functional Description
AT91F_EBI_NANDFlash_CfgPIO	None	None	
AT91F_NANDFlash_Init	None	None	
AT91F_NANDFlash_Reset	None	None	Resets the NAND Flash device.
AT91F_NANDFlash_Read_ID	Device Information Structure Pointer	None	Identifies the NAND Flash device type and fills device information structure.
AT91F_NANDFlash_Create_Bad_Block_Table	Device Information Structure Pointer, Bad Block Table Pointer	Number of bad blocks	Fills the bad block table.
AT91F_NANDFlash_Page_Read	Device Information Structure Pointer, Page Buffer Table Pointer, Block Reference, Page Reference	None	Reads the entire data from a specified page within a block. Fills the data read into the page buffer table

Table 7-1. Software Function (Continued)

AT91F_NANDFlash_Block_Erase	Device information Structure Pointer, Bad Block Table Pointer, Block Reference	None	Erase an entire block of data. Prevents bad block information erasure.
AT91F_NANDFlash_Page_Write	Device information Structure Pointer, Bad Block Table Pointer, Page Buffer Table Pointer, Block Reference, Page Reference	None	Write the data contained in the page buffer table. Prevents overwriting bad block information
AT91F_NANDFlash_Status_Read	None	Last operation status	Check if the previous erase/write operation has been done successfully

8. High Level File System Software Drivers

High level software drivers for managing file systems in NAND Flash devices are available from different sources. These drivers provide support for wear leveling, bad block management, etc...

The table below gives a non-exhaustive list of proprietary software drivers from third parties and free software drivers from open source projects available through the internet.

Table 8-1. File System Software Drivers

Product Name	Company	URL Link
YAFFS	Adelph One Ltd.	http://www.aleph1.co.uk/taxonomy/term/31
smxFFS	Micro Digital Inc.	http://www.smxinfo.com/rtos/fileio/smxffs.htm
JFFS2	Red Hat Inc.	http://sources.redhat.com/jffs2/
Fusion Flash File System	Unicoi Systems Inc.	http://www.unicoi.com/fusion_ffs/fusion_flash_file_system.htm
TrueFFS®	SanDisk/MSystems	http://www.m-systems.com/site/en-US/Support/SoftwareDownload/default.htm
FlashFX®	Datalight Inc.	http://datalight.com/products/flashfx/
TargetFFS®NAND	Blunk Microsystems	http://www.blunkmicro.com/ffs.htm
EFFS-TINY	HCC-Embedded	http://www.hcc-embedded.com/site.php?mid=60
CMX-FFS	CMX Systems, Inc.	http://www.cmx.com/
emFile - File System	Segger	http://www.segger.com/emfile.html



Revision History

Doc. Rev	Comments	Change Request Ref.
6301A	First issue	





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Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics

Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-47-50
Fax: (33) 4-76-58-47-60

Literature Requests

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