

PIC16C716 → PIC16F716 Migration

DEVICE MIGRATIONS

This document is intended to describe the functional differences that are present when migrating from the PIC16C716 to the PIC16F716.

- Note 1:** This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.
- 2:** The user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and/or the Oscillator mode may be required.

Table 1 shows the considerations that must be taken into account when migrating from the PIC16C716 to the PIC16F716.

TABLE 1: PIC16C716 → PIC16F716 MIGRATION DIFFERENCES

Functional Differences				
No.	Difference	H/W	S/W	Prog.
1	Removed TRISCCP and DATA CCP registers	✓	✓	—
2	Program Memory Code Protection Scheme – All or Nothing	—	—	✓
3	BOR independent from PWRT	✓	—	—
4	Timer1 Oscillator designed only for 32.768 kHz operation.	✓	—	—
5	BODEN Configuration bit name changed to BOREN	—	✓	—
6	CCP module changed to ECCP	✓	✓	—
7	Four-word programming	✓	—	—

TABLE 2: PIC16C716 → PIC16F716 NEW FEATURES

No.	Feature
1	PIC16F716 has 2K words of Flash program memory
2	PIC16F716 GPR space 0xF0 to 0xFF accesses GPR space 0x70 to 0x7F
3	PIC16F716 has two-level Brown-out Reset detection selectable via BORV Configuration bit

PIC16F716

DEVICE MIGRATIONS

The PIC16F716 is mainly a technology process change from the PIC16C716 family of 18-pin parts. There are some changes that may affect older designs looking to use the new parts. The changes are grouped into two categories: those that affect hardware and those that affect software. In most cases, an older design will have little or no problems migrating to these new parts.

HARDWARE CHANGES

DATAACP and TRISCCP Removed

The DATAACP and corresponding direction control register, TRISCCP, have been eliminated.

The DATAACP register, bit<2> (DCCP) in combination with the TRISCCP register bit<2> (TCCP), provided access to the PIC16C716 CCP1 I/O bit, independent of the PORTB access and TRISB control. Direction control and read access of the CCP1 I/O bit in the PIC16F716 is a function of bit<3> of the TRISB and PORTB registers.

Bit<0> of the DATAACP register was the PIC16C716 software induced Timer1 clock input bit, DT1CK. Software clocking of Timer1 in the PIC16F716 can be accomplished by setting RB1 as an output (TRISB.1 = 1), TMR1CS for external clock operation (T1CON.1 = 1), and then cycling the RB1 output bit. Extra care must be exercised when cycling RB1 with bit set and bit clear commands as this may adversely affect the other output latches of the PORTB register.

Flash Program Memory Code Protection

Code protection for the program memory has changed from code-protect sections of memory to code-protect of the whole memory. Configuration bits<12,10,8,4> ($\overline{\text{CP0}}$) and bits<13,11,9,5> ($\overline{\text{CP1}}$) in the PIC16C716 do not exist in the PIC16F716. They have been replaced with one Configuration bit<13> ($\overline{\text{CP}}$).

New BOR PWRT Relationship

Enabling Brown-out Reset (BOR) does not automatically enable the Power-up Timer (PWRT) the way it did in the PIC16C716.

Timer1 Oscillator Speed Change

The Timer1 oscillator is now designed for operation with a 32.768 kHz tuning fork crystal. In the PIC16C716 the Timer1 oscillator was designed to run up to 200 kHz.

GPR Space common to Bank 0 and Bank 1

The last 16 bytes of data RAM in Bank 0, addresses 0x70 to 0x7F, are accessible from Bank 1 at addresses 0xF0 to 0xFF. This is most useful as a context storage space for interrupt processing since it makes altering the Bank Select bits unnecessary.

ECCP Replaces CCP module

The Enhanced CCP module (ECCP) of the PIC16F716 contains all the features of the PIC16C716 CCP module and adds to it control of up to 4 PWM outputs with deadband control, PWM auto shutdown and a toggle output on Compare mode.

The two Most Significant bits of the CCPCON1 register, unused in the PIC16C716, are used in the PIC16F716 to select the PWM output configuration. When porting PIC16C716 code to the PIC16F716, ensure that these bits are set to the intended configuration.

Added BORV Configuration Bit

The PIC16F716 uses Configuration bit<7> (BORV) to select between typical Brown-out Reset voltages of 4.0V (BORV = 1) or 2.5V (BORV = 0).

Four Word Programming

The PIC16F716 supports programming four words at a time (i.e., only one program command is required for every four load data word commands). As a result, programming the PIC16F716 by the four-word method takes only 25% of the time compared to the single-word method.

Process Differences

Because the PIC16F716 family uses a newer process technology, there will be subtle behavior differences between the PIC16C716 and the PIC16F716 parts. Before starting on a design migration, check the data sheets and verify that the electrical specifications for the new part are appropriate for your application.

SOFTWARE CHANGES

BOREN Configuration Bit

Configuration bit<6> was labeled BODEN on the PIC16C716. This Configuration bit is labeled BOREN on the PIC16F716 to be consistent with the new Brown-out Reset (BOR) terminology.

TERMINOLOGY CHANGES

The “Brown-out Detect (BOD)” terminology has changed to “Brown-out Reset (BOR)” to better represent the function that Brown-out circuitry performs.

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