AT91RM9200-EK Evaluation Board

User Guide

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Section 1

Overview

1.1 Scope

The AT91RM9200-EK Evaluation Board enables real-time code development and evaluation. It supports the AT91RM9200 ARM9™-based 32-bit RISC microcontroller.

This guide focuses on the AT91RM9200-EK Evaluation Board as an evaluation and demonstration platform:

- Section 1 is this overview.
- Section 2 gives information on setting up the installation.
- Section 3 contains a description of the development board.
- Section 4 details the configuration straps.
- Section 5 shows board schematics.
- Section 6 contains errata.

1.2 Deliverables

The development kit is delivered with:

- One AC adapter 100 - 240V ~ 1.2A, 12V, 50 - 60 Hz with adapters
- One modem RS232 cable
- One RJ45 Ethernet crossed cable
- One A/B-type USB cable
- One AT91 DVD-ROM containing summary and full datasheets, datasheets with electrical and mechanical characteristics, application notes and getting started documents for all development boards and AT91 microcontrollers. An AT91 software package with C and assembly listings is also provided. This allows the user to begin evaluating the AT91 ARM® Thumb® 32-bit microcontroller quickly.
- CD ROMs from third parties, providing solutions for operating system evaluation
- DataFlash® Cards to provide demonstrations of operating systems when inserted in the bootable slot

Note: To boot on a DataFlash Card:
- Ensure J15 (BMS) is set on position 1-2
- Insert the DataFlash Card in the J200 socket (bottom side)
- Reset the board

Further details are given on the AT91 DVD-ROM.

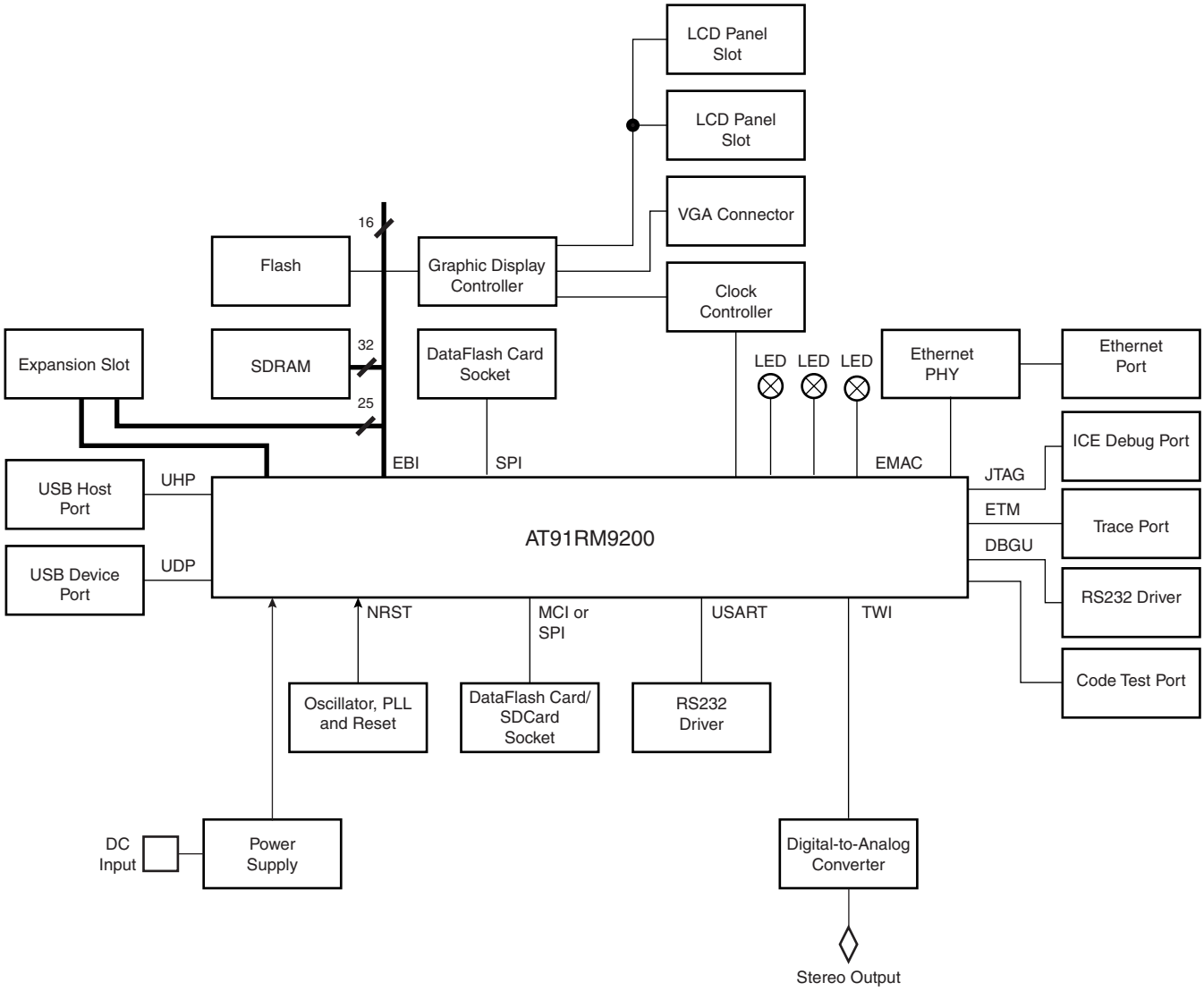
Note: These deliverables are subject to change without notice.

1.3 The AT91RM9200-EK Evaluation Board

The board consists of an AT91RM9200 together with the following:

- 8 Mbytes of parallel Flash memory
- Four banks of 2M x 32-bit SDRAM
- DataFlash® or SD/MMC memory expansion socket
- Additional DataFlash memory expansion socket
- Digital-to-Analog Converter (DAC) for a stereo audio signal
- Four communication ports (USB host and device, Ethernet, serial and DBGU)
- Graphic controller with output to a standard VGA monitor
- JTAG/ICE, ETM and code test port interface
- Expansion connector
- Onboard prototype area

Figure 1-1. AT91RM9200-EK Evaluation Board Block Diagram



Section 2

Setting Up the AT91RM9200-EK Evaluation Board

2.1 Electrostatic Warning

The AT91RM9200-EK Evaluation Board is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

2.2 Requirements

In order to connect the AT91RM9200-EK Evaluation Board, the following element is required:

- The AT91RM9200-EK Evaluation Board itself

2.3 Powering Up the Board

DC power is supplied to the board via the 2.1 mm socket (J1). The polarity of the power supply is not critical. The minimum voltage required is 7V.

The board has three voltage regulators providing 1.8V, 3.3V and 5V. The regulators allow the input voltage range to be from 7V to 12V.

2.4 Getting Started with the AT91RM9200

The AT91RM9200-EK Evaluation Board is delivered with a DVD-ROM containing all necessary information and step-by-step procedures for working with the most common development tool chains. Please refer to this DVD-ROM, or to the AT91 web site, http://www.atmel.com/products/AT91/ for the most up-to-date information on getting started with the AT91RM9200.

Section 3

Board Description

3.1 AT91RM9200 Processor

- Incorporates the ARM920T™ ARM® Thumb® Processor
  - 200 MIPS at 180 MHz
  - 16-KByte Data Cache, 16-KByte Instruction Cache, Write Buffer
  - Memory Management Unit
  - In-circuit Emulator including Debug Communication Channel
  - Mid-level Implementation Embedded Trace Macrocell™
- Additional Embedded Memories
  - 16K Bytes of SRAM and 128K Bytes of ROM
- External Bus Interface (EBI)
  - Supports SDRAM, Static Memory, Burst Flash, Glueless Connection to CompactFlash®, SmartMedia® and NAND Flash
- System Peripherals:
  - Enhanced Clock Generator and Power Management Controller
  - Two On-chip Oscillators with Two PLLs
  - Very Slow Clock Operating Mode and Software Power Optimization Capabilities
  - Four Programmable External Clock Signals
  - System Timer Including Periodic Interrupt, Watchdog and Second Counter
  - Real-time Clock with Alarm Interrupt
  - Debug Unit, Two-wire UART and Support for Debug Communication Channel
  - Advanced Interrupt Controller with 8-level Priority, Individually Maskable Vectored Interrupt Sources, Spurious Interrupt Protected
  - Seven External Interrupt Sources and One Fast Interrupt Source
  - Four 32-bit PIO Controllers with Up to 122 Programmable I/O Lines, Input Change Interrupt and Open-drain Capability on Each Line
  - 20-channel Peripheral DMA Controller (PDC)
- Ethernet MAC 10/100 Base-T
- USB 2.0 Full Speed (12 M-bits per second) Host Double Port and Device Port

- MultiMedia Card Interface (MCI)
- Three Synchronous Serial Controllers (SSC)
- Four Universal Synchronous/Asynchronous Receiver/Transmitters (USART)
- Master/Slave Serial Peripheral Interface (SPI)
- Two 3-channel, 16-bit Timer/Counters (TC)
- Two-wire Interface (TWI)
- IEEE 1149.1 JTAG Boundary Scan on All Digital Pins

3.2 Memory

- 8-Mbyte parallel Flash memory
- Four banks of 2M x 32-bit SDRAM

3.3 Memory Card

- SD Card/MMC
  - Supports MultiMedia and SD Card
  - Analog switches provide support for DataFlash® Card
- Additional DataFlash Card Socket

3.4 Clock Circuitry and Analog Functions

- 32.768 kHz standard crystal for the AT91RM9200
- 18.432 MHz standard crystal for the AT91RM9200
- 50 MHz CMOS oscillator for the Display Controller and Ethernet PHY

3.5 Reset Circuitry

- Reset Controller

3.6 Power Supply Circuitry

- 5V DC/DC converter
- 3.3V DC/DC converter
- 1.8V Linear regulator

3.7 Remote Communication

- Fast Ethernet Physical Layer Single Chip Transceiver
- Host Interface via RS-232 DB9 male socket
- Debug Port via RS-232 DB9 connector
- Host and Device USB socket

3.8 User Interface

- Graphic Display Controller
- TFT/SNT panel socket

- 15-pin standard socket for an external VGA monitor
- Three LEDs managed via general PIO lines
- Stereo Audio Jack connected to a DAC

3.9 Expansion Slot

- The expansion slot gives access to all the microcontroller's signals.

3.10 Debug Interface

- 38-pin trace Port socket (ETM)
- 38-pin Code Test port socket
- 20-pin JTAG ICE interface connector
- Serial Debug Unit

3.11 Wrapping User Area

- Onboard prototype area allowing the developer to fit additional components.

Section 4

Configuration Straps

4.1 Configuration Straps and Jumper Settings

Table 4-1 gives details on configuration straps and jumper settings on the AT91RM9200-EK Evaluation Board and their default settings.

Table 4-1. Configuration Straps and Jumper Settings

Designation	Default Setting	Feature
J13	Closed	Available for measuring VDDCORE current.
J15	1 - 2	The AT91RM9200 boots from internal ROM and can also boot from external SPI DataFlash® connected on NPCS0.
	2 - 3	The AT91RM9200 boots from Flash memory connected on NCS0.

Section 5

Schematics

5.1 Schematics

This section contains the following schematics:

- AT91RM9200-EK Board Layout, Rev. 63PC042262A01 - Top View
- AT91RM9200-EK Board Layout, Rev. 63PC042262A01 - Bottom View
- Power Supply
- AT91RM9200 Chip
- Debug
- SDRAM and Flash
- RMII Ethernet
- Stereo Audio DAC
- Serial Interfaces
- VGA Display
- Expansion Connector

Figure 5-1. AT91RM9200-EK Board Layout, Rev. 63PC042262A01 - Top View

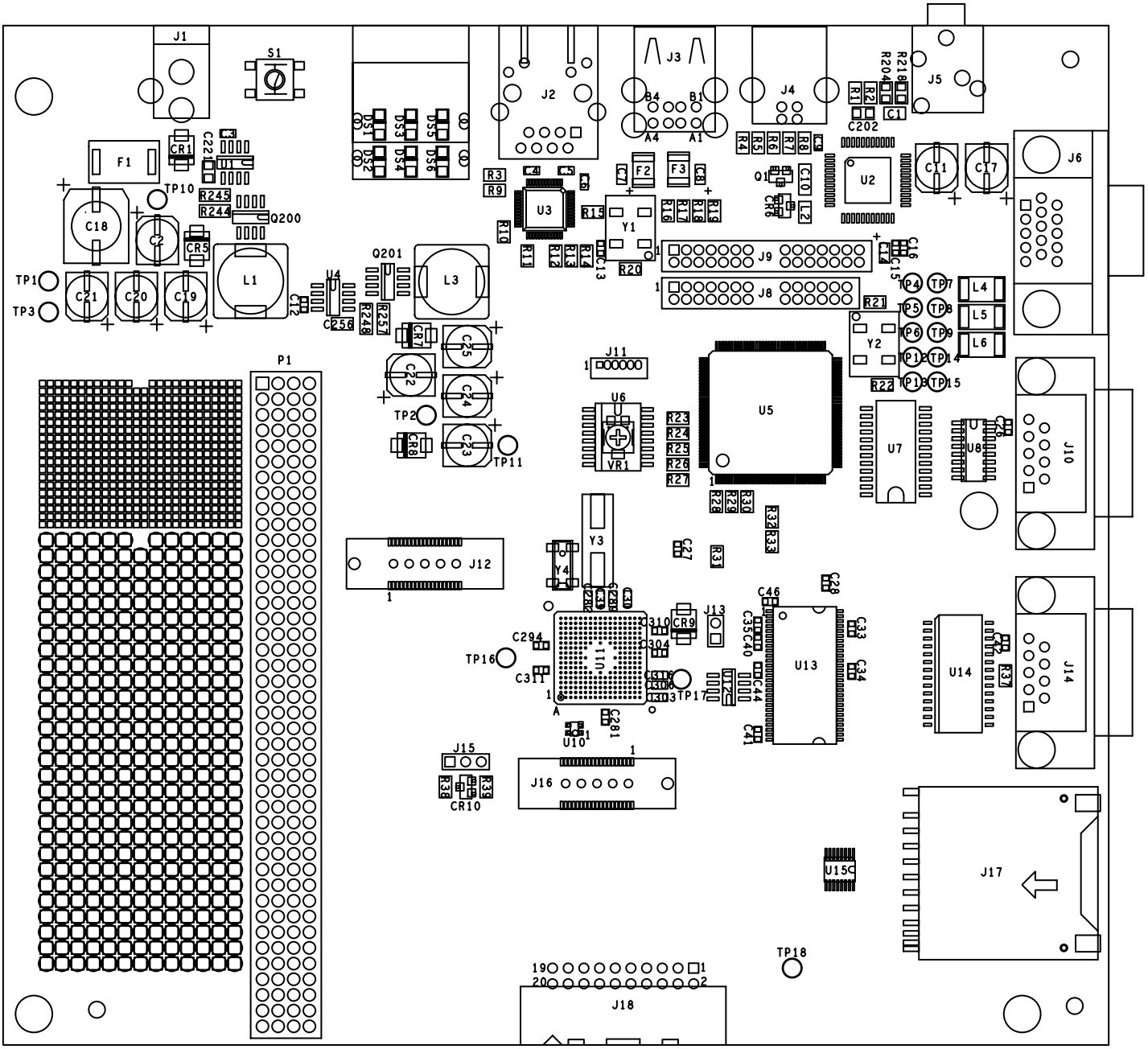
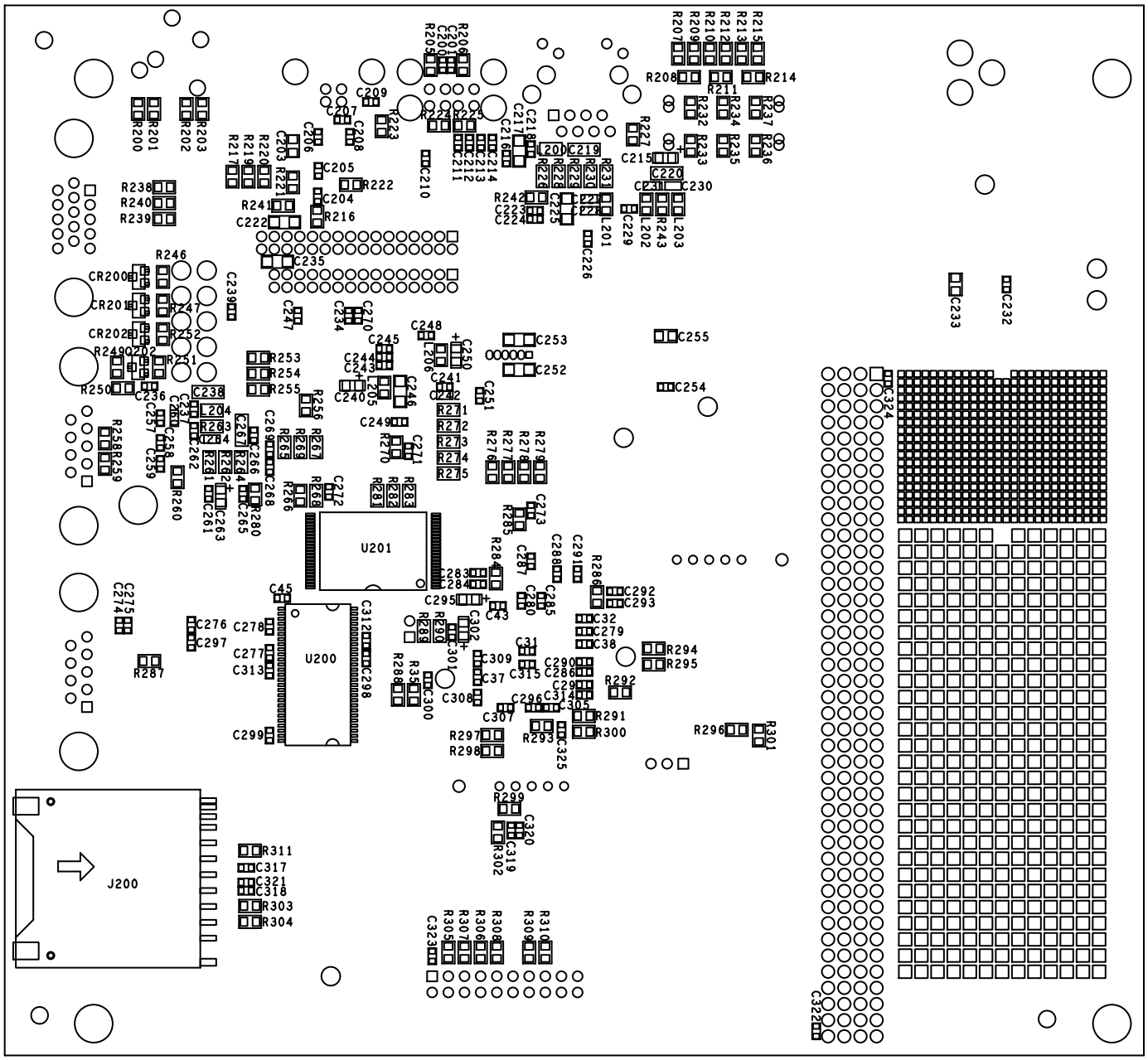
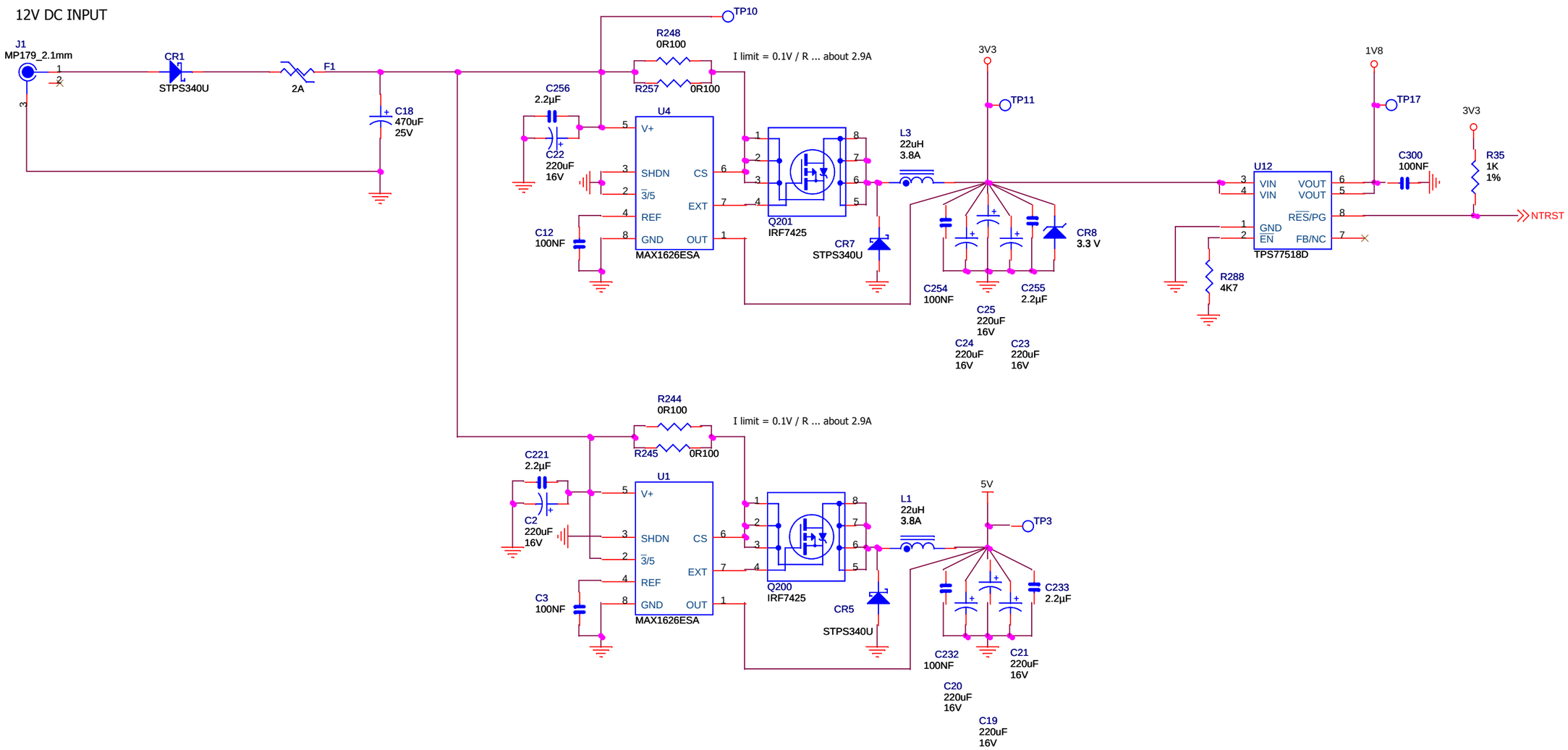
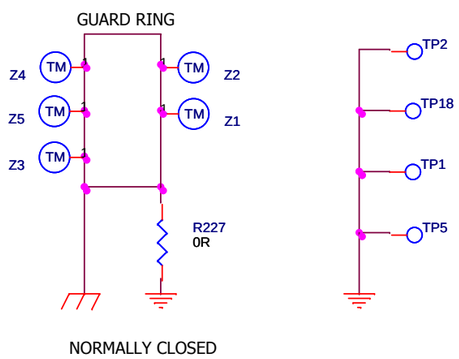


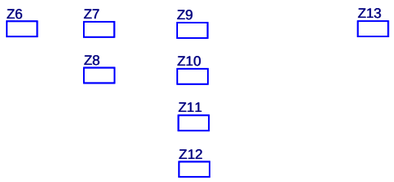
Figure 5-2. AT91RM9200-EK Board Layout, Rev. 63PC042262A01 - Bottom View





Z3 - Z5 are mounting holes.
The Z reference designators
are not listed on the actual
board.





Wednesday, February 23, 2005

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B	101-3-05-106	ELX	23/02/05	JPG	23/02/05
A	INIT EDIT	MDZ	04/01/05	JPG	06/01/05

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AT91RM9200-EK

POWER SUPPLY

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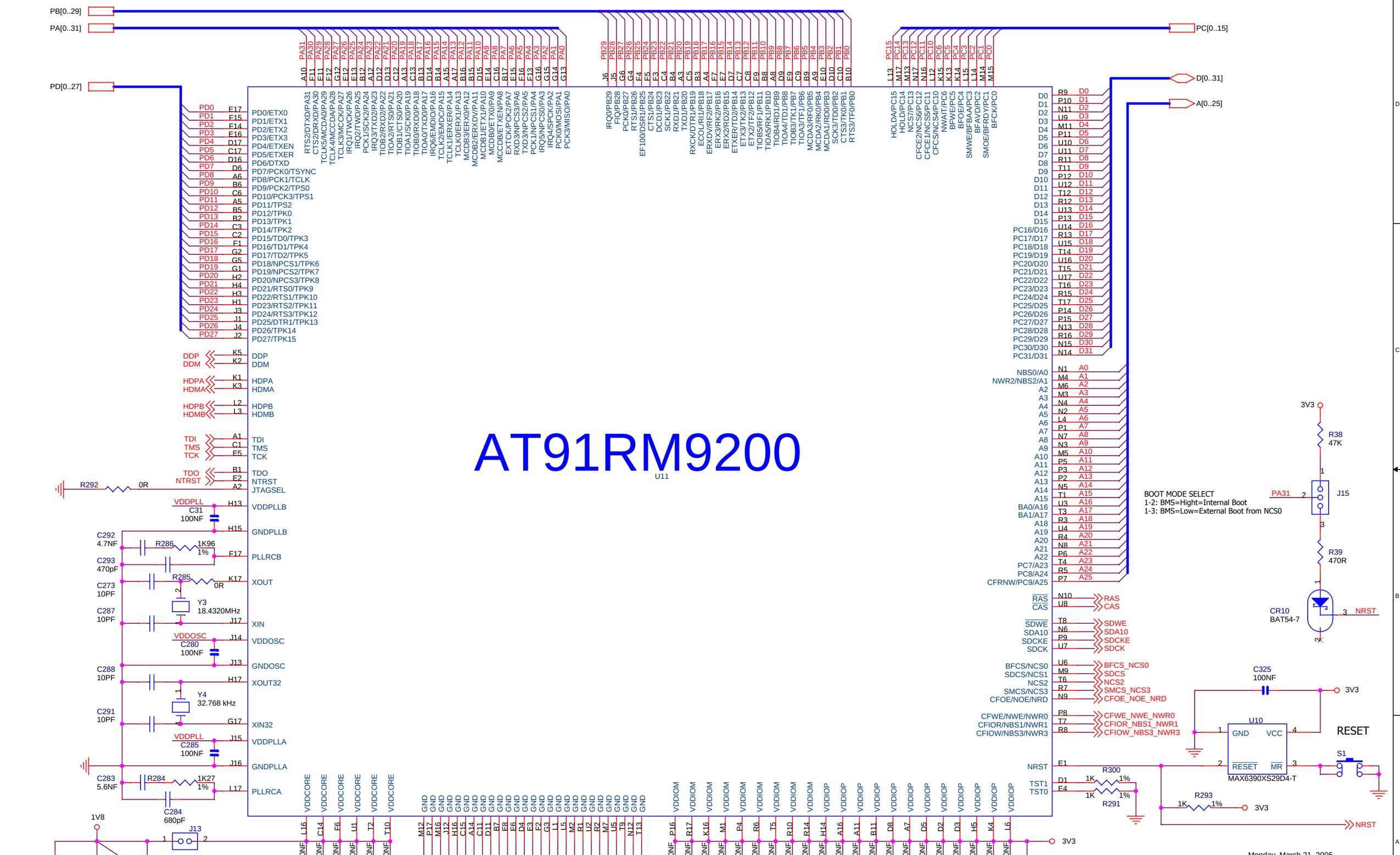

Monday, March 21, 2005

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A	INIT EDIT	MDZ	04/01/05	JPG	06/01/05

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AT91RM9200

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63SC042261 A01

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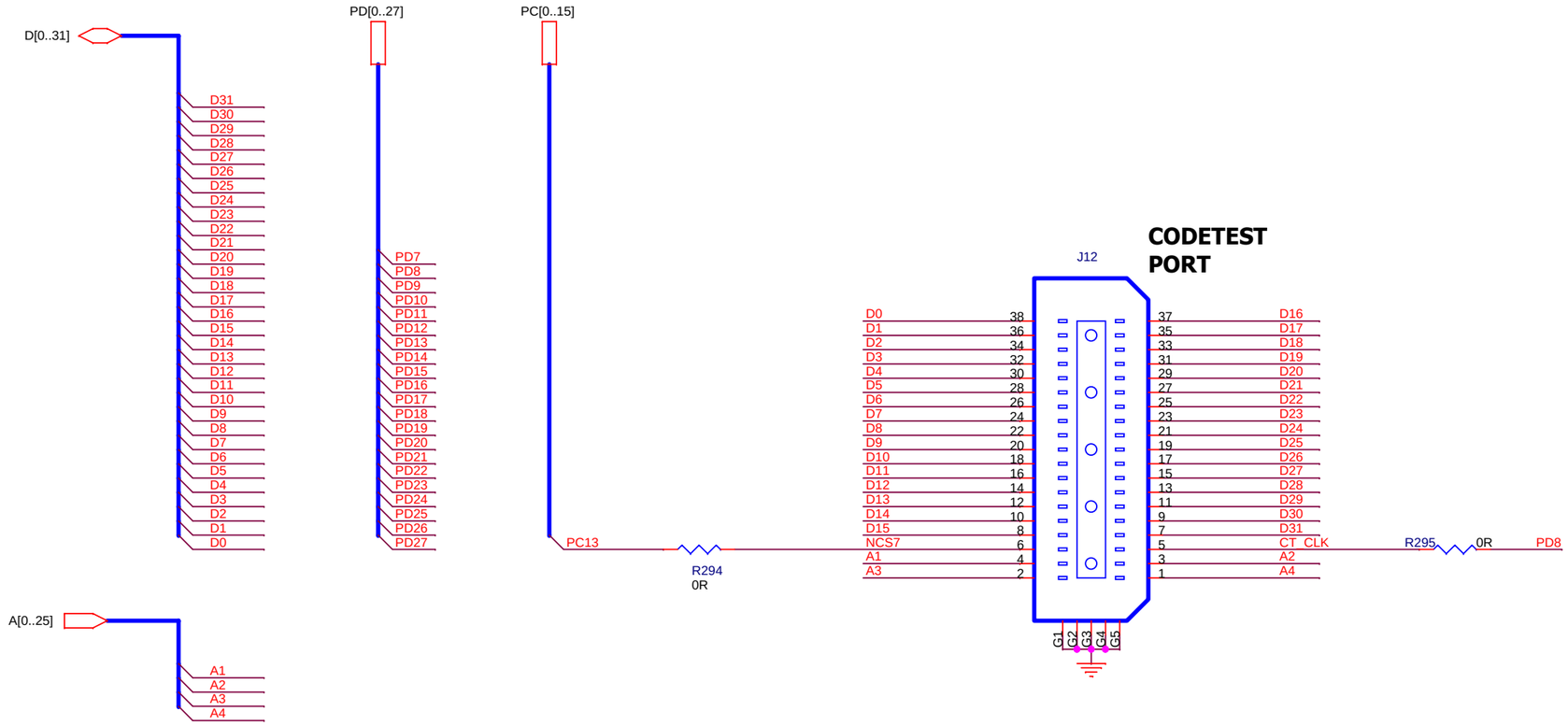

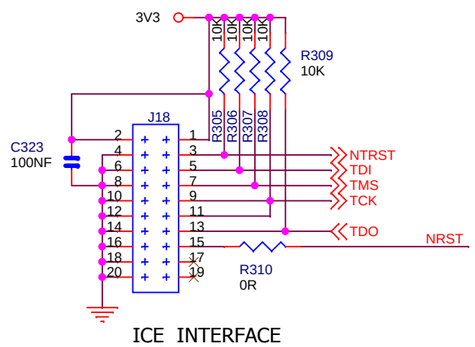

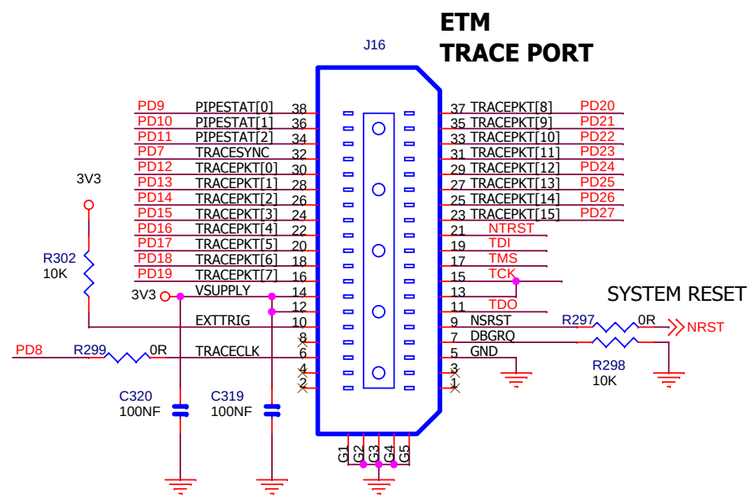

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A	INIT EDIT	MDZ	04/01/05	JPG	06/01/05

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AT91RM9200-EK

ETM - ICE - TEST

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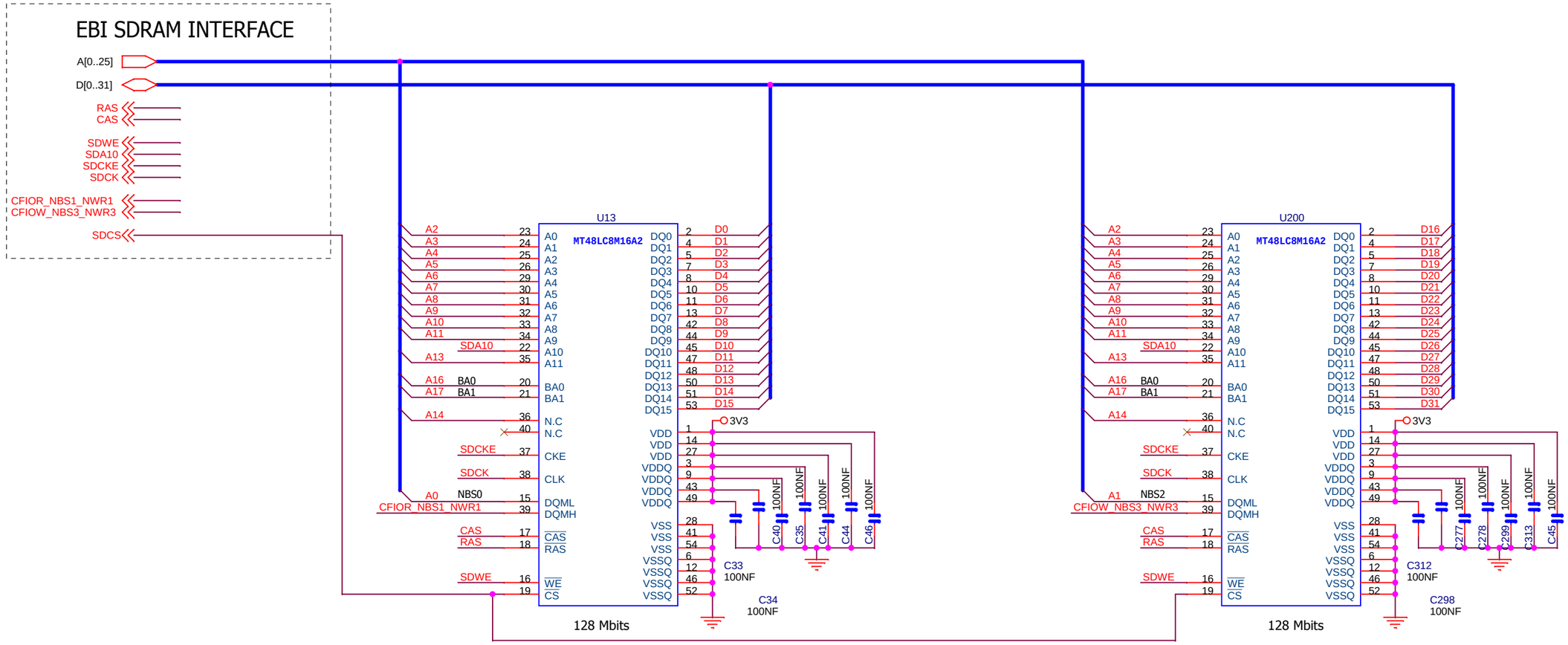

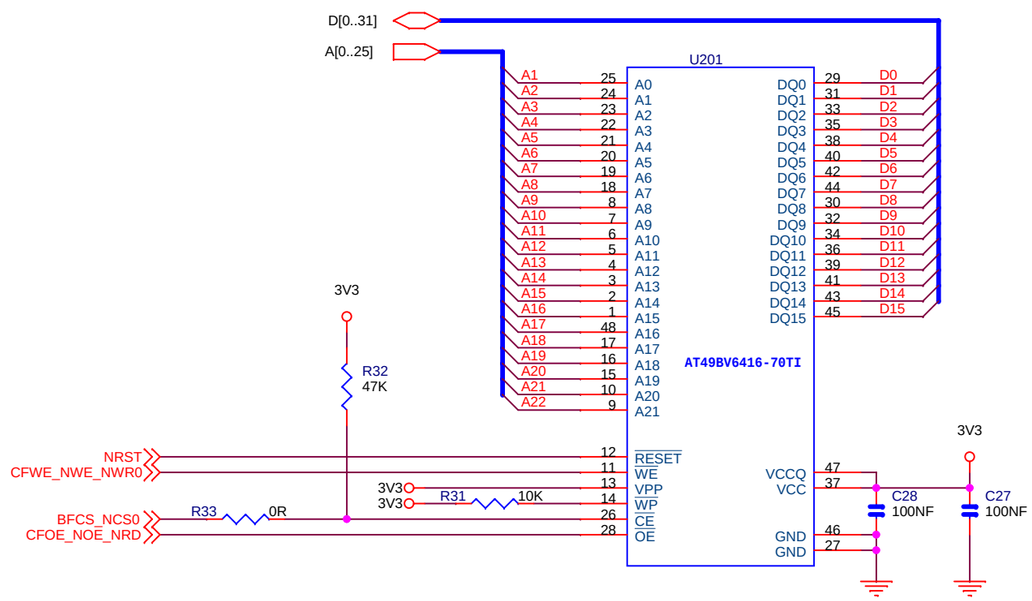

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AT91RM9200-EK

SDRAM & FLASH

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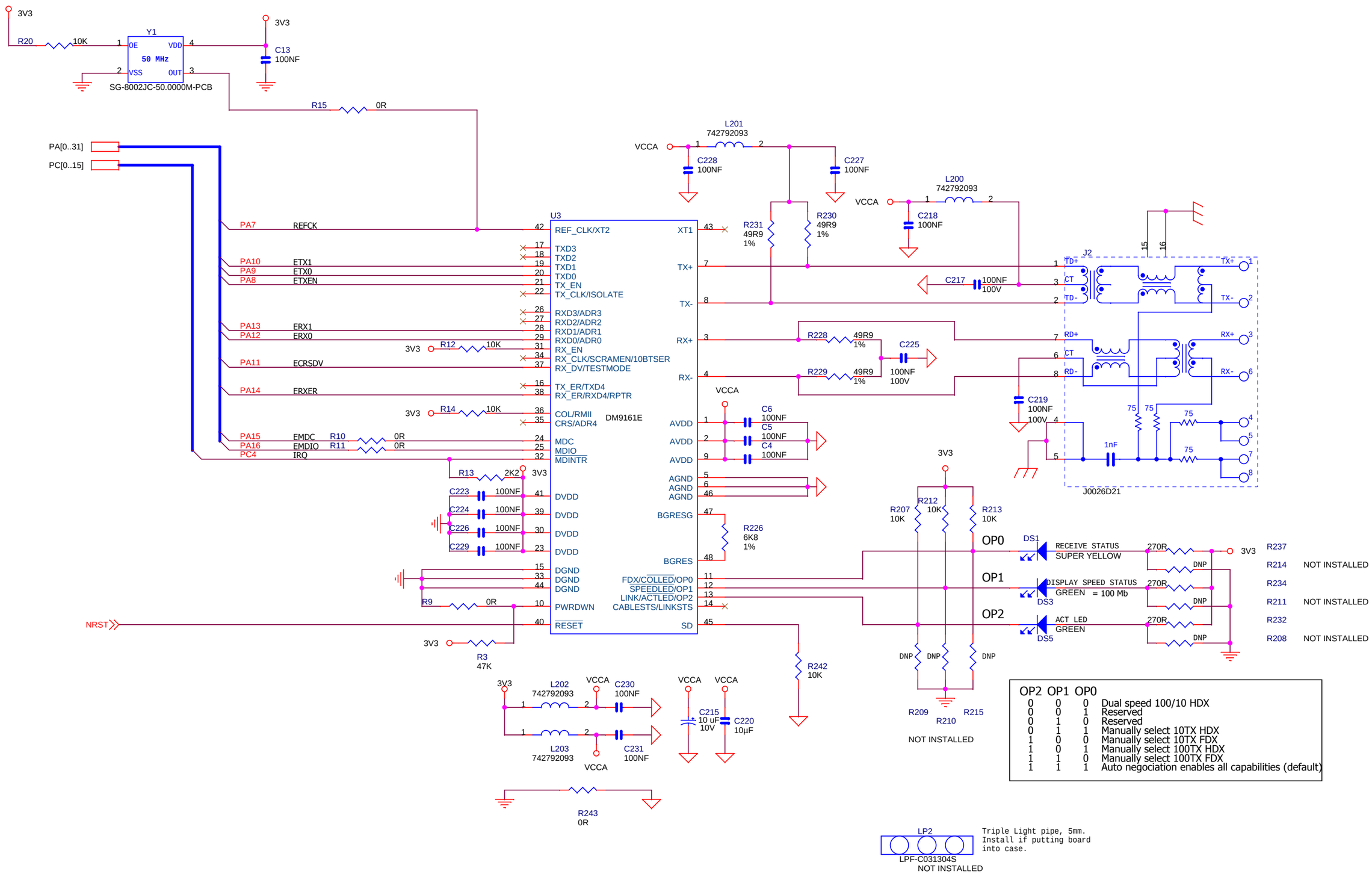

OP2	OP1	OP0	
0	0	0	Dual speed 100/10 HDX
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Manually select 10TX HDX
1	0	0	Manually select 10TX FDX
1	0	1	Manually select 100TX HDX
1	1	0	Manually select 100TX FDX
1	1	1	Auto negociation enables all capabilities (default)

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AT91RM9200-EK

ETHERNET

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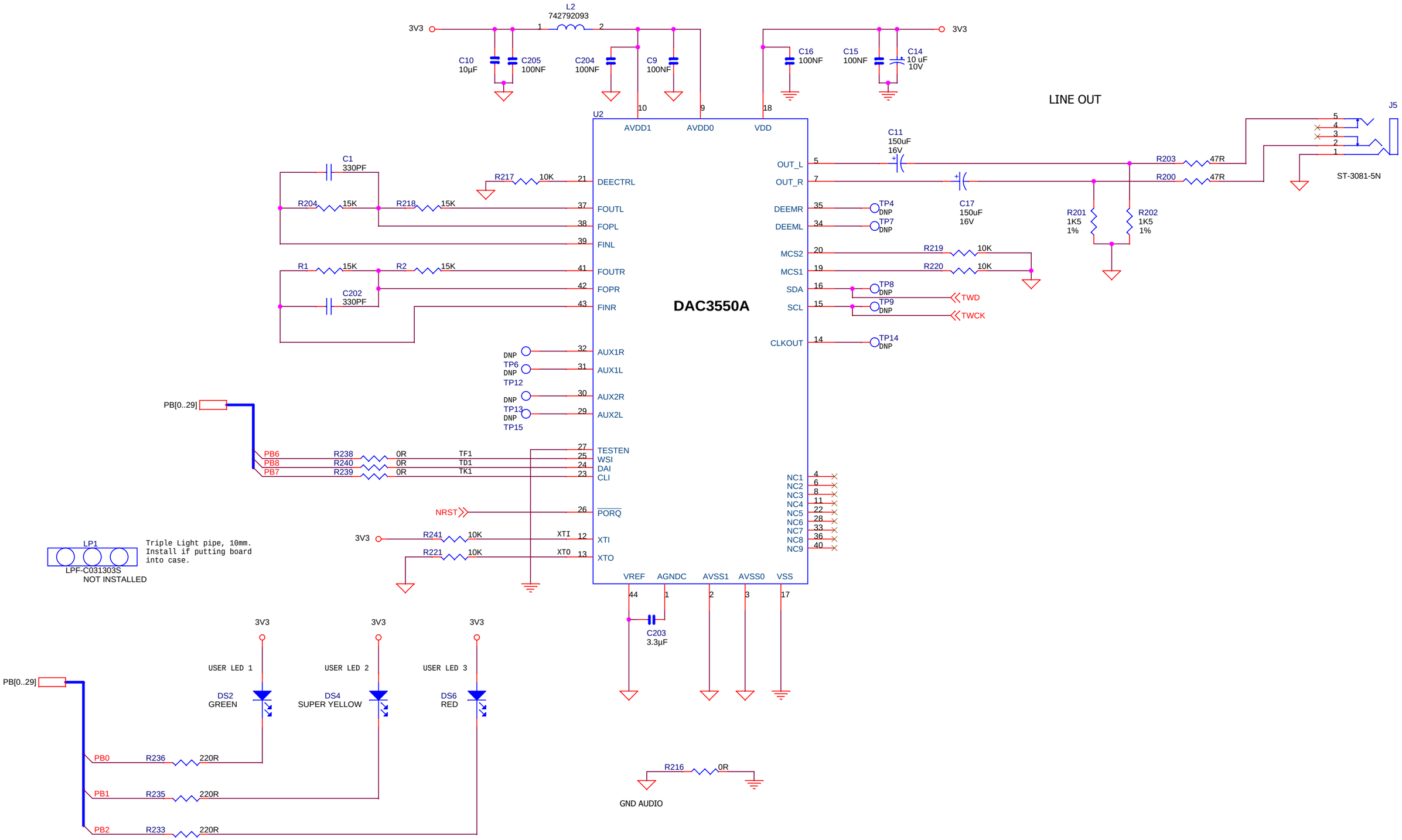

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AT91RM9200-EK

I2S STEREO DAC

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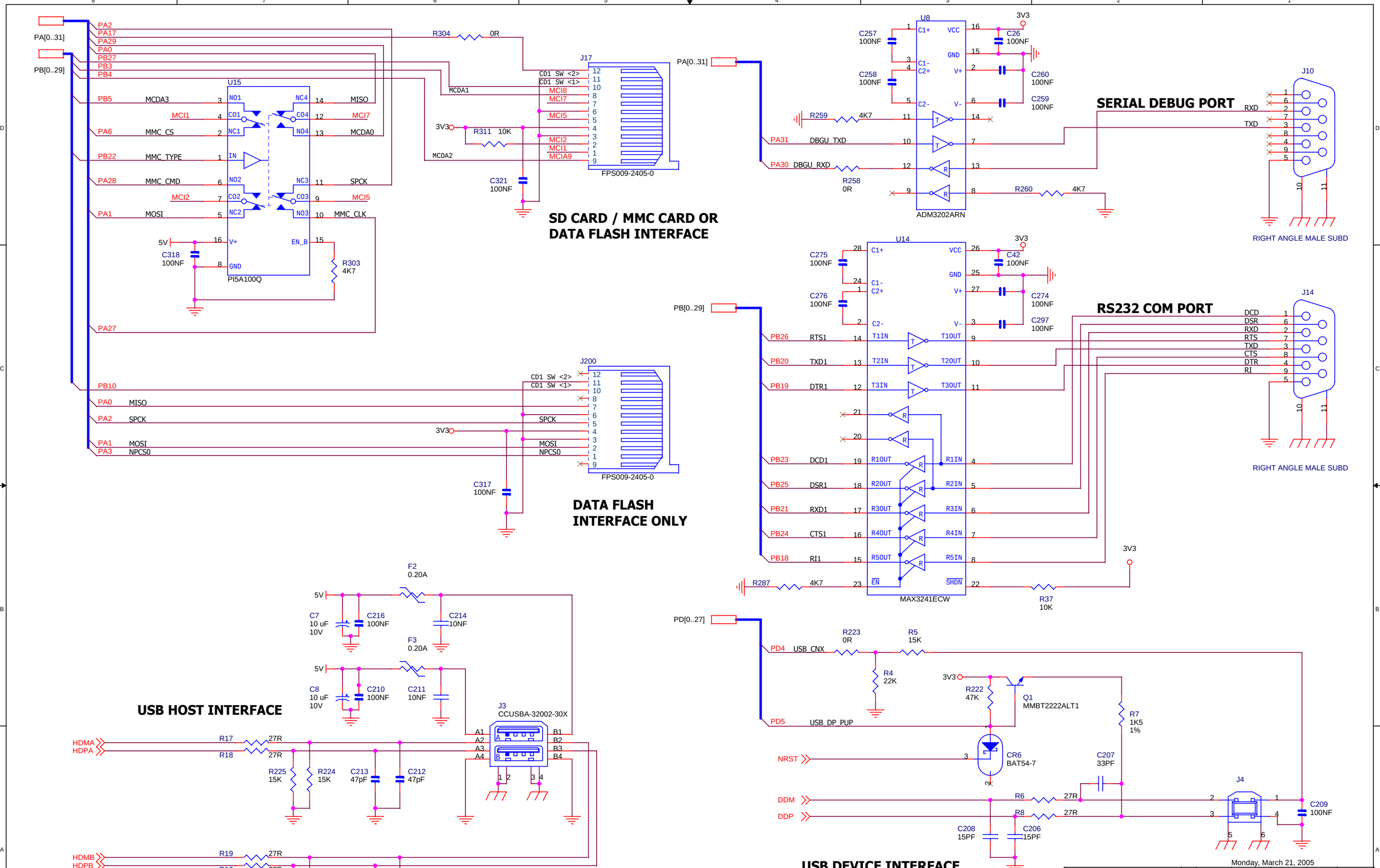
SD CARD / MMC CARD OR DATA FLASH INTERFACE
U15
PI5A100Q
J17
FPS009-2405-0
SERIAL DEBUG PORT
U8
ADM3202ARN
J10
RIGHT ANGLE MALE SUBD
DATA FLASH INTERFACE ONLY
J200
FPS009-2405-0
RS232 COM PORT
U14
MAX3241ECW
J14
RIGHT ANGLE MALE SUBD
USB HOST INTERFACE
J3
CCUSBA-32002-30X
USB DEVICE INTERFACE
J4
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AT91RM9200-EK
SERIAL INTERFACES
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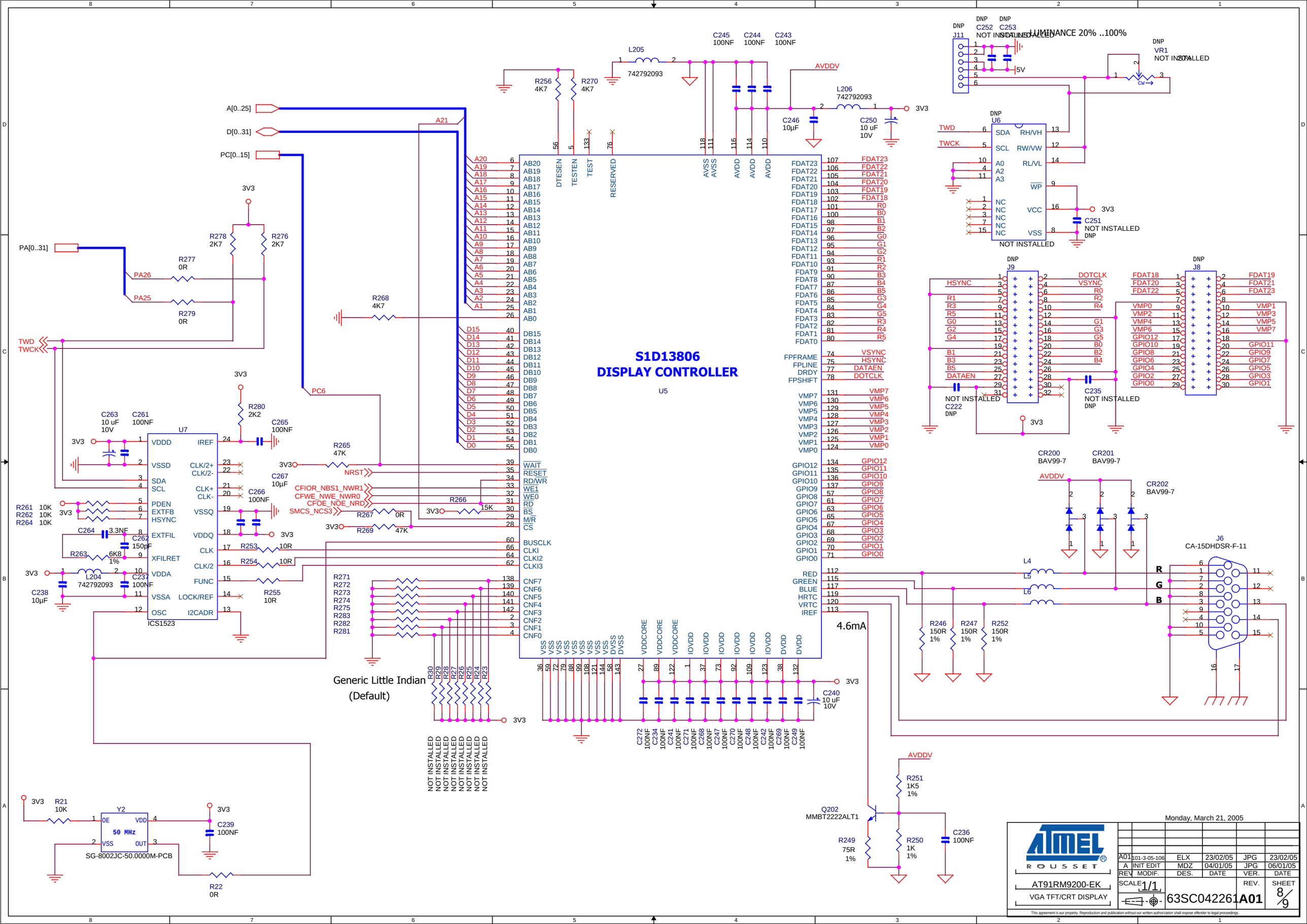
SHEET 7/9


S1D13806
DISPLAY CONTROLLER
U5
ICS1523
U7
SG-8002JC-50.0000M-PCB
Y2
50 MHz
J6
CA-15DHDSR-F-11
J9
J8
J11
U6
LUMINANCE 20% ..100%
VR1
NOT INSTALLED
Generic Little Indian
(Default)
4.6mA
Q202
MMBT2222ALT1
CR200
BAV99-7
CR201
BAV99-7
CR202
BAV99-7
L205
742792093
L206
742792093
L204
742792093
AVDDV
3V3
5V
A[0..25]
D[0..31]
PC[0..15]
PA[0..31]
TWD
TWCK
NRST
CFIOR_NBS1_NWR1
CFWE_NWE_NWR0
CFOE_NOE_NRD
SMCS_NCS3
DOTCLK
VSYNC
HSYNC
DATAEN
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AT91RM9200-EK
VGA TFT/CRT DISPLAY
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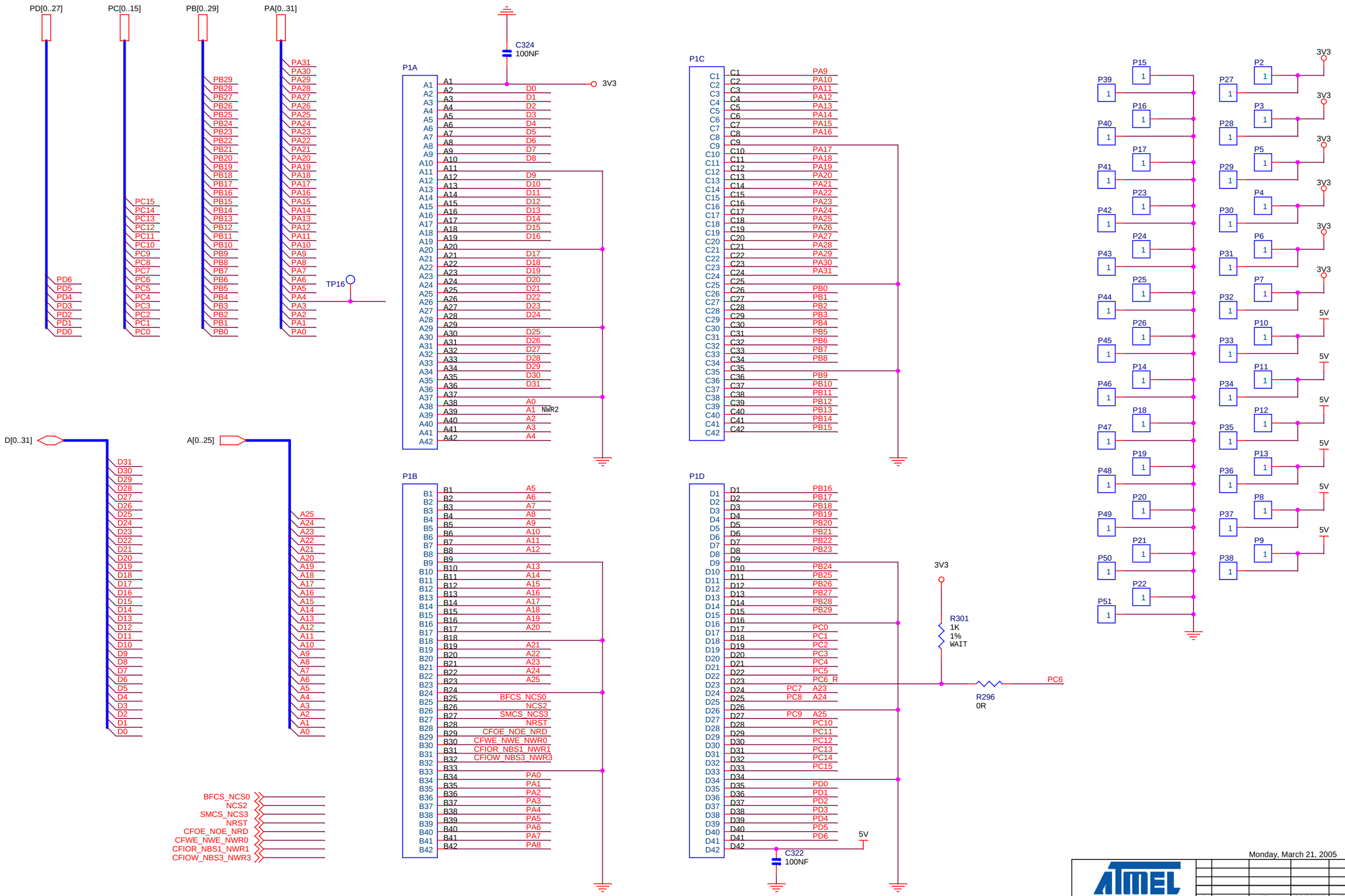

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A	INIT EDIT	MDZ	04/01/05	JPG	06/01/05

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AT91RM9200-EK

EXPANSION CONNECTORS

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Section 6

Errata

6.1 Errata

6.1.1 SD/MMC Card Slot Communication Problem

On the AT91RM9200-EK Board, revision 700-20226 REV X5, a communication problem may occur on the SD/MMC interface.

This issue has been corrected on all boards of revision 63PC042262A by adding a 10 kOhm pull-up resistor between the pin connectors J17-2 and J17-4.

Revision History

Doc. Rev.	Date	Comments	Change Request Ref.
6103A	24-Sep-04	First issue.	
6103B	02-Mar-05 19-Jul-05	Section 1.2, “Deliverables” on page 2; List simplified Table 4-1, Boot information modified New schematics added in Section 5.	CSR 04-361, CSR 05-028, CSR 05-246
6103C	07-Nov-05	Added Section 6, Errata.	CSR 05-478

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Fax: (33) 4-42-53-60-01

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