Section 12. Input Capture

HIGHLIGHTS

This section of the manual contains the following major topics:

Note: This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33F/PIC24H devices.

Please consult the note at the beginning of the **"Input Capture"** chapter in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com.

12.1 INTRODUCTION

This section describes the Input Capture module and its associated operational modes. The Input Capture module is used to capture a timer value from one of the two selectable time bases upon an event on an input pin. The Input Capture features are useful in applications that require frequency (time period) and pulse measurement. Figure 12-1 illustrates a simplified block diagram of the Input Capture module.

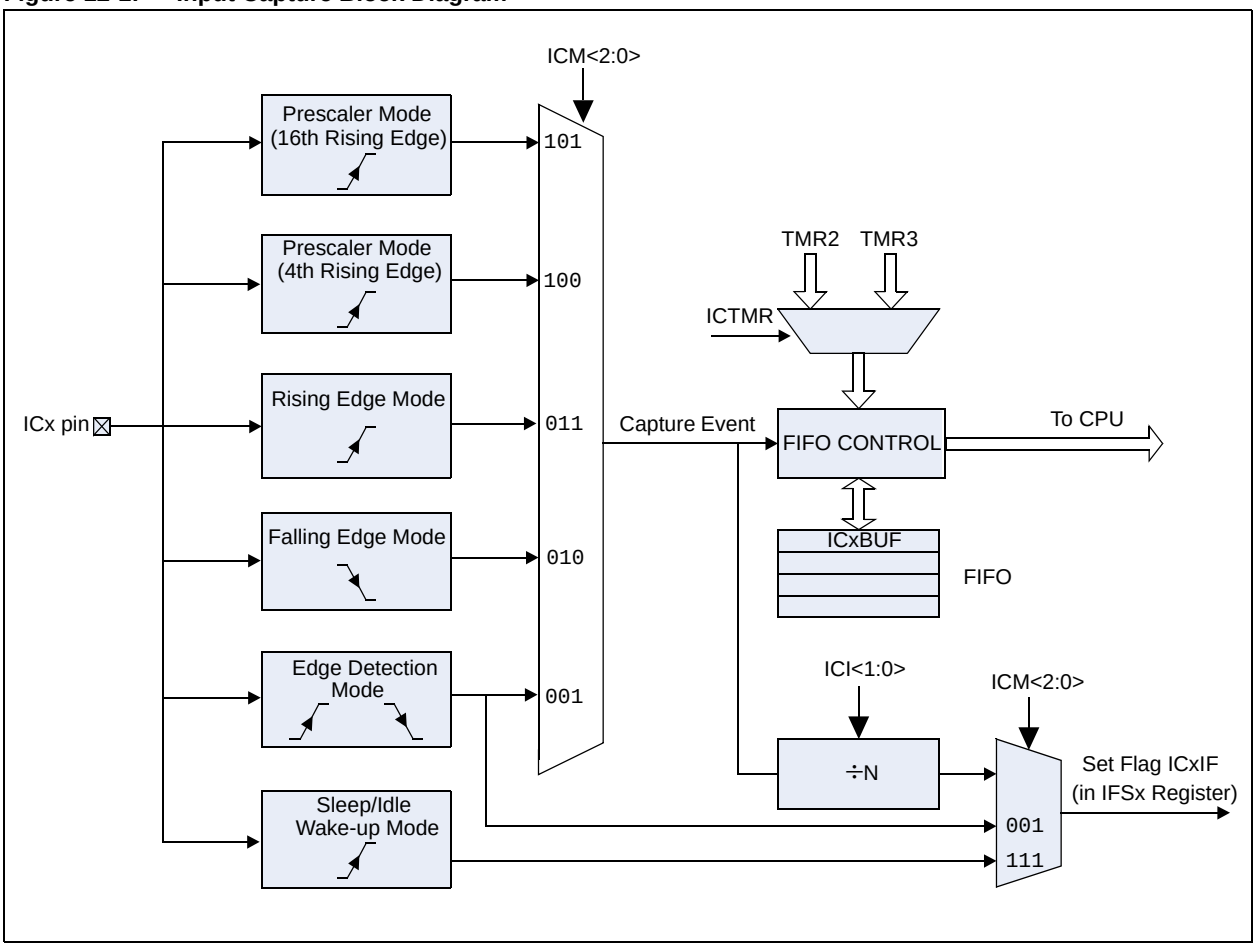
The Input Capture module has multiple operating modes. The operating modes are selected through the Input Capture Control (ICxCON) register and include:

- Capture timer value on every falling edge of the input applied at the ICx pin
- Capture timer value on every rising edge of the input applied at the ICx pin
- Capture timer value on every 4th rising edge of the input applied at the ICx pin
- Capture timer value on every 16th rising edge of the input applied at the ICx pin
- Capture timer value on every rising and every falling edge of the input applied at the ICx pin
- Device wake-up from Sleep and Idle mode on the rising edge of the input applied at the ICx pin

The Input Capture module has a four level First-In First-Out (FIFO) buffer. The user-assigned application can select the number of capture events required to generate a CPU interrupt.

Note: Each dsPIC33F/PIC24H device has one or more Input Capture modules. An 'x' used in the names of pins, control/status bits and registers denotes the particular Input Capture module number. Refer to the **"Input Capture"** chapter in the specific device data sheet for more details.

Figure 12-1: Input Capture Block Diagram



12.2 INPUT CAPTURE REGISTERS

Each capture channel available on dsPIC33F/PIC24H family devices has these registers:

- ICxCON: Input Capture Control register
- ICxBUF: Input Capture Buffer register (see Table 12-3 for bit information)

Register 12-1: ICxCON: Input Capture x Control Register

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	ICSIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-0, HC	R-0, HC	R/W-0	R/W-0	R/W-0
ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		
bit 7							bit 0

Legend:	HC = Cleared in Hardware		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **ICSIDL:** Input Capture x Stop in Idle Control bit
1 = Input capture halts in CPU Idle mode
0 = Input capture continues to operate in CPU Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **ICTMR:** Input Capture x Timer Select bit
1 = TMR2 contents are captured on capture event
0 = TMR3 contents are captured on capture event

bit 6-5 **ICI<1:0>:** Select Number of Captures per Interrupt bits
11 = Interrupt on every fourth capture event
10 = Interrupt on every third capture event
01 = Interrupt on every second capture event
00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture x Overflow Status Flag bit (read-only)
1 = Input capture overflow occurred
0 = No input capture overflow occurred

bit 3 **ICBNE:** Input Capture x Buffer Empty Status Flag bit (read-only)
1 = Input capture buffer is not empty, at least one more capture value can be read
0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture x Mode Select bits
111 = Input capture functions as interrupt pin only when device is in Sleep or Idle mode (rising edge detect only, all other control bits are not applicable)
110 = Unused (Input Capture module disabled)
101 = Capture mode, every 16th rising edge
100 = Capture mode, every 4th rising edge
011 = Capture mode, every rising edge
010 = Capture mode, every falling edge
001 = Capture mode, every edge – rising and falling (ICI<1:0> bits do not control interrupt generation for this mode)
000 = Input Capture module turned off

12.3 CAPTURE EVENT GENERATION

12.3.1 Timer Selection

Each dsPIC33F/PIC24H family device has one or more input capture channels. Each channel can select between Timer2 and Timer3 for its time base. Selection of the timer resource is accomplished through the Input Capture Timer Select (ICTMR) bit in the Input Capture Control (ICxCON<7>) register. This timer can be set using the internal clock source (FOSC/2), or an external clock source applied at the TxCK pin.

12.3.2 Input Capture Event Modes

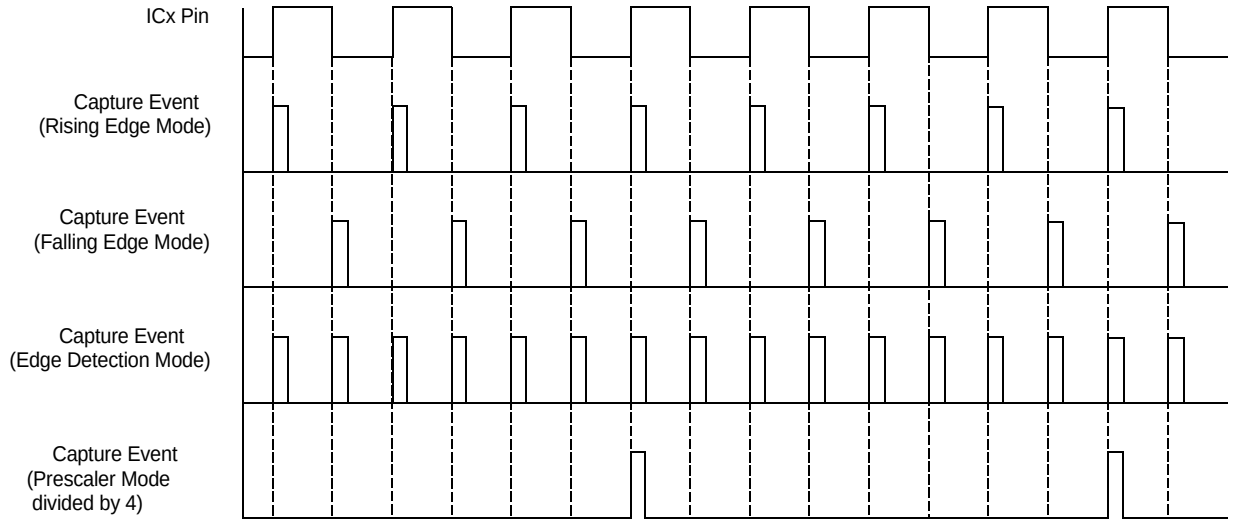
The Input Capture module captures the 16-bit value of the selected timer (Timer2 or Timer3), when a capture event occurs. A capture event is defined as a write of a timer value into the capture buffer.

The Input Capture modes are configured by setting the appropriate Input Capture Mode (ICM<2:0>) bits in the Input Capture Control (ICxCON<2:0>) register. Table 12-1 lists the Input Capture mode and capture events for the different bit settings. The user-assigned application must disable the Input Capture module (i.e., ICM<2:0> = 000) before changing a Capture mode. Figure 12-2 illustrates the capture events for various Capture modes.

Table 12-1: Input Capture Modes

ICM<2:0> Value	Input Capture Mode	Capture Event Generation
000	Module disabled	—
001	Edge Capture mode	On both rising and falling edge of the capture input signal.
010	Falling Edge mode	On the falling edge of the capture input signal.
011	Rising Edge mode	On the rising edge of the capture input signal.
100	Prescaler mode (divided by 4)	On every 4th rising edge of the capture input signal.
101	Prescaler mode (divided by 16)	On every 16th rising edge of the capture input signal.
110	Unused (module disabled)	—
111	Sleep/Idle Wake-up mode	No capture event.

Figure 12-2: Input Capture Event Generation



Note: Refer to the **"Electrical Characteristics"** chapter in the specific device data sheet for more details.

Note 1: The Input Capture (ICx) pin has minimum high time and low time specifications. Refer to the specific device data sheet for more details.

2: The latency from the time the transition happens at the ICx pin to the time the capture event is generated is two instruction cycles.

12.4 CAPTURE BUFFER OPERATION

The Input Capture module can select Timer2 or Timer3 as its time base. The selected timer value is captured and stored in a four deep FIFO buffer on every capture event as shown in Figure 12-3. The ICxBUF register provides access to the FIFO buffer as it is memory mapped.

Two status flags are associated with the FIFO buffer:

- Input Capture x Buffer Empty Status (ICBNE) flag
- Input Capture x Overflow Status (ICOV) flag

These status flags are cleared:

- On any device Reset
- When the module is disabled by the Input Capture Mode Selection bits (ICM<2:0>)

12.4.1 Input Capture Buffer Not Empty (ICBNE)

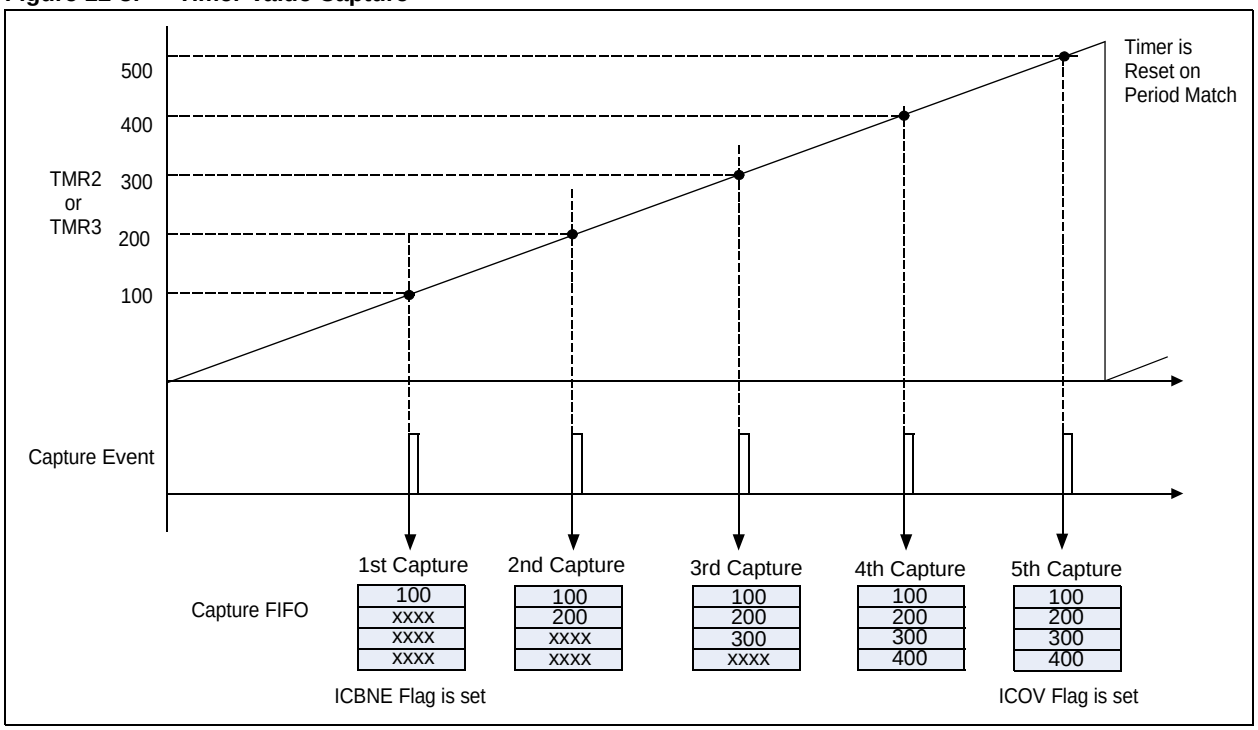
The ICBNE read-only status bit (ICxCON<3>) is set on the first input capture event and remains set until all capture events are read from the capture buffer. For example, if three capture events occur, then three reads of the capture buffer are required before the ICBNE bit (ICxCON<3>) is cleared. Similarly, if four capture events occur, four reads are required to clear the bit. Each read of the capture buffer allows the remaining word(s) to move to the next available top location.

12.4.2 Input Capture Overflow (ICOV)

The ICOV read-only status bit (ICxCON<4>) is set when the capture buffer overflows. If the event that the buffer is full with four capture events, and a fifth capture event takes place before the buffer is read, an overrun condition occurs, and the ICOV bit (ICxCON<4>) is set to a logic '1'.

To clear the overrun condition, the capture buffer must be read four times. On the fourth read, the ICOV status flag (ICxCON<4>) is cleared. The capture event does not write timer values into the FIFO buffer when it is full. When ICI<1:0> = 00 or ICM<2:0> = 001, interrupts continue to occur and the ICOV bit remains clear even after a buffer overflow has occurred.

Figure 12-3: Timer Value Capture



Note 1: The latency from the time the transition happens at the capture input (ICx pin) to the time the capture event is generated is two instruction cycles.

2: The Overflow flag remains cleared in Edge Detect mode (ICM<2:0> = 001).

12.5 INPUT CAPTURE INTERRUPTS

The input capture channel can generate an interrupt based on the selected number of capture events, as illustrated in Figure 12-4. The number of events is set by the Input Capture Interrupt (ICI<1:0>) bits in the Capture Control register (ICxCON<6:5>) is listed in Table 12-2. The user-assigned application must disable the Input Capture module (ICM<2:0> = 000) before changing the ICI<1:0> bits.

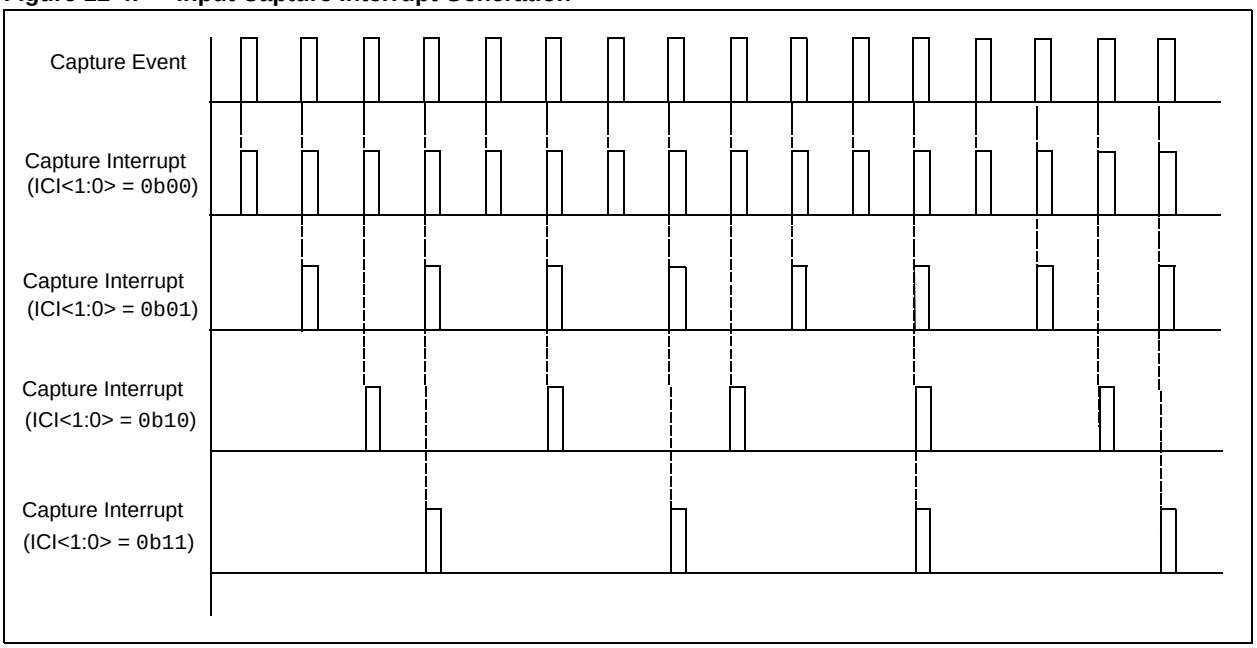
When the capture interrupt is generated on every capture event (ICI<1:0> = 00), the FIFO overflow condition does not inhibit the capture interrupt. If the capture interrupt is not generated on every capture event, the FIFO overflow condition inhibits the capture interrupt. Therefore, all the captured values must be read from the capture buffer on every capture interrupt. For example, if the capture interrupt is generated on every second capture event (ICI<1:0> = 01), the capture buffer must be read twice. Similarly, if the capture interrupt is generated on every third capture event (ICI<1:0> = 10), the capture buffer must be read three times.

Note: In Edge Detection Mode (ICM<2:0> = 001), the interrupt is generated on every capture event and the Input Capture Interrupt (ICI<1:0>) bits are ignored.

Table 12-2: Input Capture Interrupt Selection

ICI<1:0> Values	Input Capture Interrupt Generation
00	Interrupt on every capture event
01	Interrupt on every second capture event
10	Interrupt on every third capture event
11	Interrupt on every fourth capture event

Figure 12-4: Input Capture Interrupt Generation



Note: Each Input Capture channel has interrupt flag status bits (ICxIF), Interrupt Enable bits (ICxIE) and Interrupt Priority Control bits (ICxIP<2:0>). Refer to **Section 6. "Interrupts"** (DS70184) in the "*dsPIC33F Family Reference Manual*" for more details on peripheral interrupts.

12.5.1 Code Example for Period Measurement

The following code example shows the time period measurement using the Input Capture module. The capture event is generated on every rising edge and the capture interrupt is generated after taking two time stamps for period measurement, as illustrated in Figure 12-5.

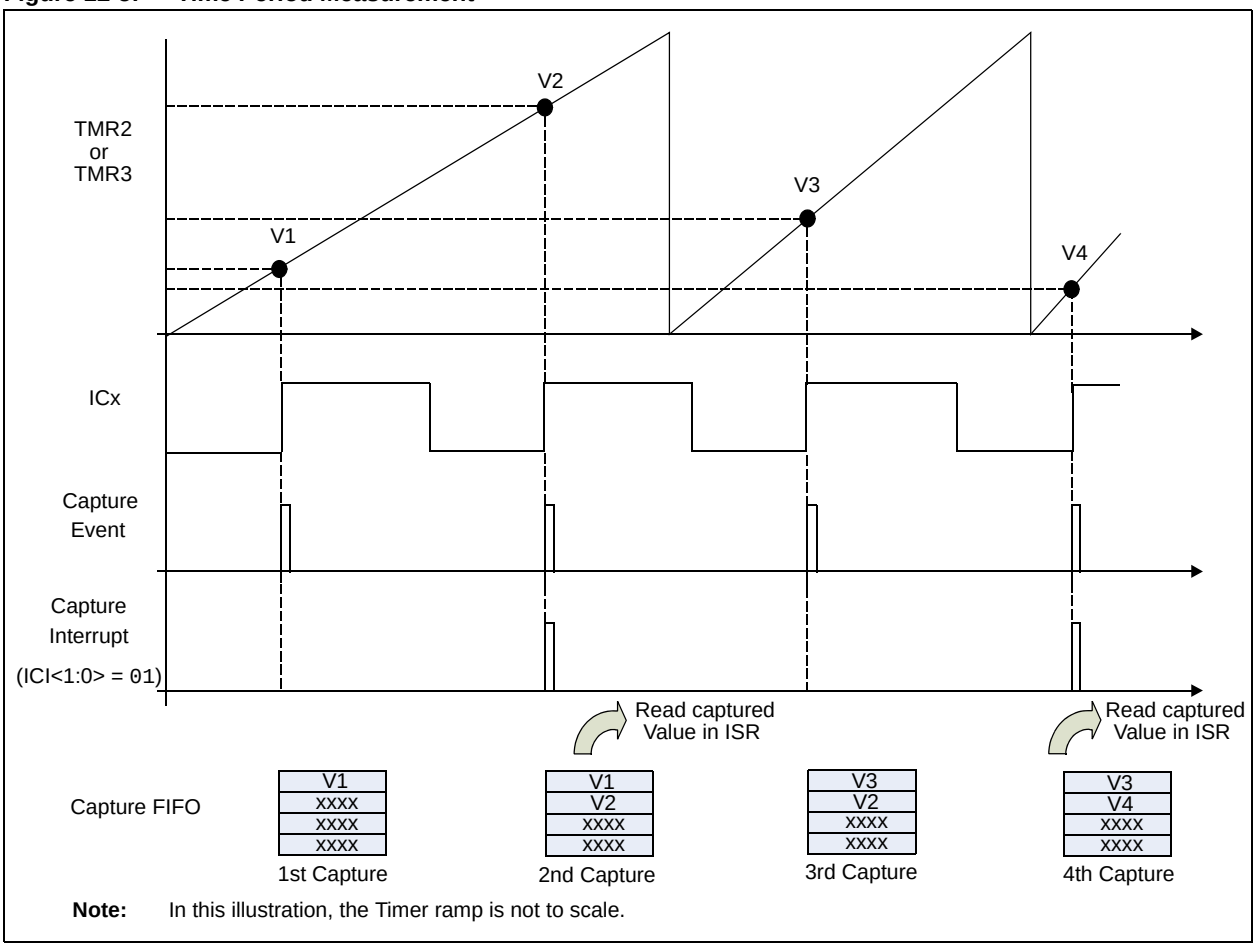
Example 12-1: Capture Code Example

```
// Initialize the Input Capture Module
    IC1CONbits.ICM = 0b00;    // Disable Input Capture 1 module
    IC1CONbits.ICTMR = 1;     // Select Timer2 as the IC1 Time base
    IC1CONbits.ICI = 0b01;    // Interrupt on every second capture event
    IC1CONbits.ICM = 0b011;   // Generate capture event on every Rising edge

// Enable Capture Interrupt And Timer2
    IPC0bits.IC1IP = 1;       // Setup IC1 interrupt priority level
    IFS0bits.IC1IF = 0;       // Clear IC1 Interrupt Status Flag
    IEC0bits.IC1IE = 1;       // Enable IC1 interrupt

// Capture Interrupt Service Routine
    unsigned int timePeriod= 0;
    void __attribute__((__interrupt__)) _IC1Interrupt(void)
    {
    unsigned int t1,t2;
    t1=IC1BUF;
    t2=IC1BUF;
    IFS0bits.IC1IF=0;
    if(t2>t1)
     timePeriod = t2-t1;
    else
     timePeriod = (PR2 - t1) + t2;
}
```

Figure 12-5: Time Period Measurement



Note: In this illustration, the Timer ramp is not to scale.

12.5.2 Input Capture Operation with DMA

Some dsPIC33F/PIC24H family devices include a Direct Memory Access (DMA) module, which allows data to be transferred from the Input Capture module to data memory without CPU intervention. Refer to the **"Direct Memory Access (DMA)"** chapter in the specific device data sheet to see if DMA is available on your particular device. In addition, see **Section 22. "Direct Memory Access (DMA)"** (DS70182) in the *"dsPIC33F/PIC24H Family Reference Manual"* for more details on the DMA module.

When the Input Capture module and DMA channel are appropriately configured, the Input Capture module issues a DMA request for every capture event. The DMA transfers data from the Input Capture Buffer (ICxBUF) register into RAM, and issues a CPU interrupt after a predefined number of transfers.

The DMA channel must be initialized with the following:

- The DMA Request Source Selection (IRQSEL<6:0>) bits in the DMA Request register (DMAxREQ<6:0>) must select the DMA transfer request from Input Capture module
- The DMA Channel Peripheral Address (DMAxPAD) register must be initialized with the address of the Input Capture Buffer (ICxBUF) register
- The Transfer Direction (DIR) bit in DMA Control register (DMAxCON<13>) must be cleared. In this condition, data is read from the peripheral and written to the dual port DMA memory.

In addition, the input capture interrupt bits (ICI<1:0> = 00) must be cleared to generate a DMA request for every capture event.

Example 12-2 provides sample code that transfers the capture values to RAM with DMA.

DMA Channel 0 is set up for the Input Capture module with the following configuration:

- Transfer data from the Input Capture module to RAM
- One-shot operating mode
- Register Indirect with Post-Increment addressing
- Single buffer
- 256 transfers per buffer
- Transfer words

Example 12-2: Input Capture with DMA

```
// Initialize the Input Capture module
    IC1CONbits.ICM = 0b00;    // Disable Input Capture 1 module
    IC1CONbits.ICTMR = 1;     // Select Timer2 as the IC1 time base
    IC1CONbits.ICI = 0b00;    // Interrupt on every capture event
    IC1CONbits.ICM = 0b001;   // Generate capture event on every rising edge
```

Set up DMA for Input Capture:

```
// Define Buffer in DMA RAM
    unsigned int BufferA[256] __attribute__((space(dma)));

    DMA0CONbits.AMODE = 0b00; // Register indirect with post increment
    DMA0CONbits.MODE = 0b01;  // One Shot, Ping-Pong mode disabled
    DMA0CONbits.DIR = 0;      // Peripheral to RAM
    DMA0PAD = (int)&IC1BUF;   // Address of the capture buffer register
    DMA0REQ = 1;              // Select IC module as DMA request source
    DMA0CNT = 255;            // Number of words to buffer

    DMA0STA = __builtin_dmaoffset(&BufferA);

    IFS0bits.DMA0IF = 0;      // Clear the DMA interrupt flag bit
    IEC0bits.DMA0IE = 1;      // Enable DMA interrupt enable bit
    DMA0CONbits.CHEN = 1;
```

Set up DMA Interrupt Handler:

```
    void __attribute__((__interrupt__)) _DMA0Interrupt(void)
{
// Process the captured values

    IFS0bits.DMA0IF = 0;      // Clear the DMA0 Interrupt Flag
}
```


12.5.3 Capture Pin as External Interrupt

The Input Capture (ICx) pin can be used as an auxiliary external interrupt source by clearing the Input Capture Interrupt bits (ICI<1:0> = 00). In this condition an interrupt is generated on every capture event, and the FIFO overflow condition does not inhibit the capture interrupt. Consequently, the input capture buffer need not be read in the Capture Interrupt Service Routine (ISR). The Input Capture Mode bits (ICM<2:0>) can be used to select the edge polarity for the interrupt.

12.6 INPUT CAPTURE OPERATION IN POWER-SAVING MODES

12.6.1 Input Capture Operation in Sleep Mode

The Input Capture module does not operate when the device is in Sleep mode. In Sleep mode, the Input Capture (ICx) pin can only function as an external interrupt source for wake-up. The Sleep mode is enabled by setting the Input Capture Mode bits (ICM<2:0> = 111). In this mode, if the input capture interrupt is enabled, a rising edge on the capture pin generates capture interrupt.

The capture interrupt wakes up the device from Sleep, and the following occurs:

- If the assigned priority for the interrupt is less than, or equal, to the current CPU priority, the device wakes up and continues code execution from the instruction following the PWRSAV instruction that initiated Sleep mode
- If the assigned priority level for the interrupt source is greater than the current CPU priority, the device wakes up and the CPU exception process begins. Code execution continues from the first instruction of the capture ISR

12.6.2 Input Capture Operation in Idle Mode

When the device enters Idle mode, the system clock sources remain functional and the CPU stops executing code. The Input Capture Stop-in Idle (ICSIDL) bit selection in the Input Capture Control register (ICxCON<13>) determines whether the module stops in Idle mode or continues to operate in Idle mode.

If ICSIDL = 0 (ICxCON<13>), the module continues to operate in Idle mode providing full functionality of the Input Capture module including the 4:1 and 16:1 prescaler capture settings. The prescaler capture settings are defined by the ICM<2:0> control bits (ICxCON<2:0>). These modes require that the selected timer is enabled during Idle mode as well.

If ICSIDL = 1 (ICxCON<13>), the module stops in Idle mode. The module performs the same functions as Sleep mode, when stopped in Idle mode. Refer to **12.6.1 “Input Capture Operation in Sleep Mode”**.

12.7 I/O PIN CONTROL

When the Input Capture module is enabled, the user-assigned application must ensure that the I/O pin direction is configured for an input by setting the associated TRIS bit. The pin direction is not set when the Input Capture module is enabled. All other peripherals multiplexed with the input pin must be disabled.

12.8 REGISTER MAPS

The summaries of the registers associated with the dsPIC33F/PIC24H Input Capture module are provided in Table 12-3.

Table 12-3: Input Capture Register Map

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ICxBUF	Input Capture x Register																xxxx
ICxCON	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

12.9 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33F/PIC24H device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Input Capture module are:

Title	Application Note #
Using the CCP Module(s)	AN594
Implementing Ultrasonic Ranging	AN597

Note: For additional application notes and code examples for the dsPIC33F/PIC24H family of devices, visit the Microchip web site (www.microchip.com).

12.10 REVISION HISTORY

Revision A (March 2007)

This is the initial released version of this document.

Revision B (April 2007)

Minor edits have been incorporated throughout the document.

Revision C (July 2009)

This revision incorporates the following updates:

- Examples:
  - Updated Example 12-1 as per the code example explanation
- Sections:
  - The heading Revision B (April 2007), in **12.10 “Revision History”** has been corrected as Revision A (March 2007)
- Additional minor corrections such as language and formatting updates were incorporated throughout the document

Revision D (January 2012)

This revision includes the following updates:

- Updated the second paragraph of **12.4.2 “Input Capture Overflow (ICOV)”** to clarify the state of the ICOV bit during a buffer overflow
- Updated the Input Capture with DMA code example (see Example 12-2)
- Removed Timer Register Map (Table 12-4) and Interrupt Controller Register Map (Table 12-5). Refer to the respective family reference manual section and the specific device data sheet for current information on these registers.
- Removed 12.9 “Design Tips”
- All occurrences of dsPIC33F were changed to dsPIC33F/PIC24H
- The Preliminary document status was removed
- Minor updates to text and formatting were incorporated throughout the document

NOTES:

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